

**FEATURES**

**High Off Isolation** -75 dB at 100 MHz  
**-3 dB Signal Bandwidth** 300 MHz  
**+1.8 V to +5.5 V Single Supply**  
**Low On-Resistance** (15  $\Omega$ )  
**Fast Switching Times**  
 $t_{ON}$  Typically 9 ns  
 $t_{OFF}$  Typically 3 ns  
**Typical Power Consumption** <0.01  $\mu$ W  
**TTL/CMOS Compatible**

**APPLICATIONS**

**Audio and Video Switching**  
**RF Switching**  
**Networking Applications**  
**Battery Powered Systems**  
**Communication Systems**  
**Relay Replacement**  
**Sample-and-Hold Systems**

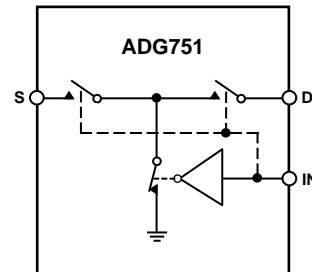
**GENERAL DESCRIPTION**

The ADG751 is a low voltage SPST (single pole, single throw) switch. It is constructed in a T-switch configuration, which results in excellent Off Isolation while maintaining good frequency response in the ON condition.

High off isolation and wide signal bandwidth make this part suitable for switching RF and video signals. Low power consumption and operating supply range of +1.8 V to +5.5 V make it ideal for battery powered, portable instruments.

The ADG751 is designed on a submicron process that provides low power dissipation yet gives high switching speed and low on resistance. This part is a fully bidirectional switch and can handle signals up to and including the supply rails.

The ADG751 is available in 6-lead SOT-23 and 8-lead  $\mu$ SOIC packages.

**FUNCTIONAL BLOCK DIAGRAM**

SWITCH SHOWN FOR A LOGIC "1" INPUT

**PRODUCT HIGHLIGHTS**

1. High Off Isolation -75 dB at 100 MHz.
2. -3 dB Signal Bandwidth 300 MHz.
3. Low On-Resistance (15  $\Omega$ ).
4. Low Power Consumption, typically <0.01  $\mu$ W.
5. Tiny 6-lead SOT-23 and 8-lead  $\mu$ SOIC packages.

REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**  
**Tel: 781/329-4700      World Wide Web Site: <http://www.analog.com>**  
**Fax: 781/326-8703      © Analog Devices, Inc., 1999**

# ADG751—SPECIFICATIONS ( $V_{DD} = +5\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Grade		A Grade		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>						
Analogue Signal Range	0 V to $V_{DD}$		0 V to $V_{DD}$		V	
On-Resistance ( $R_{ON}$ )	28		15		$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ ; Test Circuit 1
	35	40	18	20	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	3		2		$\Omega$ typ	$V_S = 0\text{ V to }2.5\text{ V}$ , $I_{DS} = 10\text{ mA}$ ; $V_{DD} = 4.5\text{ V}$
		5		3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_{DD} = +5.5\text{ V}$ ; $V_D = 4.5\text{ V/1 V}$ , $V_S = 1\text{ V/4.5 V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3.0$	$\pm 0.25$	$\pm 3.0$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_D = 4.5\text{ V/1 V}$ , $V_S = 1\text{ V/4.5 V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3.0$	$\pm 0.25$	$\pm 3.0$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_D = V_S = 1\text{ V}$ , or $4.5\text{ V}$ ; Test Circuit 3
	$\pm 0.25$	$\pm 3.0$	$\pm 0.25$	$\pm 3.0$	nA max	
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$		2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8		0.8	V max	
Input Current						
$I_{INL}$ or $I_{INH}$	0.001		0.001		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.5$		$\pm 0.5$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2		2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>						
$t_{ON}$	9		9		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 3\text{ V}$ , Test Circuit 4
		13		13	ns max	
$t_{OFF}$	3		3		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 3\text{ V}$ , Test Circuit 4
		5		5	ns max	
Charge Injection	1		1		pC typ	$V_S = 1\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1.0\text{ nF}$ ; Test Circuit 5
Off Isolation	-75		-65		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ MHz}$ ; Test Circuit 6
-3 dB Bandwidth	180		300		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 7
$C_S$ (OFF)	4		4		pF typ	
$C_D$ (OFF)	4		4		pF typ	
$C_D$ , $C_S$ (ON)	26		15		pF typ	
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	0.001		0.001		$\mu\text{A}$ typ	$V_{DD} = +5.5\text{ V}$ ; Digital Inputs = 0 V or +5.5 V
	0.1	0.5	0.1	0.5	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# SPECIFICATIONS ( $V_{DD} = +3\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Grade		A Grade		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C		
ANALOG SWITCH						
Analog Signal Range		0 V to $V_{DD}$		0 V to $V_{DD}$	V	
On-Resistance ( $R_{ON}$ )	60	90	35	50	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$ ; Test Circuit 1
LEAKAGE CURRENTS						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_{DD} = +3.3\text{ V}$ $V_D = 3\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/3\text{ V}$ ; Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$	$\pm 3.0$	$\pm 0.01$	$\pm 3.0$	nA max nA typ	$V_D = 1\text{ V}/3\text{ V}$ , $V_S = 3\text{ V}/1\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$	$\pm 3.0$	$\pm 0.01$	$\pm 3.0$	nA max nA typ nA max	$V_D = V_S = 1\text{ V}$ , or $3\text{ V}$ ; Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, $V_{INH}$		2.0		2.0	V min	
Input Low Voltage, $V_{INL}$		0.4		0.4	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.001	$\pm 0.5$	0.001	$\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	2		2		pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>						
$t_{ON}$	12	19	12	19	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 2\text{ V}$ , Test Circuit 4
$t_{OFF}$	4	6	4	6	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 2\text{ V}$ , Test Circuit 4
Charge Injection	1		1		pC typ	$V_S = 1\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1.0\text{ nF}$ ; Test Circuit 5
Off Isolation	-75		-65		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ MHz}$ ; Test Circuit 6
-3 dB Bandwidth	180		280		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 7
$C_S$ (OFF)	4		4		pF typ	
$C_D$ (OFF)	4		4		pF typ	
$C_D$ , $C_S$ (ON)	26		15		pF typ	
POWER REQUIREMENTS						
$I_{DD}$	0.001		0.001		$\mu\text{A}$ typ	$V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or +3.3 V
	0.1	0.5	0.1	0.5	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG751

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to GND	-0.3 V to +6 V
Analog, Digital Inputs <sup>2</sup>	-0.3 V to V <sub>DD</sub> +0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (A, B Versions)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T <sub>J</sub> Max)	+150°C
Power Dissipation	(T <sub>J</sub> Max - T <sub>A</sub> ) / θ <sub>JA</sub>
μSOIC Package	
θ <sub>JA</sub> Thermal Impedance	206°C/W
θ <sub>JC</sub> Thermal Impedance	44°C/W

## SOT-23 Package

θ <sub>JA</sub> Thermal Impedance	229.6°C/W
θ <sub>JC</sub> Thermal Impedance	91.99°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## ORDERING GUIDE

Model	Temperature Range	Brand*	Package Descriptions	Package Options
ADG751BRM	-40°C to +85°C	SDB	μSOIC	RM-8
ADG751BRT	-40°C to +85°C	SDB	SOT-23	RT-6
ADG751ARM	-40°C to +85°C	SDA	μSOIC	RM-8
ADG751ART	-40°C to +85°C	SDA	SOT-23	RT-6

\*Brand on these packages is limited to three characters due to space constraints.

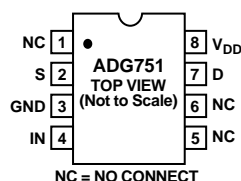
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG751 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

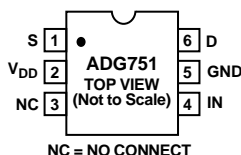


## PIN CONFIGURATIONS

### 8-Lead $\mu$ SOIC (RM-8)



### 6-Lead SOT-23 (RT-6)



## TERMINOLOGY

$V_{DD}$	Most positive power supply potential.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
$R_{ON}$	Ohmic resistance between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
$I_S$ (OFF)	Source leakage current with the switch "OFF."
$I_D$ (OFF)	Drain leakage current with the switch "OFF."
$I_D, I_S$ (ON)	Channel leakage current with the switch "ON."
$V_D$ ( $V_S$ )	Analog voltage on terminals D and S.
$C_S$ (OFF)	"OFF" switch source capacitance.
$C_D$ (OFF)	"OFF" switch drain capacitance.
$C_D, C_S$ (ON)	"ON" switch capacitance.
$t_{ON}$	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
$t_{OFF}$	Delay between applying the digital control input and the output switching off.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by $-3$ dBs.
On Response	The frequency response of the "ON" switch.
Insertion Loss	Loss due to the ON resistance of the switch.
$V_{INL}$	Maximum input voltage for Logic "0."
$V_{INH}$	Minimum input voltage for Logic "1."
$I_{INL}(I_{INH})$	Input current of the digital input.
$I_{DD}$	Positive supply current.

**Table I. Truth Table**

ADG751 IN	Switch Condition
0	ON
1	OFF

# ADG751—Typical Performance Characteristics

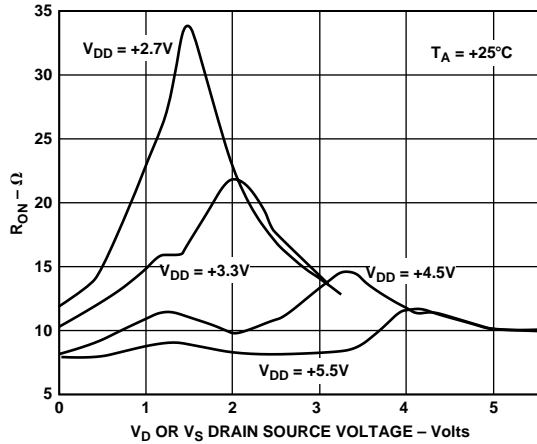


Figure 1. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supplies (A Grade)

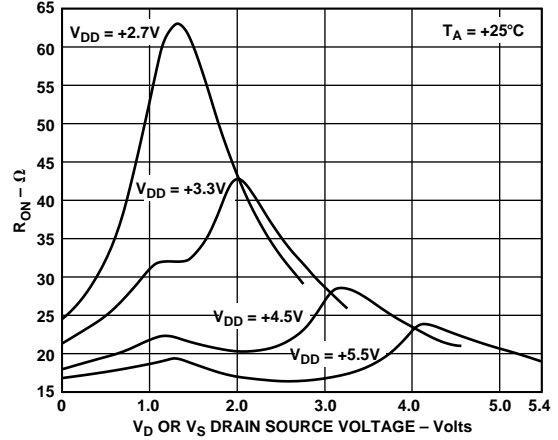


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supplies (B Grade)

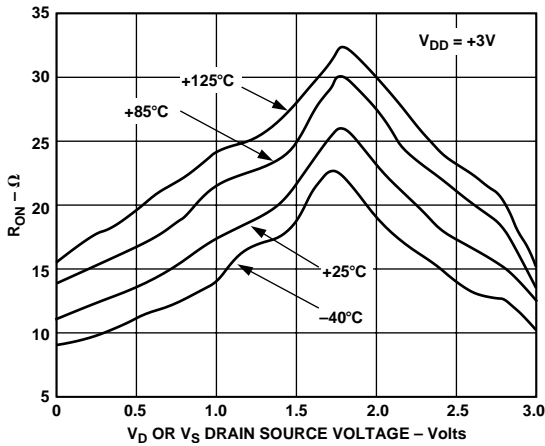


Figure 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 3$  V (A Grade)

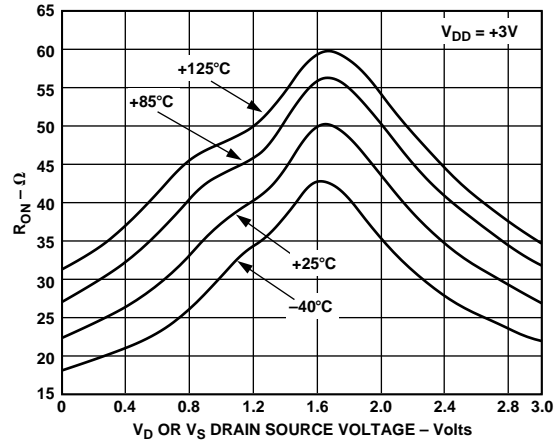


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 3$  V (B Grade)

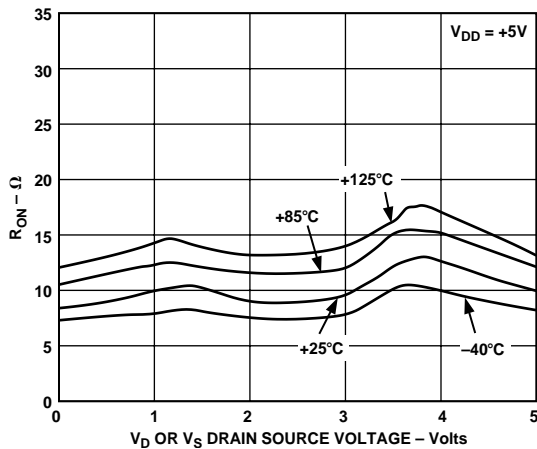


Figure 3. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 5$  V (A Grade)

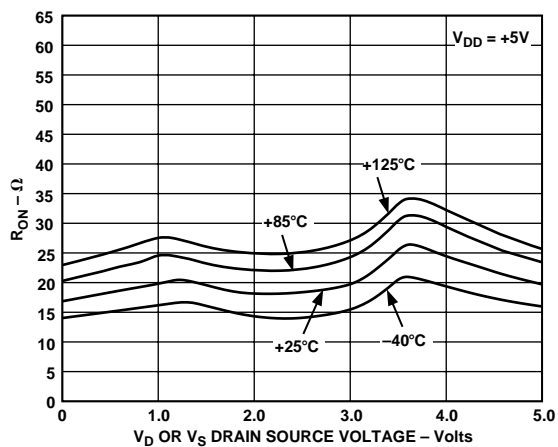


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 5$  V (B Grade)

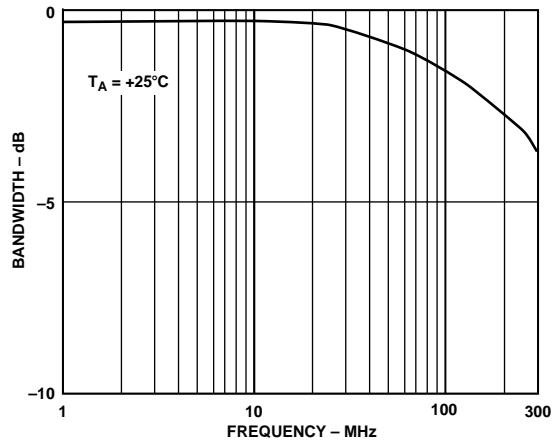


Figure 7. On Response vs. Frequency (A Grade)

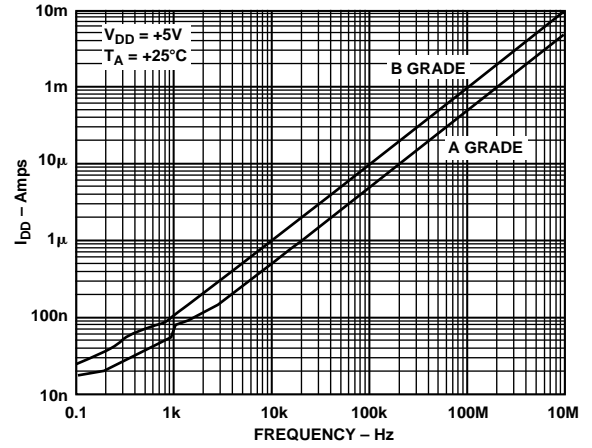


Figure 10. Supply Current vs. Input Switching Frequency

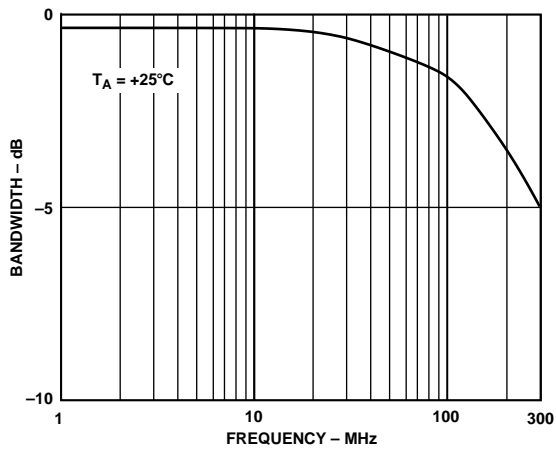


Figure 8. On Response vs. Frequency (B Grade)

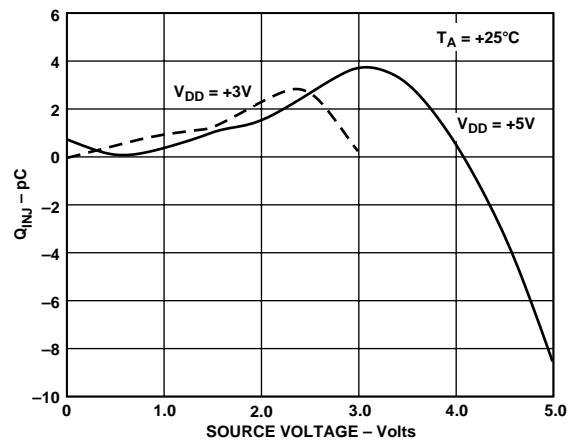


Figure 11. Charge Injection vs. Source/Drain Voltage

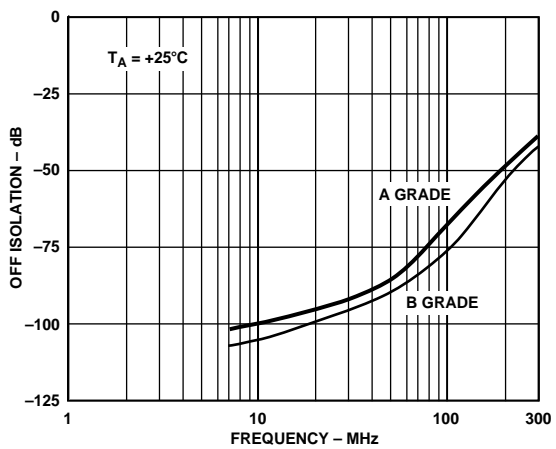


Figure 9. Off Isolation vs. Frequency for Both Grades

# ADG751

## GENERAL DESCRIPTION

The ADG751 is an SPST switch constructed using switches in a T configuration to obtain high “OFF” isolation while maintaining good frequency response in the “ON” condition.

Figure 12 shows the T-switch configuration. While the switch is in the OFF state, the shunt switch is closed and the two series switches are open. The closed shunt switch provides a signal path to ground for any of the unwanted signals that find their way through the off capacitances of the series’ MOS devices. This results in improved isolation between the input and output than with an ordinary series switch. When the switch is in the ON condition, the shunt switch is open and the signal path is through the two series switches which are now closed.

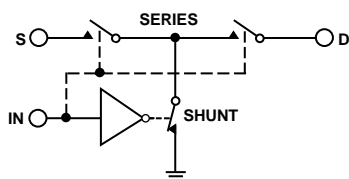


Figure 12. Basic T-Switch Configuration

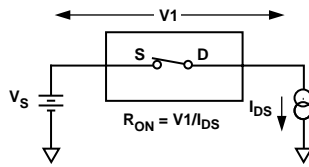
## LAYOUT CONSIDERATIONS

Where accurate high frequency operation is important, careful consideration should be given to the printed circuit board layout and to grounding. Wire wrap boards, prototype boards and sockets are not recommended because of their high parasitic inductance and capacitance. The part should be soldered directly to a printed circuit board. A ground plane should cover all unused areas of the component side of the board to provide a low impedance path to ground. Removing the ground planes from the area around the part reduces stray capacitance.

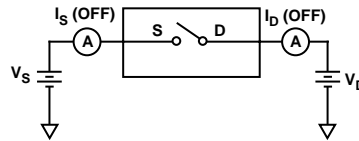
Good decoupling is important in achieving optimum performance.  $V_{DD}$  should be decoupled with a  $0.1 \mu\text{F}$  surface mount capacitor to ground mounted as close as possible to the device itself.



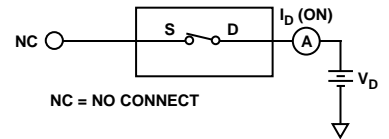
### Test Circuits



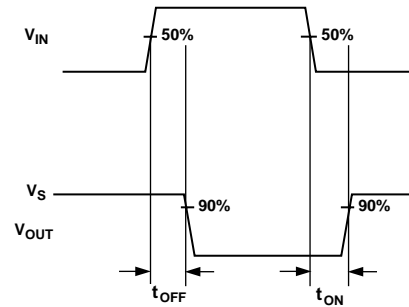
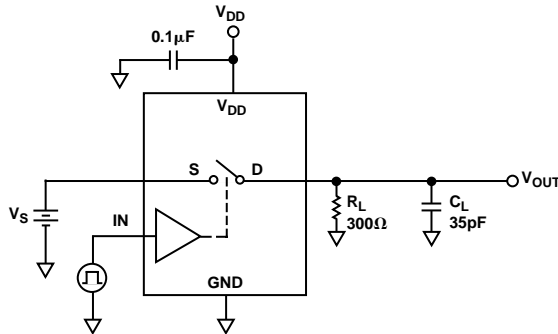
Test Circuit 1. On Resistance



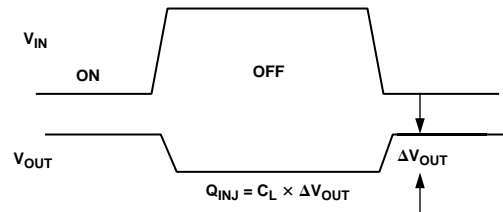
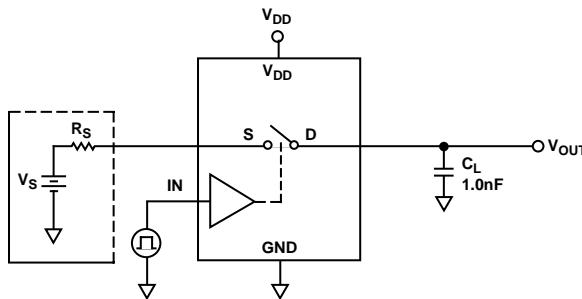
Test Circuit 2. Off Leakage



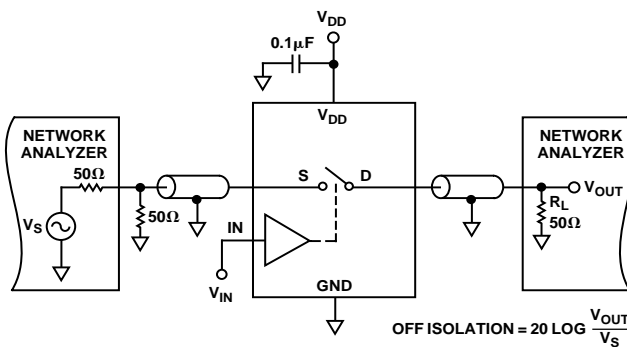
Test Circuit 3. On Leakage



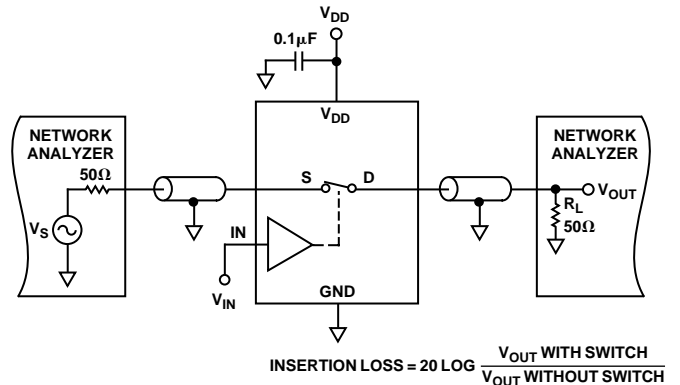
Test Circuit 4. Switching Times



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation

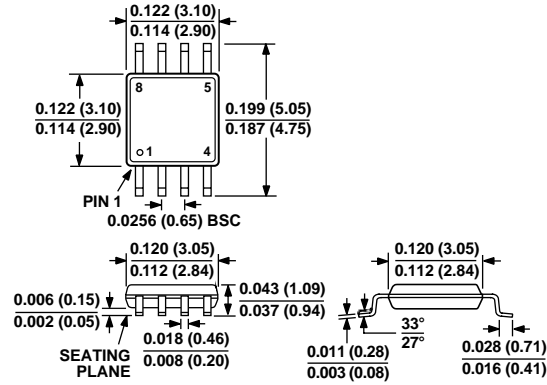


Test Circuit 7. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead  $\mu$ SOIC  
(RM-8)



6-Lead SOT-23  
(RT-6)

