VLSI TECHNOLOGY, INC.

T-75-37-07

VL86C110

RISC MEMORY CONTROLLER (MEMC)

FEATURES

- Drives up to 32 standard dynamic RAMs giving 4M bytes of real memory with 1M bit devices
- Logical-to-physical address translation (32M byte logical address space) supporting three protection levels:
  - Supervisor Mode
  - Operating System Mode
  - User Mode
- Uses fast page mode DRAM accesses to maximize bandwidth from commodity memories
- Internal DMA address generators for video, cursor and sound data buffers
- Various ROM speeds supported (access times of 450 ns, 325 ns, 200 ns)
- Provides all critical system timing including processor clocks, –RAS, –CAS, and DMA data transfer strobes
- Arbitrates memory between the processor and DMA systems

DESCRIPTION

The memory controller (MEMC) acts as the interface between the ARM (Acorn RISC Machine) processor and other functions in the system. The four circuits in the RISC family: MEMC, ARM, VIDC-video controller, and IOC-I/O controller, can be used to implement a small computer system. MEMC uses a single clock input to derive timing information for the other components.

In addition to providing interface signals to the other controllers, MEMC generates all the control signals for several access times of read-only memory (ROM) plus high-resolution timing and refresh control for dynamic RAM (DRAM). The controller outputs can drive up to 32 memory devices directly in a wide variety of configurations using various architectures of standard DRAMs. A logical-to-physical address translator maps the 4M byte physical memory into the 32M byte logical address space with three levels of protection.

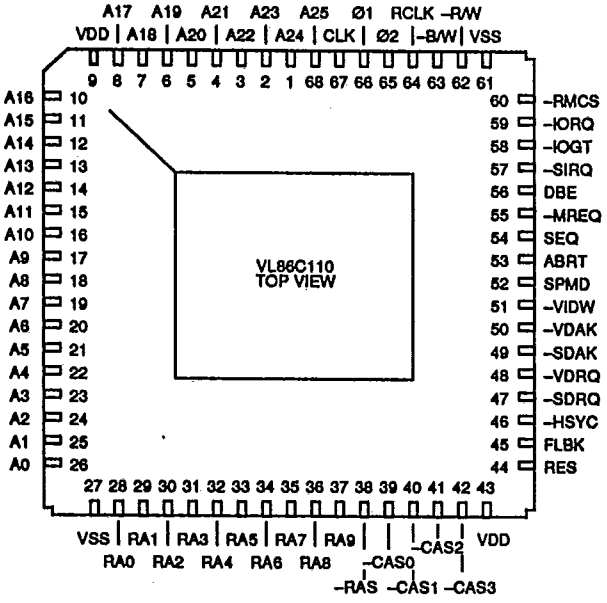
Address translation is performed by a simple 128 entry content-addressable memory (CAM). MEMC provides a descriptor entry for every page of physical memory which eliminates descriptor thrashing (address translation misses) from degrading system performance.

The simple structure allows memory address translation to be performed without increasing required memory access time or decreasing the system clock. MEMC allows virtual memory and multi-tasking operations to be implemented without the usual performance degradation associated with each function. Fast page mode DRAM accesses are used to maximize memory bandwidth from inexpensive commodity memory devices.

MEMC supports direct memory access (DMA) read operations with three programmable address generators. Video refresh is performed using a circular buffer to enhance scrolling capability plus a separate linear buffer for a cursor sprite. Sound data uses a double buffering system.

PIN DIAGRAM

JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER



ORDER INFORMATION

Part Number	Bus Clock Frequency	Package
VL86C110-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C110-08LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature range is 0°C to + 70°C.

PLEASE CONSULT RISC FAMILY DATA MANUAL FOR DETAILED INFORMATION