Winbond Electronics Corp.

USB HUB CONTROL INTERFACE

GENERAL DESCRIPTION

W81C180 implements a medium speed (12Mhz) Universal Serial Bus (USB) hub control interface. It supports four downstream ports and an I2C serial interface to microcontrollers.

W81C180 acts as a USB hub controller and a hub repeater at the direction of an external microcontroller. W81C180 controls the traffic among the host, four downstream ports, and the microprocessor. As a hub controller, it can enable/disable ports, send and receive resets, and detect devices of high or low speeds. The W81C180 contains two function endpoints and two hub endpoints to allow both USB Control and Interrupt Transfers between the host and microcontroller.

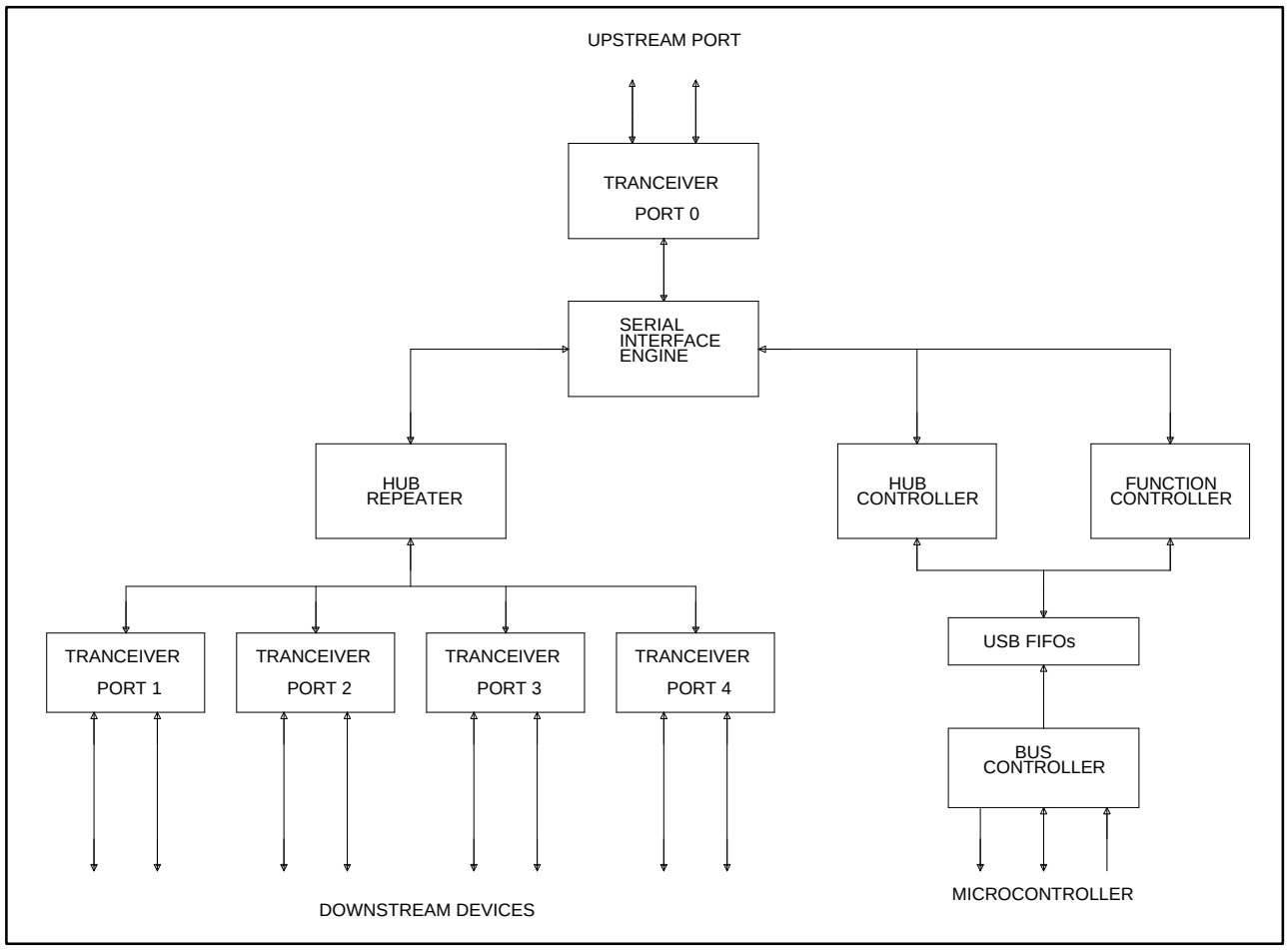
W81C180 is a compound USB device (hub with embeded function attached) with totally five downstream ports. Four of them are removable and the other is permanently attached to the microprocessor connected. W81C180 can be used as a hub controller in a standalone hub with attached function or in a microcontroller based USB device with hub functionality. In the latter case, the microcontroller does not need a USB interface and does not occupy one downstream port.

FEATURES

- Full compliance with USB spec Rev 1.0 and HID Class Definition Rev 1.0
- Support multiple endpoints for standalone hub with attached function
- Support USB device with embedded hub functionality
- USB function controller
- USB hub controller/repeater
- Bus-powered/self-powered hub option
- Four downstream ports with per port overcurrent protection
- Two endpoints for hub (Control and Interrupt)
- Two endpoints for attached device (Control and Interrupt)
- 6KV ESD protection
- 32-pin PDIP
- 5V CMOS device

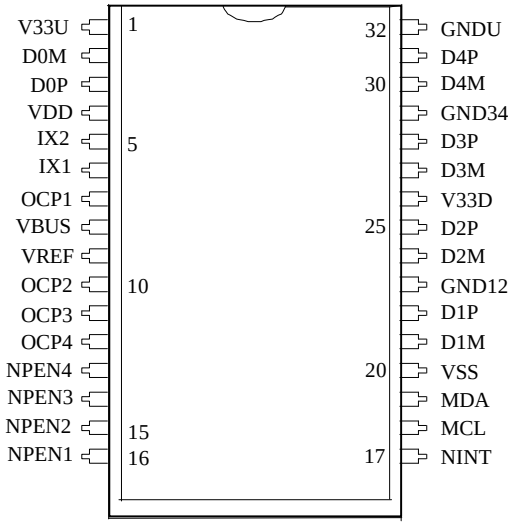
USB BLOCK DIAGRAM:

The Serial Interface Engine (SIE) controls the USB data flow between the uCs and the USB bus. Port0 is a high speed (HS) transceiver for the upstream data path. The Hub Repeater is the traffic controller which directs the bus data to and from the correct paths. The hub Controller and Function Controller determines what data is to be written to or read from the various FIFOs. The Bus Controller directs the interface between the uC and the W81C180.



PIN CONFIGURATION:

32 Pin PDIP



PIN DESCRIPTION:

PIN #	NAME	TYPE	DESCRIPTION
1	V33U	Power	Voltage 3.3V to Upstream Transceiver
2	D0M	UI/O	USB upstream port, negative connection
3	D0P	UI/O	USB upstream port, positive connection
4	VDD	Power	Analog/Digital Voltage 5V
5	X2	OUTPUT	Crystal connection
6	X1	INPUT	Crystal input (12 MHz)
7	OCP1	INPUT	Analog connection for Downstream Port1 Overcurrent Status
8	VBUS	INPUT	Vcc from the upstream port
9	VREF	INPUT	Comparator reference voltage with all OCPs, Maximum reference voltages is 4.1V.
10	OCP2	INPUT	Analog connection for Downstream Port2 Overcurrent Status
11	OCP3	INPUT	Analog connection for Downstream Port3 Overcurrent Status

PIN DESCRIPTION, continued

PIN #	NAME	TYPE	DESCRIPTION
12	OCP4	INPUT	Analog connection for Downstream Port4 Overcurrent Status
13	NPEN4	OUTPUT	Power switch of Downstream Port4
14	NPEN3	OUTPUT	Power switch of Downstream Port3
15	NPEN2	OUTPUT	Power switch of Downstream Port2
16	NPEN1	OUTPUT	Power switch of Downstream Port1
17	NINT	I/OD	Enabled when valid data is received or a port changed occurred.(open drain)
18	MCL	I/OD	Serial clock from uC (open drain)
19	MDA	I/OD	Serial data to/from uC (open drain)
20	VSS	Ground	Analog/Digital Ground
21	D1M	UI/O	USB downstream port1, negative connection
22	D1P	UI/O	USB downstream port1, positive connection
23	GND12	Ground	D1/D2 Transceiver Ground
24	D2M	UI/O	USB downstream port2, negative connection
25	D2P	UI/O	USB downstream port2, positive connection
26	V33D	Power	3.3V supply for downstream Transceivers
27	D3M	UI/O	USB downstream port3, negative connection
28	D3P	UI/O	USB downstream port3, positive connection
29	GND34	Ground	D3/D4 Transceiver Ground
30	D4M	UI/O	USB downstream port4, negative connection
31	D4P	UI/O	USB downstream port4, positive connection
32	GNDU	Ground	Upstream Transceiver Ground

FIRST IN FIRST OUT STORAGE (FIFO'S):

The W81C180 has five FIFO's, one receiving register.

FIFO or SRAM	SIZE*	NOTES
Endpt 0 Receiving	32	Data received on Port0 which contains the correct address and pids will be stored here for the uC to read.
Endpt 0 Transmitting	32	The uC writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 1 Receiving	1	Data received on Port1 which contains the ack pid from host responds to the transmitted by W81C180 will be stored here for the uC to read.
Endpt 1 (Hub) Transmitting	32	The uC writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 1 (Function) Transmitting	32	The uC writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.

*: byte unit, maximum capability

INTERFACE TO THE MICROCONTROLLER:

The W81C180 communicates with the uC via a 2 wire bus. One signal is the data and the other the clock. The clock is always generated by the uC. The data is bi directional. After each byte of data (MSB first) an acknowledge bit (MDA=0) is sent by the receiver. The uC always initiates the communication with a start condition (MDA from 1 change to 0 while MCL=1) and the W81C180's address. The uC ends the transmission with a stop condition (MDA from 0 change to 1 while MCL=1). Data is always changed while MCL=0 and clocked in on the rising edge of MCL. The W81C180 acts as a slave memory device at address E8h.

W81C180'S ADDRESS	READ FROM W81C180	WRITE TO W81C180
1110 100S	S=1	S=0

The format for describing the interface to the W81C180 is as follows:

ST = Start (MDA from 1 change to 0 while MCL=1)

AW = An acknowledge given by the W81C180 (the W81C180 brings MDA=0 during the 9th MCL pulse.)

AU = An acknowledge given by the uC (the uC brings MDA=0 during the 9th MCL pulse.)

NA = No acknowledge (this signifies the end of data being read from the W81C180.)

SP = Stop (MDA from 0 change to 1 while MCL=1)

For example, for the uC to read the W81C180's StatusRegister0 only and the value is E9h:

ST	11101001	AW	SR0 (8)	NA	SP

ST=Start AW=W81C180 Acknowledge AU= uC Acknowledge NA=No Acknowledge SP=Stop

SR0 (8) = Status Register 0 (8 bits) (MSB 1st) 11101001=W81C180's Read Address

W81C180 INTERRUPTS:

The NINT pin will be enabled and disabled under the following actions:

ENABLE INTERRUPT	DISABLE INTERRUPT
Any USB port changes status (connect/disconnect.)	After the uC reads the StatusRegisters.
Downstream resume	After the uC reads the StatusRegisters.
Endpoint 1 data received	After endpoint 1's FIFO is read.
Endpoint 0 data received	After the uC reads the StatusRegisters.
Turnaround time-out	After the uC reads the StatusRegisters.
Suspend (no activity) on the USB bus	After the uC reads the StatusRegisters.
Reset sent from upstream	After the uC reads the StatusRegisters.
Babble or loss of data on the USB bus	After the uC reads the StatusRegisters.
OCP tripped	After the uC reads the StatusRegisters.

REACTING TO W81C180 INTERRUPTS:

Since there is no condition which requires immediate attention by the uC, the NINT pin does not necessarily have to be used. The uC can access the W81C180 in a number of possible ways:

- Do not use the NINT pin. Read the Status Register 0 periodically, i.e. every vertical refresh.
- Have the NINT pin go to any pin on the uC, poll that pin periodically and read the W81C180 Status registers when it is enabled.
- Have the NINT pin go to an interrupt pin to the uC and read the W81C180 Status registers when it is enabled.

USB RESET:

The W81C180 handles the USB reset function independently from the uC. If a Single Ended Zero (SE0) is detected on the upstream port (port0) for greater then 2.5us, then the SE0 is transmitted to all configured ports and the interrupt is enabled. The uC should then disable all downstream ports, reset its address to 0, and enter the active state.

USB SUSPEND:

If there is no upstream activity for 3msec then the SUSPEND flag is set and the interrupt enabled. The uC is not required to perform any functions during a USB suspend. The W81C180 stops sending low speed keep alive EOP's when in the suspend state.

USB RESUME:

The suspend mode can be disabled by a 'resume'. The resume can occur by four methods.

- The host can send a resume to all ports by placing a 0 (K state) on the bus. The W81C180 sees the resume, disables the SUSPEND flag, and enables the interrupt. In this case, the uC does not have to perform any functions.
- The host can reset the bus.
- The uC can initiate a resume by setting URESUME in the Control Register which will cause a K state to be sent to all ports. To un-resume, the uC must clear the URESUME bit in the Control Register.
- A downstream port can issue a resume by sending a K state upstream. When the W81C180 senses this K state, it sets the REC_RES flag and interrupt. The uC then has to set the URESUME bit to do a global resume as described above.

USB REPEATER:

The W81C180 controls the traffic between the upstream (port0) and downstream (ports1,2,3,4) ports without uC intervention. If a 'Start of Packet' SOP is seen on port0, and no other port is transmitting, then the W81C180 will transmit the incoming data to all enabled high speed ports until an 'End of Packet' (EOP) is sent (an EOP is a SE0 for 2 bit times followed by a J state.) The EOP from port0 is sent to the enabled ports as well.

If a SOP is seen on an enabled downstream port, any no other port is transmitting, then its data is sent to port0 until an EOP is received which is also sent to port0.

USB FRAME TIMER:

The W81C180 contains a 1ms timer which is synchronized to the 'Start of Frame' (SOF) packet sent from the host every 1ms. If the W81C180 is waiting for an EOP from a downstream port when the SOF is about to approach, it will disable the port, send an EOP upstream, set the babble/LOA (loss of activity) flag, and enable the interrupt. The uC will then have to unconfigure the port which caused the error, and inform the host via the Interrupt Transfer.

BABBLE AND LOST OF ACTIVITY (LOA)

If a babble or LOA is found by reading the status registers, then the uC must disable the port which caused it. It must then set the appropriate bit in the Host_Sta byte and send that byte to the endpoint 1 FIFO for the host. The uC will continue to send this byte, after 'DAVEP1' =1, until the host sends a ClearPortFeature via a Control Transfer to the hub's endpoint 0.

PORT STATUS:

If any downstream port changes state (attached/detached) for >2.5us, then the port flag is set and the interrupt enabled. The uC will then have to inform the host that a change has occurred via endpoint 1.

LOW SPEED DETECTION:

The W81C180 detects if a port is high speed (HS) or low speed (LS) and sets the appropriate flag. When the port is configured, the uC has to configure it as a HS or LS port and inform the host when asked. The W81C180 will only transmit data from the host to a LS port if the data is preceded by the LS PID and the port is enabled.

LOW SPEED KEEP ALIVE:

Before every SOF, the W81C180 will transmit two LS single ended zeros (SEO's) to all enabled LS ports, unless the hub is in the suspend mode.

USB PHASE LOCK LOOP (PLL):

The W81C180's PLL is synchronized to the J-K state from port0 and assures that the data from the host is stored into memory accurately.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	LIMIT
Supply Voltage (Vcc to Vss)	5.5V
Analog Input Voltage	Vss-0.5V to Vcc+0.5V
Digital Input Voltage	Vss-0.5V to Vcc+0.5V
Power Dissipation	TBD
Ambient Operating Temperature	0^{o}C to 70^{o}C
Lead Temperature (Soldering, 10 sec)	250^{o}C

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 5V +/-5%, Ta=0° to 70°C

PARAMETER	Symbol	Conditions	Min	Max	Unit
VCC Supply Current	Icc			TBD	mA
Logic Output High	VOH	Io≥24ma	2.5	VCC	V
Logic Output Low	VOL	Io≥6ma		0.4	V
Logic Input Leakage Current		Ta=70°C		10	uA
Serial Interface Frequency				300k	Hz
USB CHARACTERISTICS					
Leakage Current:					
Hi-Z State Output Leakage	ILO	V< V IN <3.3 V	-10	+10	uA
Input Levels:					
Differential Input Sensitivity	VDI	|(D+)-(D-)|	0.2		V
Single Ended Signal "0"	VSE0		0.8	2.0	V
Differential Common Mode Range	V_{CM}	Includes VDI range	0.8	2.5	
Output Levels:					
Driver Output Low	VOLU	RL of 1.5 kΩ to 3.6 V		0.3	V
Driver Output High	VOHU	RL of 15 kΩ to GND	2.8	3.6	V
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V
Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
Full Speed Timings:					
PARAMETER	**Symbol**	**Conditions**	**Min**	**Max**	**Unit**
Output Rise/Fall Times	t R /t F	Note 1, 4 (C_L= 50 pF)	4	20	ns
Source Differential Driver Jitter to Next Transition / to Paired Transition	t DJ1 /tDJ2	Note 2, 3	-4 /-2	4 /2	ns ns
Differential to EOP transition Skew	t_{DEOP}	Note 3	-2	5	ns
Hub Differential Data Delay(without cable)	t HDD2	Note 2,3,5		40	ns
Hub Differential Driver Jitter to Next Transition / to Paired Transition (including cable)	t HDJ1 / t HDJ2	Note 2,3,5	-3 / -1	3 /1	ns
Data bit width distortion after SOP	t SOP	Note 3,5	-5	3	ns
Hub SE0 Delay Relative to t_{HDD}	t EOPD	Note 3,5	0	15	ns
Hub EOP Output Width Skew	t HESK	Note 3,5	-15	15	ns

Note 1: Measured from 10% to 90% of the data signal.

Note 2: Timing difference between the differential signals.

Note 3: Measured at crossover point of differential data signals.

Note 4: The rising and falling edges should be smoothly transitioning(monotonic)

Note 5: Full Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D+ (DP) data line.

Note 6: Low Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D- (DM) data line.

Note 7: The maximum load specification is the maximum effective capacitive load allowed that meets the target hub VBUS droop of 330 mV.

TYPICAL APPLICATION: