TSM35N03

Preliminary

N-Channel Enhancement Mode MOSFET

TO-252

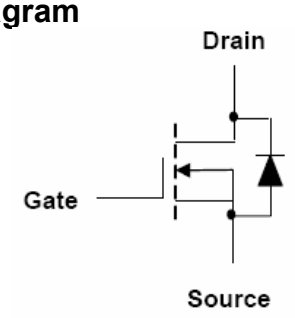
Pin assignment:
1. Gate
2. Drain
3. Source

V_{DS} = 30V
I_D = 50A
$R_{DS\ (on)}$, Vgs @ 10V, Ids @ 30A = 8.5mΩ
$R_{DS\ (on)}$, Vgs @ 4.5V, Ids @ 30A = 13mΩ

Features

- ✧ Advanced trench process technology
- ✧ High Density Cell Design for Ultra Low On-Resistance
- ✧ Fully Characterized Avalanche Voltage and Current
- ✧ Specially Designed for DC/DC Converters and Motor Drivers

Block Diagram



Ordering Information

Part No.	Packing	Package
TSM35N03CP	Tape & Reel	TO-252

Absolute Maximum Rating (T_A = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current		I_D	50	A
Pulsed Drain Current		I_{DM}	350	
Maximum Power Dissipation	T_A = 25 °C	P_D	57	W
	T_A = 100 °C		23	W/°C
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C
Single Pulse Drain to Source Avalanche Energy (V_{DD} = 100V, V_{GS}=10V, I_{AS}=2A, L=10mH, R_G=25Ω)		E_{AS}	300	mJ

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	10	S
Junction-to-case Thermal Resistance	Rθjc	2.2	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	Rθja	50	

Note: 1. Maximum DC current limited by the package
2. 1-in^2 2oz Cu PCB board

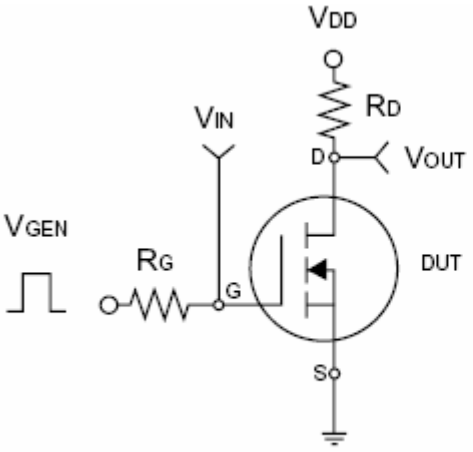
Electrical Characteristics

T_J = 25 °C, unless otherwise noted

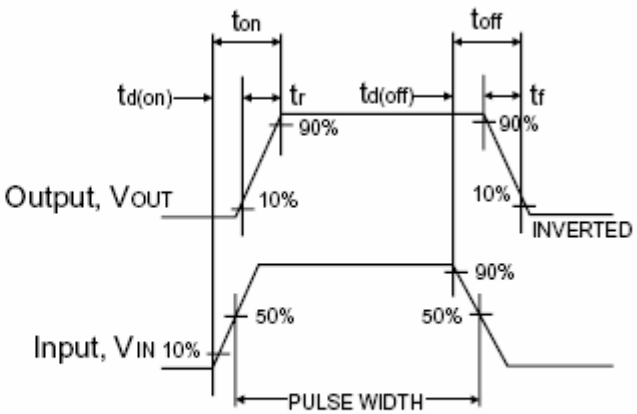
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	30	--	--	V
Drain-Source On-State Resistance	V_{GS} = 4.5V, I_D = 30A	$R_{DS(ON)}$	--	10.0	13.0	mΩ
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 30A	$R_{DS(ON)}$	--	6.5	8.5	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	1.0	1.6	3.0	V
Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V	I_{DSS}	--	--	1.0	uA
Gate Body Leakage	V_{GS} = ± 20V, V_{DS} = 0V	I_{GSS}	--	--	± 100	nA
Gate Resisrance		Rg	--	--	--	
Forward Transconductance	V_{DS} =10V, I_D = 35A	g_{fs}	--	--	--	S
Dynamic						
Total Gate Charge	V_{DS} = 15V, I_D = 35A, V_{GS} = 10V	Q_g	--	24	--	nC
Gate-Source Charge		Q_{gs}	--	5.4	--	
Gate-Drain Charge		Q_{gd}	--	4.0	--	
Turn-On Delay Time	V_{DD} = 15V, R_L = 15Ω, I_D = 1A, V_{GEN} = 10V, R_G = 24Ω	$t_{d(on)}$	--	15	--	nS
Turn-On Rise Time		t_r	--	3.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	36	--	
Turn-Off Fall Time		t_f	--	4.8	--	
Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1940	--	pF
Output Capacitance		C_{oss}	--	312	--	
Reverse Transfer Capacitance		C_{rss}	--	122	--	
Source-Drain Diode						
Max. Diode Forward Current		I_S	--	--	50	A
Diode Forward Voltage	I_S = 20A, V_{GS} = 0V	V_{SD}	--	0.87	1.5	V

Note: 1. pulse test: pulse width <=300uS, duty cycle <=2%

2. Negligible, Dominated by circuit inductance.

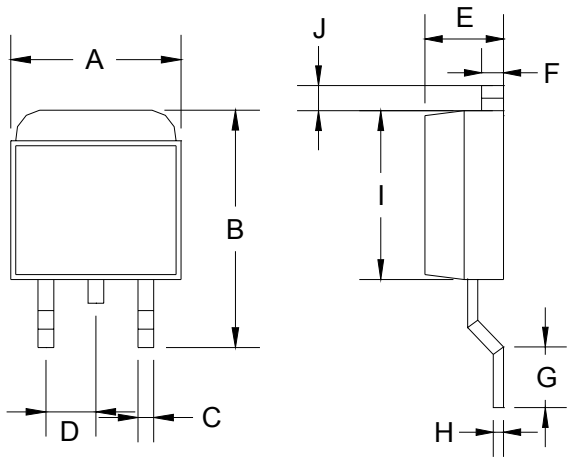


Switching Test Circuit



Switchin Waveforms

TO-252 Mechanical Drawing



TO-252 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.570	6.840	0.259	0.269
B	9.250	10.400	0.364	0.409
C	0.550	0.700	0.022	0.028
D	2.560	2.670	0.101	0.105
E	2.300	2.390	0.090	0.094
F	0.490	0.570	0.019	0.022
G	1.460	1.580	0.057	0.062
H	0.520	0.570	0.020	0.022
I	5.340	5.550	0.210	0.219
J	1.460	1.640	0.057	0.065