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**MSM5259**

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**40-DOT SEGMENT DRIVER**

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**GENERAL DESCRIPTION**

The MSM5259 is a dot matrix LCD segment driver which is fabricated using low power CMOS metal gate technology. This LSI consists of 40-bit shift register, 40-bit latch and 40-bit 4-level driver.

It converts serial data, which is received from an LCD controller LSI, to parallel data and outputs LCD driving waveforms to LCD.

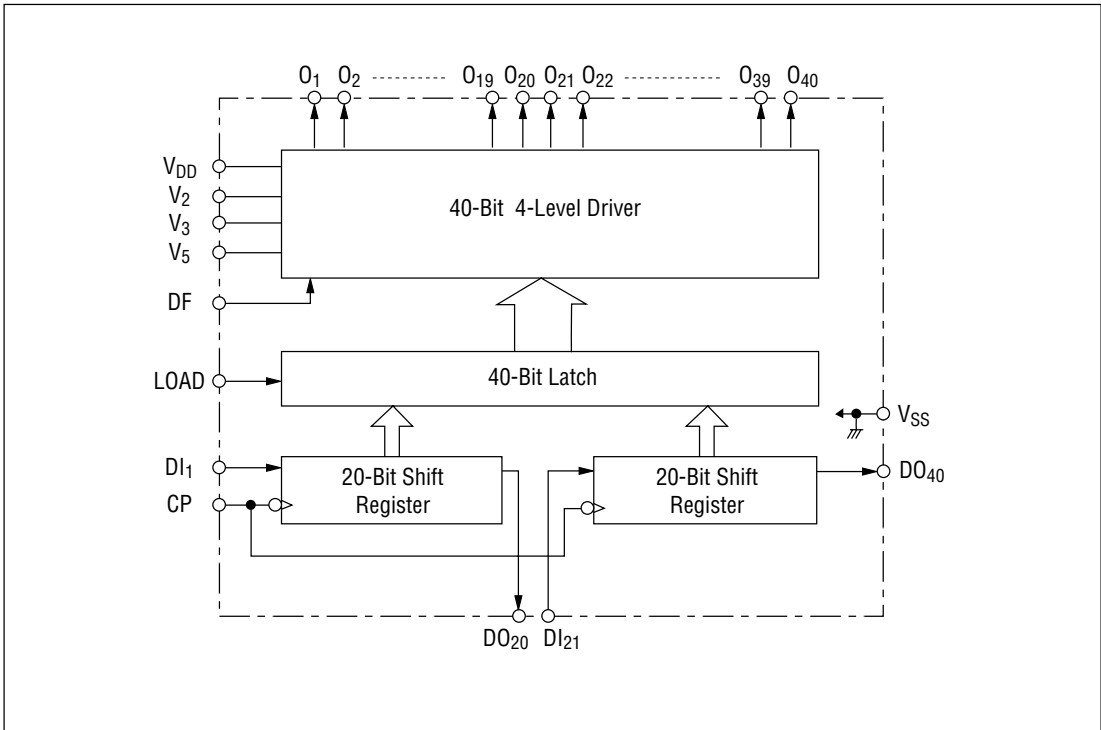
Expansion of the display can be easily made according to the number and structure of characters. Since the 40-bit shift register of this device consists of two 20-bit shift registers, it is possible to allot bits efficiently according to the number of characters.

The MSM5259 can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source. For static operation only, the device is available with a power supply voltage of 2.5V or more.

**FEATURES**

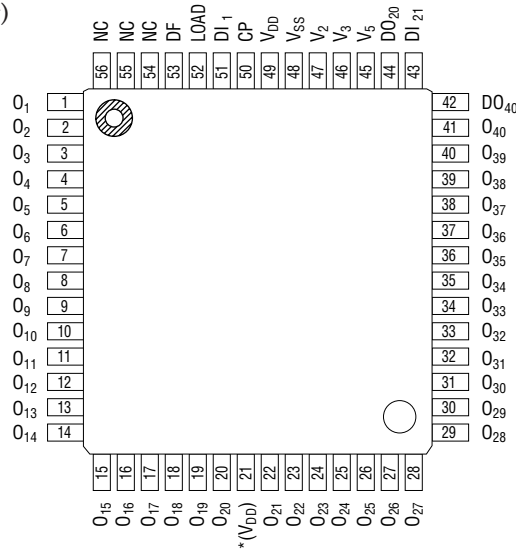
- Supply voltage : 3.5 to 6.0V (Dynamic display)  
: 2.5 to 6.0V (Static display)
- LCD driving voltage : 2.5 to 6.0V (Static display)
- Applicable LCD duty : 1/8 to 1/16
- Interface with MSM6222-xx (Dot matrix LCD controller with 16-dot common driver and 40-dot segment driver)
- Bias voltage can be supplied externally.
- Package options:
  - 56-pin plastic QFP (QFP56-P-910-0.65-K) (Product name : MSM5259GS-K)
  - 56-pin plastic QFP (QFP56-P-910-0.65-L2) (Product name : MSM5259GS-L2)
  - 56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name : MSM5259GS-2K)
  - 56-pin plastic QFP (QFP56-P-910-0.65-2L2) (Product name : MSM5259GS-2L2)

**BLOCK DIAGRAM**



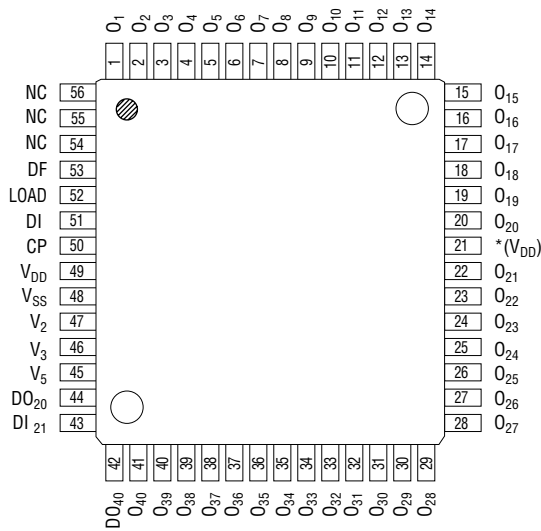
**PIN CONFIGURATION**

(Top View)



NC : No connection

**56-Pin Plastic QFP (Type K)**



NC : No connection

**56-Pin Plastic QFP (Type L)**

\* Do not connect pin 21 to the other signal pins, because the pin is internally connected to  $V_{DD}$ . Do not use pin 21 as a single  $V_{DD}$  signal line. It is permissible to use pin 21 for supplying a higher power of  $V_{DD}$ .

Note : The figure for Type L shows the configuration viewed from the reverse side of the package. Pay attention to the difference in pin arrangement.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	$V_{DD}$	$T_a = 25^\circ\text{C}$	-0.3 to +6.5	V
Supply Voltage (2)	$V_{DD} - V_5$ *1		0 to +6.5	V
Input Voltage	$V_I$		-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{STG}$	—	-55 to +150	$^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Rnage	Unit
Supply Voltage (1)	$V_{DD}$	Dynamic	3.5 to 6.0	V
		Static	2.5 to 6.0	
Supply Voltage (2)	$V_{DD} - V_5$ *1	—	2.5 to 6.0	*2 V
Operating Temperature	$T_{OP}$	—	-30 to +85	$^\circ\text{C}$

\*1  $V_{DD} > V_2 > V_3 > V_5 > V_{SS}$  (Dynamic display)

$V_{DD} = V_3 > V_2 = V_5 = V_{SS}$  (Static display)

For  $V_{DD}$  of less than 3.5V, the device is available only for static operation.

\*2  $V_{DD}$  is the reference potential for the LCD driving voltage.

To determine the LCD driving voltage, change the value of  $V_5$ . (0V Minimum)

## ELECTRICAL CHARACTERISTICS

### DC Characteristics (1)

(V<sub>DD</sub> = 5V±10%, T<sub>a</sub>=-30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V <sub>IH</sub> *1	—	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	V
"L" Input Voltage	V <sub>IL</sub> *1	—	0	—	0.2V <sub>DD</sub>	V
"H" Input Current	I <sub>IH</sub> *1	V <sub>IH</sub> = V <sub>DD</sub>	—	—	1	μA
"L" Input Current	I <sub>IL</sub> *1	V <sub>IL</sub> = 0V	—	—	-1	μA
"H" Output Voltage	V <sub>OH</sub> *2	I <sub>O</sub> = -40μA	4.2	—	—	V
"L" Output Voltage	V <sub>OL</sub> *2	I <sub>O</sub> = 0.4mA	—	—	0.4	V
ON Resistance	R <sub>ON</sub> *3	V <sub>DD</sub> -V <sub>5</sub> = 5V  V <sub>N</sub> -V <sub>O</sub>   = 0.25V *4	—	—	5	kΩ
Supply Current	I <sub>DD</sub>	f <sub>CP</sub> = 0Hz, No load	—	—	0.5	mA

\*1 Applicable to DF, LOAD, DI<sub>1</sub> and DI<sub>21</sub>.

\*2 Applicable to DO<sub>20</sub> and DO<sub>40</sub>.

\*3 Applicable to O<sub>1</sub> to O<sub>40</sub>.

\*4 Dynamic display : V<sub>N</sub> = V<sub>DD</sub> to V<sub>5</sub>, V<sub>2</sub> =  $\frac{2}{3}$  (V<sub>DD</sub> - V<sub>5</sub>), V<sub>3</sub> =  $\frac{1}{3}$  (V<sub>DD</sub> - V<sub>5</sub>)

Static display : V<sub>N</sub> = V<sub>DD</sub> to V<sub>5</sub>, V<sub>3</sub> = V<sub>DD</sub>, V<sub>2</sub> = V<sub>5</sub> = V<sub>SS</sub>

### DC Characteristics (2)

(Only for static operation)

(V<sub>DD</sub> = 3V±0.5V, T<sub>a</sub>=-30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V <sub>IH</sub> *1	—	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	V
"L" Input Voltage	V <sub>IL</sub> *1	—	0	—	0.2V <sub>DD</sub>	V
"H" Input Current	I <sub>IH</sub> *1	V <sub>IH</sub> = V <sub>DD</sub>	—	—	1	μA
"L" Input Current	I <sub>IL</sub> *1	V <sub>IL</sub> = 0V	—	—	-1	μA
"H" Output Voltage	V <sub>OH</sub> *5	I <sub>O</sub> = -40μA	2.2	—	—	V
"L" Output Voltage	V <sub>OL</sub> *5	I <sub>O</sub> = 0.2mA	—	—	0.4	V
ON Resistance	R <sub>ON</sub> *6	V <sub>3</sub> = V <sub>DD</sub> = 3V, V <sub>2</sub> = V <sub>5</sub> = V <sub>SS</sub> = 0V,  V <sub>N</sub> -V <sub>O</sub>   = 0.25V	—	—	10	kΩ
Supply Current	I <sub>DD</sub>	f <sub>CP</sub> = 0Hz, No load	—	—	0.5	mA

\*5 Applied to DO<sub>20</sub> and DO<sub>40</sub>.

\*6 Applied to O<sub>1</sub> to O<sub>40</sub>.

## Switching Characteristics (1)

 $(V_{DD} = 5V \pm 10\%, T_a = -30 \text{ to } +85^\circ\text{C}, C_L = 15\text{pF})$ 

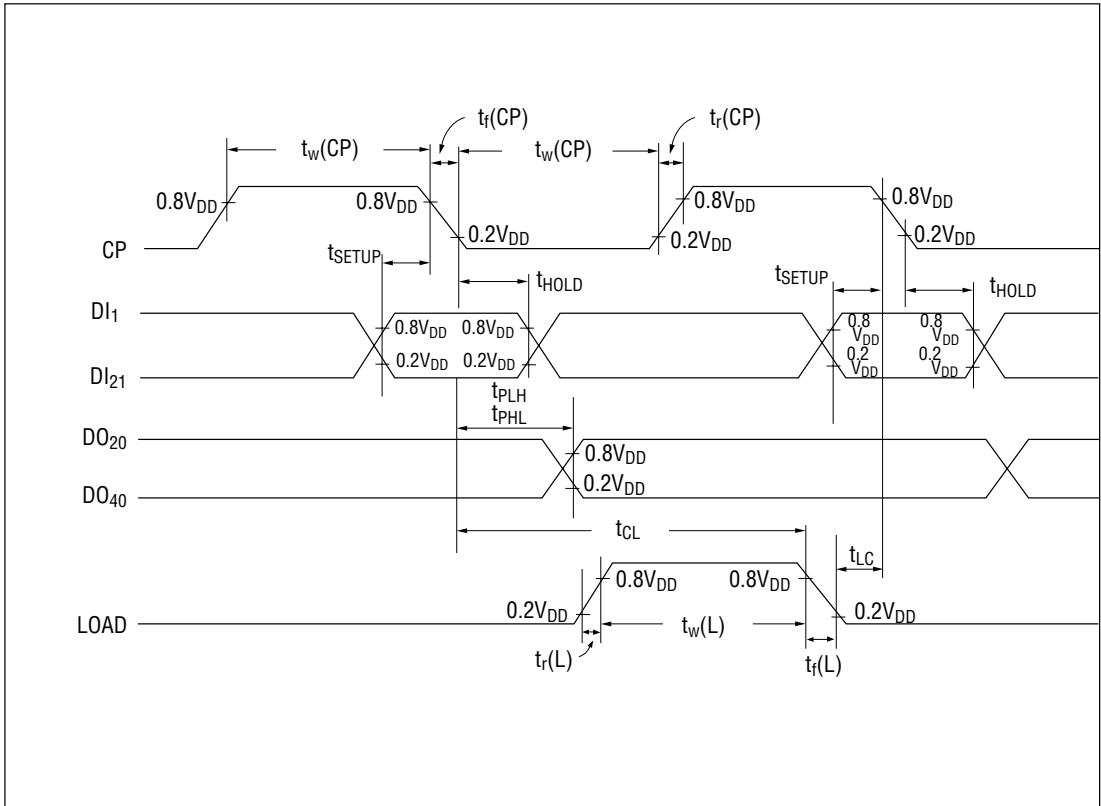
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	$t_{PLH}, t_{PHL}$	—	—	—	250	ns
Clock Frequency	$f_{CP}$	Duty = 50%	—	—	3.3	MHz
Clock Pulse Width	$t_W (CP)$	—	125	—	—	ns
Load Pulse Width	$t_W (L)$	—	125	—	—	ns
Data Set-up Time DI → CP	$t_{SETUP}$	—	50	—	—	ns
Data Hold Time DI → CP	$t_{HOLD}$	—	50	—	—	ns
CP → LOAD Set-up Time	$t_{CL}$	—	250	—	—	ns
LOAD → CP Hold Time	$t_{LC}$	—	0	—	—	ns
CP Rise/Fall Time	$t_r(CP), t_f(CP)$	—	—	—	50	ns
LOAD Rise/Fall Time	$t_r(L), t_f(L)$	—	—	—	1	$\mu\text{s}$

## Switching Characteristics (2)

(Only for static operation)

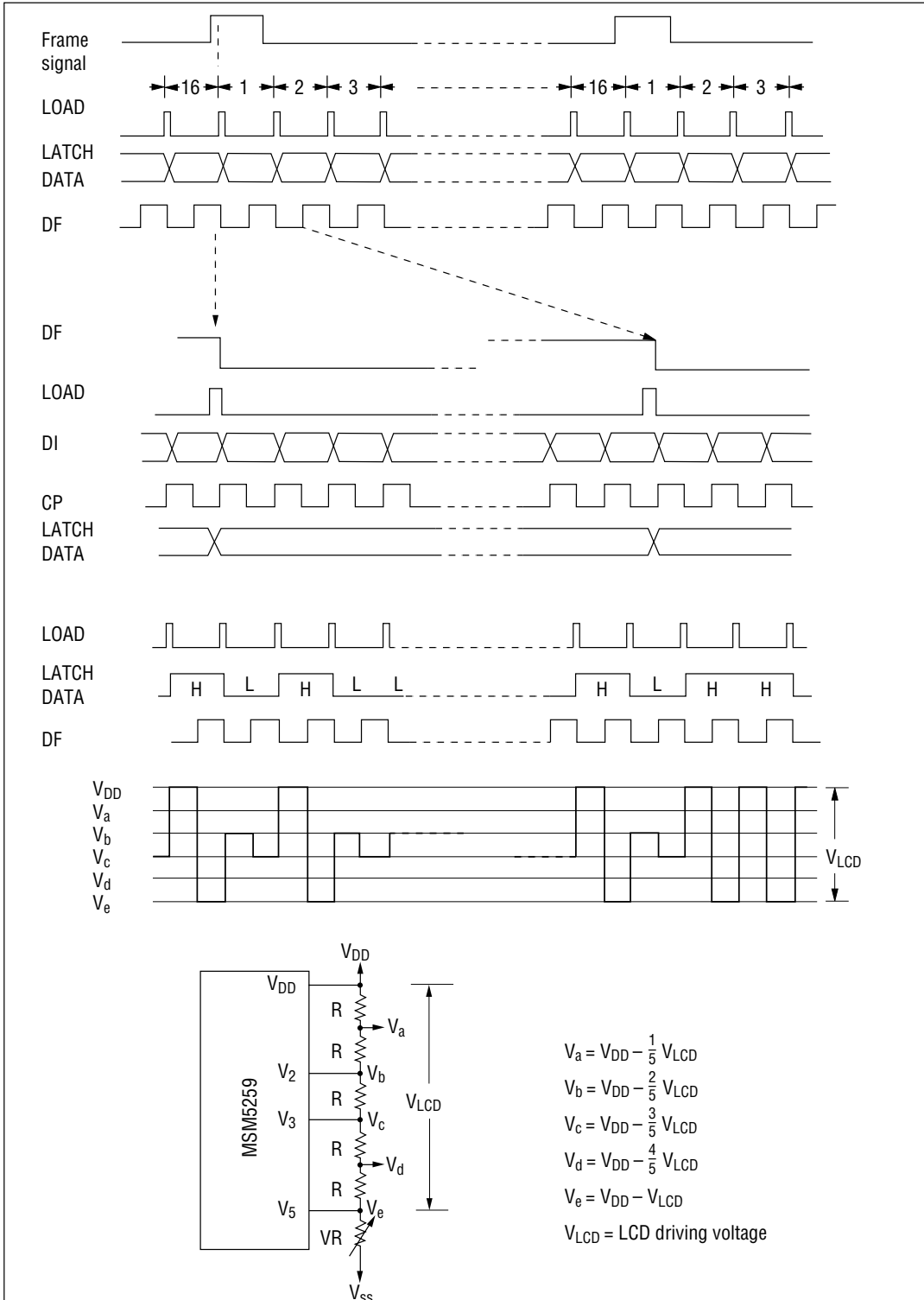
 $(V_{DD} = 3V \pm 0.5V, T_a = -30 \text{ to } +85^\circ\text{C}, C_L = 15\text{pF})$ 

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	$t_{PLH}, t_{PHL}$	—	—	—	800	ns
Clock Frequency	$f_{CP}$	Duty = 50%	—	—	1.0	MHz
Clock Pulse Width	$t_W (CP)$	—	300	—	—	ns
Load Pulse Width	$t_W (L)$	—	300	—	—	ns
DI → CP Set-up Time	$t_{SETUP}$	—	200	—	—	ns
DI → CP Hold Time	$t_{HOLD}$	—	200	—	—	ns
CP → LOAD Set-up Time	$t_{CL}$	—	800	—	—	ns
LOAD → CP Hold Time	$t_{LC}$	—	0	—	—	ns
CP Rise/Fall Time	$t_r(CP)$	—	—	—	1	$\mu\text{s}$
LOAD Rise/Fall Time	$t_r(L), t_f(L)$	—	—	—	1	$\mu\text{s}$



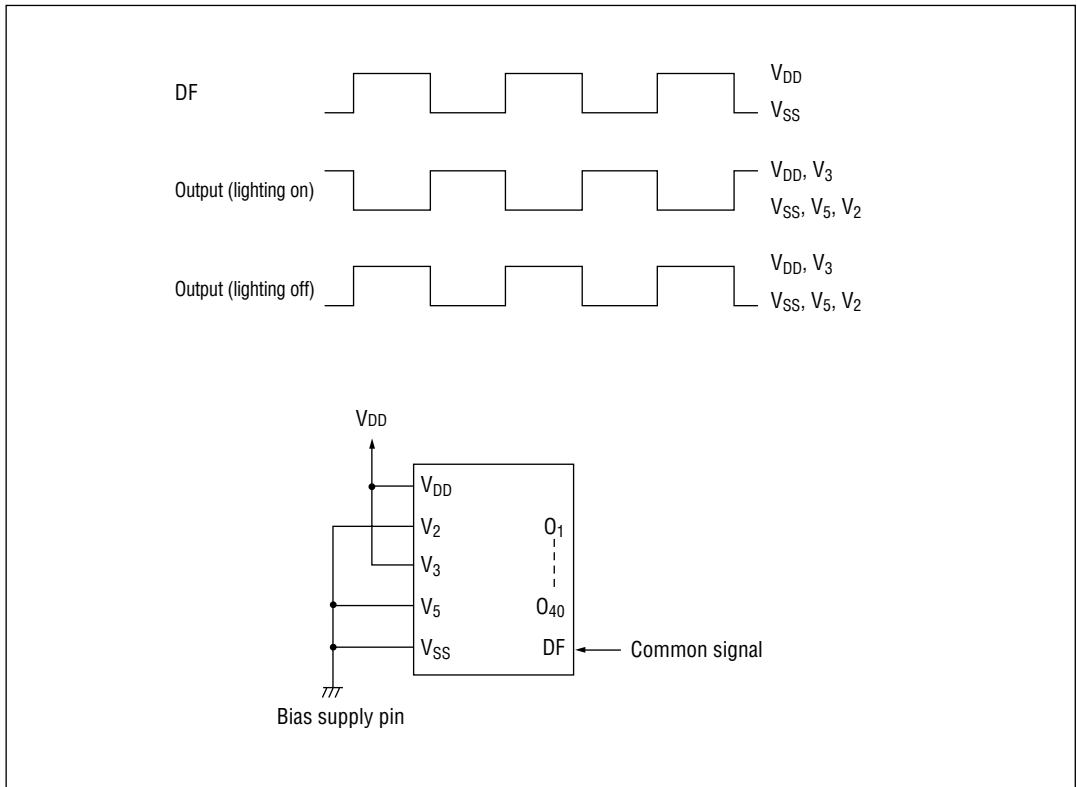
**TIMING DIAGRAM**

1/5 bias, 1/16 duty





Static Display



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

- **DI<sub>1</sub>**  
The data (1st to 20th bit) from the LCD controller LSI is input to 20-bit shift register from DI<sub>1</sub>. (Positive logic)
- **DI<sub>21</sub>**  
Data input to the shift register (21st to 41st bit).  
Connecting DO<sub>20</sub> and DI<sub>21</sub> allows configuration of a 40-bit register.  
If DI<sub>21</sub> is not used, connect this pin to V<sub>SS</sub>.
- **CP**  
Clock pulse input pin for the two 20-bit shift registers. The data is input to the 20-bit shift register at the falling edge of the clock pulse. A data set up time (t<sub>SETUP</sub>) and data hold time (t<sub>HOLD</sub>) are required between the DI<sub>1</sub> and DI<sub>21</sub> signals and a clock pulse.
- **DO<sub>20</sub>**  
20th bit of the shift register contents is output from DO<sub>20</sub>. The data which was input from DI<sub>1</sub> is output from this pin with a delay of the number of bits of the shift register (20), synchronized with the clock pulse. By connecting DO<sub>20</sub> to DI<sub>21</sub>, two 20-bit shift registers can be used as a 40-bit shift register.
- **DO<sub>40</sub>**  
40th bit of the shift register contents is output from DO<sub>40</sub>. The data which was input from DI<sub>21</sub> is output from this pin with a delay of the number of bits of the shift register (20), synchronized with the clock pulse. By connecting DO<sub>40</sub> to the next MSM5259's DI<sub>1</sub>, this LSI is applicable to a wide screen LCD.  
Refer to the application circuit.
- **DF**  
Alternate signal input pin for LCD driving.
- **LOAD**  
Signal for latching the shift register contents is input from this pin. When the LOAD pin is set at "H" level, the shift register contents are transferred to the 40-bit 4-level driver. When LOAD pin is set at "L" level, the last display output data (O<sub>1</sub> - O<sub>40</sub>), which was transferred when LOAD pin was at "H" level, is held.
- **V<sub>DD</sub>, V<sub>SS</sub>**  
Supply voltage pins.  
V<sub>DD</sub> is generally set to 4.0 to 6.0V. V<sub>SS</sub> is a ground pin (V<sub>SS</sub> = 0V)
- **V<sub>2</sub>, V<sub>3</sub>, V<sub>5</sub>**  
Bias supply voltage pins to drive the LCD. Bias voltage divided by the register is usually used as supply voltage source.  
Refer to the application circuit.  
For static operation, connect V<sub>3</sub> to V<sub>DD</sub> and also connect V<sub>2</sub>, V<sub>5</sub>, to V<sub>SS</sub>.

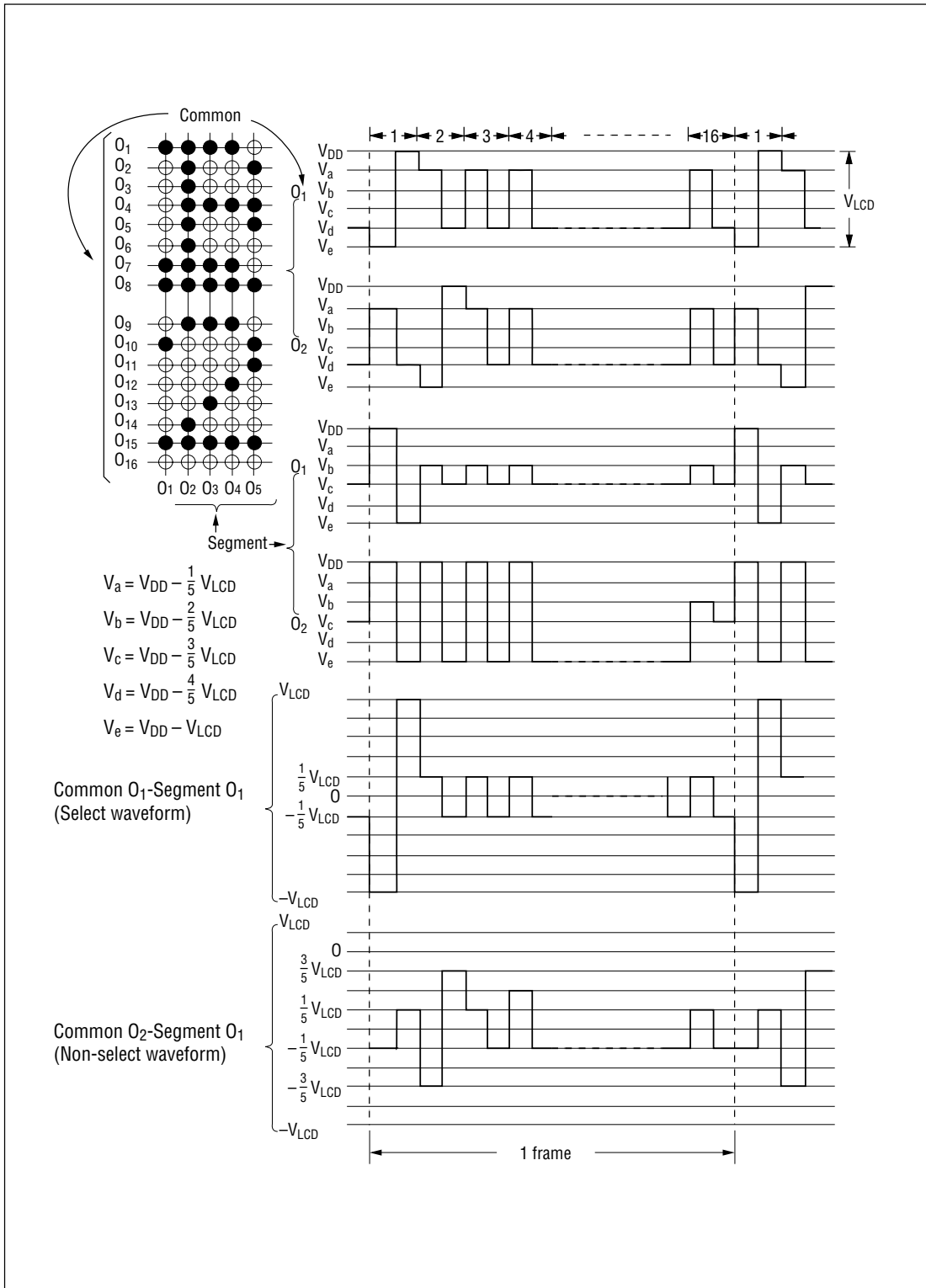
- **O<sub>1</sub> to O<sub>40</sub>**

Display data output pin which corresponds to each data bit in the latch. One of  $V_{DD}$ ,  $V_2$ ,  $V_3$  and  $V_5$  is selected as a display driving voltage source according to the combination of latched data level and DF signal. (Refer to the truth table below.)

**Truth Table**

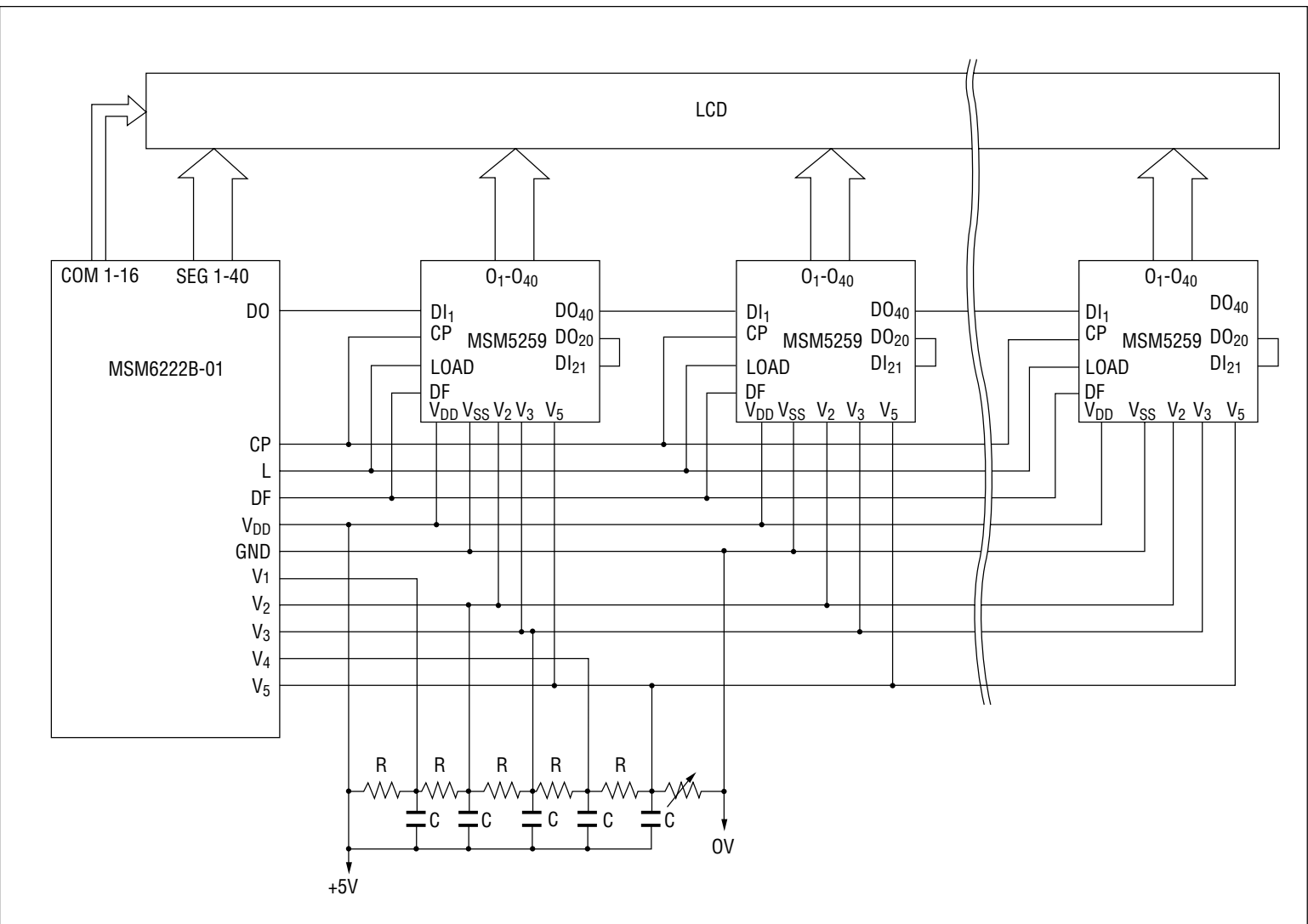
Latched data	DF	Driver output level
"H" (Select)	H	$V_5$
	L	$V_{DD}$
"L" (Non-select)	H	$V_3$
	L	$V_2$

LCD Driving Waveform (1/5 bias, 1/16 duty)



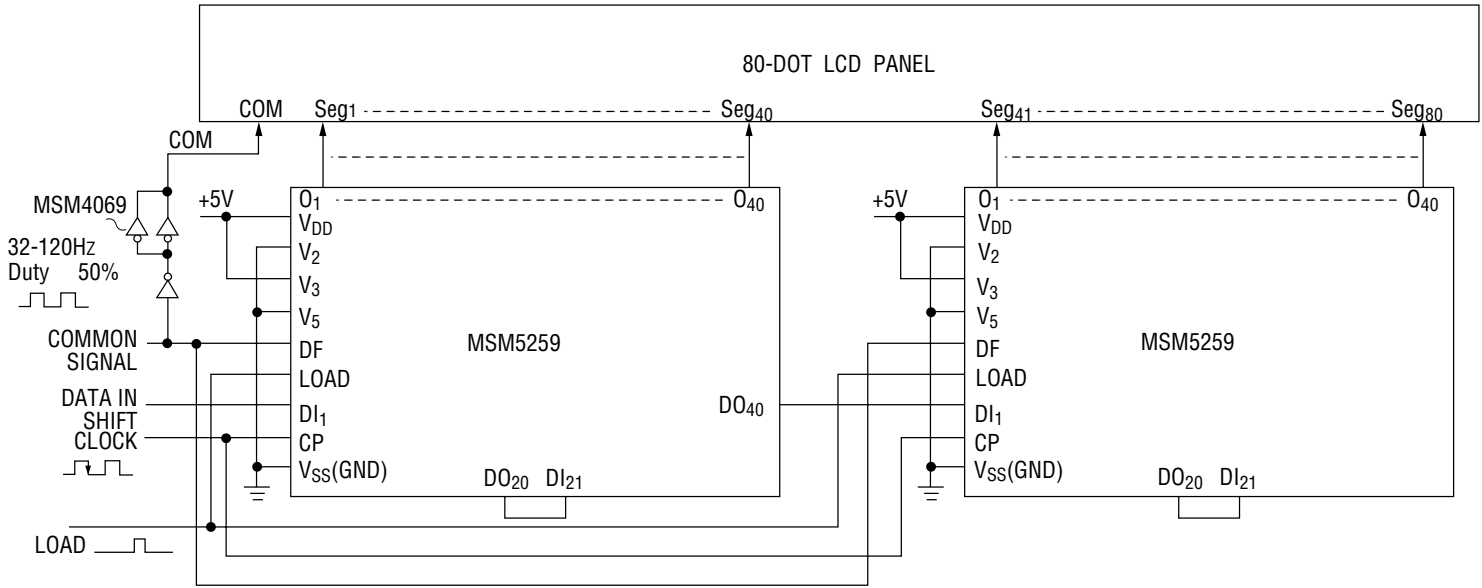
**APPLICATION CIRCUITS**

(Connected to MSM6222B-01 LCD Controller)



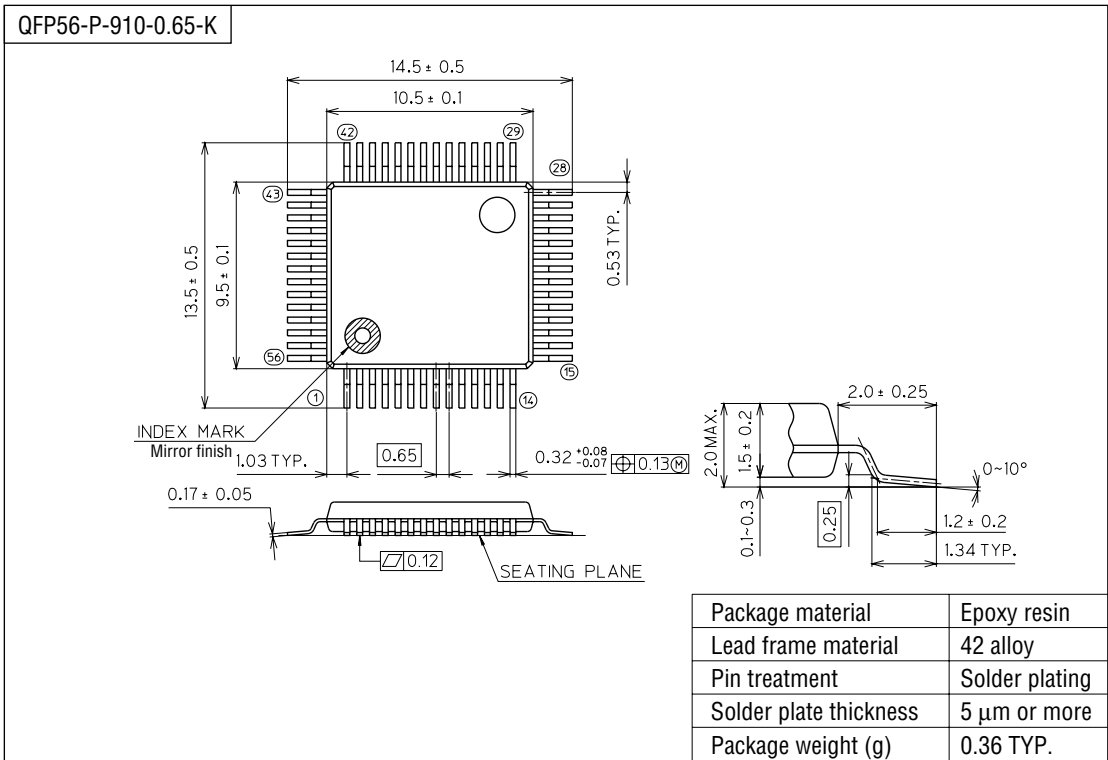
Application Circuit for Static Display

The MSM5259 is applicable to a static LCD by setting  $V_2$  and  $V_5$  at ground level, connecting  $V_3$  to  $V_{DD}$  and inputting COMMON SIGNAL to DF pin.  
 This sample application circuit below is the case when the MSM5259 is applied to an 80-bit LCD panel by connecting two MSM5259s in series.



**PACKAGE DIMENSIONS**

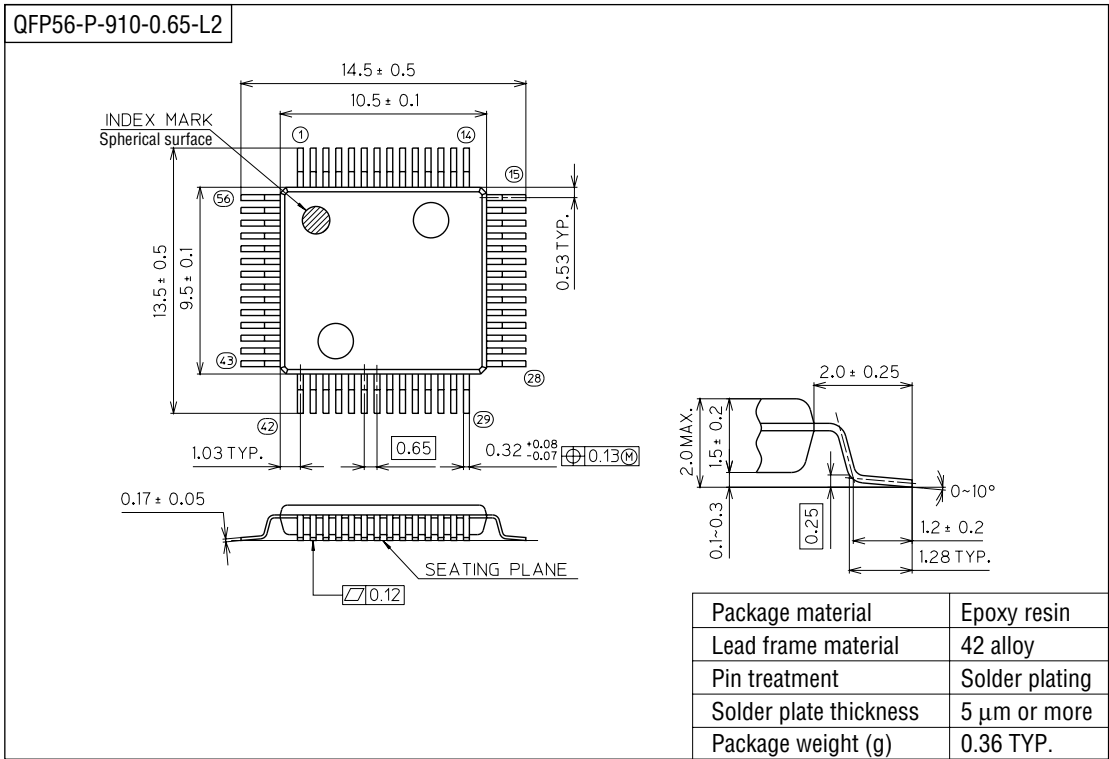
(Unit : mm)



**Notes for Mounting the Surface Mount Type Package**

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

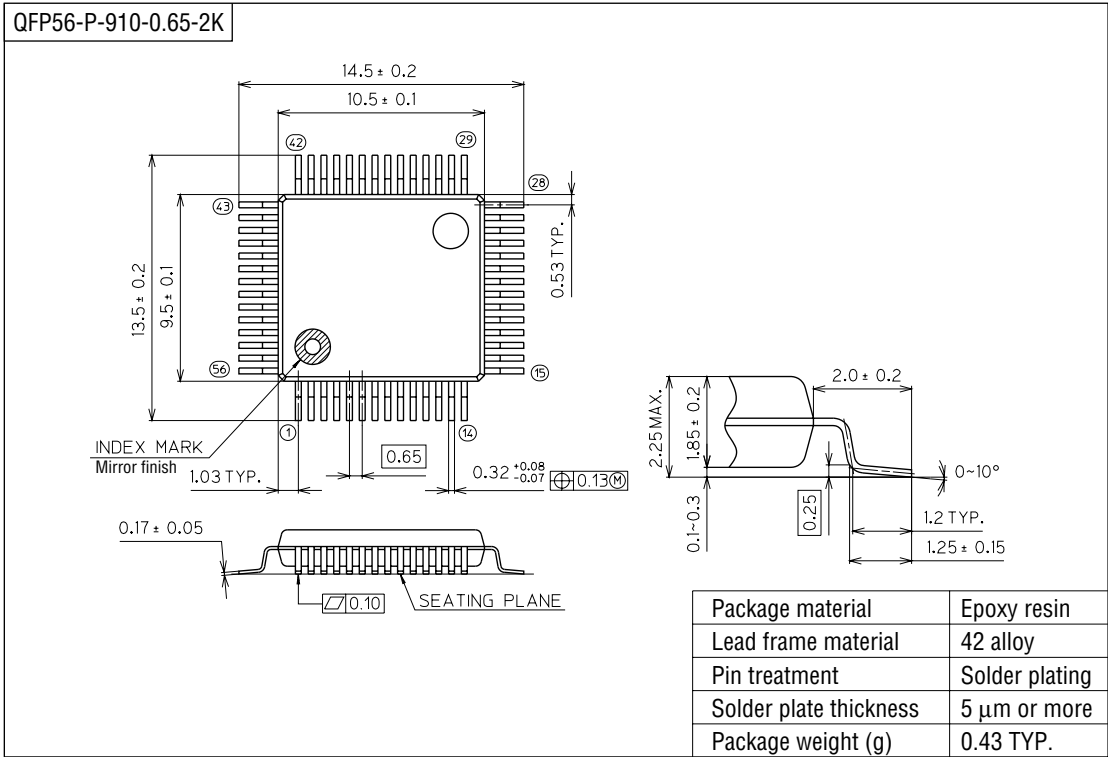


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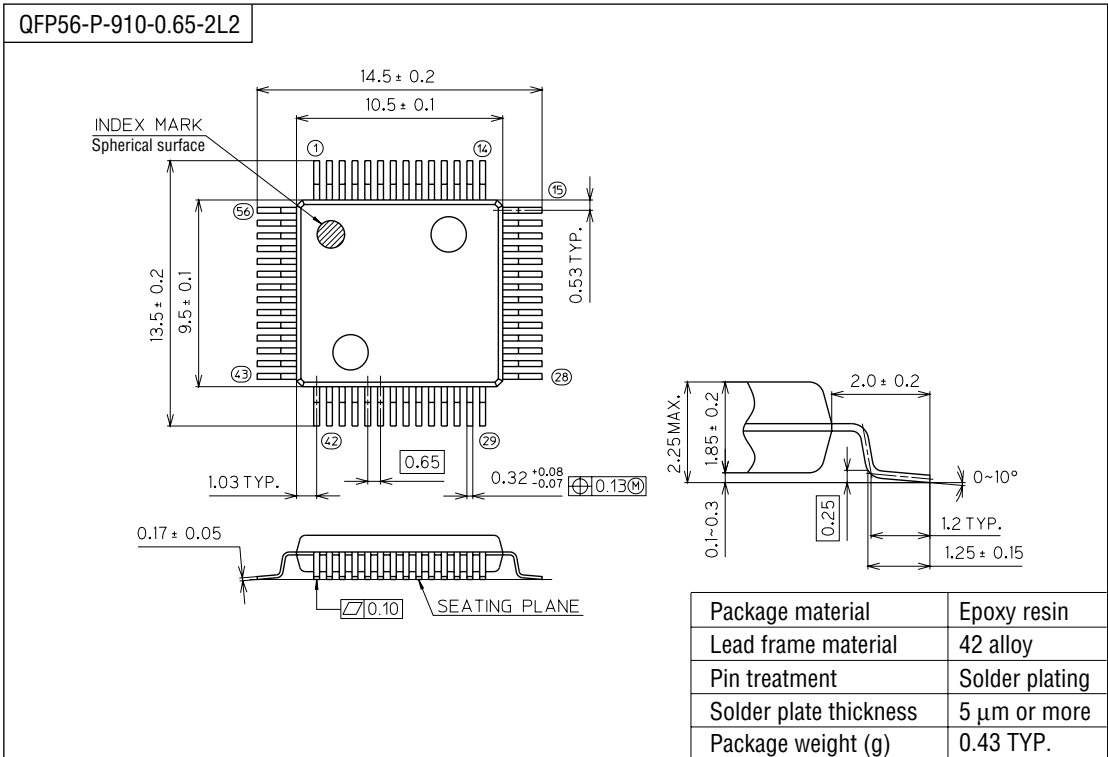
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