T-49-19-08
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CMOS 8-BIT MICROCONTROLLERS
TMP90C840N/TMP90C841N
TMP90C840F

1. OUTLINE AND CHARACTERISTICS

The TMP90C840 is a high-speed advanced 8-bit micro controller applicable to a variety of equipment.
With its 8-bit CPU, ROM, RAM, A/D converter, multi-function timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP90C840 allows the expansion of external memories for programs (up to 56K bytes) and data (1M bytes).

The characteristics of the TMP90C840 include:

(1) Efficient instruction system
  163 basic instructions
  Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions
(2) Minimum instruction executing time: 400 ns (at 10 MHz oscillation frequency)
(3) Internal ROM: 8K bytes
(4) Internal RAM: 256 bytes
(5) Memory expansion
  External program memory: 56K bytes
  External data memory: 1M bytes
(6) Super-precision 8-bit A/D converter (6 channels)
(7) General-purpose serial interface (1 channel)
  Asynchronous mode, I/O interface mode
(8) Multi-function 16-bit timer/event counter
(9) Four 8-bit timers
(10) 2-channel stepping motor control port
(11) Input/Output ports (54 pins)
(12) Interrupt function: 10 internal interrupts and 4 external interrupts
(13) Micro Direct Memory Access (DMA) function (11 channels)
(14) Watchdog timer
(15) Standby function (4 HALT modes)
(16) Complementary metal oxide semiconductor (CMOS)
(17) Single power source

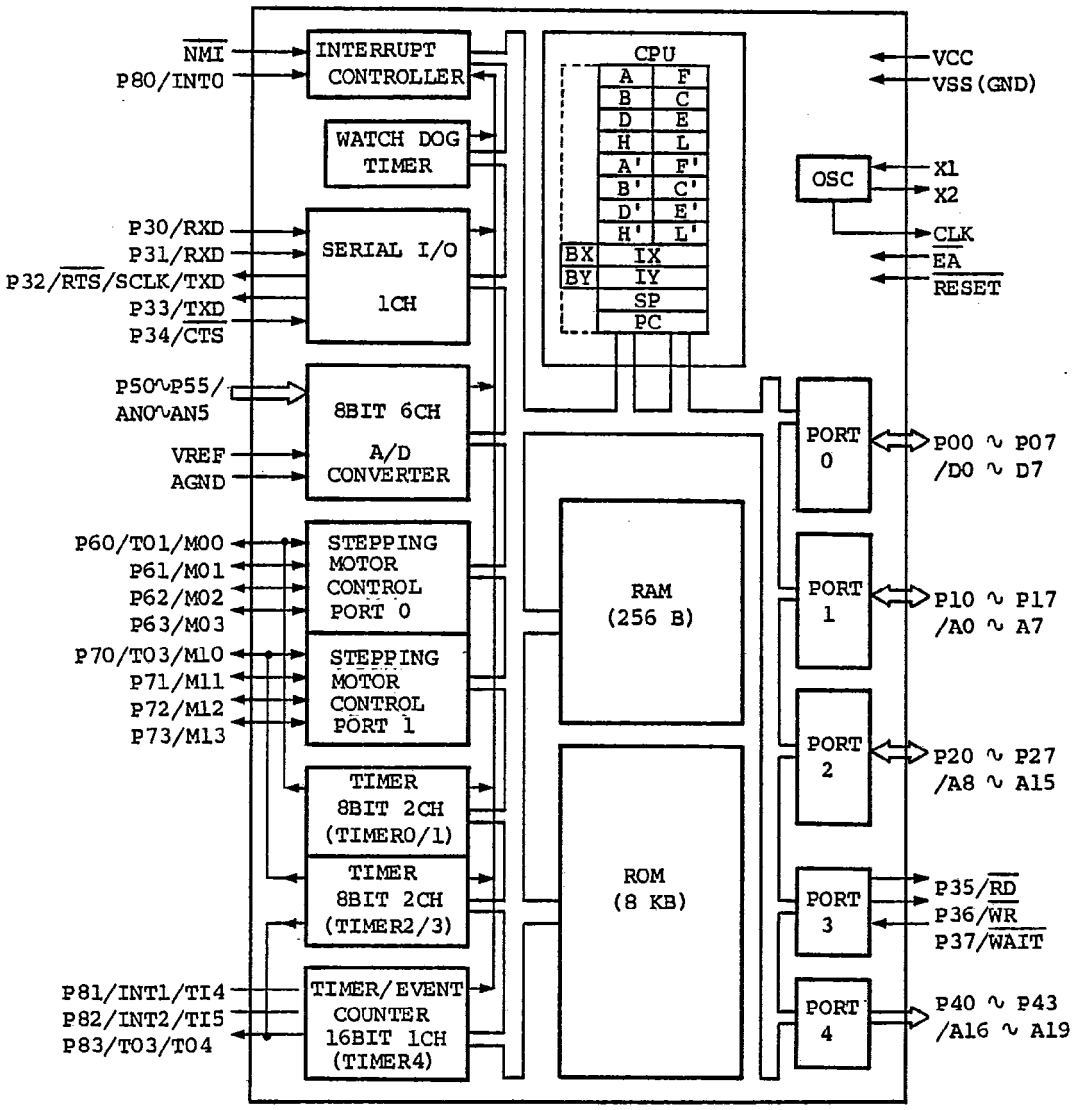

Fig. 1 TMP90C840 Block Diagram

2. PIN ARRANGEMENT AND FUNCTIONS

The arrangement of input/output pins, their names and functions are described below.

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2.1 Pin Arrangement

Fig. 2.1 shows where the input/output pins are located in the TMP90C840.

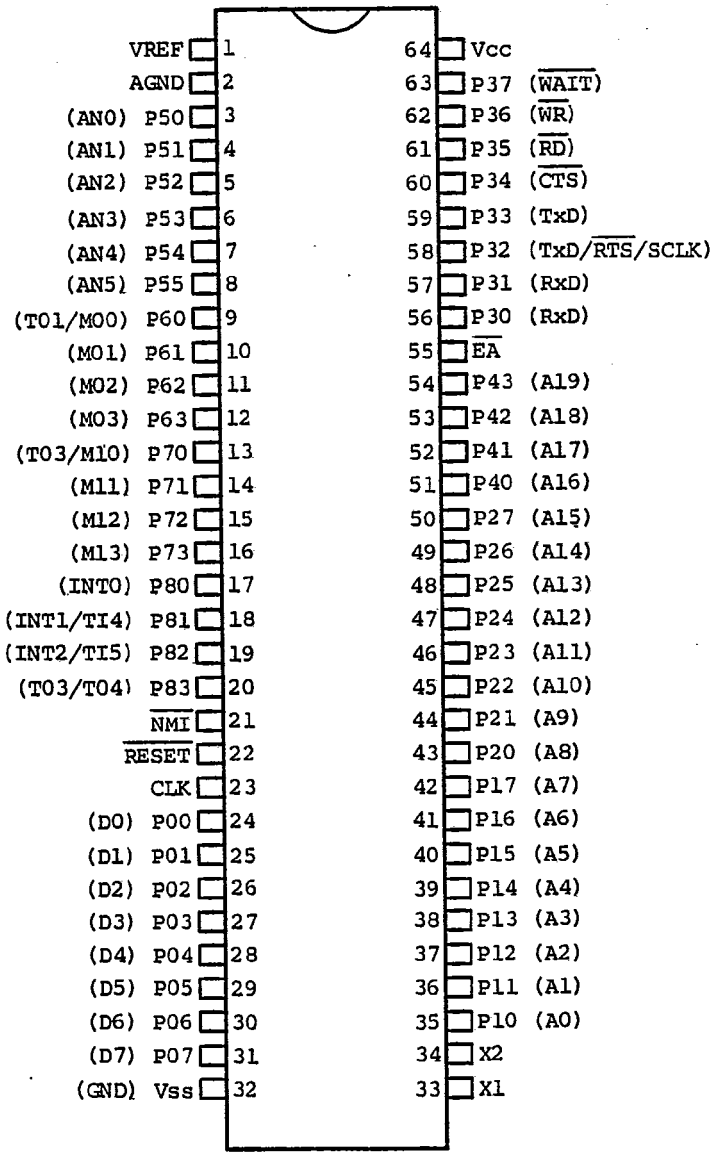

Fig. 2.1-(1) Pin Arrangement (Shrink Dual Inline Package)

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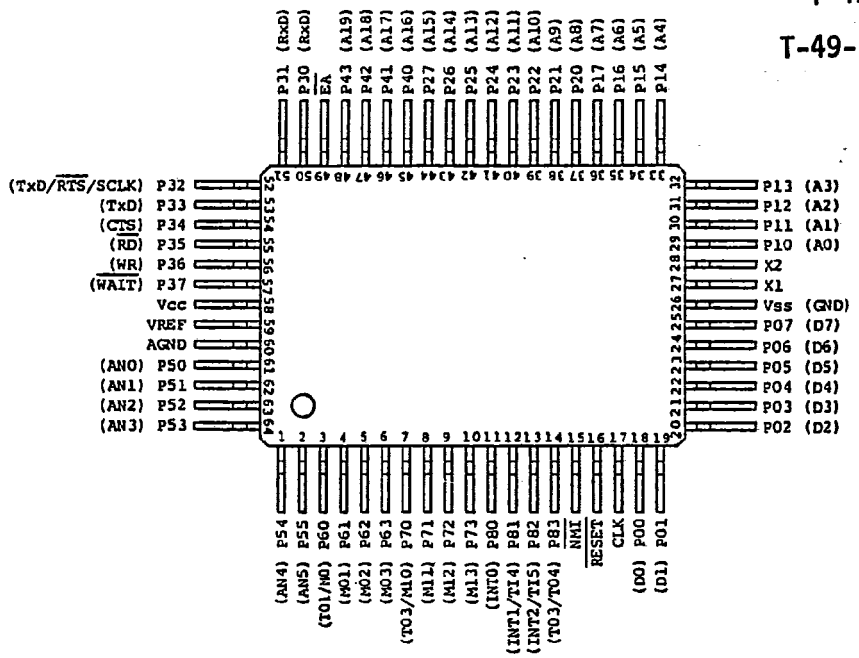

Fig. 2.1-(2) Pin Arrangement (Flat Package)

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2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

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Table 2.2 Pin Names and Functions

Pin Name	No. of pins	I/O 3 states	Function
P00 - P07 /D0 - D7	8	I/O 3 states	Port 0: 8-bit I/O port that allows selection of input/output on byte basis Data bus: Also functions as 8-bit bidirectional data bus for external memory
P10 - P17 /A0 - A7	8	I/O /Output	Port 1: 8-bit I/O port that allows selection on byte basis Address bus: The lower 8 bits function as address bus for external memory
P20 - P27 /A8 - A15	8	I/O /Output	Port 2: 8-bit I/O port that allows selection on bit basis Address bus: The upper 8 bits function as address bus for external memory
P30 /RxD	1	Input	Port 30: 1-bit input port Serial data receiving
P31 /RxD	1	Input	Port 31: 1-bit input port Serial data receiving
P32 /TxD /$\overline{\text{PTS}}$ /SCLK	1	Output	Port 32: 1-bit output port Serial data transmission Request serial data transmission Serial clock output
P33 /TxD	1	Output	Port 33: 1-bit output port Serial data transmission
P34 /$\overline{\text{CTS}}$	1	Input	Port 34: 1-bit input port Capable of serial data transmission
P35 /$\overline{\text{RD}}$	1	Output	Port 35: 1-bit output port Read: Generates strobe signal for reading external memory
P36 /$\overline{\text{WR}}$	1	Output	Port 36: 1-bit output port Write: Generates strobe signal for writing into external memory
P37 /$\overline{\text{WAIT}}$	1	Input	Port 37: 1-bit input port Wait: Input pin for connecting slow access memory or peripheral LSI

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Pin Name	No. of pins	I/O 3 states	Function
P40 - P43 /A16 - A19	4	Output	Port 4: 4-bit output port that allows selection of port/address bus on bit basis Address bus: Also functions as address bus for external memory (4 bits of bank address)
P50 - P55 /AN0 - AN5	6	Input	Port 5: 6-bit input port Analog input: 6 points for analog input to A/D converter
VREF	1		Input of reference voltage to A/D converter
AGND	1		Ground pin for A/D converter
P60 - P63 /M00 - M03 /T01	4	I/O /Output /Output	Port 6: 4-bit I/O port that allows I/O selection on bit basis Stepping motor control port 0 Timer output 1: Output of Timer 0 or 1
P70 - P73 /M10 - M13 /T03	4	I/O /Output /Output	Port 7: 4-bit I/O port that allows I/O selection on bit basis Stepping motor control port 1 Timer output 3: Output of Timer 2 or 3
P80 /INT0	1	Input	Port 80: 1-bit input port Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable)
P81 /INT1 /T14	1	Input	Port 81: 1-bit input port Interrupt request pin 1: interrupt request pin (Level/falling edge is programmable) Timer input 4: Counter/capture trigger signal for Timer 4
P82 /INT2 /T15	1	Input	Port 82: 1-bit input port Interrupt request pin 2: rising edge interrupt request pin Timer input 5: capture trigger signal for Timer 4
P83 /T03/T04	1	Output	Port 83: 1-bit output port Timer output 3/4: Output of Timer 3/4
NMI	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin

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Pin Name	No. of pins	I/O 3 states	Function
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is a high-level while resetting.
EA	1	Input	External access: Connects with Vcc pin in the TMP90C840 using internal ROM, and with GND pin in the TMP90C841 with no internal ROM.
RESET	1	Input	Reset
X1/X2	2	Input/ Output	Pin for quartz crystal oscillator
Vcc	1		Power supply pin (+5V)
Vss(GND)	1		Ground pin (0V)

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3. OPERATION

This chapter describes the functions and the basic operations of the TMP90C840 in every block.

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3.1 CPU

The TMP90C840 incorporates a high-performance 8-bit CPU. This CPU improves its speed of processing, addressing and executing instructions compared to the conventional 8-bit versions.
This section describes the CPU functions available to the programmer.

3.1.1 Memory map

The TMP90C840 supports a program memory of up to 64K bytes and a data memory of maximum 1M bytes.
The program memory may be assigned to the address space from 00000H to 0FFFFH, while the data memory can be allocated to any address from 00000H to FFFFFH.

(1) Internal ROM
The TMP90C840 internally contains an 8K-byte ROM. The address space from 0000H to 1FFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.
The addresses 0010H to 007FH in this internal ROM area are used for the entry area for the interrupt processing.

(2) Internal RAM
The TMP90C840 also contains a 256 byte RAM, which is allocated to the address space from FEC0H to FFBFH. The CPU allows the access to a certain RAM area (FF00H to FFBFH, 192 bytes) by a short operation code (opcode) in a "direct addressing mode".
The addresses from FF10H to FF7FH in this RAM area can be used as parameter area for micro DMA processing (and for any other purposes when the micro DMA function is not used).

(3) Internal I/O
The TMP90C840 provides a 48-byte address space as an internal I/O area, whose addresses range from FFC0H to FFEFH. This I/O area can be accessed by the CPU using a short opcode in the "direct addressing mode".

Fig. 3.1 (1) is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

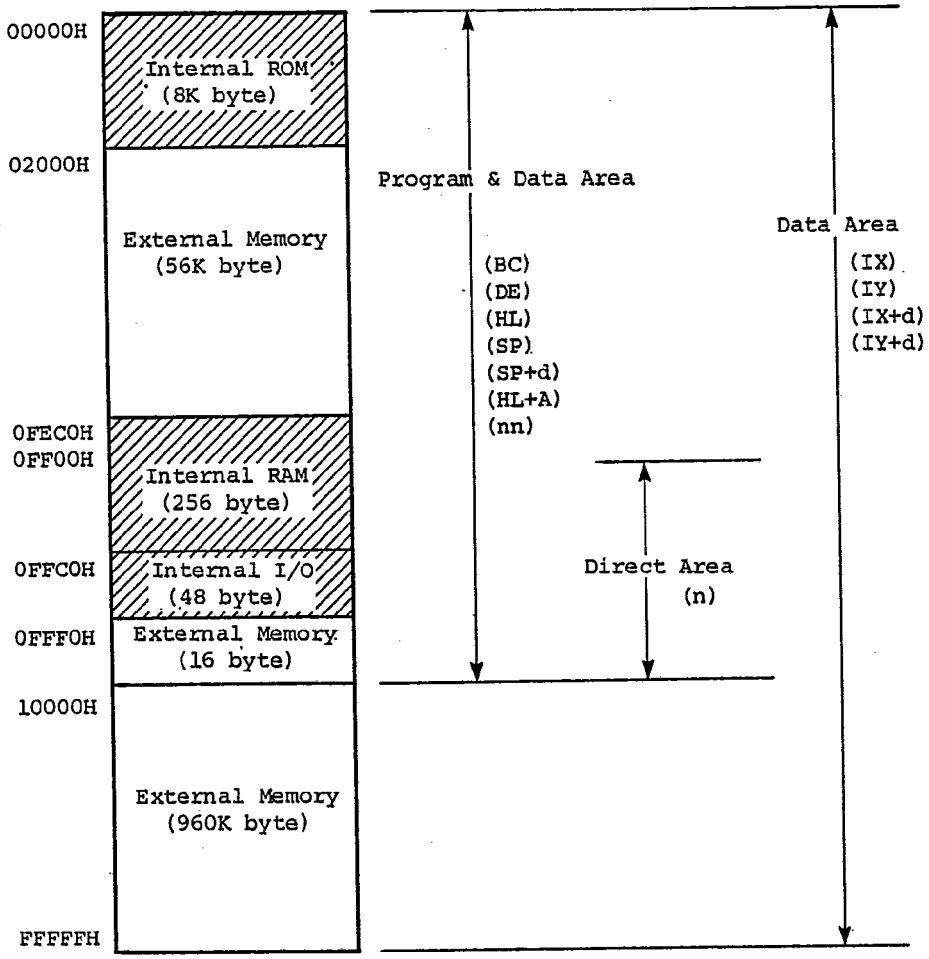

Fig. 3.1 (1) Memory Map

3.1.2 Registers

Fig. 3.1 (2) shows the configuration of registers. T-49-19-59

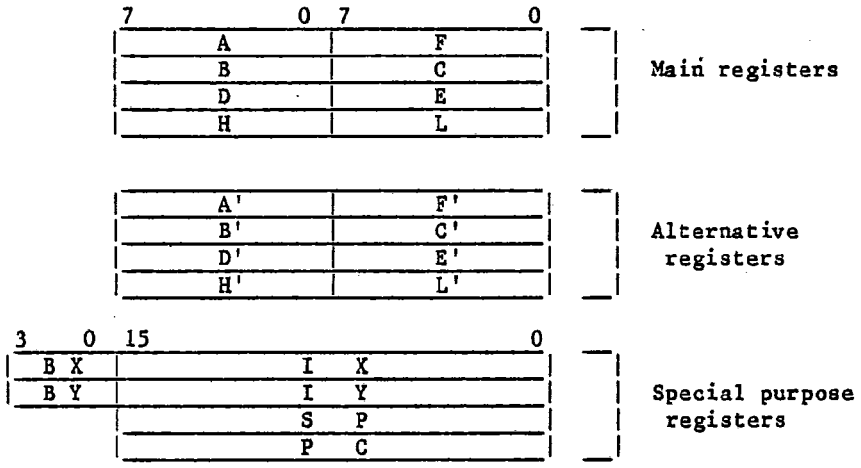

Fig. 3.1 (2) Configuration of Registers

The TMP90C840 uses main registers, alternative registers and dedicated registers. The main registers and the alternative registers are allowed to be exchanged of their contents by a register exchange instruction.

(1) Register A
This is an 8-bit register used mainly for 8-bit arithmetic and logic operations.

(2) Register F
This is an 8-bit register that stores the status of operation results. Configuration of register F is shown in Fig. 3.1 (3).

	7	6	5	4	3	2	1	0	
MSB	S	Z	IFF	H	X	P/V	N	C	LSB

Fig. 3.1 (3) Configuration of Register F

- o Sign flag (S)
  The sign flag is set to "1" when the arithmetic result is negative. It stores the contents of the most significant bit (MSB) of the arithmetic and logic unit (ALU).
- o Zero flag (Z)
  Z flag is set to "1" when the all bits of the ALU after operation are "0".

- o Parity/Overflow flag (P/V)
  This flag has two functions. One is to indicate the parity (P) resulted from a logical opepration (AND, OR, or XOR). It is set to "1" when the result is even, and "0" for odd parity.
  The other is to indicates the overflow (V) in an arithmetic operation (ADD, ADC, SUB, SBC, or CP). The flag is set to "1" when the result cannot be expressed by a signed integral number.
  The P/V flag selects either function according to the instruction.
- o Carry flag (C)
  The flag is set to "1" if a carry or borrow has occurred on the MSB of the ALU.
- o Expansion carry flag (X)
  Like the carry flag (C), it is set to "1" when the MSB of the ALU involves a carry or borrow as a result of an operation except that it applies to a wider range of instructions (e.g., INC rr).
- o Half carry flag (H)
  It is set to "1" when a carry or borrow has occurred on the 4th bit of the lower side in the ALU.
- o Addition/Subtraction flag (N)
  This flag is set to "1" if the executed operation is a subtraction (SUB, SBC, CP, or DEC).
- o Interrupt enable flag (IFF)
  A maskable interrupt is enabled or disabled by this flag. This flag is set to "1" by an EI instruction and "0" by an DI instruction.

(Note) This flag is shared with the alternative register F'.

(3) Registers B, C, D, E, H and L
All these registers have an 8-bit configuration. They function as 16-bit register pairs (concatenated BC, DE and HL) as well as independent 8-bit register. Registers B or register pair BC is also used as a counter for the loop instruction (DJNZ). Register pair HL is used for 16-bit data processing including 16-bit arithmetic/logic operations.

(4) Registers A', F', B', C', D', E', H' and L'
These registers have the same structure as the main registers (A, F, B, C, D, E, H and L). They are called alternative registers. There is no instruction that directly accesses these alternative registers, but its data can be processed by a register exchange instruction.
Following are examples of register exchange insturctions that allow the exchange of data between a main register and an alternative register:

```
EX     AF,AF'
EXX
```

(5) Registers IX, IY, BX and BY
IX and IY are 16-bit independent registers called index registers. BX and BY are 4-bit independent registers and referred to as bank registers.
These registers are used mainly for specifying memory addresses, and generate 20-bit addresses. IX and IY registers are also used for 16-bit additions.

BX and BY registers are allocated to the memory addresses FFECH (BX register) and FFEDH (BY register) in the internal I/O address spaces. Only their lower four bits are effective, with the upper four bits being undefined. These undefined bits are always set to "1" when reat out. By resetting, the lower four bits of BX and BY registers are initialized to "0".

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BX (FFECH)	-	-	-	-	BX3	BX2	BX1	BX0	R/W
BY (FFECH)	-	-	-	-	BY3	BY2	BY1	BY0	R/W

(6) SP register
SP register is a 16-bit register called a stack pointer (SP), that stores the start address of the memory stack area (Last in, first out basis). It is decremented when a CALL or PUSH instruction is executed or an interrupt is accepted. It is incremented by execution of RET instruction or a POP instruction.

(7) PC register
This is a 16-bit register called a program counter, and stores the memory address of the next instruction to be executed.
It is initialized to 0000H when the RESET pin becomes low.

(8) Other
By executing the data exchange instruction [EXX] between a main register and an alternative register, the EXF bit (exchange flag: Bit 1 of memory address FFD2H) of the internal I/O register is inverted. This is a read-only bit, and is not initialized by resetting.

3.1.3 Addressing modes

Eight addressing modes are available for the TMP90C840. They are used in combination with various instructions to enhance the CPU's processing capabilities.
They are: Register mode, immediate mode, register indirect mode, index mode, register index mode, extend mode, direct mode and relative mode. The first seven addressing modes are used most frequently. The relative addressing mode is only applicable to specific instructions.

(1) Register addressing mode
In the register addressing mode, the operand represents a specified register.
Example: LD A, B
The contents of Register B are loaded into Register A.

(2) Immediate addressing mode
In this mode, the operand is in the instruction.
Example: LD A, 12H
Immediate data "12H" are loaded into Register A.

(3) Register indirect addressing mode
In the register indirect addressing mode, the operand is located in a memory address indicated by a register pair (BC, DE, HL, IX, IY or SP).
Example: LD A, (HL)

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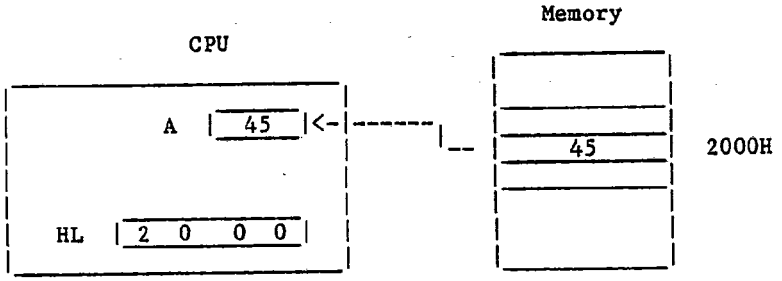
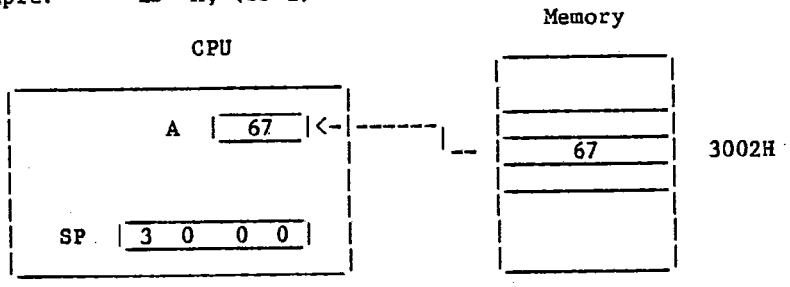


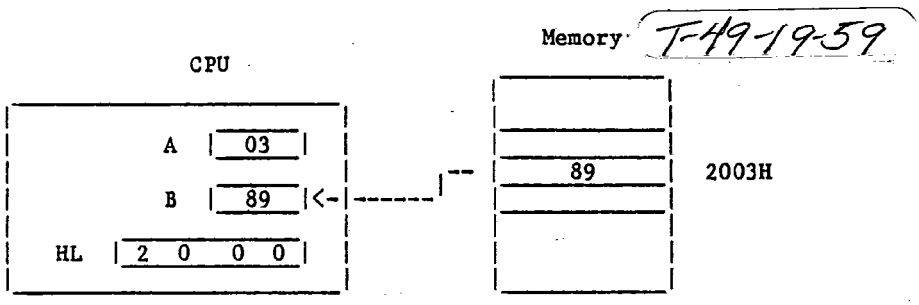
"45H" in the memory address 2000H is loaded into Register A.

(4) Index addressing mode
In the index addressing mode, the operand is located in a memory address specified by adding an 8-bit displacement value in the opcode to the contents of a specified register pair (IX, IY or SP).
Example: LD A, (SP+2)



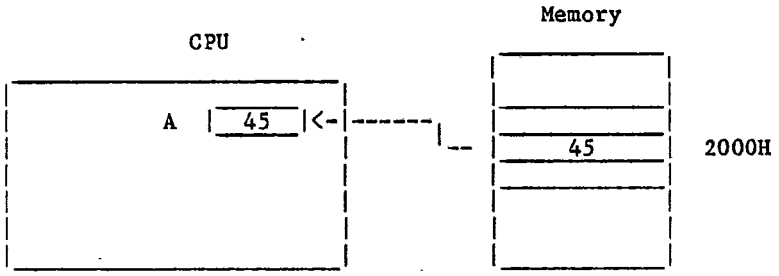
"67H" in the memory address 3002H is loaded into Register A. The displacement value ranges from -128 to +127.

(5) Register index addressing mode
In this mode, the operand is located in a memory address specified by adding the displacement value of Register A to the contents of register pair HL.
Example: LD B, (HL+A)



"89H" in the memory address 2003H is loaded into Register B. In this mode, the data in Register A are considered as 8-bit signed number, and the displacement value ranges from -128 to +127.

(6) Extended addressing mode
In this mode, the operand is accessed by 2-byte (16-bit) data in the opcode.
Example: LD A, (2000H)



"45H" in the memory address 2000H is loaded into Register A.

(7) Direct addressing mode
The operand in this mode is located in a memory address from FF00H to FFFFH specified by 1-byte (8 bits) data in the opcode. Compared with the extended addressing mode, it saves both program memory and executing time. This mode allows the access to 256-byte addresses from FF00H to FFFFH.
For the TMP90C840, this direct area is divided into the internal RAM (192 bytes from FF00H to FFBFH) and the internal I/O area (48 bytes from FFC0H to FFEFH).

Example: LD A, (FF10H)

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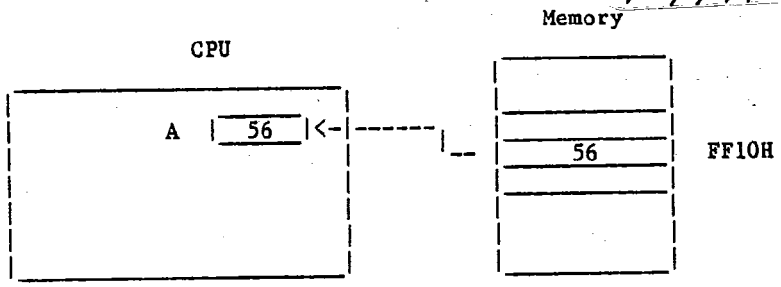
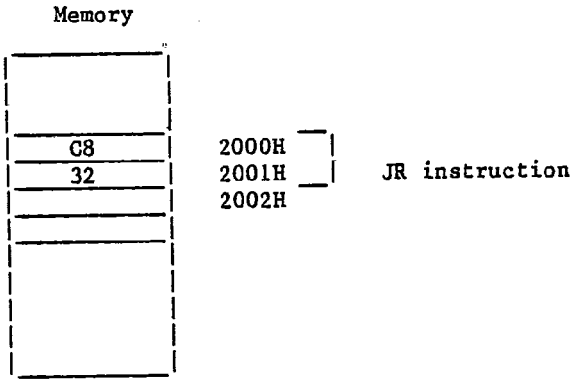


"56H" in the memory address FF10H is loaded into Register A.

(8) Relative addressing mode
In the relative addressing mode, the operand is found at the address relative to the current instruction. This mode is applicable to instructions involving an 8-bit displacement value (JR and DJNZ) and a 16-bit displacement value (LDAR, JRL and CALR).

Example: JR 2034H



In this example, the program execution jumps to the address 2034H. Since the program counter is already incremented by 2 at the time of address computation, the displacement is obtained by the following formula based on the "memory address of the JR instruction + 2":

Destination address - (address of instruction being executed + 2)

In the example, the displacement "32H" is obtained by:

2034H - (2000H + 2)

In any other instructions using the relative addressing mode (DJNZ, LDAR, JRL and CALR), the displacement is always calculated based on the "address of the current instruction + 2".

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(9) Addressing modes for extended data area

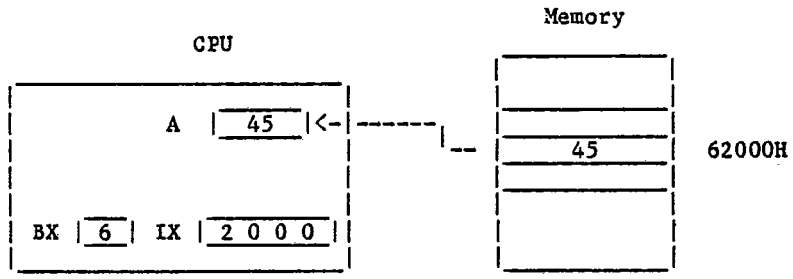
The TMP90C840 provides up to 1M bytes of data.
The addresses 00000H to 0FFFFH can be accessed in a normal addressing mode.
However, the addresses from 10000H to FFFFFH called an "extended data area" require a special addressing mode for access.
Accessing the extended data area requires to select the addressing mode which uses the index register IX or IY for obtaining the address of the operand (the register indirect addressing mode or the index addressing mode).

The following four special modes are available:

(IX)
(IY)
(IX+d)
(IY+d)

In these modes, the extended data area is accessed by using a 20-bit address consisting of a 16-bit offset address (address bus A0 to A15) and a bank address (address bus A16 to A19).
The 16-bit offset address is obtained by the same way as in a normal address computation. The 4-bit bank address is specified by the bank register BX or BY. The register pair BX is selected when the index register IX is used, and BY is selected when IY is used.

Example: LD A, (IX)



"45H" in the address 62000H is loaded into Register A.

In the index addressing mode, a carry resulted from calculating the 16-bit offset address is ignored; i.e., it is not added to the bank address.

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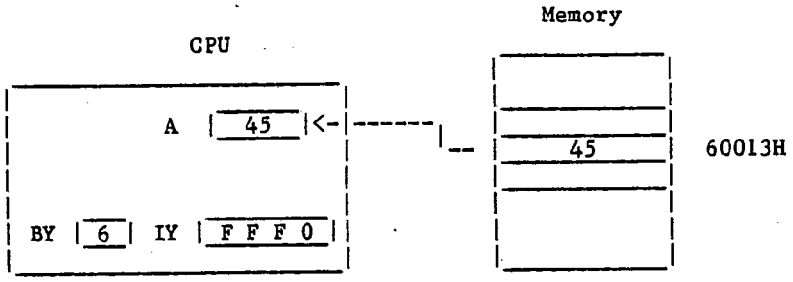
Example: LD A, (IY+23H)



In this example, "45H" in the address 60013H is loaded into Register A.
In any other addressing mode that accesses a non-extended data area (the index register IX or IY is not used for address computing of the operand), the 4-bit bank address (address bus A16 to A19) becomes "0", indicating that the access range is from 00000H to 0FFFFH.

(Note) Given "FFECH" to the IX value of (BX address) an instruction "LD (IX), x", the normal write cycle is not performed, making the result indefinite.

3.1.4 Instructions

The TMP90C840 supports a rich variety of addressing modes as well as powerful instruction sets. There are 163 basic instructions as categorized into the following nine groups:

- o 8-bit transfer instruciton
- o 16-bit transfer instruciton
- o Exchange, block transfer and search instructions
- o 8-bit arithmetic and logical operation instruction
- o Special operation and CPU control instructions
- o 16-bit arithmetic and logical operation instruciton
- o Rotate and shift instructions
- o Bit manipulation instruction
- o Jump, call and return instruction

Table 3.1 (1) lists the 163 basic instructions. Table 3.1. (2) describes the mnemonics and their meaning.

(1) 8-bit transfer instruction
The 8-bit transfer instructions inclued those for transferring 8-bit data between registers, register and immediate address, register and memory, or memory and immediate address.

(2) 16-bit transfer instruction
The 16-bit transfer instructions include those for transferring 16-bit data between registers, register and immediate address, register and memory, and memory and immediate address, PUSH and POP instructions using the stack, and LDA (Load Address) instruction that calculates an effective address and loads its value into a register.

(3) Exchange, block transfer and search instructions
The data exchange instructions are executed to exchange 16-bit data between registers, between memory and register, or between a main register and an alternative register.
The block transfer instructions can transfer data in any memory block to other memory area.
The block search instructions are executed to find out a particular 8-bit character in a given memory block. LDIR, LDDR, CPIR and CPDR included in the block transfer and search instructions read the current instruction each time a 1-byte memory is transferred or compared, thus making it possible to acknowledge an interrupt before reaching to the end of the block.

(4) 8-bit arithmetic and logical operation instruction
8-bit arithmetic and logical operation instructions perform 8-bit arithmetic and logical operations between Register A and another register, Register A and immediate address, Register A and memory, register and immediate address, and memory and immediate address (ADD, ADC, SUB, SBC, AND, OR XOR and CP), or increment/decrement the contents of register or memory by 1 (INC, DEC, INCX and DECX).
The INCX (Increment if X) instruction increments the contents of a memory specified by the operand if the X flag is "1", and does nothing if not. The DECX instruction performs the same operation except that it decrements the data. These instructions are executed to increment or decrement the data with 20-bit width in the 20-bit address pointers (registers BX and IX or BY and IY) mainly to access an extended data area.

Examples:

```
INC IX          :  Increment Register IX
INCX (FFECH)    :  Increment Register BX if X
LD A,(IX)       :  Load contents of memory into Register A
```

Table 3.1 (1) TMP90C840 Basic Instructions (163 types)

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LD r,r	SBC r,n	MUL HL,r	RRCA
LD r,n	SBC mem,n	MUL HL,n	RRC r
LD r,mem	AND A,r	MUL HL,mem	RRC mem
LD mem,r	AND A,n	DIV HL,r	RLA
LD mem,n	AND A,mem	DIV HL,n	RL r
LD rr,rr'	AND r,n	DIV HL,mem	RL mem
LD rr,nn	AND mem,n	ADD HL,rr	RRA
LD rr,mem	OR A,r	ADD HL,nn	RR r
LD mem,rr	OR A,n	ADD HL,mem	RR mem
LDW mem,nn	OR A,mem	ADC HL,rr	SLAA
PUSH qq	OR r,n	ADC HL,nn	SLA r
POP qq	OR mem,n	ADC HL,mem	SLA mem
LDA rr,mem	XOR A,r	SUB HL,rr	SRAA
EX DE,HL	XOR A,n	SUB HL,nn	SRA r
EX AF,AF'	XOR A,mem	SUB HL,mem	SRA mem
EXX	XOR r,n	SBC HL,rr	SLLA
EX mem,rr	XOR mem,n	SBC HL,nn	SLL r
LDI	CP A,r	SBC HL,mem	SLL mem
LDIR	CP A,n	AND HL,rr	SRLA
LDD	CP A,mem	AND HL,nn	SRL r
LDDR	CP r,n	AND HL,mem	SRL mem
CPI	CP mem,n	OR HL,rr	RLD mem
CPIR	INC r	OR HL,nn	RRD mem
CPD	INC mem	OR HL,mem	BIT b,r
CPDR	DEC r	XOR HL,rr	BIT b,mem
ADD A,r	DEC mem	XOR HL,nn	RES b,r
ADD A,mem	INCX (n)	XOR HL,mem	RES b,mem
ADD r,n	DECX (n)	CP HL,rr	SET/TSET b,r
ADD mem,n	DAA A	CP HL,nn	SET/TSET b,mem
ADC A,r	CPL A	CP HL,mem	JP cc,mem
ADC A,mem	NEG A	ADD ix,rr	JR cc,PC+d
ADC r,n	LDAR HL,PC+dd	ADD ix,nn	JRL PC+dd
ADC mem,n	CCF	ADD ix,mem	CALL cc,mem
SUB A,r	SCF	INC rr	CALR PC+dd
SUB A,mem	RCF	INCW mem	DJNZ [BC,]PC+d
SUB r,n	NOP	DEC rr	RET cc
SUB mem,n	HALT	DECW mem	RETI
SBC A,r	DI	RLCA	
SBC A,n	EI	RLC r	
SBC A,mem	SWI	RLC mem	

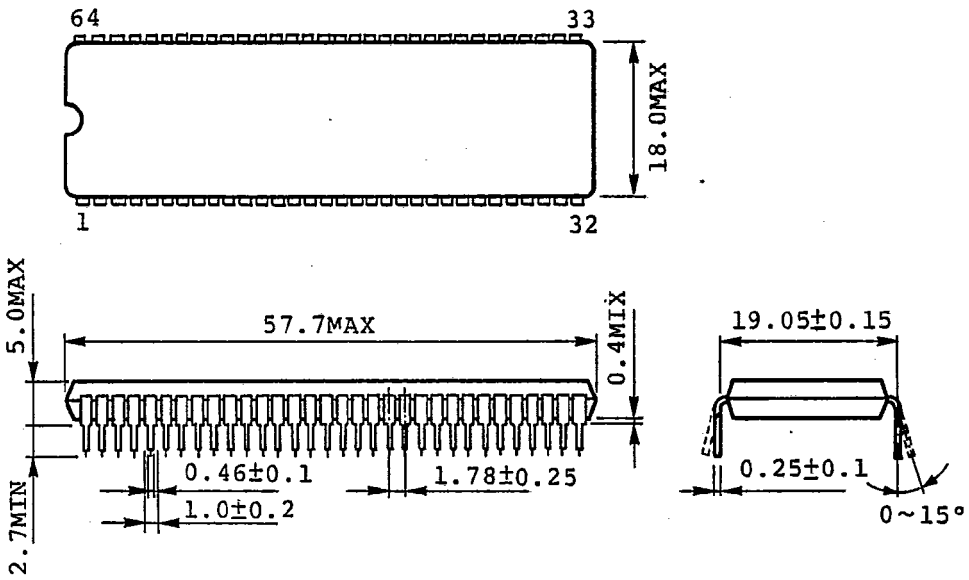
Table 3.1 (2) TMP90C840 Mnemonics and Their Meaning

Mnemonic	Meaning	Mnemonic	Meaning
LD	Load	MUL	Multiply
LDW	Load Word	DIV	Divide
PUSH	Push	INCW	Increment Word
POP	Pop	DECW	Decrement Word
LDA	Load Address	RLCA	Rotate Left Circular Accumulator
EX	Exchange		
EXX	Exchange X	RLC	Rotate Left Circular
LDI	Load and Increment	RRCA	Rotate Right Circular Accumulator
LDIR	Load, Increment and Repeat		
LDD	Load and Decrement	RRC	Rotate Right Circular
LDDR	Load, Decrement and Repeat	RLA	Rotate Left Accumulator
CPI	Compare and Increment	RL	Rotate Left
CPIR	Compare, Increment and Repeat	RRA	Rotate Right Accumulator
		RR	Rotate Right
CPD	Compare and Decrement	SLAA	Shift Left Arithmetic Accumulator
CPDR	Compare, Decrement and Repeat	SLA	Shift Left Arithmetic
ADD	Add	SRAA	Shift Right Arithmetic Accumulator
ADC	Add with Carry		
SUB	Subtract	SRA	Shift Right Arithmetic
SBC	Subtract with Carry	SLLA	Shift left Logical Accumulator
AND	And		
OR	Or	SLL	Shift Left Logical
XOR	Exclusive Or	SRLA	Shift Right Logical Accumulator
CP	Compare		
INC	Increment	SRL	Shift Right Logical
DEC	Decrement	RLD	Rotate Left Digit
INCX	Increment if X	RRD	Rotate Right Digit
DECX	Decrement if X	BIT	Bit Test
DAA	Decimal Adjust Accumulator	RES	Reset Bit
CPL	Complement	SET	Set Bit
NEG	Negate	TSET	Test and Set
LDAR	Load Address Relative	JP	Jump
CCF	Complement Carry Flag	JR	Jump Relative
SCF	Set Carry Flag	JRL	Jump Relative Long
RCF	Reset Carry Flag	CALL	Call
NOP	No Operation	CALR	Call Relative
HALT	Halt	DJNZ	Decrement and Jump if Non Zero
DI	Disable Interrupt		
EI	Enable Interrupt	RET	Return
SWI	Software Interrupt	RETI	Return from Interrupt

5. OUTSIDE DIMENSIONS T-49-19-59

5.1 DIP package

Unit: mm



Note) Lead pitch: 1.78
Tolerance: ±0.25 to the theoretical center of each lead obtained as based on the No. 1 and No. 64 pins.

5.2 Mini-flat package

T-49-19-59 Unit: mm