System Controller Chip for the RC4xxx/RC5xxx Families

IDT79RC64145
Advance Information*

RISController

Features

- **RC4xxx / RC5xxx CPU Bus Interface**
  - *Direct connection between CPU & RC64145*
  - *32- or 64-bit CPU SysAd bus width*
  - *Supports optional external secondary cache controller, including RC5000*
  - *Bus speeds up to 83MHz*
  - *Big or Little Endian support*
- **Supports 32- or 64-bit wide CPU bus and 32- or 64-bit memory**
- **Memory & Peripheral Controller**
  - *Supports SRAM, Flash ROM, dual-port memory and peripheral devices*
  - *5 chip selects*
  - *Supports 8-,16-,32- or 64-bit devices*
  - *8-bit boot PROM support*
- **SDRAM Controller**
  - *32- or 64-bit, up to 4 banks*
  - *Automatic refresh generation*
  - *Address space, up to 512MB*
  - *Stays on page between transfers*
- **General purpose counter/timers: three 24-bit & one 32-bit**
- **Interrupt Control**
  - *Allows status of each interrupt to be read and masked*
- **Programmable IO (PIO)**
  - *Input/Output/Interrupt source*
  - *Individually programmable*
- **DMA Controller**
  - *4 general purpose DMA channels*
  - *Supports memory-to-memory, memory-to-I/O,memory-to-PCI, PCI-to-PCI, and I/O-to-I/O transfers*
  - *Supports flexible descriptor based operation for scatter/gather*
  - *Supports unaligned transfers*
  - *Supports demand and burst transfers*
  - *Programmable DMA bus transaction burst size, up to 32 bytes*
- **PCI Bus Interface (Revision 2.1 compatible)**
  - *32-bit PCI, up to 66 MHz*
  - *Target or Master, Host or Satellite*
  - *Plug-and-Play compatible*
  - *Endianess swappers and byte lane data alignment*
- **UART Interface**
  - *Two 16550 compatible UARTs*
  - *Complete modem support on 1 channel*
  - *Baud rate support up to 1.5 MBps*
- **JTAG Interface (IEEE STD.1149.1 compatible)**
- **3.3V operation with 5V tolerant inputs**
- **Available in 388-pin BGA packaging, supports 32- and 64-bit CPUs**

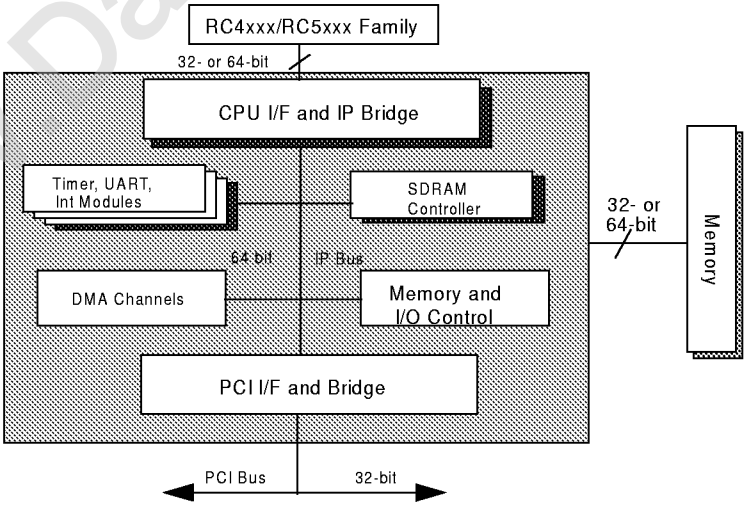


Figure 1 RC64145 Block diagram

*Notice: The information in this document is subject to change without notice

DSC 5605

Description

The RC64145 is a high performance system-controller chip that supports the full range of IDT 64-bit CPUs, from both the RC4xxx and 5xxx families, offering a direct connection to the CPU. The RC64145 also provides the system logic for boot memory, main memory, I/O, and PCI. On-chip peripherals include four general purpose DMA channels, interrupt control, four general purpose timers and two UARTs. Together, the RC64145 and the CPU form a complete, flexible CPU subsystem for embedded designs.

The RC64145 directly interfaces with either the 32- or 64-bit CPU bus and provides all of the control and address signals needed to drive the external memory and I/Os. As illustrated in the system block diagram, the memory and I/O data path is internal to the RC64145.

Device overview

The RC64145 interfaces directly to the CPU system buses, registering the address from the system CPU internally and decoding it to detect which memory, I/O, or on-chip peripheral is being accessed, per the internal address map of the device. The RC64145 generates all necessary control, address, and data buses to the external memory and I/O. For main memory, I/O, on-chip peripherals, registers, and PCI, the RC64145 divides the physical address space into 12 different regions.

The data path for memory and peripherals is internal to the RC64145.

Device Controller. The RC64145 Device Controller provides all of the address buses and control signals necessary for interfacing the system CPU to standard SRAM, FLASH, and peripherals and includes the boot ROM interface. The Device Controller provides four individual chip selects for SDRAM (64-bit only), one boot select, and four other device selects. The chip selects have highly configurable address regions, allowing selection of various memory types and widths to be supported.

SDRAM Controller. The RC64145 SDRAM Controller provides higher throughput while using available technology. The SDRAM controller register directly manages 4 banks of 32- or 64-bit physical non-interleaved memory. Total memory support is 512 MB. The SDRAM Controller has a built-in refresh generator. The RC64145 provides controls for optional external SDRAM data transceivers for systems that require fast signalling with large loads.

PCI Bus Interface. At reset time, the PCI bridge can be configured as either a host or satellite interface and supports 32-bit master and target operations at up to 66 MHz. The RC64145 PCI Interface is PCI Specification Revision 2.1 compliant.

Advance Information

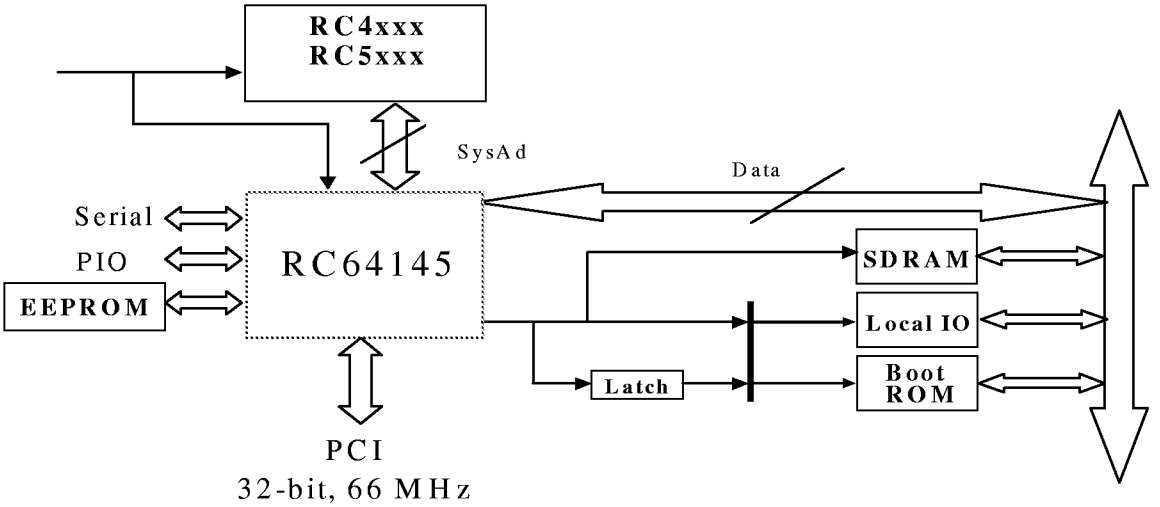


Figure 2 RC64145 System Diagram

As a PCI master, the RC64145 can generate memory, I/O, or configuration cycles for direct local-to-PCI bus accesses. As a PCI target, the RC64145 allows access to its internal registers and to the CPU core's local bus through the PCI I/O read/write or memory read/write commands. The RC64145 PCI Interface supports swapping little-endian data to big-endian data, under user configuration control. For more details on PCI products, refer to the PCI Specification revision 2.1.

Interrupt Controller. The Interrupt Controller provides the interrupt logic for software to decode and manage the various RC64145 generated system interrupts and adds to the control already provided through the system CPU's CP0 registers. Each system interrupt is registered and the pending status provided through this feature. The pending status can then be used to automatically generate a hardware interrupt to the CPU via individual mask bits. The pending interrupt status can also be optionally set or cleared by a direct software write.

DMA Controller. Four general purpose DMA channels move data between source and destination ports. Source and destination ports can be system memory, PCI or I/O devices. Any of the four channels can be used for PCI initiator reads or writes. All four channels support a descriptor structure, to allow efficient data scatter/gather. The DMA controller also supports quad-word burst transfers. All external 16 and 8-bit memory or I/Os are treated as memory-mapped, word-aligned devices.

PIO. Programmable I/O (PIO) pins are provided on the RC64145 so that any unused peripheral pins can be programmed for use as general purpose discrete I/O pins. These PIO pins can be software programmed as bidirectional lines, allowing pin values to be software programmed in output mode and software readable while in the input mode. As inputs, the PIO pins can also be used as a source of interrupts to the CPU. Maximum interfacing flexibility is thus provided without requiring extensive modifications to the board.

UART. The RC64145 incorporates two 16550 (an enhanced version of the 16450) compatible UARTs. To relieve the CPU of software overhead, the 16550 UART can be put into FIFO mode, allowing execution of either 16450 or 16550 compatible software. Two sets of 16-byte FIFOs are enabled during the 16550 mode: one set in the receive data path and one set in the transmit data path. A baud rate generator is included that divides the system clock by 1 to 64K and provides a 16X clock for driving the transmitter and receiver logic.

Timers/Counters. Four on-chip timer counters (three 24-bit and one 32-bit) are provided on the RC64145. The desired counter is loaded and decremented. An interrupt is generated when zero is reached. In time mode, the desired count is reloaded and count-down started again generating many interrupts at a repetitive frequency. In counter mode, the desired count is not reloaded, generating only one interrrupt.

Thermal considerations

The RC64145 is packaged in a thermally enhanced Ball Grid Array package, which has an anodized aluminum plate that contacts the backside of the die and does not contact the surface of the package.

The RC64145 is guaranteed in a case temperature range of 0°C to +95°C, for commercial temperature devices; -40°C to +95°C for industrial temperature devices.

The package type, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification. The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device. Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 1

	$\varnothing_{CA}$					
Airflow (ft/min)	0	200	400	600	800	1000
388 BGA	19	16	15	14.5	14	14

Table 1 Thermal Resistance ($\varnothing_{CA}$) at Various Airflows

Data Sheet Revision History

July 29, 1999: First draft.

Aug. 31, 1999: In Table 3, replaced uart1_sin_stck with uart1_sin (pin AC25), pci_par_n with pci_par (pin AD14), and data[48] with sys_data[48] (pin M23). In Figure 3, replaced sys_ready__n with sys_wait.

Pin description table

The following is a list of interface, interrupt, and miscellaneous pins that are available on the RC64145. Note that several pins are multiplexed and have been assigned alternate functions. These pins are designated and defined accordingly throughout this table. Also note that those pin names followed by _n are active-low signals.

Pin Name	Type	Drive Strength	Alternate Signal (s)	Description
CPU Interface				
cpu_rdy_n	O			**Ready** Indicates that the RC64145 is ready to accept a processor read or write request. Connects to wrdy_n and rdrdy_n of the CPU.
cpu_validout_n	I			**Valid Input** Indicates that the processor is driving valid address or data on the cpu_ad bus and a valid command or data identifier on the cpu_cmd bus.
cpu_validin_n	O			**Valid Output** Indicates that the RC64145 is driving valid data on the cpu_ad bus, and a valid command on the cpu_cmd bus.
cpu_ad[63:0]	I/O			**Address/Data Bus** Address and data bus to and from the processor. (cpu_ad[31:0] for 32-bit CPU)
cpu_adc[7:0]	O		pio[7.0]	**Address/Data Bus Parity Bits** Each bit contains parity for associated byte on cpu_ad[64:0].
cpu_cmd[8:0]	I/O			**Command/Data Identifier Bus** A 9-bit bus for command and data identifier transmission between the processor and the RC64145.
cpu_int_n	O			**Interrupt** Indicates an interrupt occurred from any of the internal interrupt sources or any of the external interrupt sources. External interrupt sources are input on a PIO pin.
PCI Interface				
pci_clk	I			**PCI Clock** Provides the timing of the PCI-related bus transaction. The PCI clock does not require a specific relationship to CPU clock.
pci_ad[31:0]	I/O			**Address/Data Bus** 32-bit multiplexed address/data lines. During the first clock of the transaction, pci_ad[31:0] contains a physical byte address (32 bits). During subsequent clock cycles, pci_ad[31:0] contains data.
pci_cbe_n[3:0]	I/O			**Bus Command/Byte Enable** These are multiplexed on the same PCI pins. During the address phase of the transaction, pci_cbe_n[3:0] provide the bus command. During the data phase, these lines provide the byte enables. The byte enables determine which bytes have valid data.
pci_par	I/O			**Parity** Calculated by RC64145 as an even parity bit for the pci_ad[31:0] and pci_ce_n[3:0] lines.

Table 2 RC64145 Pin Descriptions (Page 1 of 5)

Pin Name	Type	Drive Strength	Alternate Signal (s)	Description
pci_frame_n	I/O			**Frame** Asserted by the RC64145 to indicate the beginning and duration of a master transaction. pci_frame_n is deasserted to indicate that the next data phase is the final data phase transaction. pci_frame_n is monitored by the RC64145 when it acts as a target.
pci_trdy_n	I/O			**Target Ready** Asserted by the RC64145 to indicate the ability to complete the current target transaction. pci_trdy_n is used in conjunction with pci_irdy_n to indicate a data phase completion. During a Read, pci_trdy_n indicates data is valid on pci_ad. Wait cycles are inserted until pci_trdy_n and pci_irdy_n are asserted together.
pci_ irdy_n	I/O			**Initiator Ready** Indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both pci_trdy_n and pci_irdy_n are asserted. Wait cycles are inserted until pci_trdy_n and pci_irdy_n are asserted together.
pci_stop_n	I/O			**Stop** It indicates that the current target is requesting the bus master to stop the current transaction. As a master, the RC64145 responds to the assertion of pci_stop_n by disconnecting, retrying or aborting. As a target, the RC64145 asserts pci_stop_n to retry or disconnect.
pci_ lock_n	I			**Lock** Indicates an atomic operation that may require multiple transactions to complete. When the RC64145 is a PCI target, pci_lock_n is sampled on the rising edge of pci_lock_n when pci_frame_n is asserted. If pci_lock_n is sampled asserted, the RC64145 will ignore target read requests until pci_lock_n is sampled deasserted on the following rising edge of pci_lock_n, when pci_frame_n is sampled asserted.
pci_idsel	I			**Initialization Device Select** Asserted to act as a chip select during PCI configuration read and write transactions.
pci_devsel_n	I/O			**Device Select** Asserted by the target of the current access. When the RC64145 is bus master, it expects the target to assert pci_devsel_n within 5 bus cycles, confirming the access. If the target does not assert pci_devsel_n within the required time, the RC64145 aborts the cycle. As a target, when the RC64145 recognizes its transaction, it asserts pci_devsel_n in a medium speed mode (two cycles after the assertion of pci_frame_n).
pci_req_n	O			**Bus Request** Asserted by the RC64145 to indicate to the bus arbiter that it desires the use of the bus. This signal is active regardless of whether the internal or external arbiter is used.
pci_gnt_n	I			**Bus Grant** Asserted to indicate to RC64145 that the external arbiter has granted access.
pci_perr_n	I/O			**Parity Error** Asserted when a data parity error is detected.

Table 2 RC64145 Pin Descriptions (Page 2 of 5)

Pin Name	Type	Drive Strength	Alternate Signal (s)	Description
pci_serr_n	O			**System Error** Asserted when a serious system error is detected. The RC64145 asserts the pci_serr_n signal two cycles after the failing address. Open Drain Output.
pci_int_n	O			**Interrupt Request** Asserted by the RC64145 when one of the unmasked interrupts is asserted. Open Drain Output.
SDRAM Interface				
sd_cs_n[3:0]	O			**SDRAM Chip Select** Used for SDRAM command cycles and to select the SDRAM device.
sd_we_n	O			**SDRAM Write** Indicates the RC64145 is writing to the SDRAM.
sd_ras_n	O			**Row Address Select** Common to all banks of SDRAM.
sd_cas_n	O			**Column Address Select** Common to all banks of SDRAM
sd_ba[1:0]	O			**Bank Address[1:0]** Function as bank address bits to SDRAM and as sys_adr[25:24] during device accesses (Note: BA is valid for entire device access cycle, so it does not need to be latched when used as address bits).
sd_xcvroe_n	O			**External 245 Transceiver Output Enable** Transceiver output enable control for SDRAM data bus.
sd_xcvrdir_wr_n	O			**External Transceiver Direction** Transceiver output direction control for SDRAM data bus (0=write, 1=read).
System Interface				
sys_devoe_n	O			**Output Enable Device** Output enable common to all external devices except SDRAM.
sys_dqm_we_n[7:0]	O			**Data Mask[7:0]** DQM signals are used by SDRAM to support byte reads/writes to the SDRAM. Also used as byte write enables during device accesses.
sys_adr[11:0]	O			**SDRAM and Device Address[11:0]** In SDRAM accesses, these pins function as address bits. In device accesses, these pins are multiplexed as MSBs (23:12) and LSBs (11:0). The MSB's are latched with sys_ale.
sys_data[63:0]	I/O			**Data [63:0]** Data bits to or from memories and devices.
sys_datap[7:0]	I/O		pio[20:13]	**Data Parity[7:0]** Each bit contains parity for associated byte on sys_data[63:0]. pio[20:13]: Programmable I/O pins, selected by internal control register
sys_bootcs_n	O			**Boot Chip Select** This chip select address range contains the reset address vector.
sys_devcs_n[3:0]	O			**Device Chip Select** Chip Selects for devices.

Table 2 RC64145 Pin Descriptions (Page 3 of 5)

Pin Name	Type	Drive Strength	Alternate Signal (s)	Description
sys_ale	O			**Address Latch Enable** Used to latch the device sys_adr[23:12].
sys_wait	I/O		pio[8]	**Wait** Wait is used as a cycle extender during device accesses. This is the default function at reset. pio[8]: Programmable I/O pins, selected by internal control register
sys_rst_n	I			**Reset** Resets the RC64145, PCI, and JTAG to their initial states. When low, all output pins are put into tristate and all open drain signals are floated.
sys_ clk	I			**Clock** Input clock to the RC64145.
DMA/PIO Devices				
dma_ack_n[3:0]	I/O		pio[3:0]	**DMA Acknowledge[3:0] Output** Output to an external device during DMA in response to dma_req_n. pio[3:0]: Programmable I/O pins, selected by internal control register. Defaults to output at reset.
dma_req_n[3:0]	I/O		pio[7:4]	**DMA Request DMA request inputs** Input from an external device during DMA requesting access service. pio[7:4]: Programmable I/O pins, selected by internal control register. Defaults to input at reset.
pio[3:0]	I/O			**PIO[3:0]** Programmable I/O pins, selected by internal control register. Defaults to output at reset.
Secondary Cache Interface				
sc_tce_n	I			**Secondary Cache Tag RAM Enabled** Chip enable for secondary cache tag RAM.
sc_doe_n	O			**Secondary Cache Data RAM Output Enable** Chip enable for secondary cache data RAM.
sc_word[1:0]	O			**Secondary Cache Word Index** Determines correct double-word of secondary cache index.
sc_hit	I			**Secondary Cache Tag Hit** Asserted by tag RAM on secondary cache tag match. Fetch from SDRAM will be aborted by the RC64145 if a hit is indicated.
UART Interface				
uart0_sin	I			**UART0 Serial Data In** Serial data input
uart0_sout	O			**UART0 Serial Data Out** Serial data output
uart0_dcd_n	I			**UART0 Data Carrier Detect** When active low, it signals the detection of a modem or data set.
uart0_cts_n	I			**UART0 Clear to Send** When active low, it signals UART's readiness for exchanging data.

Table 2 RC64145 Pin Descriptions (Page 4 of 5)

Pin Name	Type	Drive Strength	Alternate Signal (s)	Description
uart0_rts_n	O			**UART0 Request to Send** When active low, it signals the modem that UART is ready to exchange data.
uart_dtr_n	O			**UART0** Data Terminal Ready When active low, it signals the modem that UART is ready to establish a communications link.
uart1_sin	I			**UART1** Serial Data In When active low, it signals the modem that UART is ready to establish a communications link.
uart1_sout	O			**UART1** Serial Data Out When active low, it signals the modem that UART is ready to establish a communications link.
JTAG Interface				
jtg_clk	I			**JTAG Clock** Clock for the test logic. jtag_ms and jtag_di are received on the rising edge. jtag_do is driven from the falling edge. This signal determines the shift rate. If JTAG is not used, this signal should be pulled up or down.
jtg_Tms	I			**JTAG Mode Select** A broadcast signal that controls the test logic. This signal is decoded by the Tap controller to control test operations.
jtg_di	I			**JTAG Data In** Serial data in. At reset used to configure the RC64145 JTAG as a 32- or 64-bit device. (1=32-bit, 0=64-bit). Serial test instructions and data are received by the test logic TDI. This signal is pulled up internally.
jtg_do	O			**JTAG Data Out** Serial data out. Serial output for test instructions and data from the test logic.

Table 2 RC64145 Pin Descriptions (Page 5 of 5)

Package pin-out 388-pin BGA

The following table lists the pin numbers and signal names for the RC64145. To maximize pin usage, some pins have alternate functions, as noted in the "Alt" column. Note that signal names ending with an _n are active when low.

Pin	Name	Alt	Pin	Name	Alt	Pin	Name	Alt	Pin	Name	Alt
A1	Vss I/O		AE6	pci_ad[10]		D1	cpu_ad[50]		M24	sys_data[49]	
A2	Vss I/O		AE7	pci_ad[6]		D2	cpu_ad[51]		M25	Vcc Core	
A3	cpu_ad[16]		AE8	pci_ad[3]		D3	cpu_ad[14]		M26	sys_data[6]	
A4	cpu_ad[18]		AE9	Vss Core		D4	Vss, Core		N1	cpu_ad[36]	
A5	cpu_ad[20]		AE10	pci_cbe_n[3]		D5	cpu_ad[55]		N2	cpu_ad[37]	
A6	cpu_ad[58]		AE11	pci_idsel		D6	VDD, I/O		N3	cpu_ad[34]	
A7	cpu_ad[60]		AE12	pci_trdy_n		D7	cpu_ad[22]		N4	Vss, Core	
A8	cpu_ad[62]		AE13	pci_devsel_n		D8	cpu_ad[24]		N11	Vss I/O	
A9	cpu_ad[63]		AE14	pci_perr_n		D9	Vss, Core		N12	Vss I/O	
A10	sys_data[57]		AE15	cpu_adc[2]		D10	cpu_ad[28]		N13	Vss I/O	
A11	sys_data[59]		AE16	cpu_adc[1]		D11	VDD, I/O		N14	Vss I/O	
A12	sys_data[61]		AE17	pci_clk		D12	cpu_ad[30]		N15	Vss I/O	
A13	sys_adr[01]		AE18	Vcc Core		D13	sys_adr[2]		N16	Vss I/O	
A14	Vss Core		AE19	sys_datap[5]	pio[18]	D14	Vss Core		N23	sys_data[5]	
A15	sys_adr[07]		AE20	sys_datap[4]	pio[17]	D15	sys_adr[4]		N24	sys_data[50]	
A16	sys_adr[09]		AE21	pio[11]		D16	Vcc I/O		N25	sys_data[52]	
A17	sys_dqm_we_n[4]		AE22	sys_datap[0]	pio[13]	D17	sys_dqm_we_n[0]		N26	sys_data[51]	
A18	sys_dqm_we_n[2]		AE23	uart0_rts_n		D18	sd_cs_n[0]		P1	cpu_ad[35]	
A19	sys_dqm_we_n[7]		AE24	no connect		D19	Vss Core		P2	Vcc Core	
A20	sd_cs_n[3]		AE25	Vss Core		D20	sd_cas_n		P3	cpu_cmd[5]	
A21	sd_ba[1]		AE26	sys_data[45]		D21	Vcc I/O		P4	cpu_cmd[6]	
A22	Vcc Core		AF1	Vss Core		D22	sys_data[30]		P11	Vss I/O	
A23	sys_data[28]		AF2	no connect		D23	Vss Core		P12	Vss I/O	
A24	sys_data[25]		AF3	Vss Core		D24	sys_data[23]		P13	Vss I/O	
A25	Vss I/O		AF4	pci_ad[15]		D25	sys_data[20]		P14	Vss I/O	
A26	Vss I/O		AF5	pci_ad[11]		D26	sys_data[42]		P15	Vss I/O	
AA1	pci_ad[27]		AF6	pci_ad[7]		E1	cpu_ad[11]		P16	Vss I/O	
AA2	pci_ad[29]		AF7	pci_ad[5]		E2	cpu_ad[13]		P23	Vss I/O	
AA3	pci_ad[23]		AF8	pci_ad[01]		E3	cpu_ad[12]		P24	Vss Core	
AA4	Vcc I/O		AF9	Vcc Core		E4	cpu_ad[49]		P25	sys_data[02]	
AA23	Vcc I/O		AF10	pci_cbe_n[1]		E23	sys_data[21]		P26	sys_data[03]	
AA24	dma_ack_n[0]	pio[00]	AF11	pci_irdy_n		E24	sys_data[22]		R1	cpu_ad[32]	

Table 3 RC64145 388-pin BGA Package Pin-Out (Page 1 of 3)

Pin	Name	Alt	Pin	Name	Alt	Pin	Name	Alt	Pin	Name	Alt
AA25	dma_req_n[03]	pio[07]	AF12	cpu_adc[07]		E25	sys_data[40]		R2	cpu_ad[33]	
AA26	dma_ack_n[01]	pio[02]	AF13	cpu_adc[05]		E26	sys_data[19]		R3	sc_word[01]	
AB1	pci_ad[24]		AF14	cpu_adc[03]		F1	cpu_ad[09]		R4	sc_word[00]	
AB2	pci_ad[25]		AF15	pci_req_n		F2	cpu_ad[48]		R11	Vss I/O	
AB3	pci_ad[19]		AF16	cpu_adc[0]		F3	cpu_ad[47]		R12	Vss I/O	
AB4	pci_ad[21]		AF17	jtg_di		F4	Vcc I/O		R13	Vss I/O	
AB23	dma_req_n[0]	pio[04]	AF18	jtg_do		F23	Vcc I/O		R14	VssI/O	
AB24	dma_req_n[01]	pio[05]	AF19	jtg_ms		F24	sys_data[41]		R15	Vss I/O	
AB25	uart0_sin		AF20	pio[12]		F25	sys_data[38]		R16	Vss I/O	
AB26	dma_req_n[02]	pio[06]	AF21	pio[10]		F26	sys_data[39]		R23	sys_data[53]	
AC1	pci_ad[20]		AF22	uart0_sout		G1	cpu_ad[08]		R24	sys_data[04]	
AC2	pci_ad[22]		AF23	uart0_dtr_n		G2	cpu_ad[46]		R25	sys_data[0]	
AC3	Vcc Core		AF24	no connect		G3	cpu_ad[45]		R26	sys_data[54]	
AC4	Vss I/O		AF25	Vss I/O		G4	cpu_ad[10]		T1	cpu_cmd[03]	
AC5	pci_ad[13]		AF26	Vss I/O		G23	sys_data[17]		T2	cpu_cmd[04]	
AC6	Vcc I/O		B1	Vss Core		G24	sys_data[18]		T3	cpu_cmd[01]	
AC7	pci_ad[09]		B2	Vss I/O		G25	sys_data[14]		T4	Vcc I/O	
AC8	Vss I/O		B3	cpu_ad[17]		G26	sys_data[15]		T11	Vss I/O	
AC9	pci_ad[02]		B4	cpu_ad[19]		H1	cpu_ad[06]		T12	Vss I/O	
AC10	pci_cbe_n[0]		B5	cpu_ad[57]		H2	cpu_ad[07]		T13	Vss I/O	
AC11	Vcc I/O		B6	cpu_ad[59]		H3	cpu_ad[43]		T14	Vss I/O	
AC12	pci_stop_n		B7	cpu_ad[61]		H4	Vss I/O		T15	Vss I/O	
AC13	VSS, I/O		B8	cpu_ad[26]		H23	sys_data[37]		T16	Vss I/O	
AC14	cpu_adc[04]		B9	sys_data[56]		H24	sys_data[16]		T23	Vcc I/O	
AC15	pci_gnt_n		B10	sys_data[58]		H25	sys_data[12]		T24	sys_data[01]	
AC16	Vss I/O		B11	sys_data[60]		H26	sys_data[13]		T25	sys_devcs_n[03]	
AC17	Vss Core		B12	sys_adr[0]		J1	cpu_ad[42]		T26	sys_data[55]	
AC18	Vss I/O		B13	sys_adr[03]		J2	cpu_ad[05]		U1	sc_tce_n	
AC19	sys_datap[03]	pio[16]	B14	sys_adr[05]		J3	cpu_ad[41]		U2	cpu_cmd[02]	
AC20	sys_datap[01]	pio[14]	B15	sys_adr[08]		J4	cpu_ad[44]		U3	cpu_validin_n	
AC21	Vcc I/O		B16	sys_adr[11]		J23	Vss I/O		U4	cpu_cmd[0]	
AC22	sys_data[46]		B17	sys_dqm_we_n[05]		J24	sys_data[36]		U23	sys_devcs_n[02]	
AC23	Vss I/O		B18	sys_dqm_we_n[06]		J25	sys_data[33]		U24	sys_devoe_n	
AC24	uart0_cts_n		B19	sd_cs_n[01]		J26	sys_data[35]		U25	sys_bootcs_n	
AC25	uart1_sin		B20	sd_ba[0]		K1	cpu_ad[03]		U26	sys_dsvcs_n[01]	
AC26	uart0_dcd_n		B21	sd_we_n		K2	cpu_ad[04]		V1	sc_hit	

Table 3 RC64145 388-pin BGA Package Pin-Out (Page 2 of 3)

Pin	Name	Alt	Pin	Name	Alt	Pin	Name	Alt	Pin	Name	Alt
AD1	no connect		B22	sys_data[29]		K3	cpu_ad[01]		V2	sc_doe_n	
AD2	pci_ad[18]		B23	sys_data[26]		K4	cpu_ad[40]		V3	sys_clk	
AD3	Vss I/O		B24	sys_data[24]		K23	sys_data[11]		V4	Vss I/O	
AD4	pci_ad[16]		B25	Vss I/O		K24	sys_data[34]		V23	no connect	
AD5	pci_ad[12]		B26	Vss I/O		K25	sys_data[09]		V24	sys_devcs_n[0]	
AD6	pci_ad[08]		C1	cpu_ad[15]		K26	sys_data[32]		V25	sys_xcvrdir_wr_n	
AD7	pci_ad[04]		C2	cpu_ad[52]		L1	cpu_ad[39]		V26	sys_xcvroe_n	
AD8	pci_ad[0]		C3	Vss I/O		L2	cpu_ad[02]		W1	cpu_rdy_n	
AD9	pci_cbe_n[02]		C4	cpu_ad[53]		L3	cpu_cmd[08]		W2	cpu_validout_n	
AD10	pci_frame_n		C5	cpu_ad[54]		L4	Vcc I/O		W3	pci_ad[30]	
AD11	cpu_adc[06]		C6	cpu_ad[56]		L11	Vss I/O		W4	cpu_int_n	
AD12	pci_lock_n		C7	cpu_ad[21]		L12	Vss I/O		W23	Vss I/O	
AD13	pci_serr_n		C8	cpu_ad[23]		L13	Vss I/O		W24	no connect	
AD14	pci_par		C9	cpu_ad[25]		L14	Vss I/O		W25	no connect	
AD15	pci_int_n		C10	cpu_ad[27]		L15	Vss I/O		W26	Vcc Core	
AD16	sys_datap[07]	pio[20]	C11	cpu_ad[29]		L16	Vss I/O		Y1	pci_ad[31]	
AD17	sys_datap[06]	pio[19]	C12	cpu_ad[31]		L23	Vcc I/O		Y2	sys_rst_n	
AD18	jtg_clk		C13	sys_data[62]		L24	sys_data[10]		Y3	pci_ad[26]	
AD19	sys_datap[02]	pio[15]	C14	sys_data[63]		L25	sys_data[07]		Y4	pci_ad[28]	
AD20	pio[09]		C15	Vcc Core		L26	sys_data[08]		Y23	sys_wait	pio[8]
AD21	sys_data[47]		C16	sys_adr[06]		M1	cpu_ad[38]		Y24	sys_ale	
AD22	Vcc Core		C17	sys_adr[10]		M2	cpu_ad[0]		Y25	dma_ack_n[02]	pio[2]
AD23	no connect		C18	sys_dqm_we_n[1]		M3	Vss Core		Y26	dma_ack_n[3]	pio[3]
AD24	Vss I/O		C19	sys_dqm_we_n[03]		M4	cpu_cmd[07]				
AD25	uart1_sout		C20	sd_cs_n[02]		M11	Vss I/O				
AD26	sys_data[44]		C21	sd_ras_n		M12	Vss I/O				
AE1	Vss I/O		C22	sys_data[31]		M13	Vss I/O				
AE2	Vss I/O		C23	sys_data[27]		M14	Vss I/O				
AE3	no connect		C24	Vss I/O		M15	Vss I/O				
AE4	pci_ad[17]		C25	sys_data[43]		M16	Vss I/O				
AE5	pci_ad[14]		C26	Vcc Core		M23	sys_data[48]				

Table 3 RC64145 388-pin BGA Package Pin-Out (Page 3 of 3)

RC64145 logic diagram

Figure 3 illustrates the direction and functional groupings of the RC64145 system controller.

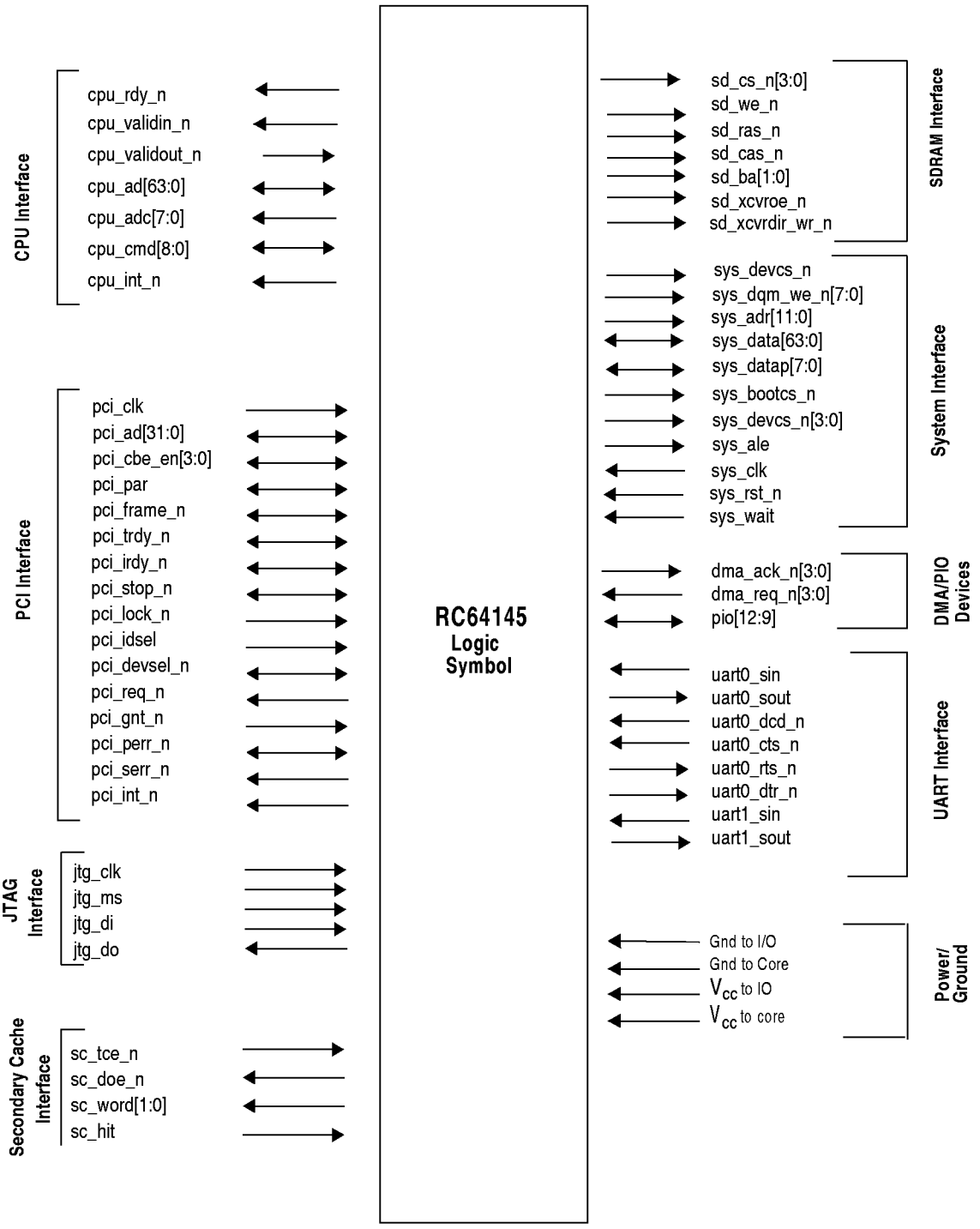


Figure 3 Logic Diagram for RC64145

Clock parameters — RC64145

(Tc = 0°C to +95°C for commercial, Tc = -40°C to +95°C for industrial, V_{cc} IO, V_{cc} Core = +3.3V±5%)

Parameter	Symbol	Test Conditions	RC64145 83MHz		Units
			Min	Max	
sys_clk HIGH	t_{SCHIGH}	Transition ≤ 3ns	4	—	ns
sys_clk LOW	t_{SCLOW}	Transition ≤ 3ns	4	—	ns
sys_clk period	t_{SCP}	—	12	100	ns
sys_clk Rise & Fall Time	t_{SCRise}, t_{SCFall}	—		5	ns
pci_clk Period	t_{PCP}		15.0		ns
pci_clk Rise & Fall Time	t_{PCRise}, t_{PCFall}	PCI 2.1		5	ns
jtag_tck Rise & Fall Time	t_{JCRise}, t_{JCFall}	—		5	ns
jtag clock period	t_{Jtag_clk}	—	100	—	ns
jtag_tck high	t_{Jtag_high}	—	40	60	ns
jtag_tck low	t_{Jtag_low}	—	40	60	ns
sys_rst_n	t_{srlow}	—	100		ns

AC timing characteristics — RC64145

(Tc = 0°C to +95°C for commercial, Tc = -40°C to +95°C for industrial, V_{cc} IO, V_{cc} Core = +3.3V±5%)

Signal	Symbol	Reference Edge	Test Condition	Min	Max	Unit	User Manual Timing Diagram Reference
CPU Interface							
cpu_ad	Tsu	sys_clk rising	15pF load	—	3	ns	TBD
cpu_ad	Thld	sys_clk rising		1	—	ns	
cpu_ad	Tdo	sys_clk rising		—	11	ns	
cpu_adc	Tdo	sys_clk rising		—	12	ns	
cpu_cmd	Tsu	sys_clk rising		—	9	ns	
cpu_cmd	Thld	sys_clk rising		0	—	ns	
cpu_cmd	Tdo	sys_clk rising		—	11	ns	
cpu_validin_n	Tdo	sys_clk rising		—	10	ns	
cpu_validout_n	Tsu	sys_clk rising		—	6	ns	
cpu_validout_n	Thld	sys_clk rising		1	—	ns	
cpu_rdy_n	Tdo	sys_clk rising		—	12	ns	
cpu_int_n	Tdo	sys_clk rising		—	12	ns	

Signal	Symbol	Reference Edge	Test Condition	Min	Max	Unit	User Manual Timing Diagram Reference
Secondary Cache Interface							
sc_tce_n	Tsu	sys_clk rising		—	2	ns	
sc_tce_n	Thld	sys_clk rising		0	—	ns	
sc_hit	Tsu	sys_clk rising		—	4	ns	
sc_hit	Thld	sys_clk rising	**15pF Load**	0	—	ns	**TBD**
sc_word	Tdo	sys_clk rising		—	?	ns	
sc_doe_n	Tdo	sys_clk rising			9		
DMA Interface							
dma_ack_n	Tsu	sys_clk rising		—	—	ns	
dma_ack_n	Thld	sys_clk rising		—	—	ns	
dma_ack_n	Tdo	sys_clk rising		—	13	ns	
dma_req_n	Tsu	sys_clk rising	**25 pF load**	—	5	ns	**TBD**
dma_req_n	Thld	sys_clk rising		0	—	ns	
dma_req_n	Tdo	sys_clk rising		—	—	ns	
pio	Tsu	sys_clk rising		—	5	ns	
pio	Thld	sys_clk rising		0	—	ns	
pio	Tdo	sys_clk rising		—	13	ns	

Signal	Symbol	Reference Edge	Test Condition	Min	Max	Unit	User Manual Timing Diagram Reference
System Interface							
sys_data	Tsu	sys_clk rising		—	9	ns	
sys_data	Thld	sys_clk rising		0	—	ns	
sys_data	Tdo	sys_clk rising		—	10	ns	
sys_datap	Tsu	sys_clk rising		—	5	ns	
sys_datap	Thld	sys_clk rising		0	—	ns	
sys_datap	Tdo	sys_clk rising	**50 pF load**	—	11	ns	**TBD**
sys_adr	Tdo	sys_clk rising		—	9	ns	
sys_dqm_we_n	Tdo	sys_clk rising		—	9	ns	
sys_devoe_n	Tdo	sys_clk rising		—	9	ns	
sys_devoe_n	Tdo	sys_clk rising		—	9	ns	
sys_bootcs_n	Tdo	sys_clk rising		—	9	ns	
sys_ale	Tdo	sys_clk rising, 1/2 sys_clk long pulse		—	10	ns	
sys_ready_n	Tsu	sys_clk rising		—	1	ns	
sys_ready_n	Thld	sys_clk rising		0	—	ns	
sys_ready_n	Tdo	sys_clk rising		—	—	ns	
PCI							
pci_ad	Tsu	pci_clk rising		—	5	ns	pci_ad
pci_ad	Thld	pci_clk rising		1	—	ns	pci_ad
pci_ad	Tdo	pci_clk rising		—	9	ns	pci_ad
pci_cbe_n	Tsu	pci_clk rising		—	4	ns	pci_cbe_n
pci_cbe_n	Thld	pci_clk rising	**PCI 2.1**	1	—	ns	pci_cbe_n
pci_cbe_n	Tdo	pci_clk rising,		—	8	ns	pci_cbe_n
pci_frame_n	Tsu	pci_clk rising		—	2	ns	pci_frame_n
pci_cbe_n	Thld	pci_clk rising		0	—	ns	pci_cbe_n
pci_ad	Tsu	pci_clk rising		—	5	ns	pci_ad
pci_cbe_n	Tdo	pci_clk rising		—	8	ns	
pci_irdy_n	Tsu	pci_clk rising		—	4	ns	
pci_irdy_n	Thld	pci_clk rising		1	—	ns	

Signal	Symbol	Reference Edge	Test Condition	Min	Max	Unit	User Manual Timing Diagram Reference
pci_irdy_n	Tdo	pci_clk rising	PCI 2.1	—	8	ns	
pci_trdy_n	Tsu	pci_clk rising		—	4	ns	
pci_trdy_n	Thld	pci_clk rising		1	—	ns	
pci_trdy_n	Tdo	pci_clk rising		—	8	ns	
pci_devsel_n	Tsu	pci_clk rising		—	4	ns	
pci_devsel_n	Thld	pci_clk rising		1	—	ns	
pci_devsel_n	Tdo	pci_clk rising		—	9	ns	
pci_stop_n	Tsu	pci_clk rising		—	4	ns	
pci_stop_n	Thld	pci_clk rising		0	—	ns	
pci_stop_n	Tdo	pci_clk rising		—	8	ns	
pci_perr_n	Tsu	pci_clk rising		—	3	ns	
pci_perr_n	Thld	pci_clk rising		0	—	ns	
pci_perr_n	Tdo	pci_clk rising		—	9	ns	
pci_par	Tsu	pci_clk rising		—	4	ns	
pci_par	Thld	pci_clk rising		0	—	ns	
pci_par	Tdo	pci_clk rising		—	9	ns	
pci_idsel	Tsu	pci_clk rising		—	3	ns	
pci_idsel	Thld	pci_clk rising		0	—	ns	
pci_gnt_n	Tsu	pci_clk rising		—	4	ns	
pci_gnt_n	Thld	pci_clk rising		0	—	ns	
pci_lock_n	Tsu	pci_clk rising		—	4	ns	
pci_lock_n	Thld	pci_clk rising		0	—	ns	
pci_serr_n	Tdo	pci_clk rising		—	9	ns	
pci_req_n	Tdo	pci_clk rising		—	8	ns	
pci_int_n	Tdo	pci_clk rising		—	14	ns	
SDRAM Interface							
sd_xcvroe_n	Tdo	sys_clk rising	50 pF load	—	9	ns	TBD
sd_xcvrdir_wr_n	Tdo	sys_clk rising		—	9	ns	
sd_cs_n	Tdo	sys_clk rising		—	9	ns	
sd_ba	Tdo	sys_clk rising		—	9	ns	
sd_ras_n	Tdo	sys_clk rising		—	9	ns	
sd_cas_n	Tdo	sys_clk rising		—	8	ns	
sd_we_n	Tdo	sys_clk rising		—	9	ns	

Signal	Symbol	Reference Edge	Test Condition	Min	Max	Unit	User Manual Timing Diagram Reference
UART Interfaces							
uart0_sin	Tsu	sys_clk rising		—	1	ns	
uart0_sin	Thld	sys_clk rising		1	—	ns	
uart0_dcd_n	Tsu	sys_clk rising		—	4	ns	
uart0_dcd_n	Thld	sys_clk rising		3	—	ns	
uart0_cts_n	Tsu	sys_clk rising		—	5	ns	
uart0_cts_n	Thld	sys_clk rising	**25 pF load**	3	—	ns	**TBD**
uart0_sout	Tdo	sys_clk rising		—	11	ns	
uart0_rts0_n	Tdo	sys_clk rising		—	10	ns	
uart0_dtr0_n	Tdo	sys_clk rising		—	10	ns	
uart1_sin	Tsu	sys_clk rising		—	4	ns	
uart1_sin	Thld	sys_clk rising		1	—		
uart1_sout	Tdo	sys_clk rising		—	10	ns	
JTAG Interface							
jtg_ms, jtg_di	Tsu	jtg_clk rising		10	—	ns	
jtg_ms, jtg_di	Thld	jtg_clk rising	**50 pF Load**	10	—	ns	**TBD**
jtg_do	Tdo	jtg_clk falling		—	10	ns	

Note: Tsu = input setup time to RC64145
Thld = input hold time to RC64145
Tdo = output propagation time from RC64145
Tdoh = output hold time from RC64145

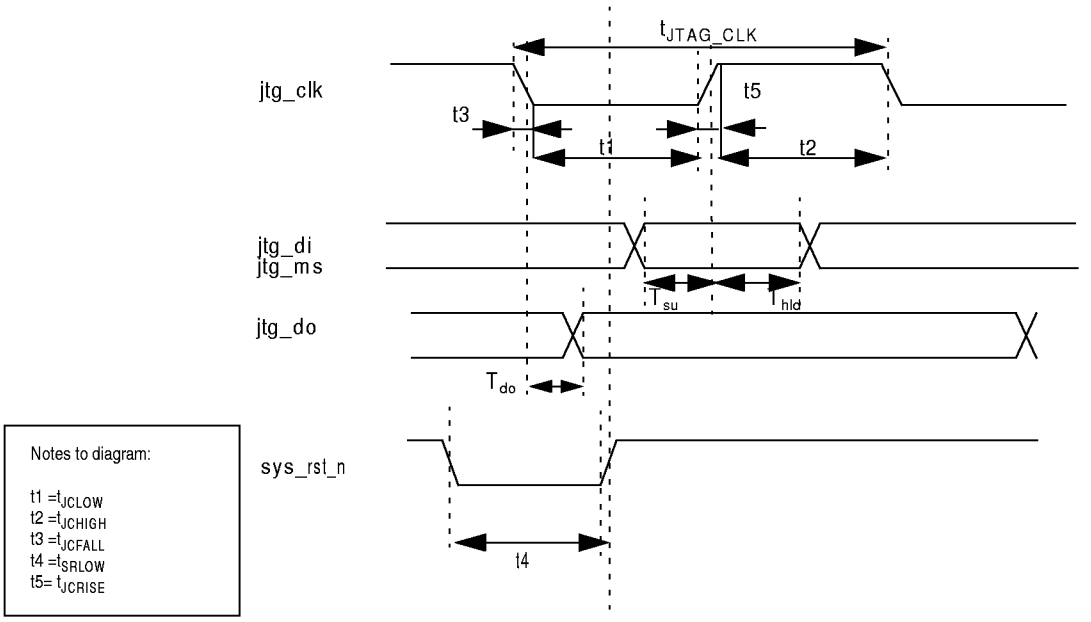


Figure 4 Standard JTAG timing

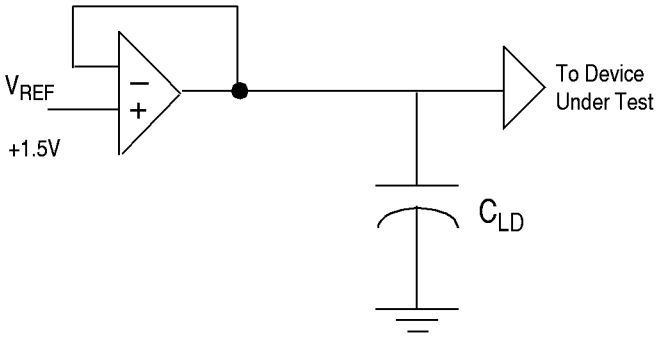
Power consumption—RC64145

Parameter		RC64145 83MHz Maximum	Conditions
I_{CC}		482mA 1.6W	C_L = 50pF T_c = 25°C V_{cc} core = 3.3V V_{cc} IO = 3.3V
P_{max}	maximum power dissipation	760mA 2.64W	V_{cc} core = 3.47V V_{cc} IO = 3.47V

Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.0	V
Vi	Input Voltage	Gnd	5.5	V
Tstg	Storage Temperature	-40	125	degrees C
Ta	Ambient Temperature Value	0	70	degrees C

Output loading for AC testing (for non-PCI signals)



Note: PCI pins have been correlated to PCI 2.1. Refer to AC parameters table for Cld values used in testing.

Recommended operation temperature and supply voltage

Grade	Temperature	Gnd_IO, GND_Core	V_{cc}IO	V_{cc}Core
Commercial	0°C to +95°C (Case)	0V	3.3V±5%	3.3V±5%
Industrial	-40°C + 95°C (Case)	0V	3.3V±5%	3.3V±5%

Capacitive load deration

Refer to the IDT document "79RC64145 IBIS Model" located on the company's web site:

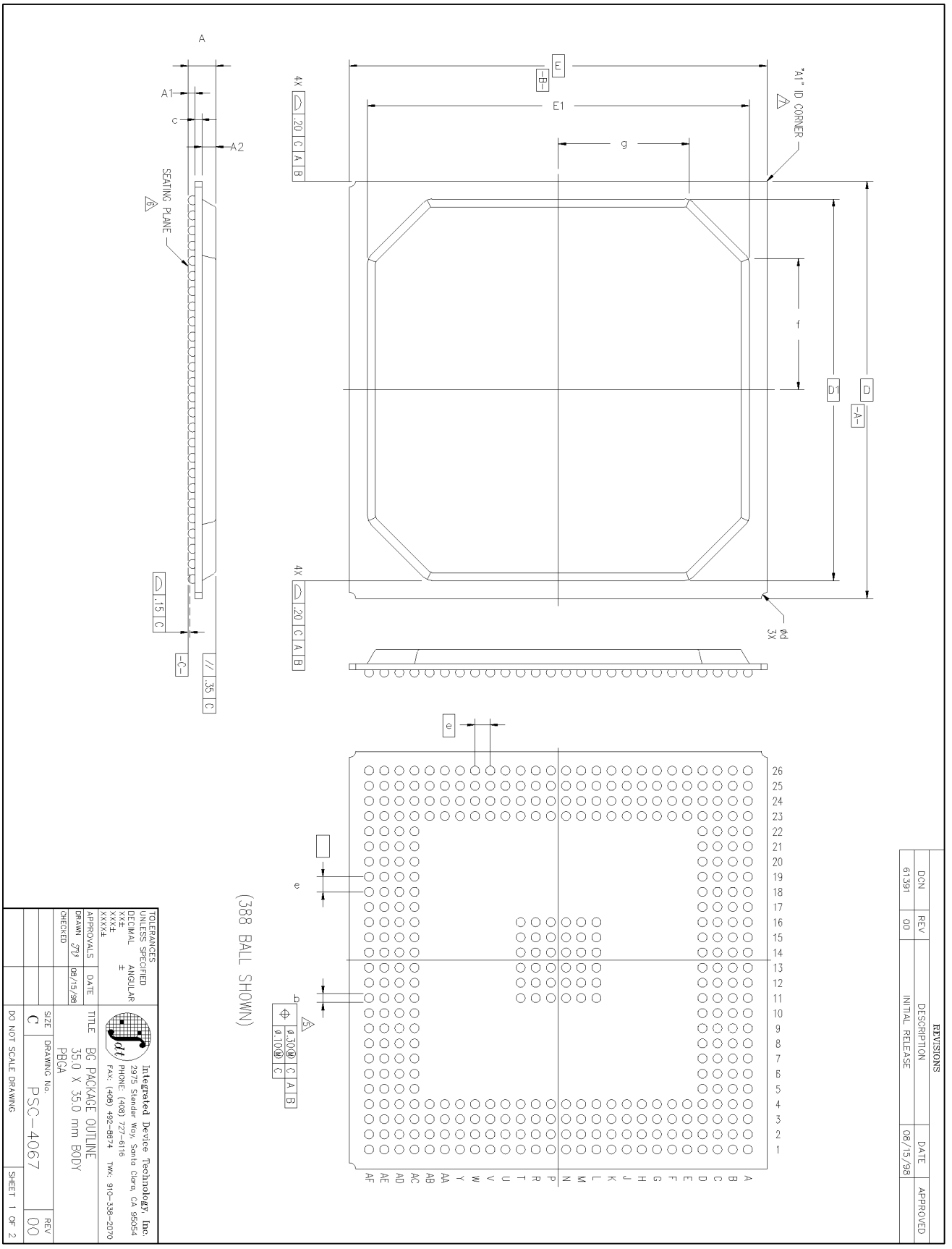
http://www.idt.com/products/pages/RISC-RC64145.html.

DC electrical characteristics

Commercial Temperature Range—RC64145

($V_{cc}IO$= 3.3±5%, T_{CASE} = 0°C to +95°C or T_{CASE} = -40°C to +95°C)

	Parameter	RC64145 100MHz		Pin Numbers	Conditions
		Minimum	Maximum		
LOW Drive Pads	V_{OL}	—	0.4V	A3, A4, A5, A6, A7, A8, A9, AA24, AA25, AA26, AB23, AB24, AB26, AC14, AD11, AD20, AD25, AE15, AE16, AE21, AE23, AF12, AF13, AF14, AF16, AF18, AF20, AF21, AF22, AF23, B3, B4, B5, B6, B7, B8, C1, C10, C11, C12, C2, C4, C5, C6, C7, C8, C9, D1, D10, D12, D2, D3, D5, D7, D8, E1, E2, E3, E4,F1, F2, F3, G1, G2, G3, G4, H1, H2, H3, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2, L3, M1, M2, M4, N1, N2, N3, P1, P3, P4, R1, R2, T1, T2, T3, U2, U3, U4, W1, W4, Y23, Y25, Y26	$\|I_{OUT}\|$ = 10.8mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 7.8mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	V_{cc} IO +2.0V		
HIGH Drive Pads	V_{OL}	—	0.4V	A10, A11, A12, A13, A15, A16, A17, A18, A19, A20, A21, A23, A24, AC19, AC20, AC22, AD16, AD17, AD19, AD21, AD26, AE19, AE20, AE22, AE26, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B9, C13, C14, C16, C17, C18, C19, C20, C21, C22, C23, C25, D13, D15, D17, D18, D20, D22,D24, D25, D26, E23, E24, E25, E26, F24, F25, F26, G23, G24, G25, G26, H23, H24, H25, H26, J24, J25, J26, K23, K24, K25, K26, L24, L25, L26, M23, M24, M25, M26, N23, N24, N25, N26, P25, P26, R23, R24, R25, R26, R3, R4, T24, T25, T26, U23, U24, U25, U26, V2, V24, V25, V26, Y24	$\|I_{OUT}\|$ = 19mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 15.6mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	V_{cc} IO +2.0V		
PCI Drive Pads	V_{OL}	—	0.4V	AA1, AA2, AA3, AB1, AB2, AB3, AB4, AC1, AC10, AC12, AC2, AC5, AC7, AC9, AD10, AD13, AD14, AD15, AD2, AD4, AD5, AD6, AD7, AD8, AD9, AE10, AE12, AE13, AE14, AE4, AE5, AE6, AE7, AE8, AF10, AF11, AF15, AF4, AF5, AF6, AF7, AF8, W3, Y1, Y3, Y4	$\|I_{OUT}\|$ = 25mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 19.5mA
	V_{IL}	—	0.8V		
	V_{IH}	2.0V	V_{cc} IO +2.0V		—
	C_{IN}	—	10pF		—
	C_{IN}	5pf	12pF		Per PCI 2.1
	C_{IN}		—		Per PCI 2.1
	C_{OUT}	—	10pF		—
	I/O_{LEAK}	—	20uA		Input/Output Leakage



Advance Information

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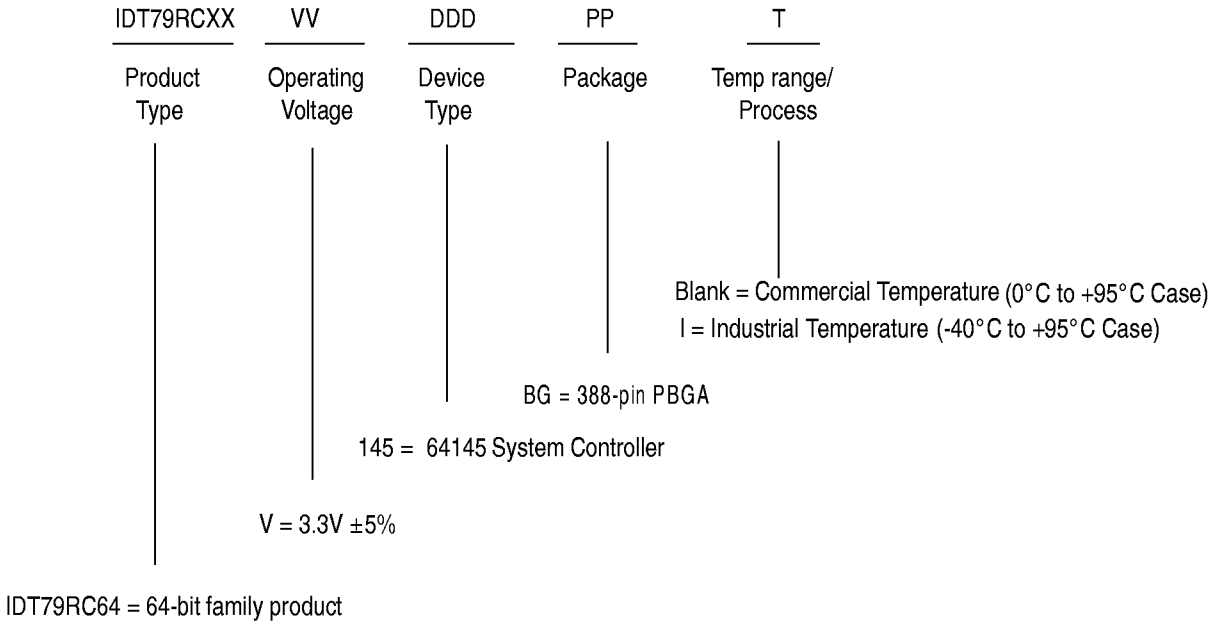

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