4M x 16 Bits x 4 Banks Synchronous DRAM

FEATURES

- Single 3.3V power supply
- Fully Synchronous to positive Clock Edge
- Clock Frequency = 133, 125, and 100MHz
- SDRAM CAS Latency = 2
- Burst Operation
  - Sequential or Interleave
  - Burst length = programmable 1,2,4,8 or full page
  - Burst Read and Write
  - Multiple Burst Read and Single Write
- DATA Mask Control per byte
- Auto Refresh (CBR) and Self Refresh
  - 8192 refresh cycles across 64ms
- Automatic and Controlled Precharge Commands
- Suspend Mode and Power Down Mode
- Industrial Temperature Range

DESCRIPTION

The WED416S16030A is 268,435,456 bits of synchronous high data rate DRAM organized as 4 x 4,196,304 words x 16 bits. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Available in a 54 pin TSOP type II package the WED416S16030A is tested over the industrial temp range (-40°C to +85°C) providing a solution for rugged main memory applications.

**This product is subject to change without notice.*

PIN CONFIGURATION

Pin	Front	Pin	Front	Pin	Front
1	V_{CC}	19	CE#	37	CKE
2	DQ0	20	BA0	38	CK
3	V_{CCQ}	21	BA1	39	UDQM
4	DQ1	22	A10/AP	40	NC/RFU
5	DQ2	23	A0	41	V_{SS}
6	V_{SSQ}	24	A1	42	DQ8
7	DQ3	25	A2	43	V_{CCQ}
8	DQ4	26	A3	44	DQ9
9	V_{CCQ}	27	V_{CC}	45	DQ10
10	DQ5	28	V_{SS}	46	V_{SSQ}
11	DQ6	29	A4	47	DQ11
12	V_{SSQ}	30	A5	48	DQ12
13	DQ7	31	A6	49	V_{CCQ}
14	V_{CC}	32	A7	50	DQ13
15	LDQM	33	A8	51	DQ14
16	WE#	34	A9	52	V_{SSQ}
17	CAS#	35	A11	53	DQ15
18	RAS#	36	A12	54	V_{SS}

PIN DESCRIPTION

A0-12	Address Inputs
BA0, BA1	Bank Select Addresses
CE#	Chip Select
WE#	Write Enable
CK	Clock Input
CKE	Clock Enable
DQ0-15	Data Input/Output
L(U)DQM	Data Input/Output Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
V_{DD}	Power (3.3V)
V_{DDQ}	Data Output Power
V_{SS}	Ground
V_{SSQ}	Data Output Ground
NC	No Connection

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Signal	Polarity	Function
CK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
CE#	Input	Pulse	Active Low	CE# disable or enable device operation by masking or enabling all inputs except CK, CKE and DQM.
RAS#, CAS# WE#	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operation to be executed by the SDRAM.
BA0,BA1	Input	Level	—	Selects which SDRAM bank is to be active.
A0-12, A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-12 defines the row address (RA0-12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-8 defines the column address (CA0-8) when sampled at the rising clock edge. In addition to the row address, A10/AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If A10/AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged . If A10/AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If A10/AP is high, all banks will be precharged regardless of the state of BA0, BA1. If A10/AP is low, then BA0, BA1 is used to define which bank to precharge.
DQ0-15	Input/Output	Level	—	Data Input/Output are multiplexed on the same pins
L(U)DQM	Input	Pulse	Mask Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high.
V_{CC}, V_{SS}	Supply			Power and ground for the input buffers and the core logic.
V_{CCQ}, V_{SSQ}	Supply			Isolated power and ground for the output buffers to improve noise immunity.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DD}	-1.0	+4.6	V
Input Voltage	V_{IN}	-1.0	+4.6	V
Output Voltage	V_{OUT}	-1.0	+4.6	V
Operating Temperature	t_{OPR}	-40	+85	°C
Storage Temperature	t_{STG}	-55	+125	°C
Power Dissipation	P_D		1.0	W
Short Circuit Output Current	I_{OS}		50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: V_{SS} = 0V, 40°C ≤ Ta ≤ 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	
Output High Voltage	V_{OH}	2.4	—	—	V	(I_{OH} = -4mA)
Output Low Voltage	V_{OL}	—	—	0.4	V	(I_{OL} = 4mA)
Input Leakage Voltage	I_{IL}	-5	—	5	µA	
Output Leakage Voltage	I_{OL}	-5	—	5	µA	

CAPACITANCE

(T_A = 25°C, f = 1MHz, V_{CC} = 3.3V TO 3.6V)

Parameter	Symbol	Max	Unit
Input Capacitance (A0-12, BA0-1)	CI1	4	pF
Input Capacitance (CK, CKE, RAS#, CAS#, WE#, CE#, L(U)DQM)	CI2	4	pF
Input/Output Capacitance (DQ0-15)	C_{OUT}	6.5	pF

OPERATING CURRENT CHARACTERISTICS

(V_{CC} = 3.3V, -40°C ≤ Ta ≤ +85°C)

Parameter/Condition		Symbol	All Speeds	Units	Notes
Operating Current Active Mode; Burst = 2; READ or WRITE t_{RC} = $t_{RC(MIN)}$		I_{CC1}	135	mA	3, 18, 19, 32
Standby Current Power-Down Mode; All banks idle; CKE = LOW		I_{CC2}	2	mA	32
Standby Current: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress		I_{CC3}	40	mA	3, 12, 19, 32
Operating Current: Burst Mode; Page burst: READ or WRITE; All banks active		I_{CC4}	135	mA	3, 18, 19, 32
Auto Refresh Current CS# = HIGH: CKE = HIGH	t_{RFC} = $t_{RFC(MIN)}$	I_{CC5}	285	mA	3, 12, 18, 19, 32, 33
	t_{RFC} = 7.81 µs	I_{CC6}	3.5	mA	
Self Refresh Current: CKE ≤ 0.2V	Standard	I_{CC7}	2.5	mA	4
	Low Power (L)	I_{CC7}	1.5	mA	

NOTES:

1. Measured with outputs open.

2. Refresh period is 64ms.

AC CHARACTERISTICS

OPERATING AC PARAMETERS

(Vcc = 3.3V, -40°C ≤ Ta ≤ +85°C)

Parameter		Symbol	7	75	8	10	Unit	Notes
Clock Cycle Time	CAS latency = 3	t_{CK}	7.5	7.5	8	10	ns	1
	CAS latency = 2		7.5	8	10	1		
Clock to Valid Output Delay		t_{AC}	5.4	6	6	7	ns	1,2
Output Data Hold Time		t_{OH}	3	3	3	3	ns	2
Clock High Pulse Width		t_{CH}	2.5	2.5	3	3	ns	3
Clock Low Pulse Width		t_{CL}	2.5	2.5	3	3	ns	3
Input Setup Time		t_{CMS}	1.5	1.5	2	2	ns	3
Input Hold Time		t_{CMH}	0.8	0.8	1	1	ns	3
Clock to Output in Low-Z		t_{LZ}	1	1	1	1	ns	2
Clock to Output in High-Z		t_{HZ}	5.4	6	6	7	ns	
Row Active to Row Active Delay		t_{RRD}	15	15	20	20	ns	4
RAS# to CAS# Delay		t_{RCD}	20	20	20	20	ns	4
Row Precharge Time		t_{RP}	20	20	20	20	ns	4
Row Active Time		t_{RAS}	45	45	50	50	ns	4
Row Cycle Time - Operation		t_{RC}	65	65	70	70	ns	4
Last Data In to New Column Address Delay		t_{CDL}	1	1	1	1	CK	5
Last Data In to Row Precharge		t_{RDL}	2	2	2	2	CK	5
Last Data In to Burst Stop		t_{BDL}	1	1	1	1	CK	5
Column Address to Column Address Delay		t_{CCD}	1	1	1	1	CK	6
Number of Valid Output Data	CAS latency = 3		2	2	2	2	ea	7
	CAS latency = 2		1	1	1	1		
Data Setup Time		t_{DS}	1.5	1.5	2	2	ns	
Data Hold Time		t_{DH}	0.8	0.8	1	1	ns	

NOTES:

1. Parameters depend on programmed CAS latency.
2. If clock rise time is longer than 1ns, (t_{RISE} 2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time = 1ns. If t_{RISE} & t_{FALL} are longer than 1ns, [(t_{RISE} + t_{FALL})/2]-1ns should be added to the parameter.
4. The minimum number of clock cycles required is determined by dividing the minimum time required by the clock cycle time and then rounding up to the next higher integer.
5. Minimum delay is required to complete write.
6. All devices allow every cycle column address changes.
7. In case of row precharge interrupt, auto precharge and read burst stop.

COMMAND TRUTH TABLE

Command			CKE		CE#	RAS#	CAS#	WE#	DQM	BA0,1	A10/AP	A0-9, A11-12	Notes
			Previous Cycle	Current Cycle									
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			
Refresh	Auto(CBR)		H	H	L	L	L	H	X	X	X	X	
	Entry Self												
Precharge	Single Bank		H	X	L	L	H	L	X	BA	L	X	2
	All Banks									X	H	X	
Bank Activate			H	X	L	L	H	H	X	BA	Row Address		2
Write	Auto Precharge Disable		H	X	L	H	L	L	X	BA	L	Column Address	2
	Auto Precharge Enable										H		
Read	Auto Precharge Disable		H	X	L	H	L	H	X	BA	L	Column Address	2
	Auto Precharge Enable										H		
Burst Stop			H	X	L	H	H	L	X	X	X	X	3
No Operation			H	X	L	H	H	H	X	X	X	X	
Device Select			H	X	H	X	X	X	X	X	X	X	
Clock Suspend/Standby Mode L			X	X	X	X	X	X	X	X	X	4	
Data	Write/Output Enable		H	X	X	X	X	X	L	X	X	X	5
	Mask/Output Disable								H				
Power Down Mode		Entry	X	L	H	X	X	X	X	X	X	X	6
		Exit		H									

(X = Don't Care, H = Logic High, L = Logic Low)

NOTES:

1. All of the SDRAM operations are defined by states of CE#, WE#, RAS#, CAS#, and DQM at the positive rising edge of the clock.
2. Bank Select (BA), if BA0, BA1 = 0, 0 then bank A is selected, if BA0, BA1 = 1, 0 then bank B, if BA0, BA1 = 0, 1 then bank C, if BA0, BA1 = 1, 1 then bank D is selected, respectively.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS# latency.
4. During normal access mode, CKE is held high and CK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibted (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode. The Power Down Mode does not perform any Refresh operations, therefore the device cannot remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.

CLOCK ENABLE (CKE0) TRUTH TABLE

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	CE#	RAS#	CAS#	WE#	BA0,1	A0-9, A11-12		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	
	L	H	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	L	X	X	X	ILLEGAL	
	L	H	L	L	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down Mode exit, all banks idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				
	H	H	L	L	H	X				
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L	OP Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				
	H	L	L	L	H	X				
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP Code		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to the Operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

NOTES:
1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CKS}) must be satisfied before any command other than Exit is issued.
3. The address inputs (A12-A0) depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Power Down Mode, Self Refresh Mode, and the Mode Register Set can only be entered from the all banks idle state.
Must be a legal command as defined in the Current State Truth Table.

CURRENT STATE TRUTH TABLE

Current State	Command							Action	Notes
	CE#	RAS#	CAS#	WE#	BA0,1	A11-12 A10/AP-A0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	2
	L	L	L	H	X	X	Auto orSelf Refresh	Start Auto orSelf Refresh	2,3
	L	L	H	L	X	X	Precharge	No Operation	
	L	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	5
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Precharge	6
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	7,8
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Terminate Burst; Start the Write cycle	8,9
	L	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read cycle	
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Terminate Burst; Start a new Write cycle	8,9
	L	H	L	H	BA	Column	Read	Terminate Burst; Start the Read cycle	
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (CONT.)

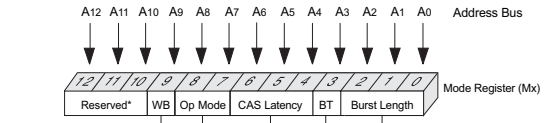
Current State	Command							Action	Notes
	CE#	RAS#	CAS#	WE#	BA0,1	A11-12, A10/AP-A0	Description		
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4,10
	L	H	L	L	BA	Column	Write	ILLEGAL	4
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{RCD}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{RCD}	
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	9
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{DPL}	
Write Recovering with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	4,9
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Precharge after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after t_{DPL}	

CURRENT STATE TRUTH TABLE (CONT.)

Current State	Command							Action	Notes
	CE#	RAS#	CAS#	WE#	BA0,1	A11-12, A10/AP-A0	Description		
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Idle after tRC	
	L	H	H	H	X	X	No Operation	No Operation; Idle after tRC	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after tRC	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

NOTES:
1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the command is being applied to.
2. Both Banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the SDRAM starts the Auto (CBR) Refresh operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The Current State refers only to one of the banks, if BA0, BA1 selects this bank then the action is illegal. If BA0, BA1 selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The RAS# to CAS# Delay (t_{RCD}) must occur before the command is given.
8. Address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

MODE REGISTER DEFINITION



*Should program M12, M11, M10 = "0, 0, 0" to ensure compatibility with future devices.

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

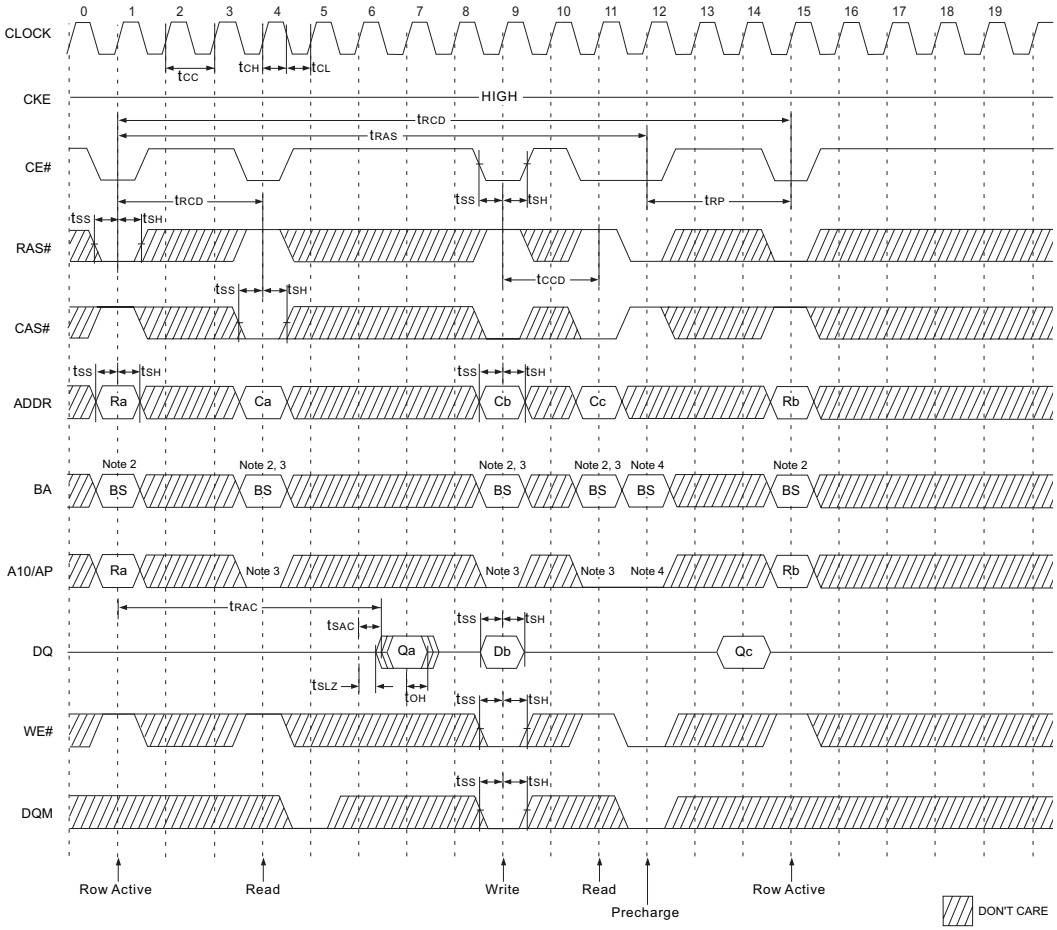
M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

SINGLE BIT READ-WRITE CYCLE (SAME PAGE) @ CAS LATENCY = 3, BURST LENGTH = 1



NOTES:

1. All input except CKE & DQM can be don't care when CE# is high at the CK high going edge.
2. Bank active & read/write are controlled by BA0~BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

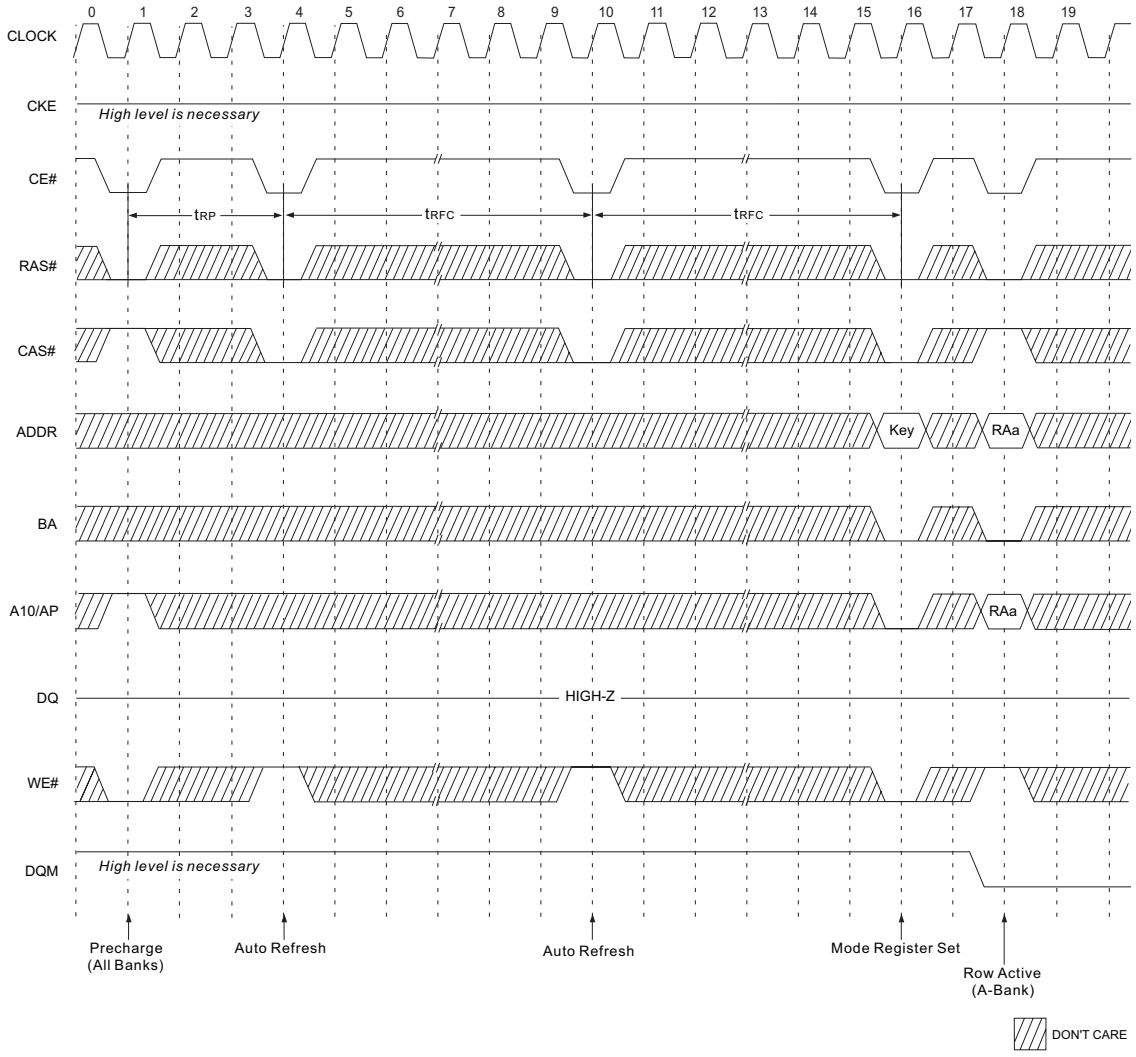
4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

A10/AP	BA0	BA1	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	x	x	All Banks

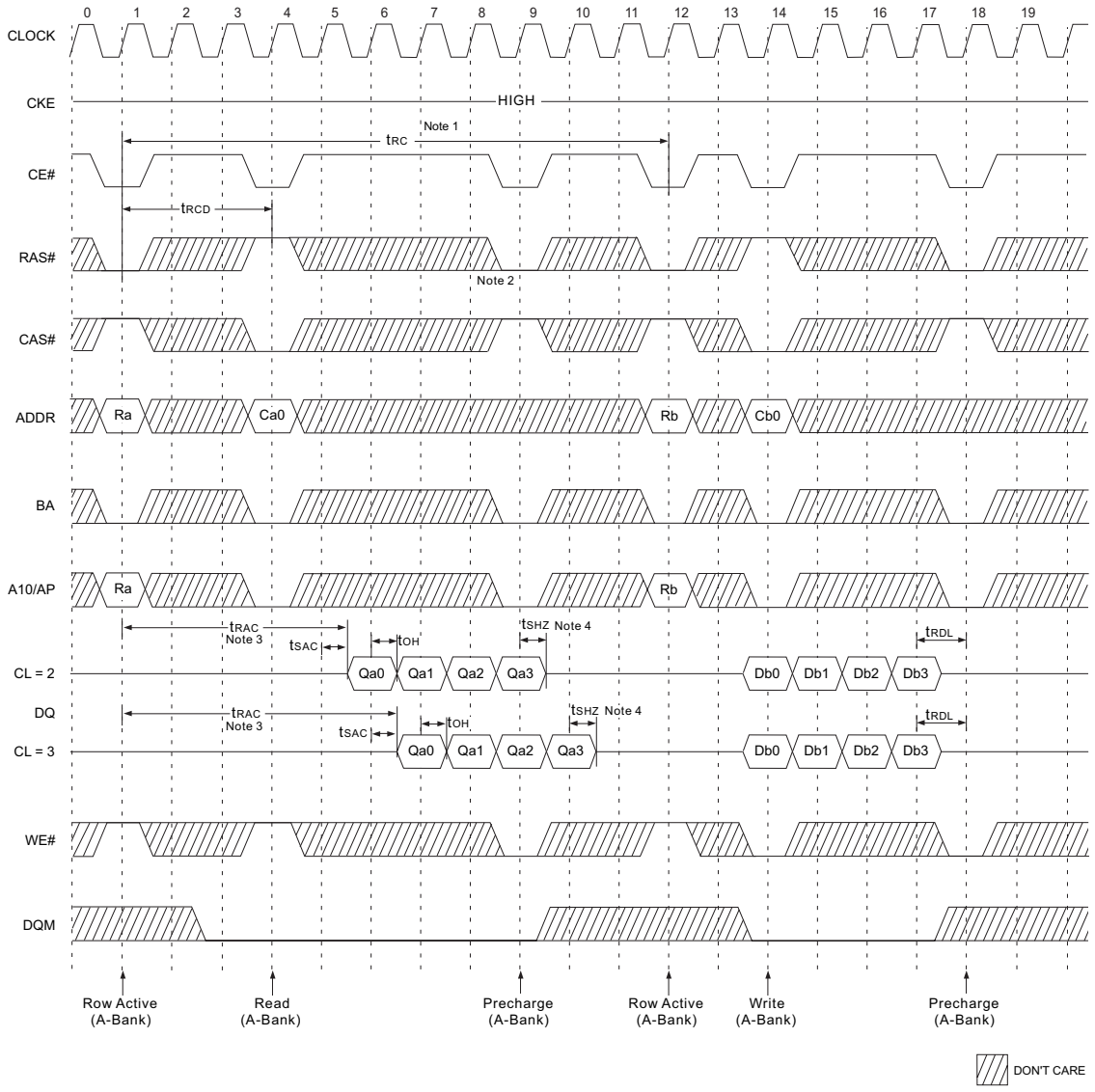
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA0	BA1	Operation
0	0	0	Distribute auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

POWER UP SEQUENCE



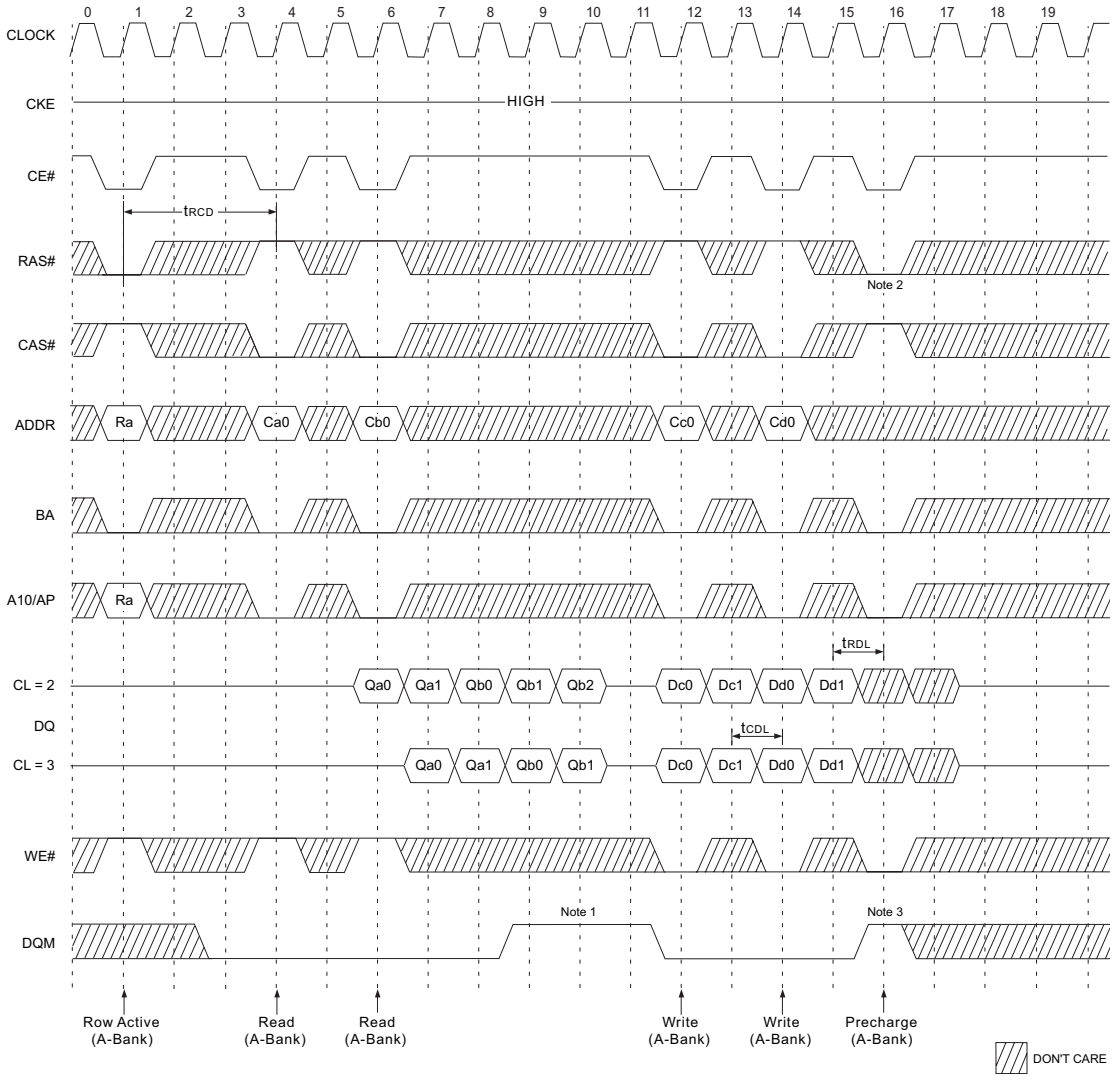
READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



NOTES:

1. Minimum row cycle times are required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. (CAS Latency - 1) number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}.
4. Output will be Hi-Z after the end of burst (1, 2, 4, 8 & full page bit burst).

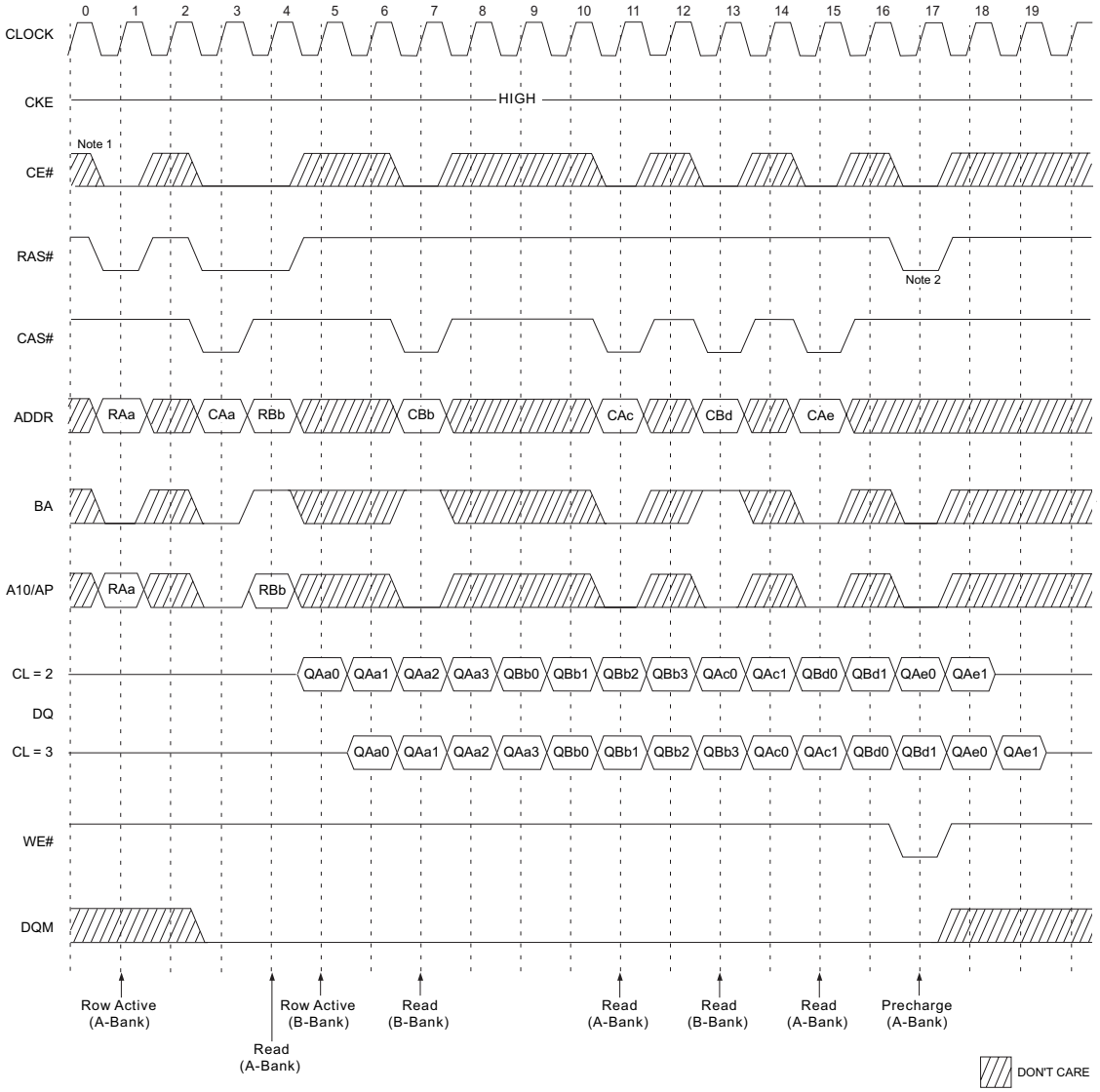
PAGE READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



NOTES:

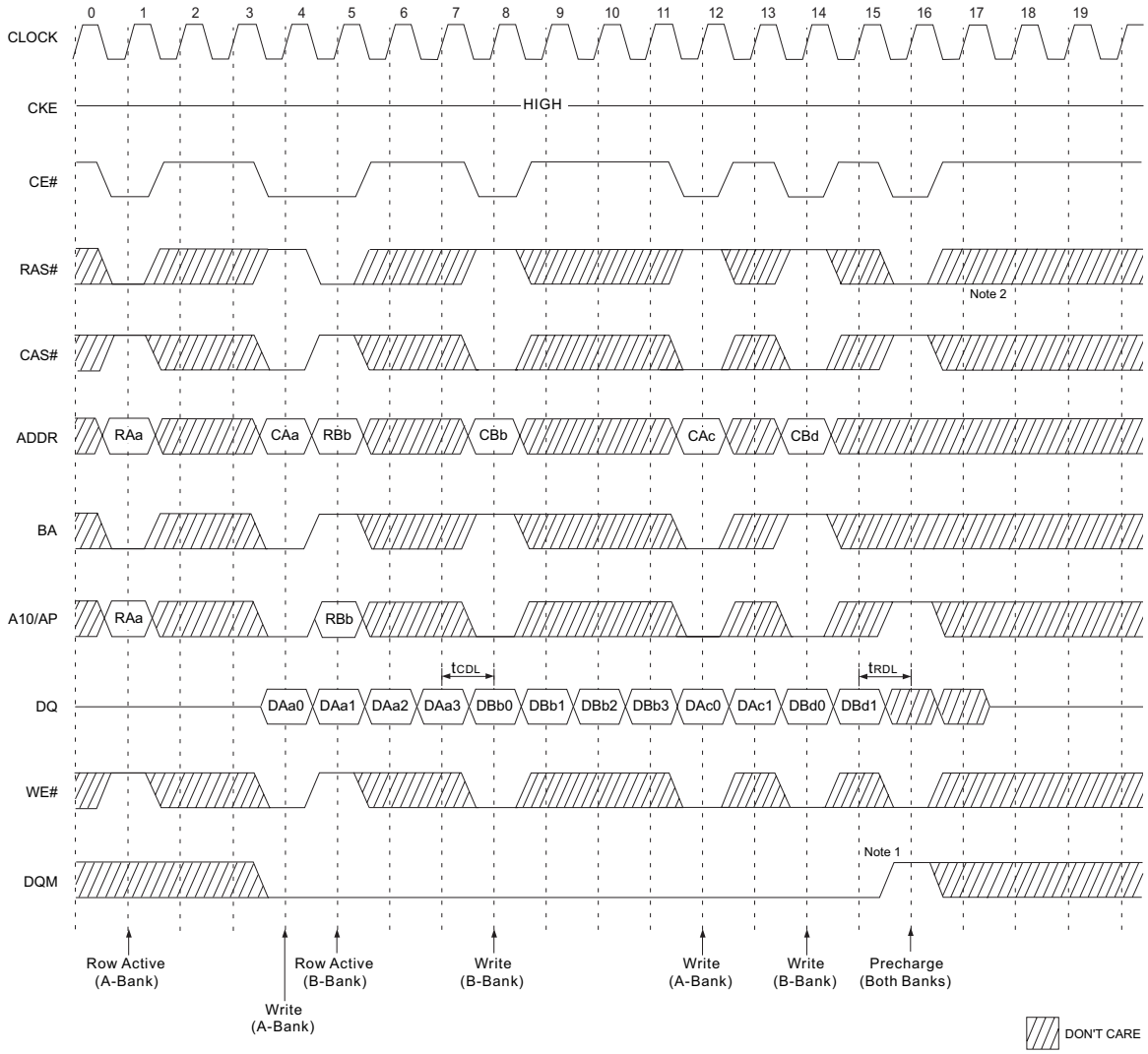
1. To write data before burst read ends, DQM should be asserted three cycles prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row prechage cycle will be masked internally.

PAGE READ CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTES:
1. CE# can be don't cared when RAS#, CAS#, and WE# are high at the clock high going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

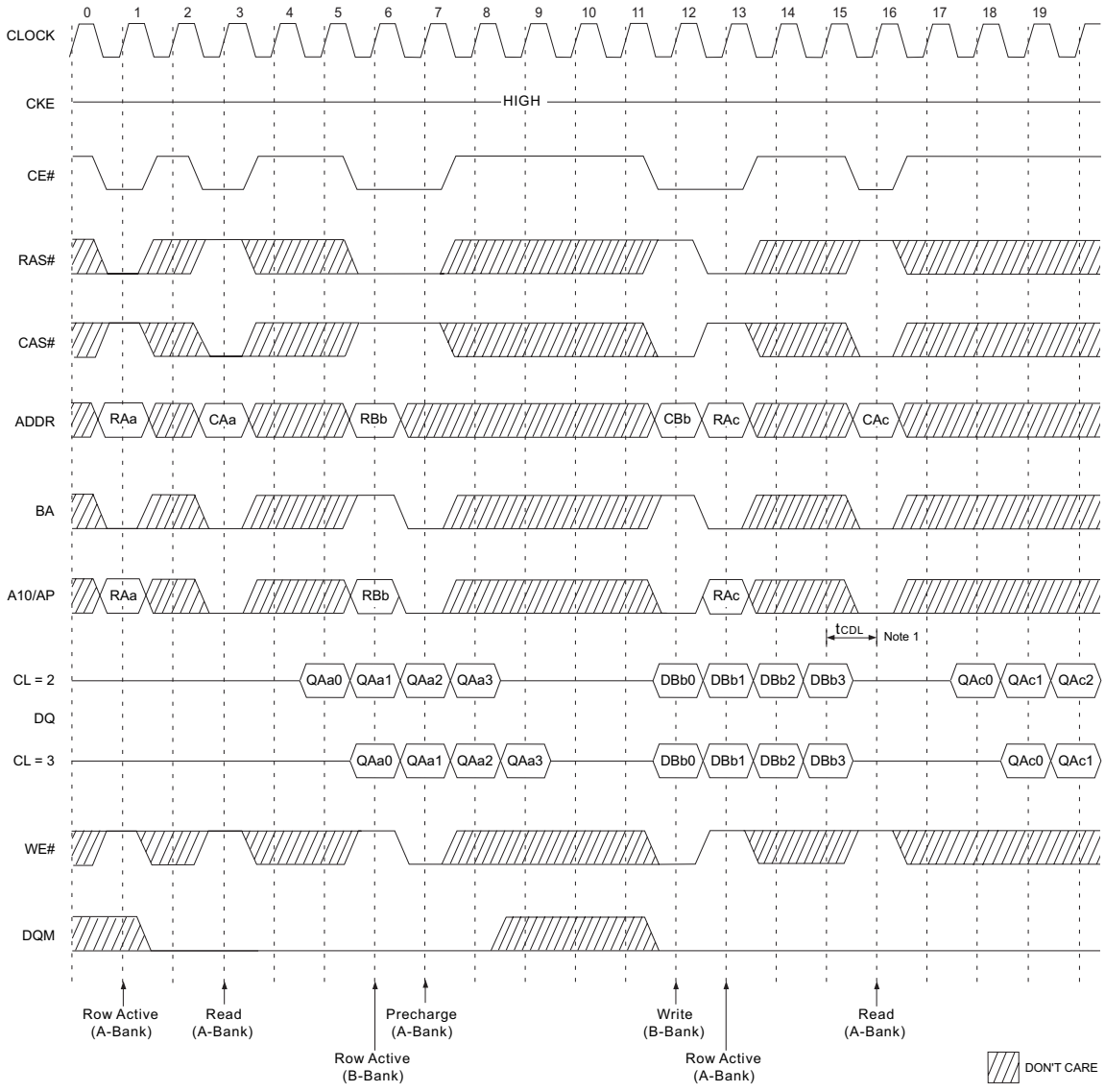
PAGE WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTES:

1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

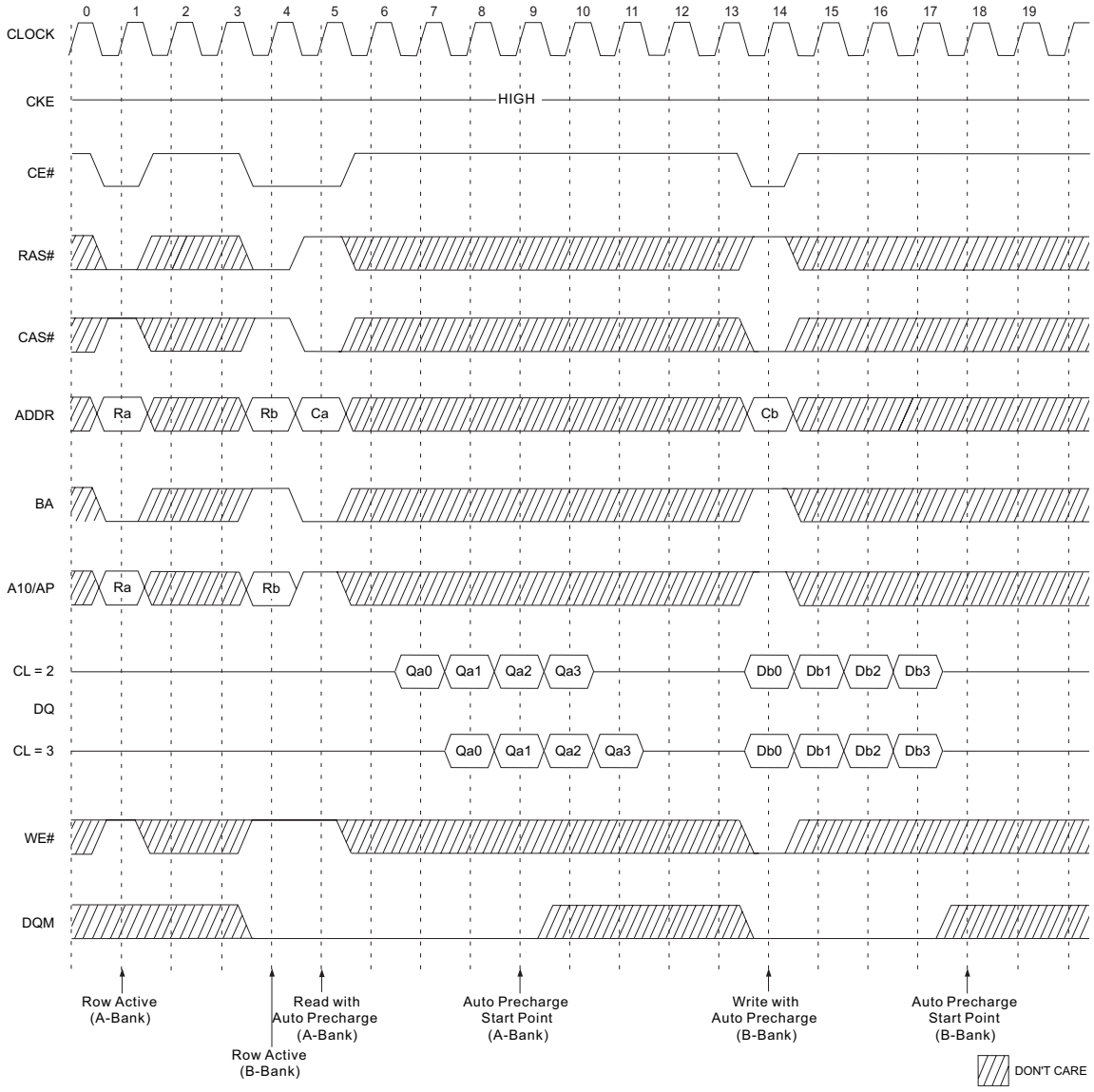
READ & WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTES:

1. t_{CDL} should be met to complete write.

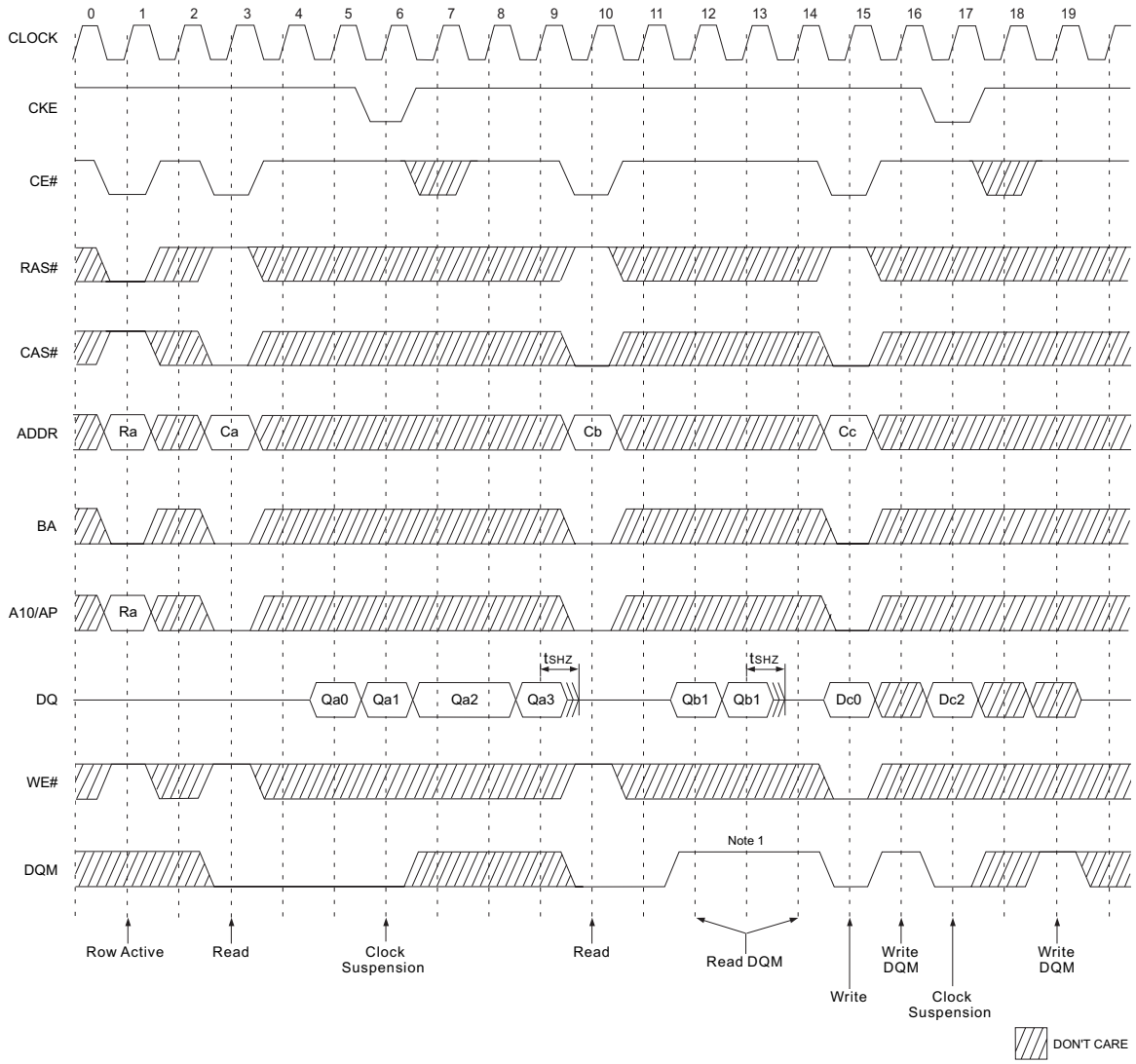
READ & WRITE CYCLE WITH AUTO PRECHARGE @ BURST LENGTH = 4



NOTES:

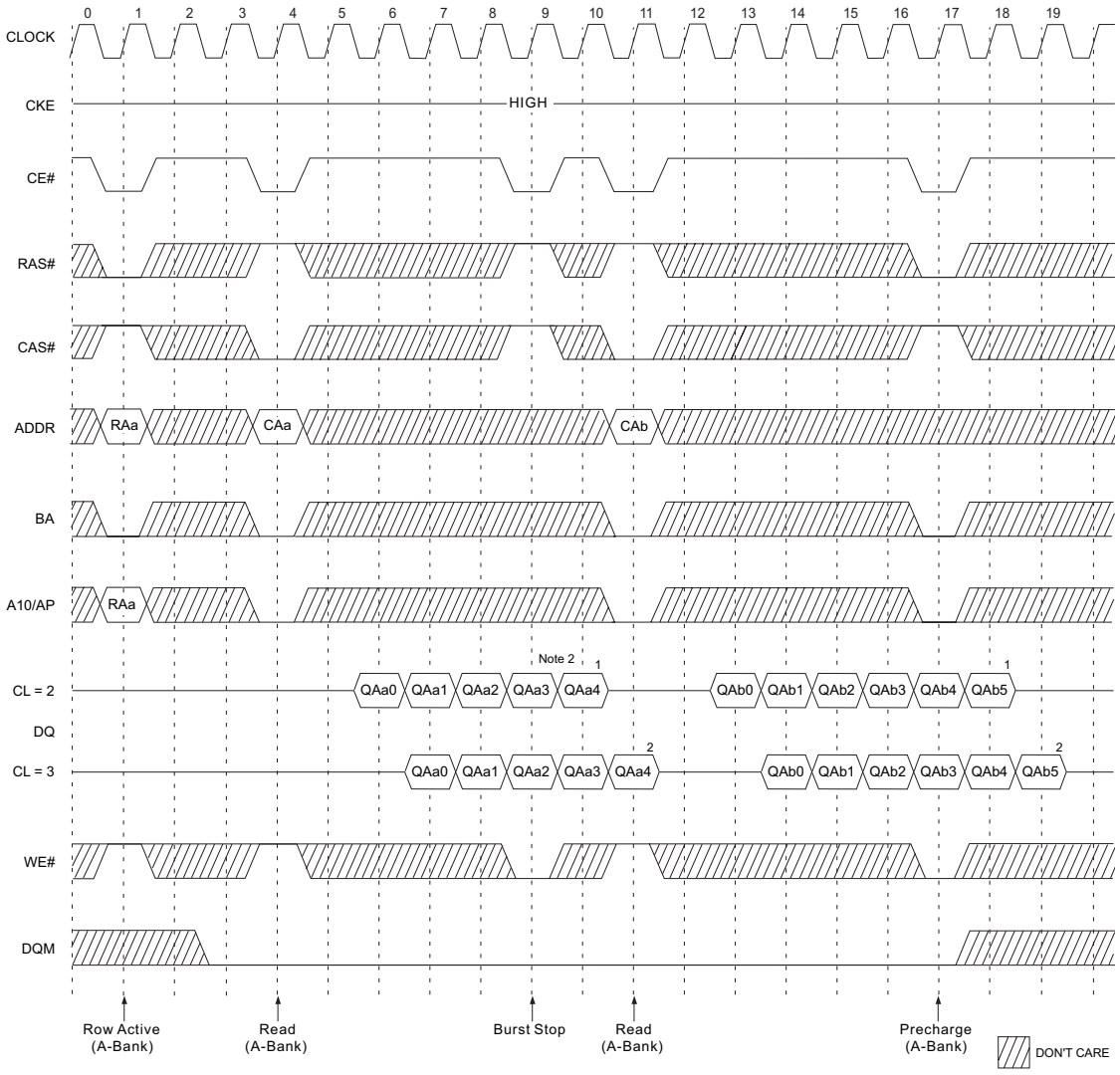
1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start. (In the case of Burst Length=1 & 2 and BRSW mode)

CLOCK SUSPENSION & DQM OPERATION CYCLE @ CAS LATENCY = 2, BURST LENGTH = 4



NOTES:
1. DQM is needed to prevent bus contention.

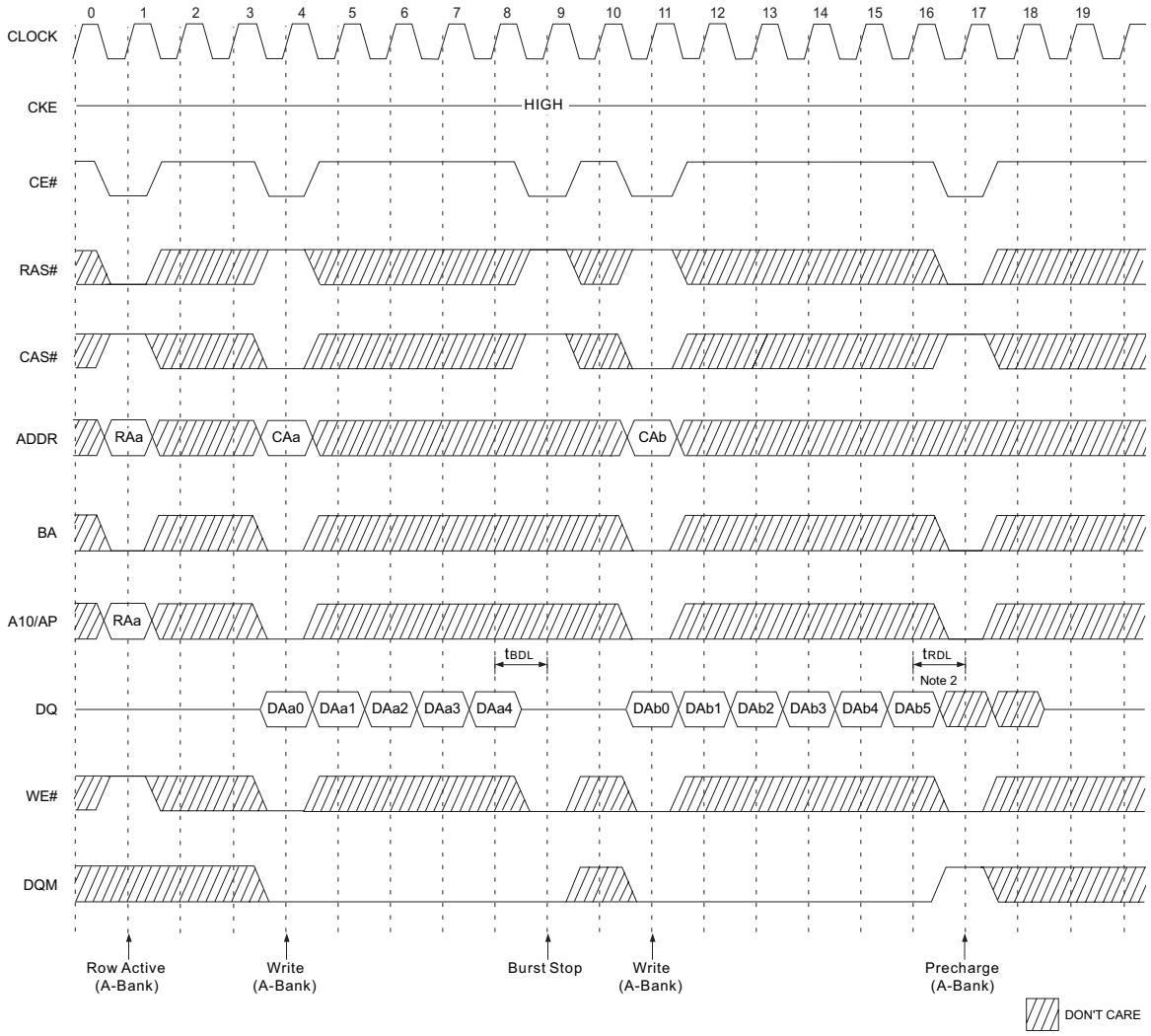
READ INTERRUPTED BY PRECHARGE COMMAND & READ BURST STOP @ BURST LENGTH=FULL PAGE



NOTES:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of RAS# interrupt. Both cases are illustrated in above timing diagram. See the label 1, 2. But at burst write, Burst stop and RAS# interrupt should be compared carefully. Refer to the timing diagram of "Full page write burst stop cycle."
3. Burst stop is valid at every burst length.

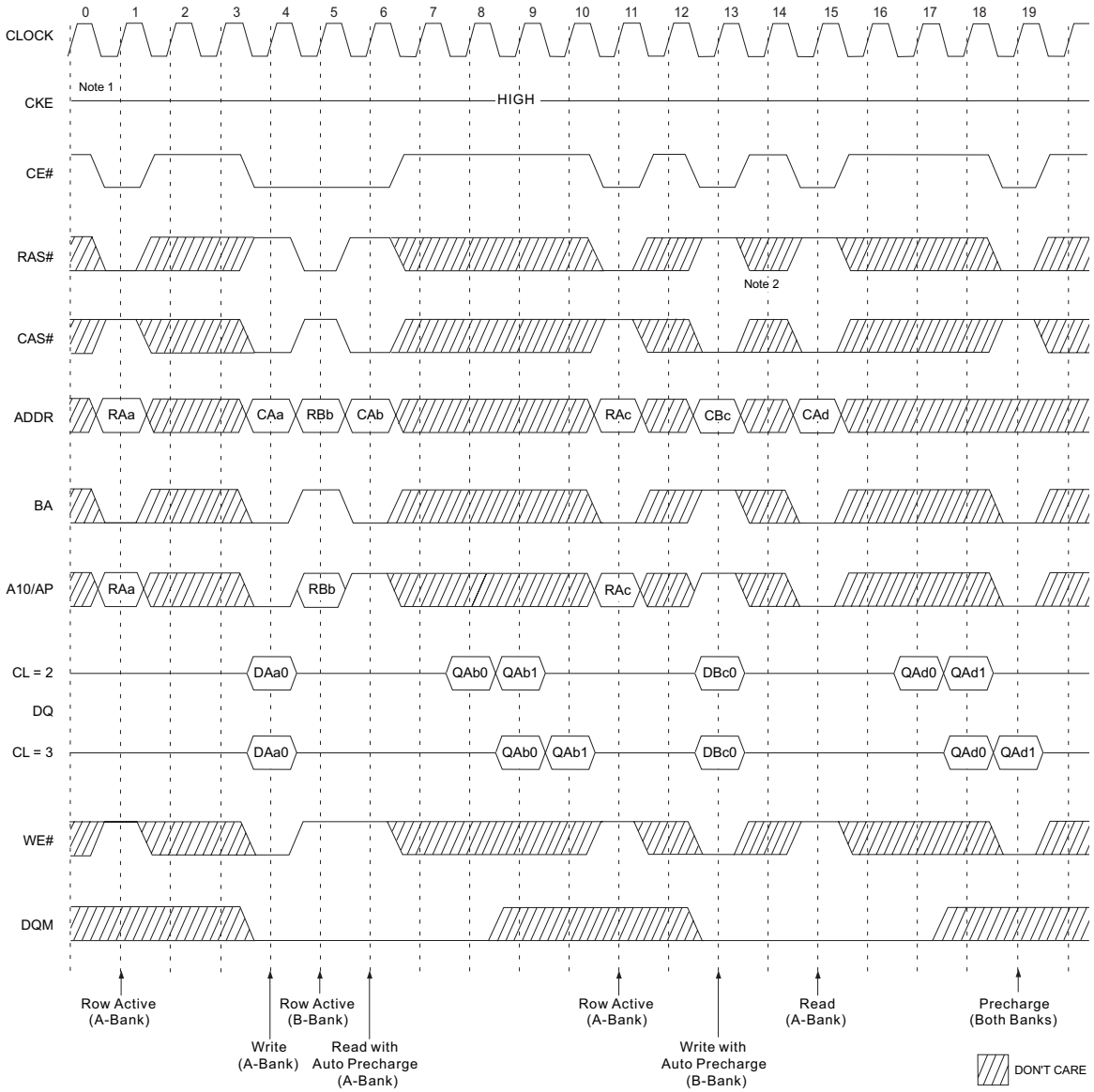
WRITE INTERRUPTED BY PRECHARGE COMMAND & WRITE BURST STOP CYCLE @ BURST LENGTH=FULL PAGE



NOTES:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. Data-in at the cycle of interrupted by precharge cannnot be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}. DQM at write interrupted by precharge command is needed to prevent invalid write. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

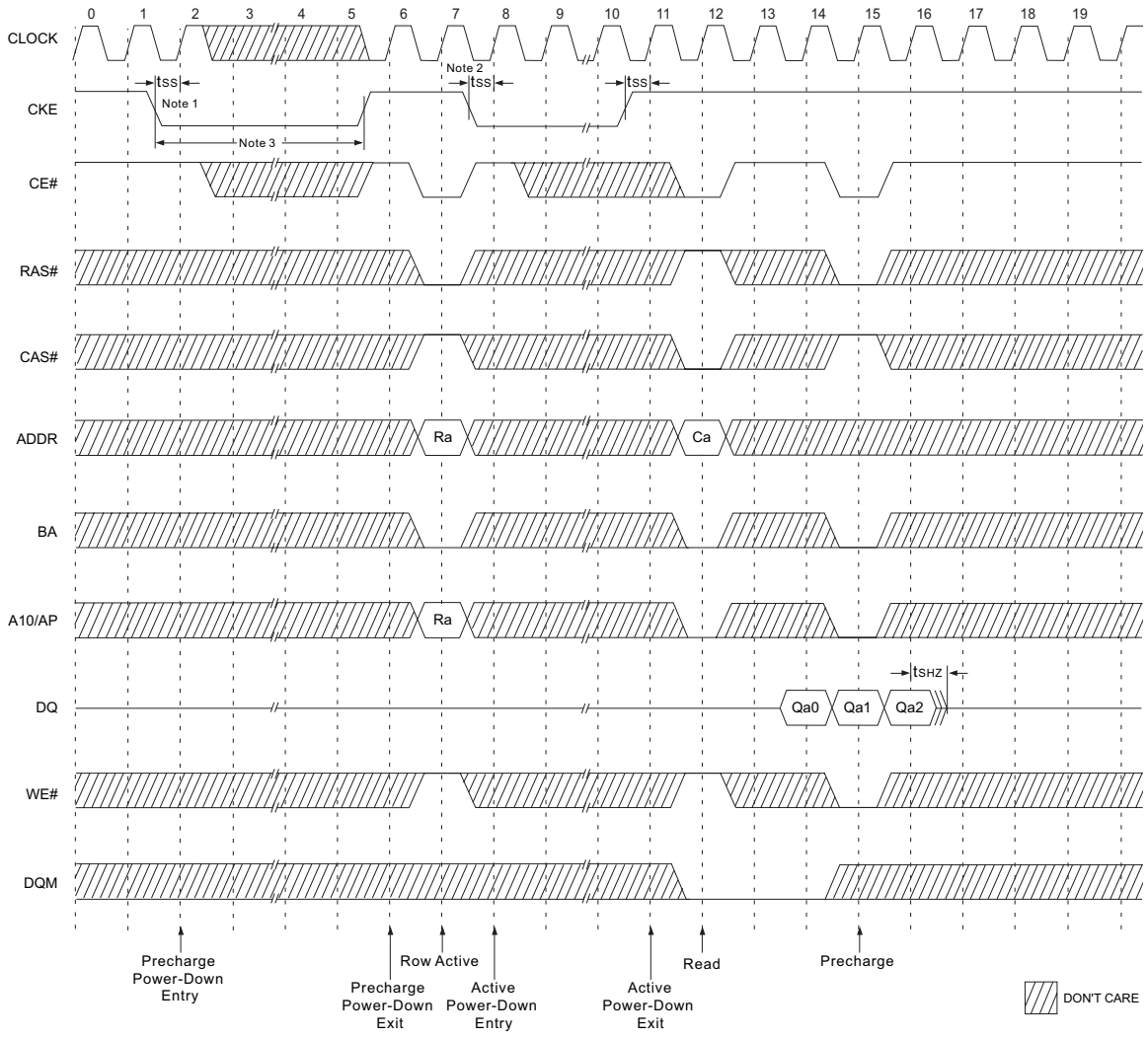
BURST READ SINGLE BIT WRITE CYCLE @ BURST LENGTH = 2



NOTES:

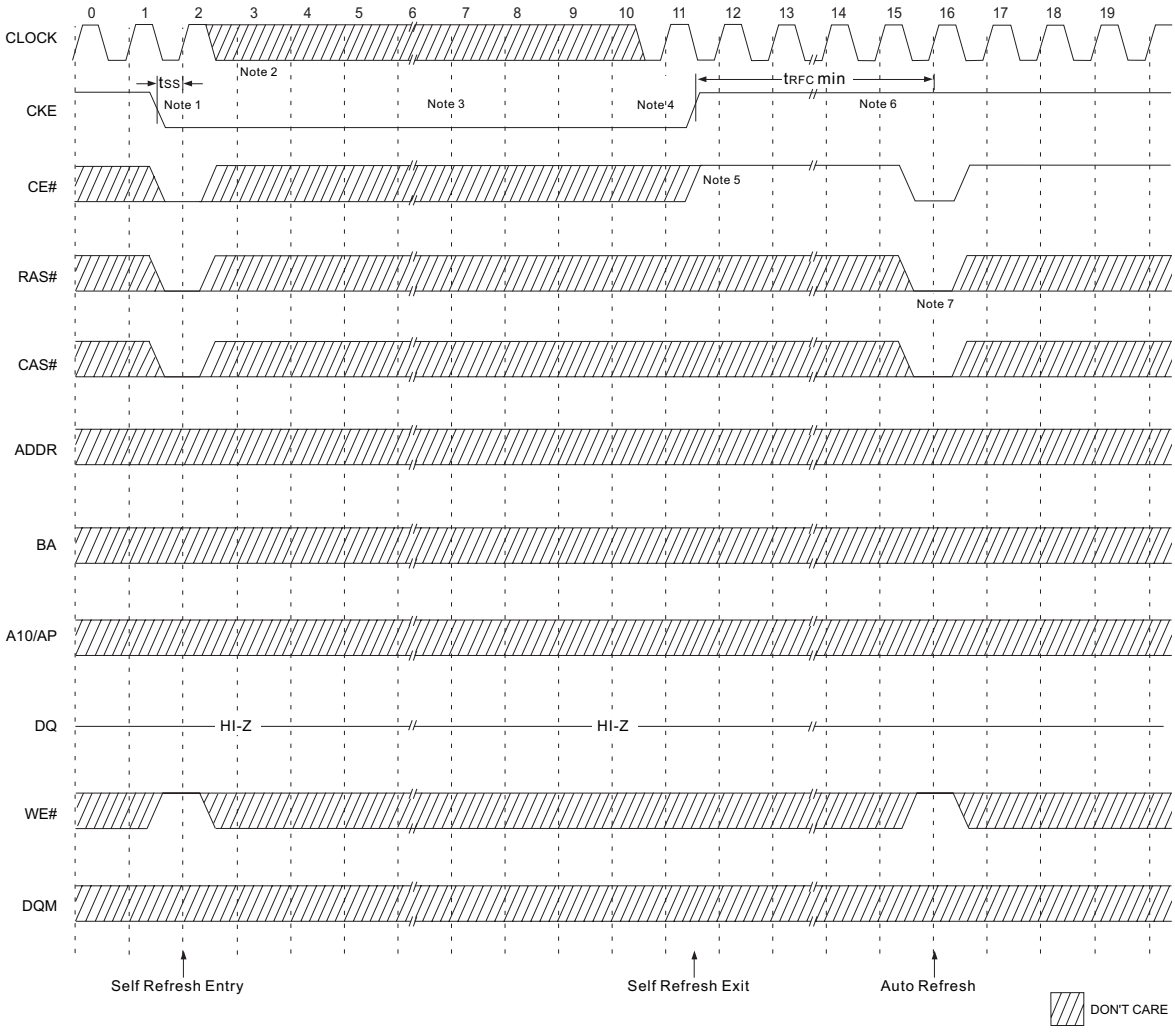
1. BRSW mode is enabled by setting A_9 "High" at MRS (Mode Register Set). At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated. Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

ACTIVE/PRECHARGE POWER DOWN MODE @ CAS LATENCY = 2, BURST LENGTH = 4



NOTES:
1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CK + t_{SS} prior to Row active command.
3. Can not violate minimum refresh specification (64ms).

SELF REFRESH ENTRY & EXIT CYCLE



NOTES:

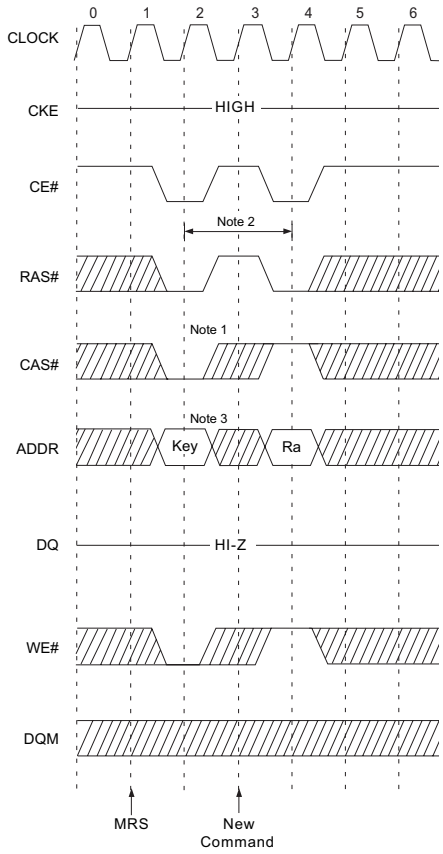
TO ENTER SELF REFRESH MODE

1. CE#, RAS# & CAS# with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low." Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

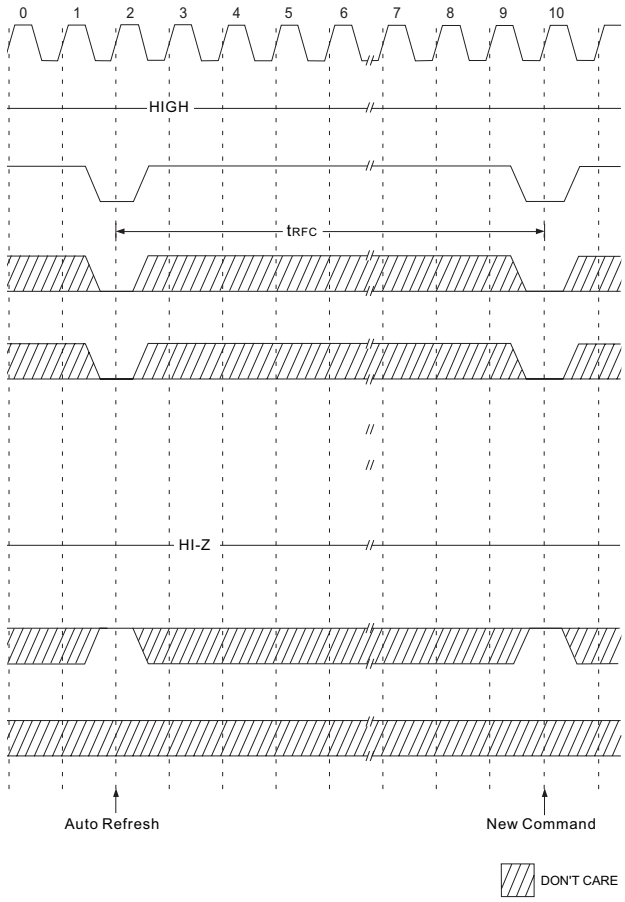
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. CE# starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

MODE REGISTER SET CYCLE



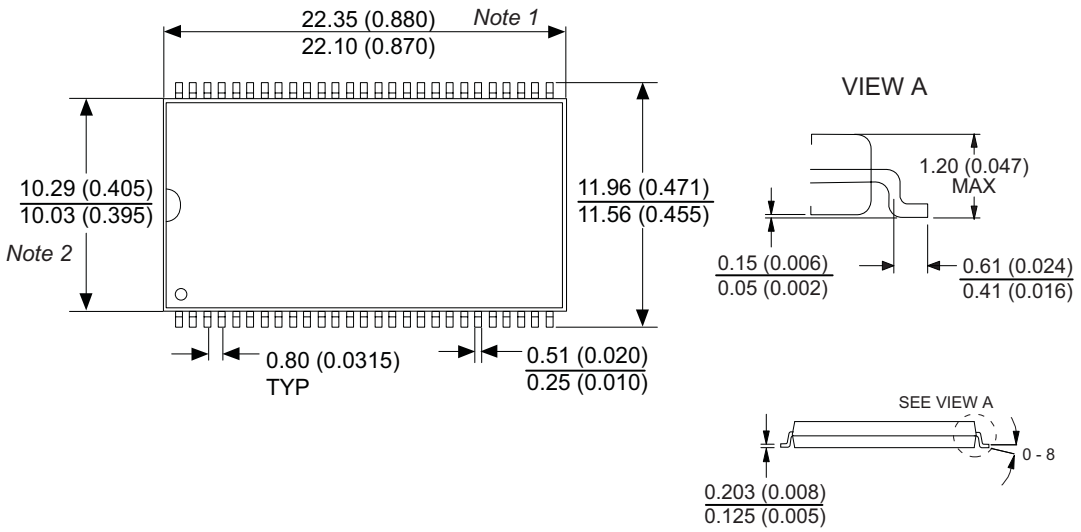
AUTO REFRESH CYCLE



NOTES:
Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE
1. CE#, RAS#, CAS#, & WE# activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new RAS# activation.
3. Please refer to Mode Register Set table.

PACKAGE DIMENSION: 54 PIN TSOP II



NOTES:
1. Dimension does not include 0.006 inch Flash each side.
2. Dimension does not include 0.010 inch Flash each side.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

Part Number	Operating Frequency	Package
WED416S16030C7SI	133MHz (CL2)	54 TSOP II
WED416S16030C75SI	133MHz (CL3)	54 TSOP II
WED416S16030C8SI	125MHz	54 TSOP II
WED416S16030C10SI	100MHz	54 TSOP II