Ordering number : EN*5537A

CMOS IC

LC78857V

Digital Audio D/A Converter IC with On-Chip Digital Filters

Preliminaly

Overview

The LC78857V is a sigma-delta type D/A converter for use in digital audio systems. It provides both digital and analog filters on chip.

Features

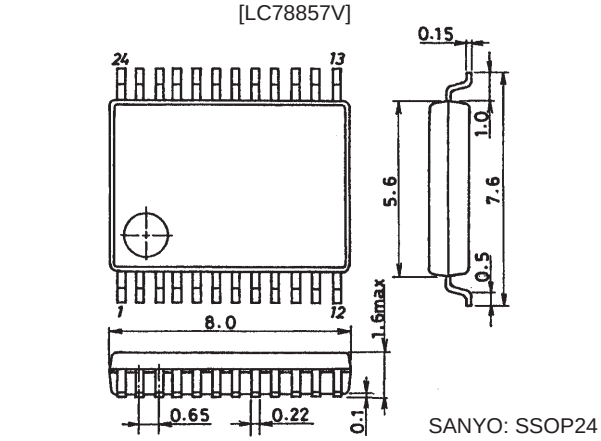
- Built-in 8x oversampling digital filters: 3-stage FIR structure (31st order, 11th order, and 3rd order filters)
- Analog low-pass filter
- Digital deemphasis (handles Fs = 44.1 kHz operation)
- Digital attenuator
- Soft muting
- Supports a 384fs system clock rate.
- 5-V single-voltage power supply
- Fabricated in a silicon gate CMOS process.

Package Dimensions

unit: mm

3175A-SSOP24

[LC78857V]



SANYO: SSOP24

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}		–0.3 to V_{DD} +0.3	V
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.5	5.0	5.5	V
Input voltage	T_{IN}		0		V_{DD}	V
Operating temperature	Topr		–30		+75	°C

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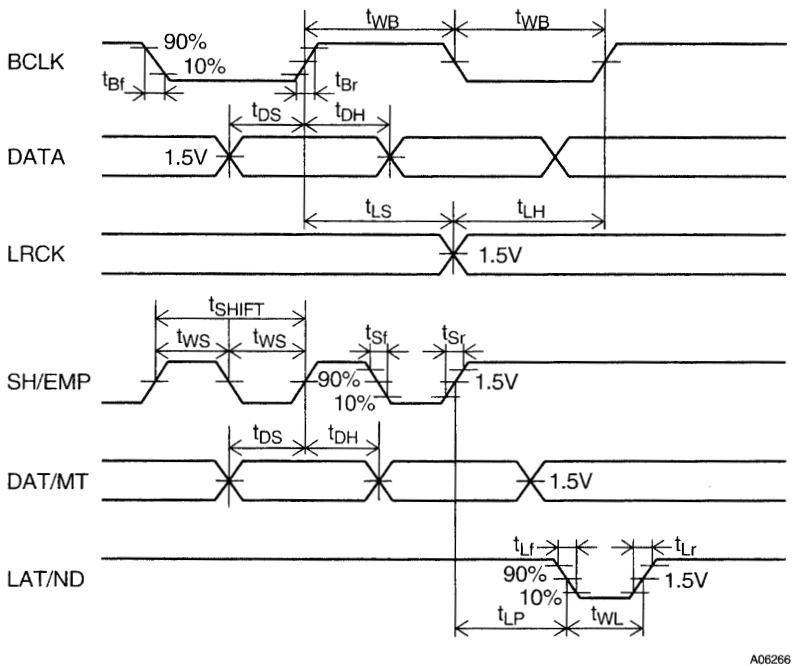
DC Characteristics at Ta = –30 to 75°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage (1)	$V_{IH}1$	Pin 15	0.7 V_{DD}			V
Input low-level voltage (1)	$V_{IL}1$	Pin 15			0.3 V_{DD}	V
Input high-level voltage (2)	$V_{IH}2$	Pins 6, 7, 8, 9, 10, 11, 14, 18, and 19	2.2			V
Input low-level voltage (2)	$V_{IL}2$	Pins 6, 7, 8, 9, 10, 11, 14, 18, and 19			0.8	V
Output high-level voltage	V_{OH}	I_{OH} = –3 mA, pin 17	2.4			V
Output low-level voltage	V_{OL}	I_{OL} = 3 mA, pin 17			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: Pins 6, 7, 8, 9, 10, 11, 14, 15, 18, and 19	–25		25	µA
Allowable power dissipation	Pd	V_{DD} = 5.0 V		135	200	mW

AC Characteristics at Ta = –30 to 75°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Oscillator frequency	f_X			169	18.5	MHz
BCLK frequency	f_{BCX}				3.0	MHz
BCLK pulse width	t_{WB}		100			ns
BCLK rise time	t_{Br}				30	ns
BCLK fall time	t_{Bf}				30	ns
DATA setup time	t_{DS}		20			ns
DATA hold time	t_{DH}		20			ns
LRCK setup time	t_{LS}		50			ns
LRCK hold time	t_{LH}		50			ns
SH/EMP pulse period	t_{SHIFT}		1000			ns
SH/EMP pulse width	t_{WS}		300			ns
SH/EMP rise time	t_{Sr}				100	ns
SH/EMP fall time	t_{Sf}				100	ns
LAT/ND pulse width	t_{WL}		300			ns
Latch pulse input time	t_{LP}		300			ns
LAT/ND rise time	t_{Lr}				100	ns
LAT/ND fall time	t_{Lf}				100	ns

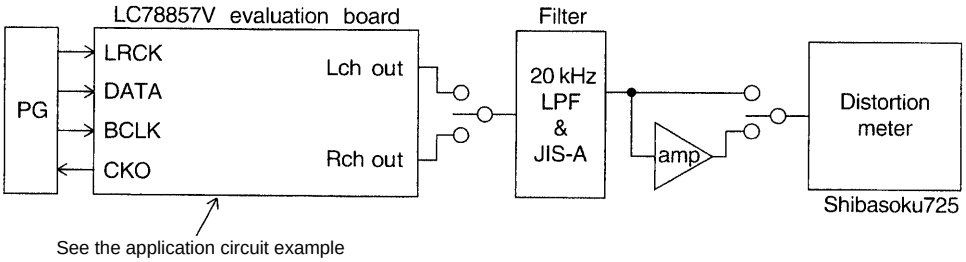
Timing Chart



Analog Characteristics at Ta = 25°C, V_{DD} = 5.0 V

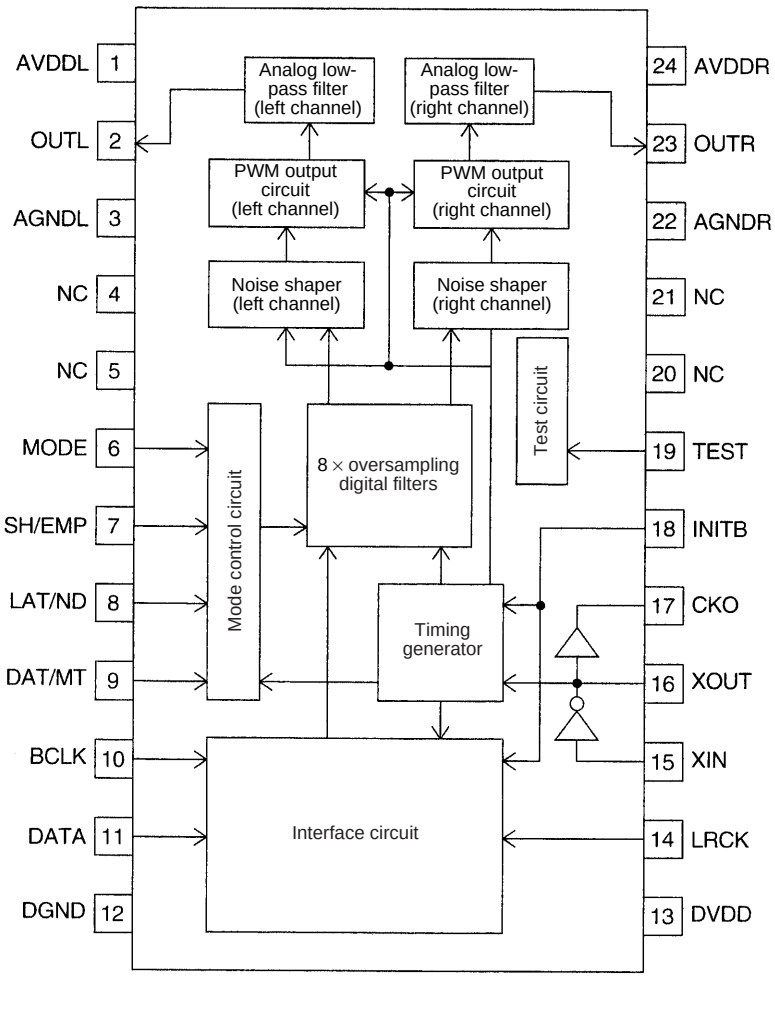
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD+N	1kHz, 0 dB		0.008	0.012	%
Signal-to-noise ratio	S/N	JIS-A	90	96		dB
Crosstalk	CT	1kHz, 0 dB	88	92		dB
Full scale output level	VFS	1 kHz, 0dB	2.8	3.0	3.2	Vp-p
Dynamic range	DR	JIS-A	84	87		dB
Output load resistance	R_L	Pins 2 and 23	5			kΩ

Test Circuit

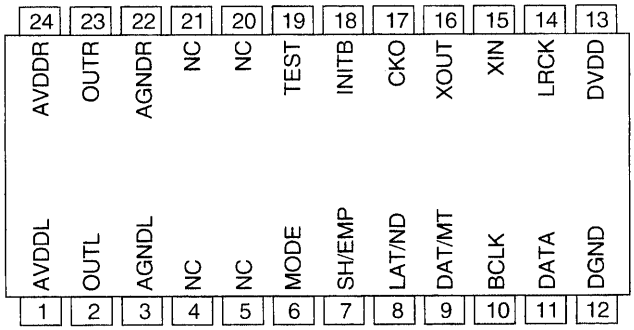


PG: Pattern generator (signal generator)
Filter: Band limiting filter

Block Diagram



Pin Assignment



(Top view)

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Pin Functions

Pin No.	Symbol	Function
1	AVDDL	Analog system power supply (left channel)
2	OUTL	Analog output (left channel)
3	AGNDL	Analog system ground (left channel)
4	NC	No Connection
5		
6	MODE	Serial/parallel input mode selection
7	SH/EMP	When MODE is low: Control data shift signal (serial mode) When MODE is high: Emphasis on/off switching (parallel mode)
8	LAT/ND	When MODE is low: Control data latch signal (serial mode) When MODE is high: normal speed/double speed switching (parallel mode)
9	DAT/MT	When MODE is low: Control data input (serial mode) When MODE is high: Soft muting control input (parallel mode)
10	BCLK	Bit clock input
11	DATA	Digital audio data input
12	DGND	Digital system ground
13	DV_{DD}	Digital system power supply
14	LRCK	LR clock input
15	XIN	Crystal oscillator element input
16	XOUT	Crystal oscillator element output
17	CKO	Clock output (384fs)
18	INITB	Initialization signal input (The IC internal state is initialized on a low input.)
19	TEST	Test pin (This pin must be connected to DGND during normal operation.)
20	NC	No Connection
21		
22	AGNDR	Analog system ground (right channel)
23	OUTR	Analog output (right channel)
24	AVDDR	Analog system power supply (right channel)

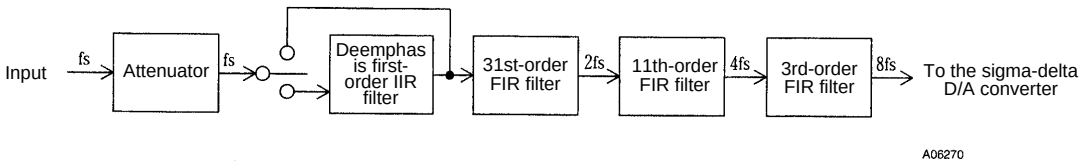
Circuit Operation

The LC78857V consists of three main blocks: the digital filter block, the sigma-delta D/A converter block, and the analog filter block.

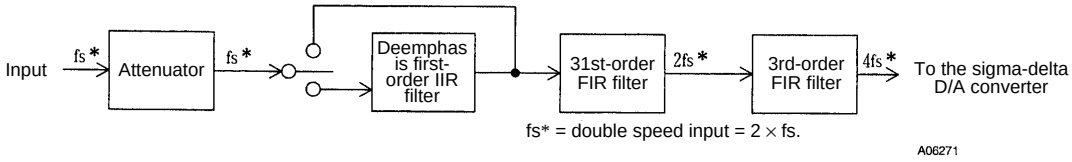
[Digital Filter Block]

The LC78857V performs the following calculations.

- Normal speed mode:

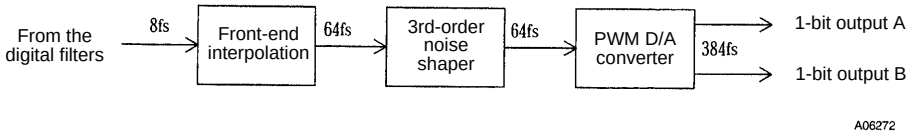


- Double speed mode:
  This mode is used, for example, when dubbing a CD to cassette tape at double speed. Although the XIN has the same frequency as normal speed mode, BCLK, LRCK, and DATA are input at twice the rate used in normal speed.



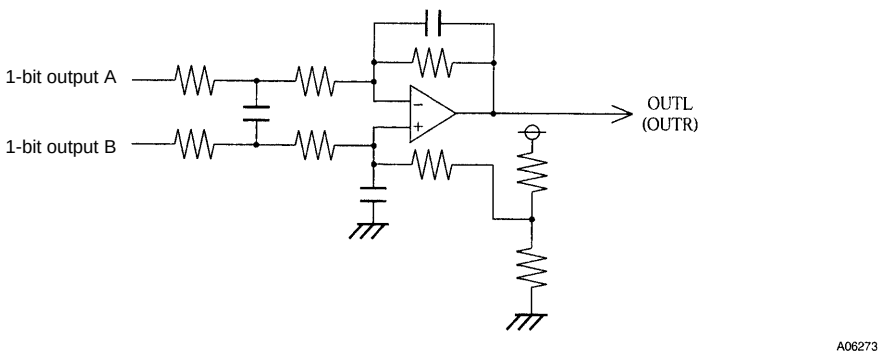
[Sigma-Delta D/A Converter Block]

This circuit accepts 8fs data input and outputs a 384fs 1-bit data sequence.



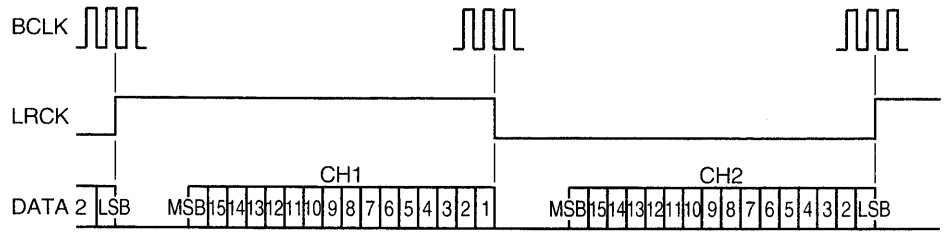
[Analog Low-Pass Filter Block]

This block consists of an analog low-pass filter that consists of on-chip resistors, capacitors, and operational amplifiers. This block converts the 384fs 1-bit data streams A and B directly to an analog voltage output.



Input Setup

1. Digital audio data input
   The digital audio data is a 16-bit serial signal in an MSB-first two's complement format. The 16-bit serial data is input from the DATA pin to an internal register on the rising edge of the BCLK signal, and is read in on the rising and falling edges of the LRCK signal.



Digital Audio Data Input Timing

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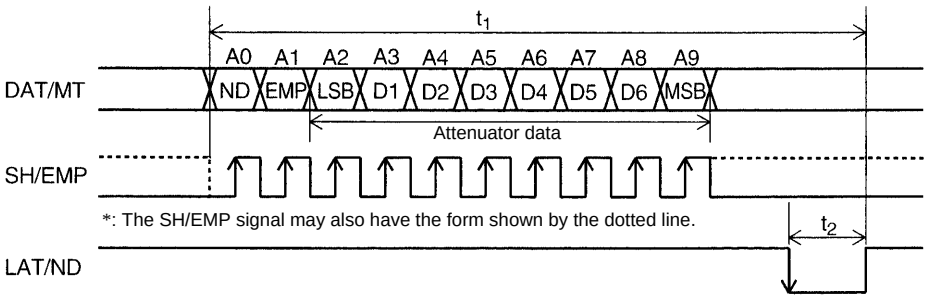
2. Mode setup
   The method used to set the speed (normal/double), deemphasis, and digital attenuator settings differs depending on the state of the mode pin (MODE).

- When MODE is low: serial input mode
  In this mode, the speed (normal/double), deemphasis, and digital attenuator settings are set by inputting serial data to the DAT/MT pin.

<Data Format>



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Notes: DAT/MT and SH/EMP: These pins must be held fixed (low or high) at all times other than the data transfer period (t1 in the figure).
LAT/ND: This pin must be held high at all times other than during data acquisition.

- A0 (ND): Normal/double speed flag
- A1 (EMP): Deemphasis flag

A0 (ND)	Normal/double speed
L	Normal speed
H	Double speed

A1 (EMP)	Deemphasis
L	Off
H	On

The deemphasis function supports operation at fs = 44.1 kHz.

• Attenuator data

The signal can be attenuated by inputting attenuation data (A2 to A9).

The attenuation specified by the attenuation data is given by the following formula:

$$20 \cdot \log \left\langle \frac{\text{Attenuation data}}{128} \right\rangle \text{(dB)}$$

Note: The attenuation is 0 dB when the data value is 7F (hexadecimal).

However, if A9 (the MSB) is 1, the A2 to A data is ignored and the prior attenuation setting is retained.

Attenuation data								Attenuation level (dB)
MSB A9	A8	A7	A6	A5	A4	A3	LSB A2	
0	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	0	–0.137
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
0	0	0	0	0	0	0	1	–42.14
0	0	0	0	0	0	0	0	–∞

If the attenuation level is changed from 0 dB to –∞ dB, the IC performs a soft muting operation. The soft muting time is 1/Fs × 1024. Also, the time required to change the attenuation follows the slope of the soft muting function.

If new attenuation data is input while the attenuation is changing, the attenuation level starts to change from the current level to the newly specified level at that point.

Note: If the IC is initialized when the MODE pin is low, the IC is initialized with serial data values of A0 = A1 = A9 = low, and A2 to A8 = high.

However, the LAT/ND must be held high during this initialization.

• When MODE is high: parallel input mode

In this mode, the speed (normal/double), deemphasis, and soft muting settings are specified with the LAT/ND, SH/EMP, and DAT/MT pins. It is not possible to set the attenuation data in this mode.

· Normal speed/double speed setting

LAT/ND	Normal/double speed
L	Normal speed
H	Double speed

· Deemphasis setting

SH/EMP	Deemphasis
L	Off
H	On

The deemphasis function supports operation at fs = 44.1 kHz.

· Soft muting setting

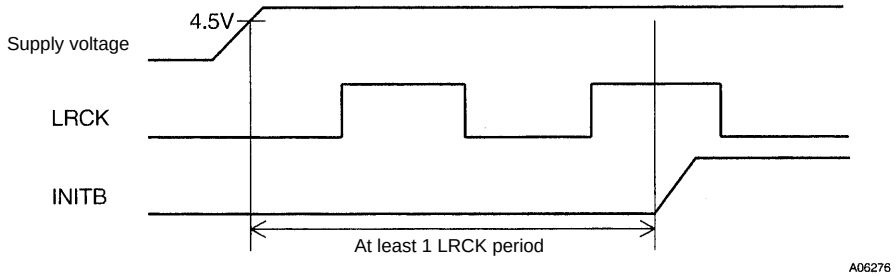
The LC78857V uses the digital attenuator to implement a soft muting function. If the input level applied to the DAT/MT pin is changed from low to high, the attenuation changes from 0 dB to –∞ dB. Inversely, if the DAT/MT pin is changed from high to low, the attenuation changes from –∞ dB to 0 dB.

The time required for the change is 1/fs × 1024.

DAT/MT	Soft muting
L	Off
H	On

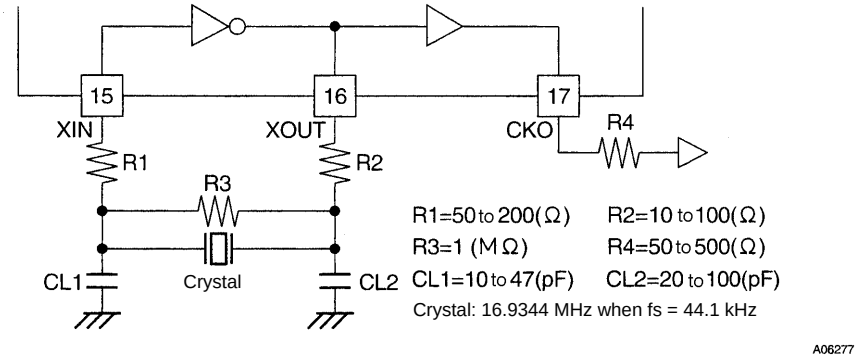
3. Initialization

   This IC requires initialization when power is first applied and for system operation switching. After the power-supply voltage has stabilized and XIN, BCLK, and LRCK have been supplied, initialization is achieved by holding the INITB pin at the low level for at least one LRCK period as shown in the figure below. When INITB is low, the digital filter outputs and the noise shaper (sigma-delta D/A converter) internal states are all set to 0, and the analog outputs (OUTL and OUTR) go to the zero cross level.



System Clock

The LC78857V operates from a 384fs system clock.



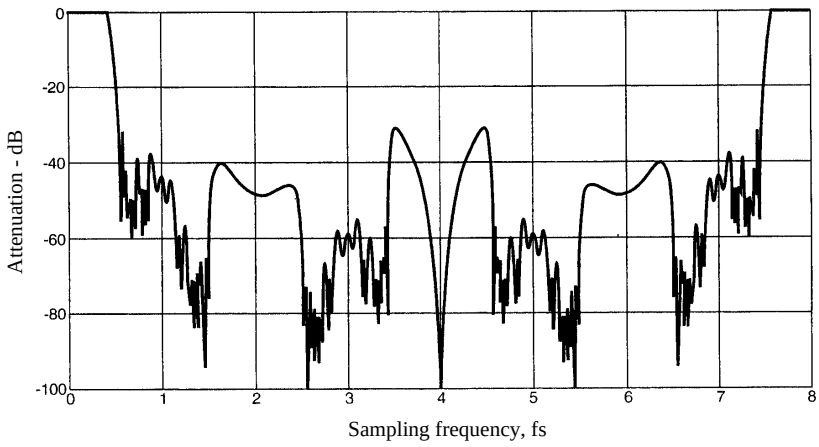
The 384fs system clock is generated using a crystal oscillator circuit consisting of a crystal element, resistors, and capacitors as shown in the figure. Optimal values for the resistors and capacitances depend on the peripheral circuits and other conditions. The sigma-delta D/A converter is a sensitive circuit, and the analog characteristics are strongly influenced by the quality of the waveform (e.g. its jitter characteristics) of the system clock input to the XIN pin. When an external signal is input as the system clock, adequate care must be taken to assure the quality of this signal's waveform.

· CKO: Outputs a clock signal with the same frequency as the signal input to the XIN pin.

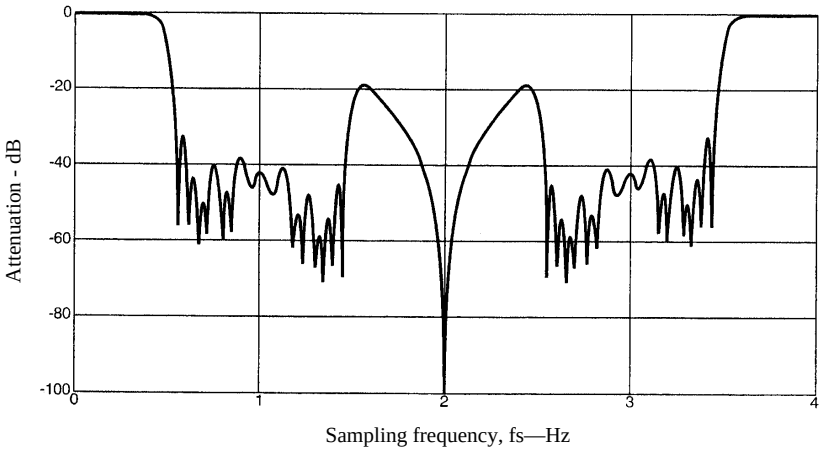
Digital Filter Characteristics

1. Frequency characteristics

   · Normal speed (deemphasis off)

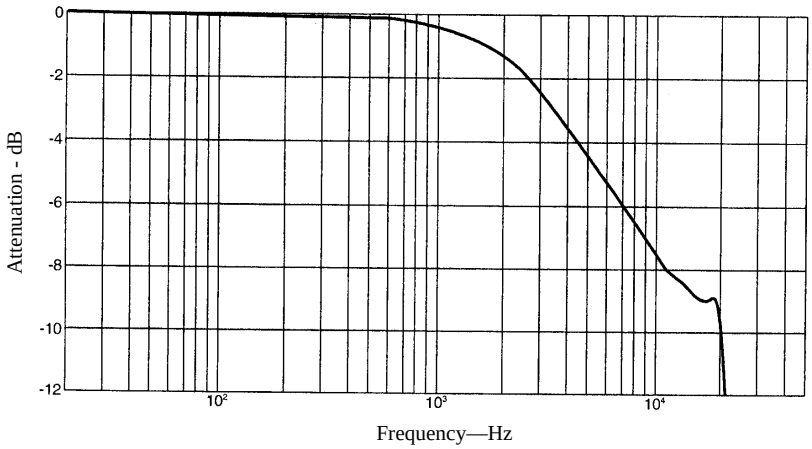


· Double speed (deemphasis off)

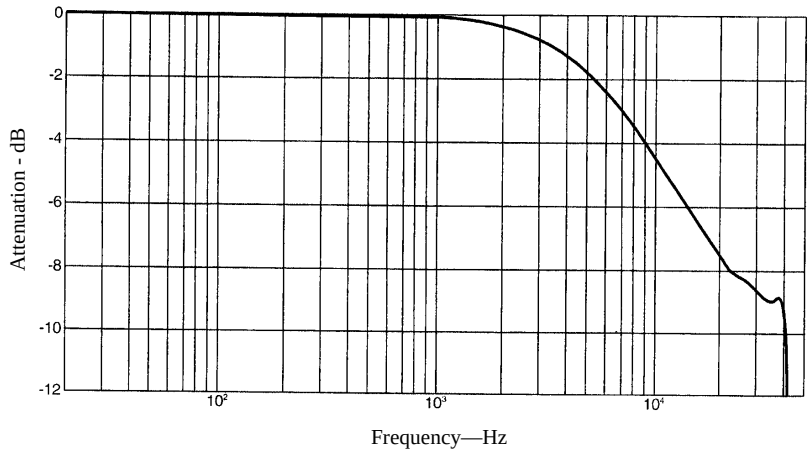


2. Deemphasis on pass band characteristics

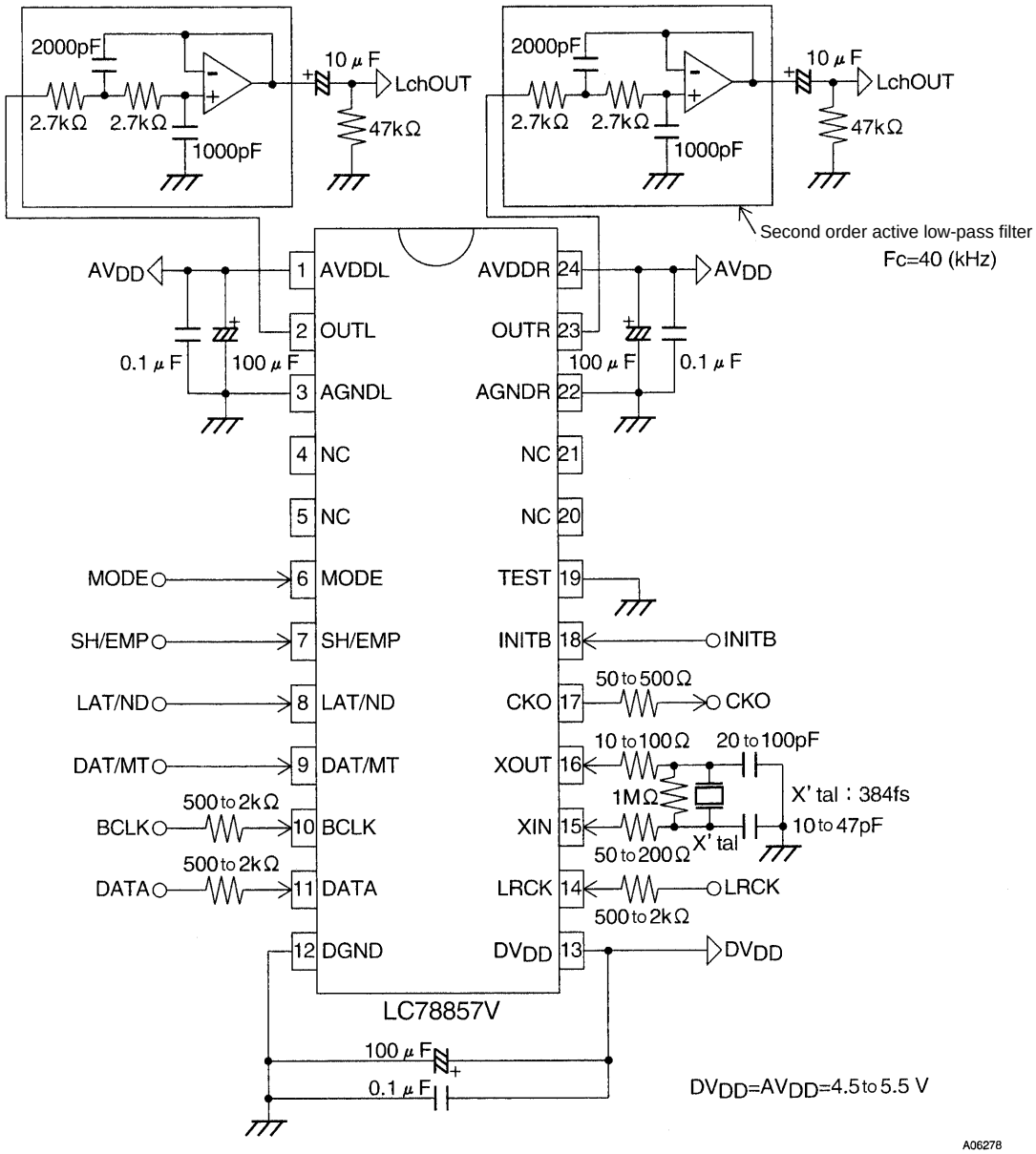
· Normal speed (deemphasis on)



· Double speed (deemphasis on)



Sample Application Circuit



Notes: · All DV_{DD} nodes in the circuit diagram must be connected to the digital system power supply, and all AV_{DD} nodes must be connected to the analog system power supply.

· Since latchup may occur if there is a discrepancy in the times at which the DV_{DD} and AV_{DD} voltages are applied, applications must be designed so that there is no time difference between the points when these voltages are applied.

· If there is a potential difference between the DV_{DD} and AV_{DD} voltages, it must not exceed 0.3 V.

· The application circuit example is an actual application circuit. Appropriate band limiting filters, which prevent adverse influence of band noise, are required to acquire the analog characteristics listed in the electrical characteristics.

Power Supply Timing

- The analog system power supplies (AVDDL and AVDDR) and the digital system power supply (DV_{DD}) must be applied and cut at the same time.
- If time lags between these power supplies are unavoidable, the timing must meet one of the following two conditions.
  (1) The power on (and power off) time lag must be under 3 ms as shown in figure 1.
  (2) If the time lag must be over 3 ms, then the rise time for the first power supply to be powered on (or powered off) must exceed 5 ms, and furthermore, the time difference must exceed 50 ms as shown in figure 2.

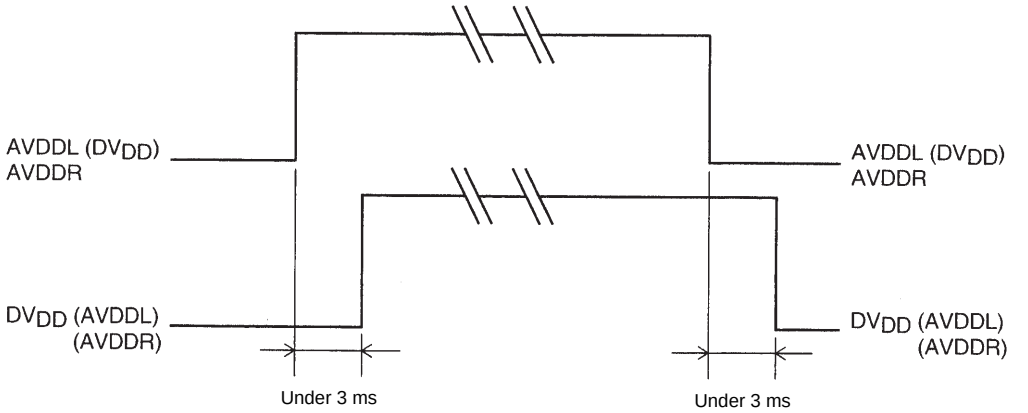


Figure 1

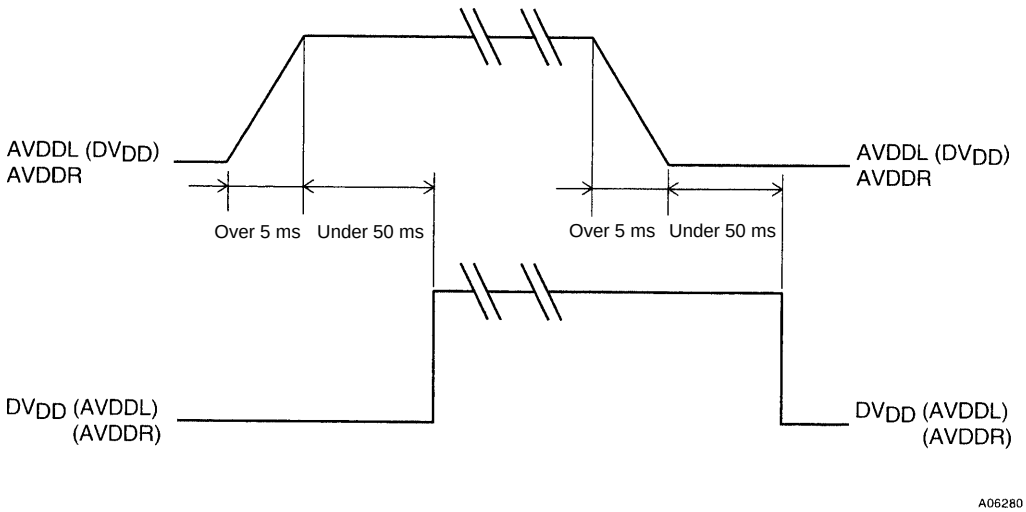


Figure 2