

TD2001Y

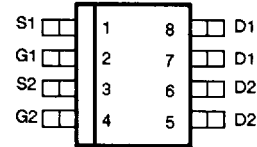
Dual P-Channel Enhancement-Mode MOSFETs

SO-8 PACKAGE

T:39-27

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-30	2	-0.5



Top View

FEATURES

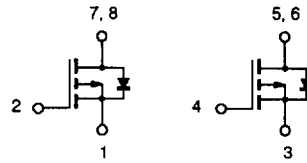
- Electrically Isolated MOSFETs
- Surface Mount
- Low Thermal Resistance

APPLICATIONS

- MOSFET Drivers
- Motor Drivers

END PRODUCTS

- Disk/Tape Drives
- Printers/Plotters
- Instrumentation



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		SINGLE MOSFET		
Drain-Source Voltage	V_{DS}	-30		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current	I_D	$T_A = 25^\circ\text{C}$	-0.65	A
		$T_A = 100^\circ\text{C}$	-0.41	
Pulsed Drain Current ¹	I_{DM}	2		
Maximum Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	1.5	W
		$T_A = 100^\circ\text{C}$	0.8	
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Lead Temperature ($1/16"$ from case for 10 sec.)	T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	83.3	K/W

¹Pulse width limited by maximum junction temperature.

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SPECIFICATIONS*		LIMITS				
PARAMETER	SYMBOL	TEST CONDITIONS	TYP ^b	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)SS}$	$V_{GS} = 0\text{ V}, I_D = -10\ \mu\text{A}$	-55	-30		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -1\ \text{mA}$	-3.6	-0.8	-4.5	
Gate-Body Leakage	I_{GBS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24\ \text{V}, V_{GS} = 0\ \text{V}$ $T_J = 125^\circ\text{C}$			-10	μA
On-State Drain Current ^c	$I_{D(ON)}$	$V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}$	-1.5	-1		A
Drain-Source On-Resistance ^c	$r_{DS(ON)}$	$V_{GS} = -10\ \text{V}, I_D = -200\ \text{mA}$ $T_J = 125^\circ\text{C}$	1.7		2	Ω
Forward Transconductance ^c	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -0.5\ \text{A}$	290	200		mS
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0\ \text{V}, V_{DS} = -15\ \text{V}, f = 1\ \text{MHz}$	130		150	
Output Capacitance	C_{oss}		75		100	pF
Reverse Transfer Capacitance	C_{rss}		20		60	
SWITCHING						
Turn-On Time	t_{ON}	$V_{DD} = -25\ \text{V}, R_L = 23\ \Omega, I_D = -1\ \text{A}$ $V_{GEN} = -10\ \text{V}, R_G = 25\ \Omega$ (Switching time is essentially independent of operating temperature)	16		30	ns
Turn-Off Time	t_{OFF}		13		30	

NOTES:

- a. $T_A = 25^\circ\text{C}$ unless otherwise noted.
- b. For design aid only, not subject to production testing.
- c. Pulse test: Pulse Width $\leq 300\ \mu\text{sec}$; Duty Cycle $\leq 2\%$.