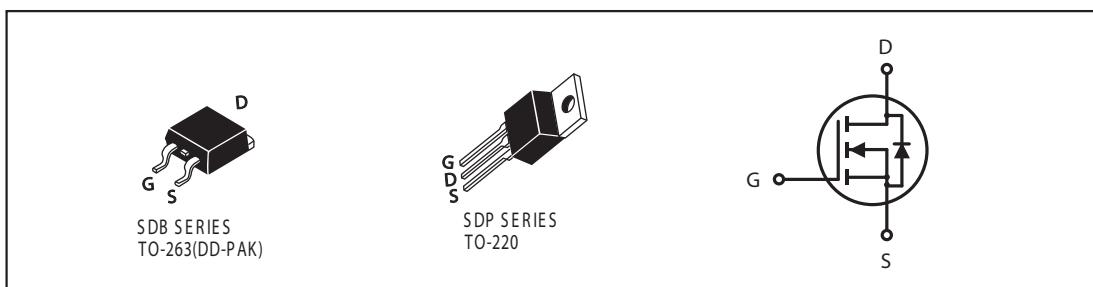


N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V _{DSS}	I _D	R _{D(on)} (mΩ) Max
30V	70A	7 @ V _{GS} = 10V
		11 @ V _{GS} = 4.5V

FEATURES

- Super high dense cell design for extremely low R_{D(on)}.
- High power and current handling capability.
- TO-220 & TO-263 package.

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous @ T _J =125°C -Pulsed ^a	I _D	70	A
	I _{DM}	210	A
Drain-Source Diode Forward Current	I _S	75	A
Maximum Power Dissipation @ T _c =25°C	P _D	75	W
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R _{θJC}	2	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}} = 0\text{V}, \text{I}_D = 250\text{\mu A}$	30	35		V
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}} = 24\text{V}, \text{V}_{\text{GS}} = 0\text{V}$			10	\mu A
Gate-Body Leakage	I_{GSS}	$\text{V}_{\text{GS}} = \pm 16\text{V}, \text{V}_{\text{DS}} = 0\text{V}$			± 100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}, \text{I}_D = 250\text{\mu A}$	1	1.5	3	V
Drain-Source On-State Resistance	$\text{R}_{\text{DS(ON)}}$	$\text{V}_{\text{GS}} = 10\text{V}, \text{I}_D = 37\text{A}$		6	7	m ohm
		$\text{V}_{\text{GS}} = 4.5\text{V}, \text{I}_D = 30\text{A}$		9	11	m ohm
On-State Drain Current	$\text{I}_{\text{D(ON)}}$	$\text{V}_{\text{GS}} = 10\text{V}, \text{V}_{\text{DS}} = 10\text{V}$	60			A
Forward Transconductance	g_{FS}	$\text{V}_{\text{DS}} = 10\text{V}, \text{I}_D = 37\text{A}$		47		S
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}} = 15\text{V}, \text{V}_{\text{GS}} = 0\text{V}$ $f = 1.0\text{MHz}$		1900		pF
Output Capacitance	C_{oss}			960		pF
Reverse Transfer Capacitance	C_{rss}			320		pF
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	$\text{t}_{\text{D(ON)}}$	$\text{V}_{\text{DD}} = 15\text{V},$ $\text{I}_D = 1\text{A},$ $\text{V}_{\text{GEN}} = 10\text{V}$ $\text{R}_G = 1.8 \text{ ohm}$ $\text{R}_L = 0.20 \text{ ohm}$		15		ns
Rise Time	t_r			12.5		ns
Turn-Off Delay Time	$\text{t}_{\text{D(OFF)}}$			5.5		ns
Fall Time	t_f			6.5		ns
Total Gate Charge	Q_{g}	$\text{V}_{\text{DS}} = 24\text{V}, \text{I}_D = 75\text{A}, \text{V}_{\text{GS}} = 10\text{V}$		61		nC
		$\text{V}_{\text{DS}} = 24\text{V}, \text{I}_D = 75\text{A}, \text{V}_{\text{GS}} = 4.5\text{V}$		32		nC
Gate-Source Charge	Q_{gs}	$\text{V}_{\text{DS}} = 24\text{V}, \text{I}_D = 75\text{A},$ $\text{V}_{\text{GS}} = 10\text{V}$		11		nC
Gate-Drain Charge	Q_{gd}			11		nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS ^a						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 37A$		0.93	1.3	V

Notes

a. Pulse Test Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

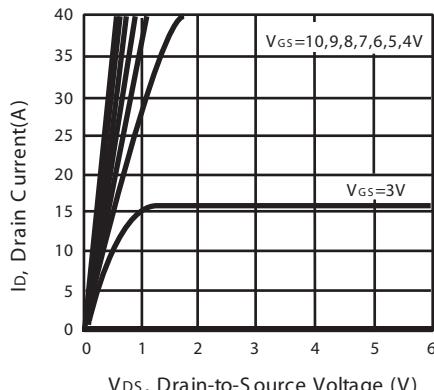


Figure 1. Output Characteristics

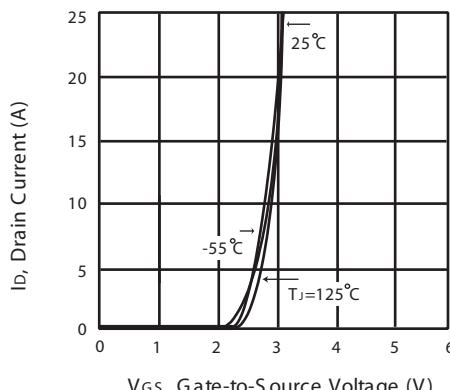


Figure 2. Transfer Characteristics

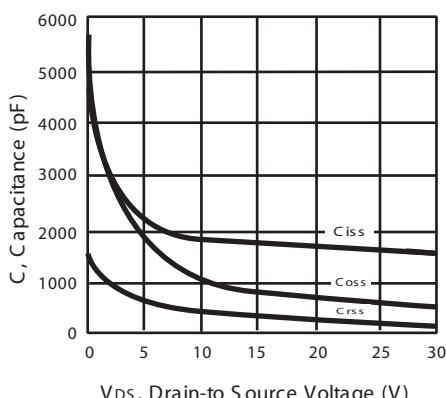


Figure 3. Capacitance

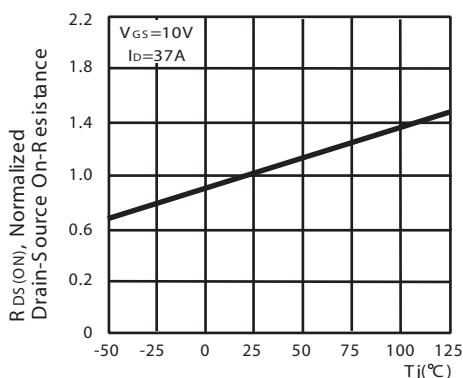


Figure 4. On-Resistance Variation with Temperature

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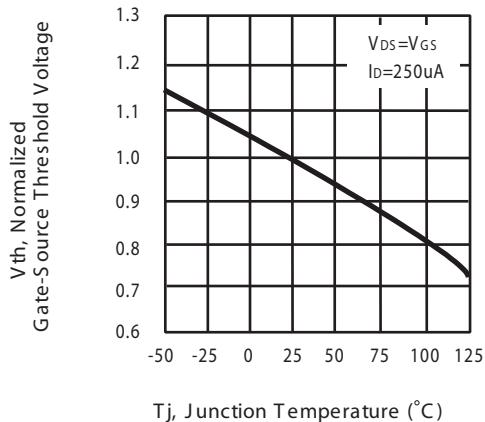


Figure 5. Gate Threshold Variation with Temperature

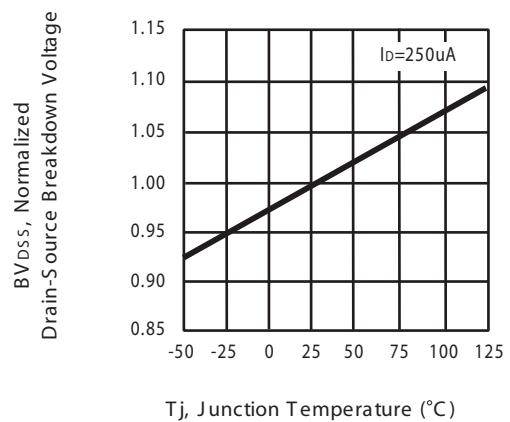


Figure 6. Breakdown Voltage Variation with Temperature

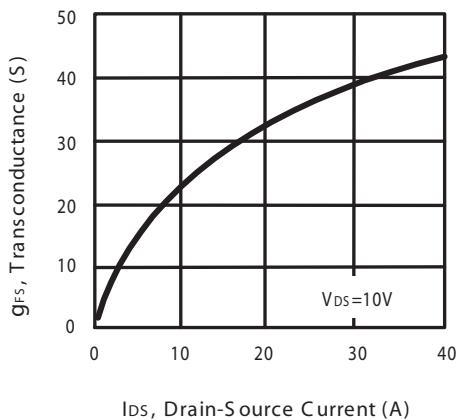


Figure 7. Transconductance Variation with Drain Current

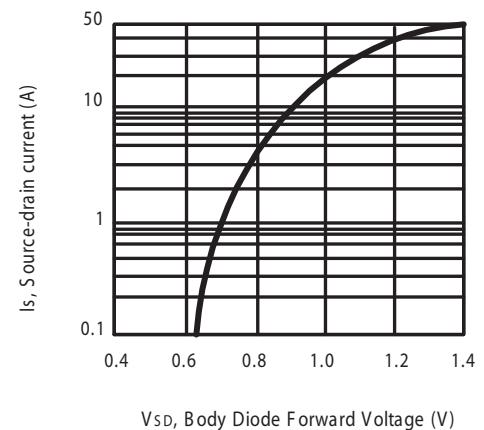


Figure 8. Body Diode Forward Voltage Variation with Source Current

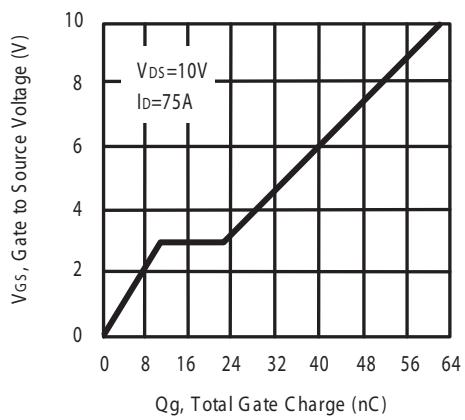


Figure 9. Gate Charge

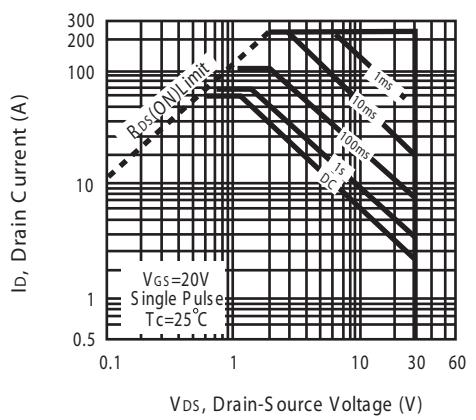


Figure 10. Maximum Safe Operating Area

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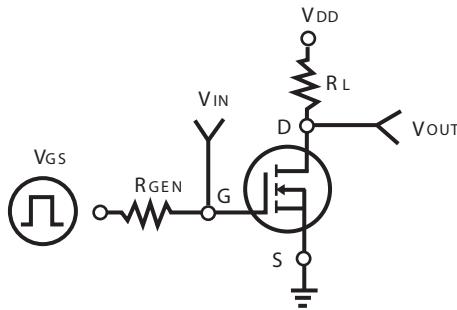


Figure 11. S switching Test Circuit

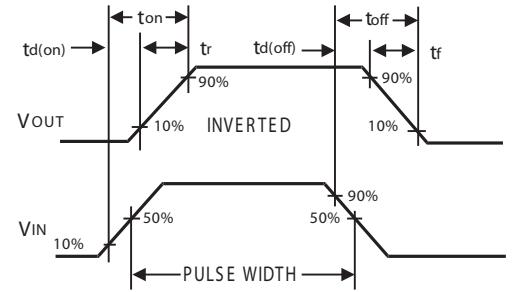


Figure 12. S switching Waveforms

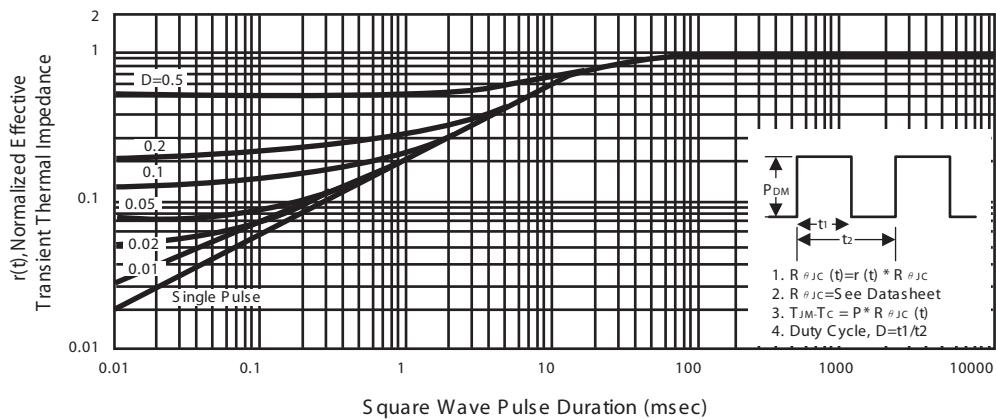
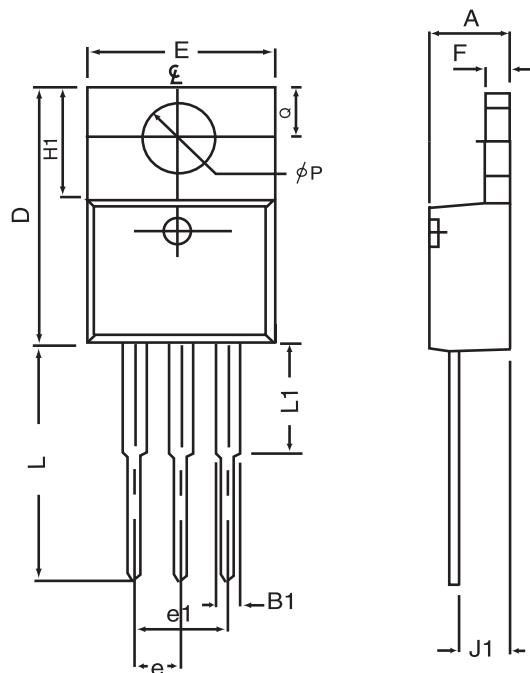


Figure 13. Normalized Thermal Transient Impedance Curve

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PACKAGE OUTLINE DIMENSIONS

TO-220



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
ϕP	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120