

## L-band Down Converter IC with On-Chip PLL

**Description**

The CXA3108AQ is a monolithic IC that down-converts the L-band (1 to 2 GHz) 1st IF to 2nd IF for satellite broadcast receivers. It integrates a local oscillator circuit, double-balanced mixer, IF AGC amplifier and tuning PLL onto a single chip.

This IC supports both analog and digital satellite broadcasts, and achieves reduction in the number of tuner components and smaller size.

**Features**

- On-chip tuning PLL
- Supports 2.65 GHz oscillator frequency
- Noise figure: 12.5 dB typ. (for IF full gain)
- IF AGC gain variation: 46 dB typ.
- Wide band IF AGC amplifier (60 to 500 MHz)
- Two IF outputs
- PLL supports I<sup>2</sup>C protocol
- On-chip high voltage drive transistor for charge pump

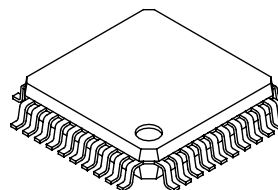
**Applications**

- Analog satellite broadcast tuners (BS/CS)
- Digital satellite broadcast tuners (DSS/DVB, etc.)

**Structure**

Bipolar silicon monolithic IC

40 pin QFP (Plastic)

**Absolute Maximum Ratings** (Ta=25 °C)

- Supply voltage  $V_{CC}$  -0.3 to +5.5 V
- Storage temperature  $T_{stg}$  -55 to +150 °C
- Allowable power dissipation  $P_D$  730 mW  
(when mounted on a substrate)

**Operating Conditions**

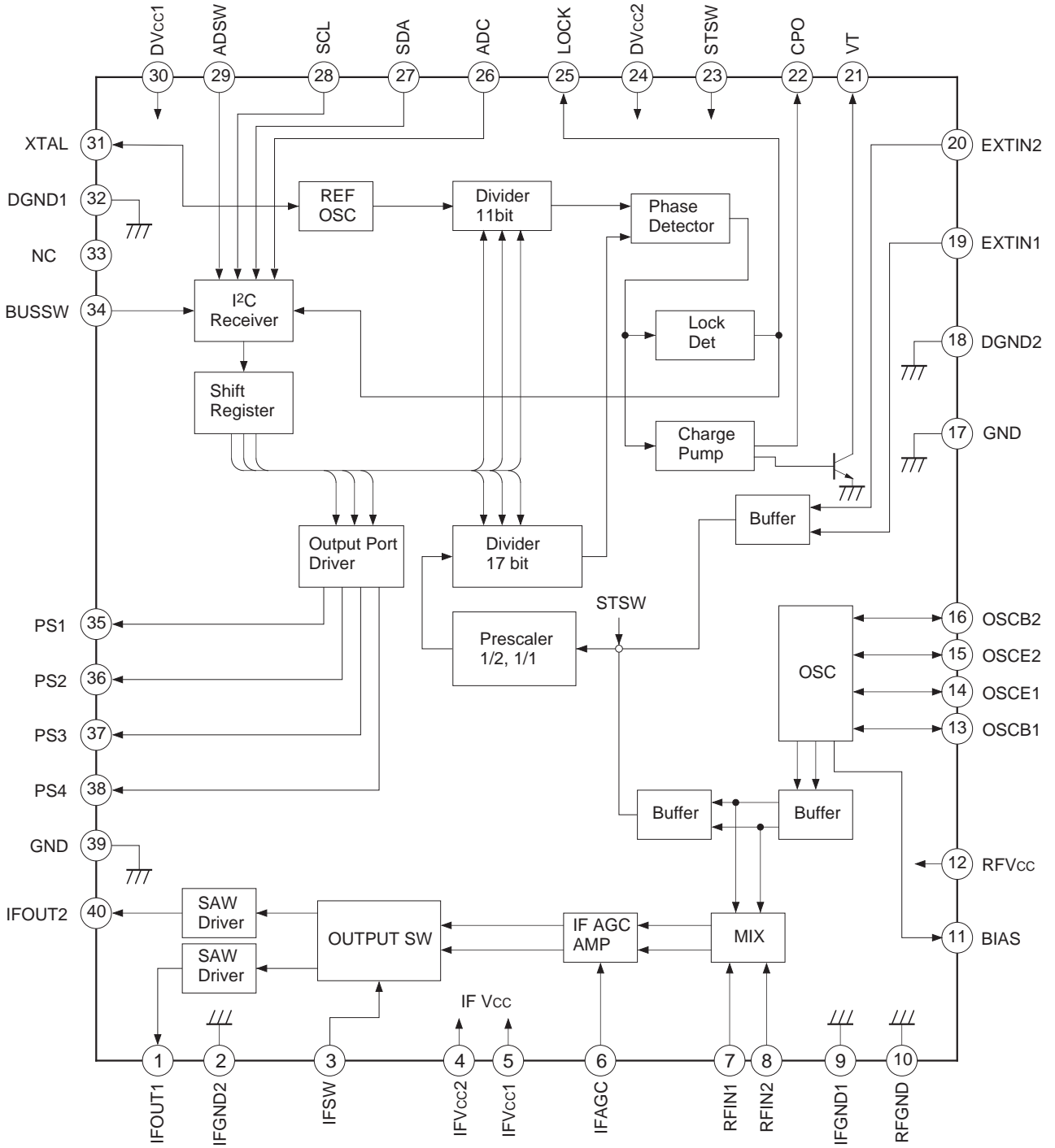
- Supply voltage  $V_{CC}$  4.75 to 5.30 V
- Operating temperature  $T_{opr}$  -25 to +75 °C

**Notes on Handling**

This IC has a weak electrostatic discharge strength. Take care when handling the IC.

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Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
1	IFOUT1	2.5 (IFSW 0 V) 4.7 (IFSW 5 V)		IF outputs.
40	IFOUT2	4.7 (IFSW 0 V) 2.5 (IFSW 5 V)		
2	IFGND2	0		IF output circuit GND.
3	IFSW	0 or 5		Selects whether IF output is Pin 1 or Pin 40. When this pin is connected to GND, the IF signal is output from Pin 1; when connected to Vcc, the IF signal is output from Pin 40.
4	IFVcc2	5		IF output circuit power supply.
5	IFVcc1	5		IF amplifier circuit power supply.
6	IFAGC	0 to 4		AGC signal input.
7	RFIN1	1.7		RF inputs.
8	RFIN2	1.7		
9	IFGND1	0		IF amplifier circuit GND.
10	RFGND	0		RF block GND.

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
11	BIAS	1.8		Oscillator circuit current adjustment. Connect this pin to GND via a capacitor.
12	RFVcc	5		RF block power supply.
13	OSCB1	2.2		Oscillator pins.
14	OSCE1	1.5		
15	OSCE2	1.5		
16	OSCB2	2.2		
17	GND	0		GND.
18	DGND2	0		Charge pump GND.
19	EXTIN1	2.5		PLL external inputs.
20	EXTIN2	2.5		
21	VT	—		NPN transistor output for varicap diode drive.
22	CPO	—		Charge pump output. Connect a loop filter.

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
23	STSW	—		<p>Selects either the internal oscillator circuit or external input for input to PLL.</p> <p>When this pin is open or connected to Vcc, the internal oscillator circuit is selected; when connected to GND, external input is selected.</p>
24	DVcc2	5		Charge pump power supply.
25	LOCK	5.0 (LOCK) 0.2 (UNLOCK)		<p>LOCK detection.</p> <p>High when locked, Low when unlocked.</p>
26	ADC	—		ADC input.
27	SDA	—		DATA input.

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
28	SCL	—		CLOCK input.
29	ADSW	1.3		I <sup>2</sup> C bus address selection.
30	DVcc1	5		PLL circuit power supply.
31	XTAL	4.4		Crystal connection for reference oscillator.
32	DGND1	0		PLL circuit GND.
33	NC	—		

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
34	BUSSW	—	<p>The diagram shows an equivalent circuit for pin 34. Pin 30 is connected to a diode pointing towards pin 34. Pin 34 is connected to another diode pointing towards ground. A resistor is connected between DVcc1 and the base of a transistor. The emitter of the transistor is connected to ground, and the collector is connected to pin 34.</p>	PLL circuit GND. Connect directly to GND.
35	PS1	5.0 (OFF) 0.2 (ON)	<p>The diagram shows an equivalent circuit for pins 35, 36, 37, and 38. DVcc1 is connected to the base of a transistor. The emitter of this transistor is connected to ground. The collector is connected to a resistor, which is then connected to the base of a second transistor. The emitter of the second transistor is connected to ground, and its collector is connected to pin 30. Pin 35 is connected to a diode pointing towards pin 36. Pin 36 is connected to a diode pointing towards pin 37. Pin 37 is connected to a diode pointing towards pin 38. Pin 38 is connected to ground.</p>	Output ports.
36	PS2			
37	PS3			
38	PS4			
39	GND	0		GND.

## Electrical Characteristics

(V<sub>CC</sub>=5 V, T<sub>a</sub>=25 °C)

## Circuit Current

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current A	AI <sub>CC</sub>	Analog circuit current Sum of RFV <sub>CC</sub> , IFV <sub>CC</sub> 1 and IFV <sub>CC</sub> 2 currents	42	62	82	mA
Circuit current D	DI <sub>CC</sub>	PLL circuit current Sum of DV <sub>CC</sub> 1 and DV <sub>CC</sub> 2 currents	18	30	40	mA

## OSC/MIX/IF Amplifier Blocks

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Conversion gain	CG1	f <sub>in</sub> =950 MHz, f <sub>F</sub> =480 MHz IFAGC=4 V (Full Gain)	15	21	25	dB
	CG2	f <sub>in</sub> =1450 MHz, f <sub>F</sub> =480 MHz IFAGC=4 V (Full Gain)	14	20	24	dB
	CG3	f <sub>in</sub> =2150 MHz, f <sub>F</sub> =480 MHz IFAGC=4 V (Full Gain)	18	24	28	dB
Noise figure	NF1	f <sub>in</sub> =950 MHz, f <sub>F</sub> =480 MHz IFAGC=4 V (Full Gain)		13	16	dB
	NF2	f <sub>in</sub> =1450 MHz, f <sub>F</sub> =480 MHz IFAGC=4 V (Full Gain)		13	16	dB
	NF3	f <sub>in</sub> =2150 MHz, f <sub>F</sub> =480 MHz IFAGC=4 V (Full Gain)		13	16	dB
IFAGC gain variation range	AGC		35	50		dB
IF maximum output	PoSAT	f <sub>F</sub> =480 MHz, 50 Ω load saturated output		9		dBm
RF pin local oscillator leak	RFLK1	f <sub>osc</sub> =1430 to 1830 MHz			-20	dBm
	RFLK2	f <sub>osc</sub> =1830 to 2230 MHz			-20	dBm
	RFLK3	f <sub>osc</sub> =2230 to 2630 MHz			-25	dBm
IF pin local oscillator leak	IFLK1	f <sub>osc</sub> =1430 to 1830 MHz			-18	dBm
	IFLK2	f <sub>osc</sub> =1830 to 2230 MHz			-18	dBm
	IFLK3	f <sub>osc</sub> =2230 to 2630 MHz			-20	dBm
Tertiary intermodulation distortion	IM3	Pin=-25 dBm IFAGC=4 V (Full Gain) f <sub>in</sub> =935 MHz, 940 MHz f <sub>out</sub> =475 MHz, 480 MHz S/I of 480 MHz and 475 MHz	38	45		dB
Local oscillator phase noise	CN1	f <sub>osc</sub> =1430 MHz 10 kHz offset		80		dBc/Hz
	CN2	f <sub>osc</sub> =1430 MHz 100 kHz offset		100		dBc/Hz
RF input impedance	r <sub>π</sub>	f=950 MHz		12.9		Ω
	C <sub>π</sub>	f=950 MHz		1.84		pF



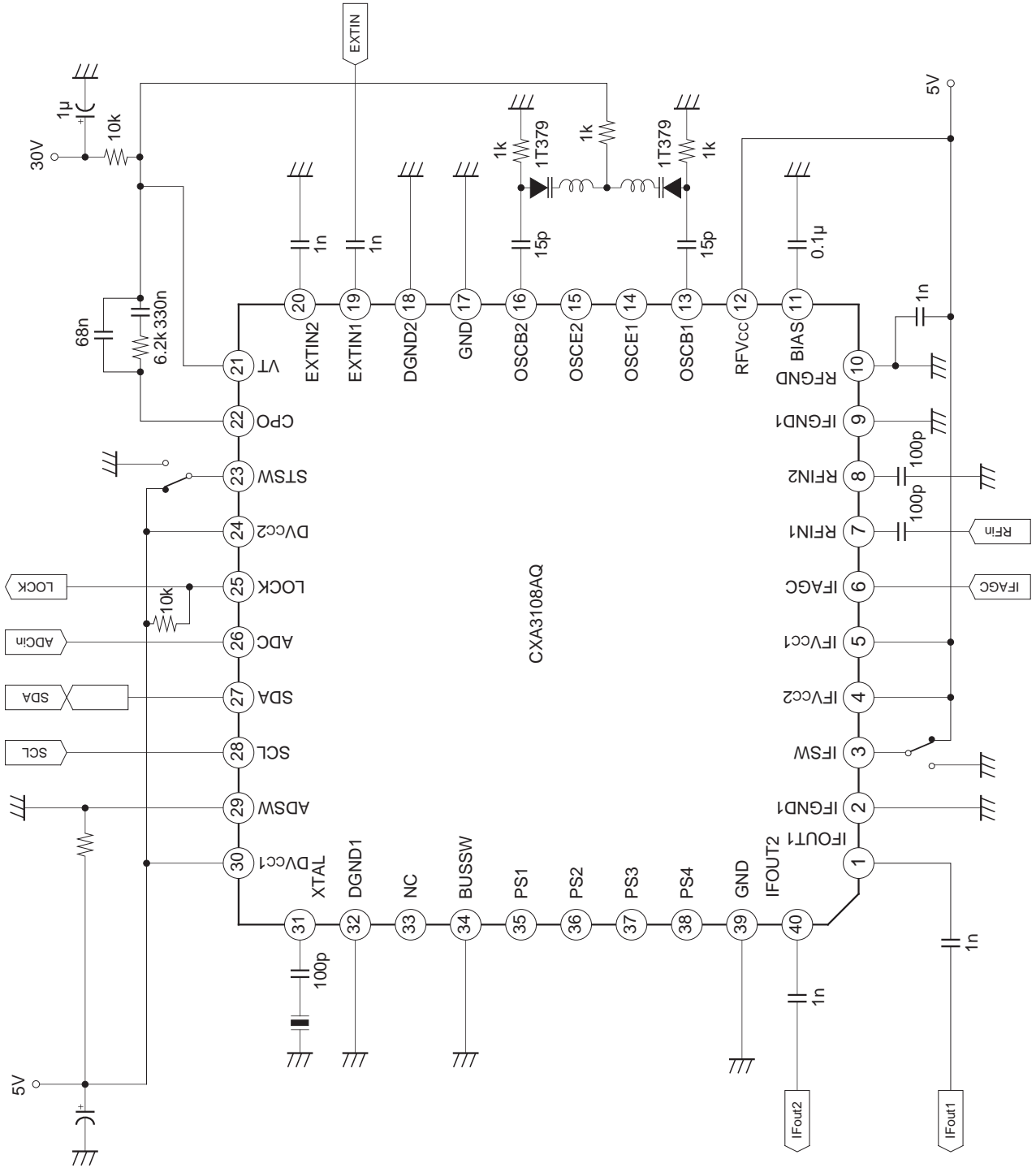
**PLL Block**

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
External local input level	EXT			-20		dBm
SDA, SCL						
High level input voltage	V <sub>IH</sub>		3		V <sub>CC</sub>	V
Low level input voltage	V <sub>IL</sub>		GND		1.5	V
High level input current	I <sub>IH</sub>	V <sub>IH</sub> =V <sub>CC</sub>		0	-0.1	μA
Low level input current	I <sub>IL</sub>	V <sub>IL</sub> =GND		-1	-2	μA
SDA Low output voltage	L <sub>SDA</sub>	Sink current=3 mA			0.4	V
Clock input hysteresis	Cl <sub>HYS</sub>		0.25	0.4	0.65	V
CPO (charge pump)						
Output current 1	I <sub>CPO1</sub>	Byte 4/bit 6=0 and for 3WB	±35	±50	±75	μA
Output current 2	I <sub>CPO2</sub>	Byte 4/bit 6	±125	±180	±270	μA
ADC						
Input current	I <sub>ADC</sub>	Input voltage=5 V		0.2		μA
LOCK						
High output voltage	V <sub>LKH</sub>	Load resistance 10 kΩ, for LOCK			V <sub>CC</sub>	V
Low output voltage	V <sub>LKL</sub>	Load resistance 10 kΩ, for UNLOCK			0.5	V
REFOSC						
Oscillator frequency range	F <sub>XTOSC</sub>		3		12	MHz
Input capacitance	C <sub>XTOSC</sub>			14		pF
Drive level	V <sub>XTOSC</sub>			200		mV
PS1 to PS4						
Pull-in current	Sink <sub>PS</sub>	When ON			1	mA
Leak current	Leak <sub>PS</sub>	When OFF			200	nA

**Bus Timing**

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
I <sup>2</sup> C Bus						
SCL clock frequency	f <sub>SCL</sub>		0		400	kHz
Start waiting time	t <sub>WSTA</sub>		1300			ns
Start hold time	t <sub>HSTA</sub>		600			ns
Low hold time	t <sub>LOW</sub>		1300			ns
High hold time	t <sub>HIGH</sub>		600			ns
Start setup time	t <sub>SSTA</sub>		600			ns
Data hold time	t <sub>HDAT</sub>		1300			ns
Data setup time	t <sub>SDAT</sub>		600			ns
Rise time	t <sub>R</sub>				300	ns
Fall time	t <sub>F</sub>				300	ns
Stop setup time	t <sub>SSTO</sub>		600			ns

Electrical Characteristics Measurement Circuit



## Description of Functions

The CXA3108AQ is a tuner IC for satellite broadcast receivers. It converts the RF signal down-converted to 1st IF (1 to 2 GHz) at the LNB to 2nd IF, so that only the desired reception frequency is selected and detected.

This IC combines the mixer, local oscillator and IF amplifier (variable gain) circuits required for frequency conversion to 2nd IF, and the PLL circuit which controls the local oscillator frequency onto a single chip.

The function of each block is described below.

### 1. Mixer Circuit

This circuit outputs the frequency difference between the signal input to RF IN and the local oscillator signal. A double-balanced mixer with minimal local oscillator signal leak is used. RF input is equivalent to a differential amplifier with emitter grounding.

### 2. Local Oscillator Circuit

A Colpitts oscillator with differential operation is used for the oscillator circuit, so it is stable relative to supply voltage fluctuation, and undesired radiation is suppressed. This circuit also contains a capacitor which is part of the resonance circuit, so there is minimal parasitic oscillation and design of external circuits is easier.

### 3. IF Amplifier Circuit

This circuit amplifies the mixer IF output, and is comprised of an AGC amplifier stage and low impedance output stage.

The gain can be varied by the AGC pin voltage (range 0 to 4 V) at the AGC amplifier stage. The maximum gain is approximately 20 dB (voltage gain between RF IN and IF OUT), and the gain variation width is 30 dB or more.

The output stage has two unbalanced outputs, and can directly connect two SAW filters with different pass bandwidths. Output pin selection is determined by the IF SW pin voltage.

The IF amplifier circuit is a wide band amplifier circuit, and can be used in the IF frequency range of 60 to 500 MHz.

### 4. PLL Circuit-1 (normal operation: when the STSW pin is open or connected to V<sub>cc</sub>)

The PLL circuit fixes the local oscillator frequency to the desired frequency. It consists of the prescaler, main divider, reference divider, phase comparator, charge pump and reference oscillator. The control format supports the I<sup>2</sup>C bus protocol.

When the power (DV<sub>cc1</sub>) is turned on, the power-on reset circuit activates and the frequency division data and control data are all initialized to 0. The power-on reset threshold is 3 V at normal temperature (T<sub>a</sub>=25 °C).

### 5. PLL Circuit-2 (external input PLL operation: when the STSW pin is connected to GND)

When the STSW pin is connected to GND, the PLL enters independent operation mode where the PLL only is used with the oscillator signal input from the external signal input pin.

## Description of PLL Block

### 1. Programming

#### 1-1. The main divider frequency division ratio is obtained according to the following formulas.

$$f_{osc} = f_{ref} \times (16M + S) \text{ or } f_{osc} = f_{ref} \times 2 \times (16M + S) \text{ (when PE = 1)}$$

$f_{osc}$  : local oscillator frequency

$f_{ref}$  : comparison frequency

2 : prescaler fixed frequency division ratio (when PE = 1)

M : main divider frequency division ratio

S : swallow counter frequency division ratio

The variable frequency division ranges of M and S are as follows.

$$S \leq M \leq 4095$$

$$0 \leq S \leq 15$$

During PLL independent operation (STSW = GND), the prescaler halving frequency division cannot be added.

#### 1-2. I<sup>2</sup>C Bus

This IC conforms to the standard I<sup>2</sup>C bus format, and bidirectional bus control is possible consisting of a write mode in which various data are received and a read mode in which various data are sent.

Write and read modes are recognized according to the setting of the final bit (R/W bit) of the address byte. Write mode is set when the R/W bit is "0", and read mode is set when the R/W bit is "1".

##### 1-2-1. Address Setting

The responding address can be changed by the ADSW pin voltage to allow more than one PLL in a system.

<Table 1> Address

ADSW pin voltage	MA1	MA0
0 to 0.1 V <sub>cc</sub>	0	0
OPEN	0	1
0.4 V <sub>cc</sub> to 0.6 V <sub>cc</sub>	1	0
0.9 V <sub>cc</sub> to V <sub>cc</sub>	1	1

**1-2-2. Data format**

Write mode is used to receive various data. In this mode, byte 1 contains the address data, bytes 2 and 3 contain the frequency data, and bytes 4 and 5 contain the various control data.

These data are latch transferred in the manner of byte 1, byte 2 + byte 3, byte 4, and byte 5. When the correct address is received, the data is recognized as frequency data if the first bit of the next byte is "0", and as control data if this bit is "1".

Also, when data transmission is stopped part-way, the previously programmed data is valid. Therefore, once the control data has been programmed, 3-byte commands consisting of the address and frequency data are possible.

Further, even if the I<sup>2</sup>C bus stop conditions are not met, data can be input by sending the start conditions and the new address.

In read mode, the power-on reset operation status, phase comparator locked/unlocked status and 5-value A/D converter input pin voltage status are transmitted to the master.

Power-on reset is set to "1" when the supply voltage (DV<sub>cc1</sub>) power supply is cut off.

If DV<sub>cc1</sub> is 3 V or higher and the status is output in the read mode, this bit is reset to "0".

Write mode: slave receiver

	MSB							LSB	
MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	M10	M9	M8	M7	M6	M5	M4	A
Divider byte 2	M3	M2	M1	M0	S3	S2	S1	S0	A
Control byte 1	1	M12	M11	PE	R3	R2	R1	R0	A
Control byte 2	OS	CP	0	0	P4	P3	P2	P1	A

Read mode: slave transmitter

MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	1	
Status byte	PR	FL	1	1	1	A2	A1	A0	

- P1 to P4 : port control  
 M0 to M12 : main divider frequency division ratio setting  
 S0 to S3 : swallow counter frequency division ratio setting  
 OS : varicap output OFF (when "1")  
 CP : charge pump current switching  
 PE : prescaler halving frequency division added (when "1")  
 PR : power-on reset  
 FL : lock detection signal  
 A0 to A2 : 5-value ADC data (ADC pin voltage conversion: Table 2)  
 R0 to R3 : reference divider frequency division ratio selection (Table 3)

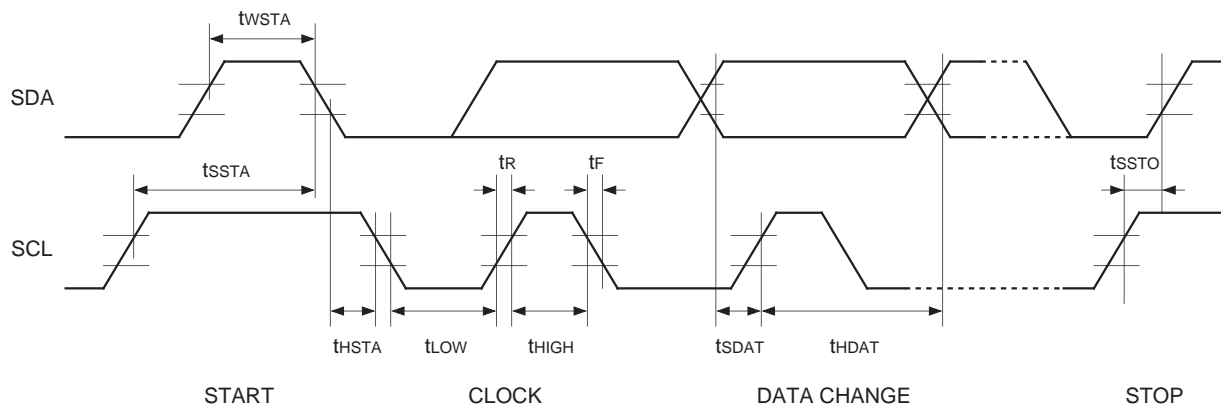
**<Table 2> ADC Conversion Table**

ADC pin voltage	A2	A1	A0
0 to 0.15V <sub>cc</sub>	0	0	0
0.15 V <sub>cc</sub> to 0.3 V <sub>cc</sub>	0	0	1
0.3 V <sub>cc</sub> to 0.45 V <sub>cc</sub>	0	1	0
0.45 V <sub>cc</sub> to 0.6 V <sub>cc</sub>	0	1	1
0.6 V <sub>cc</sub> to V <sub>cc</sub>	1	0	0

**<Table 3> Reference Divider Frequency Division Ratio**

R3	R2	R1	R0	Frequency division ratio
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	—
1	0	0	1	5
1	0	1	0	10
1	0	1	1	20
1	1	0	0	40
1	1	0	1	80
1	1	1	0	160
1	1	1	1	320

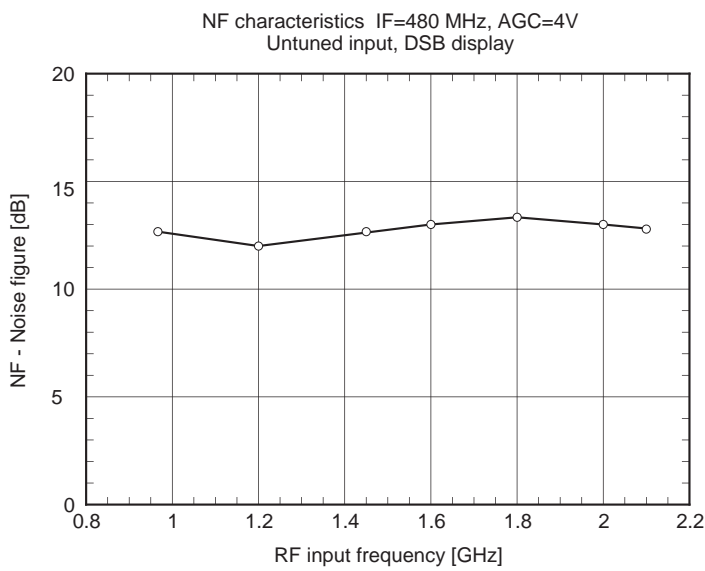
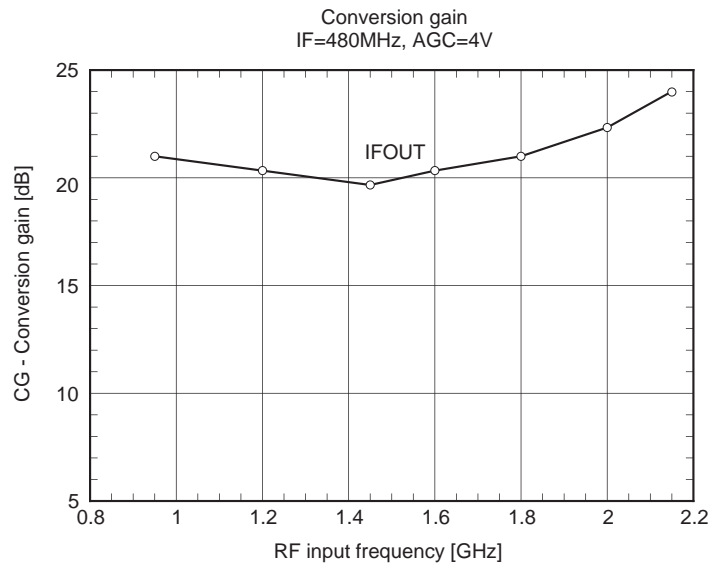
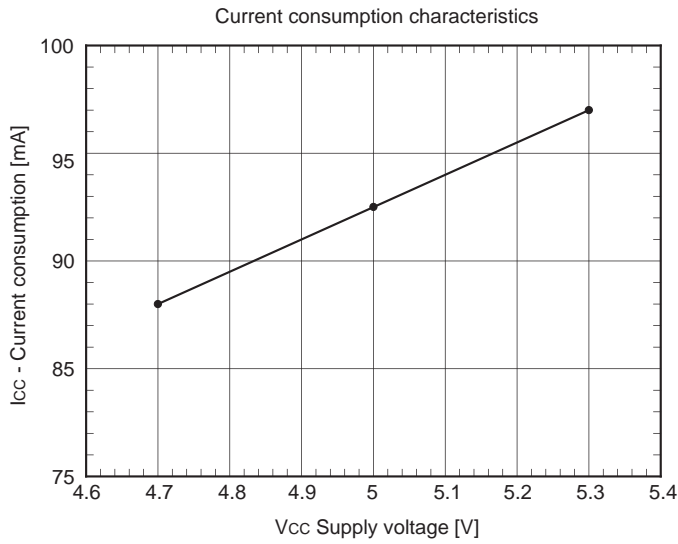
I<sup>2</sup>C Bus Timing Chart



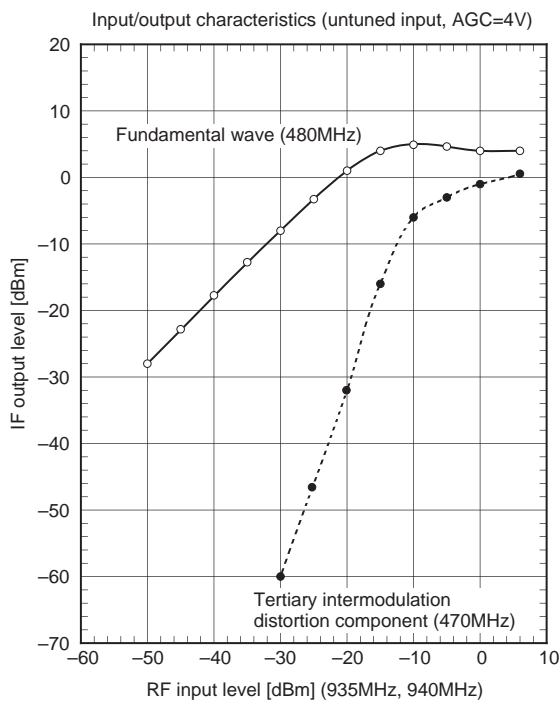
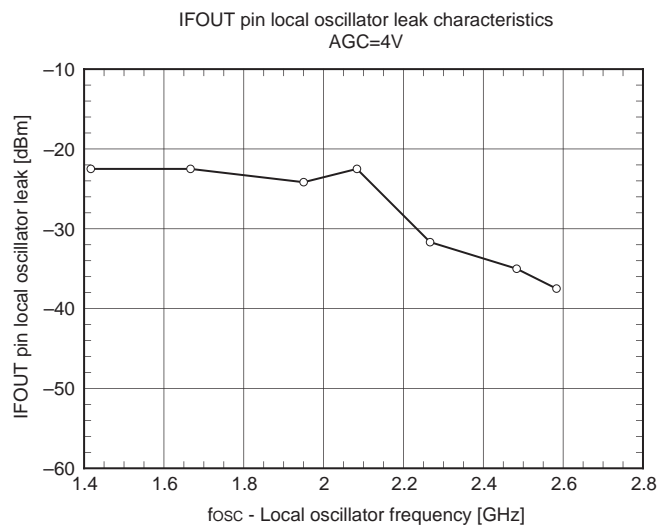
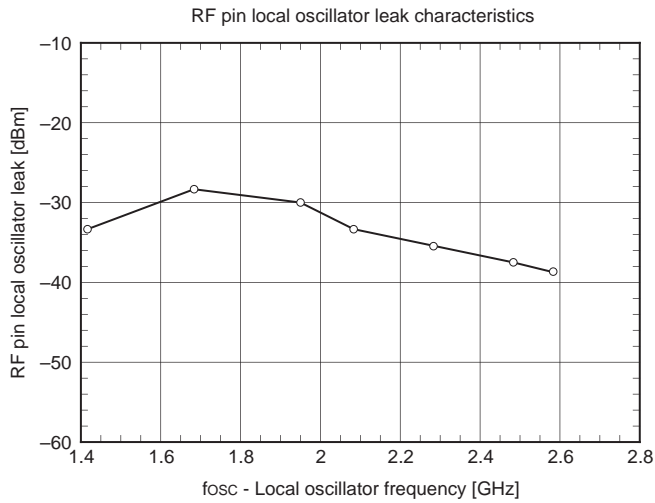
$t_{SSTA}$  =Start setup time  
 $t_{WSTA}$  =Start waiting time  
 $t_{HSTA}$  =Start hold time  
 $t_{LOW}$  =LOW clock pulse width  
 $t_{HIGH}$  =HIGH clock pulse width

$t_{SDAT}$  =Data setup time  
 $t_{HDAT}$  =Data hold time  
 $t_{SSTO}$  =Stop setup time  
 $t_R$  =Rise time  
 $t_F$  =Fall time

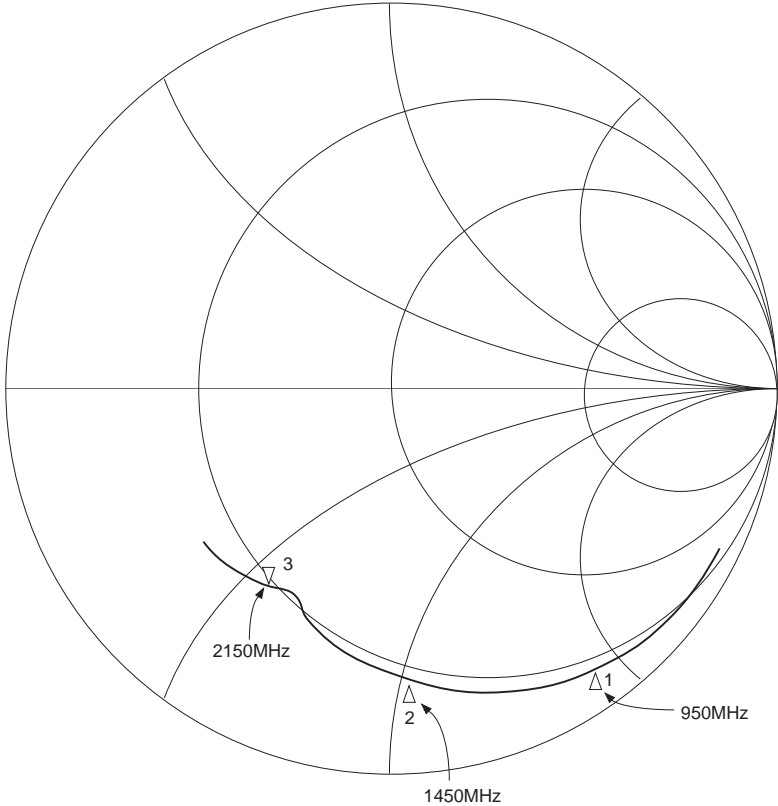
Example of Representative Characteristics



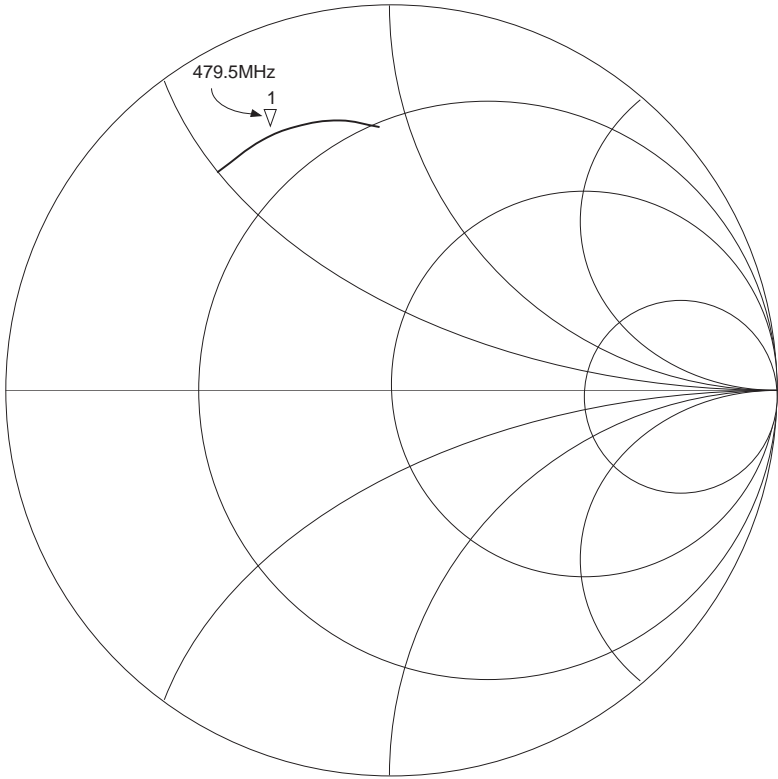




Input Impedance

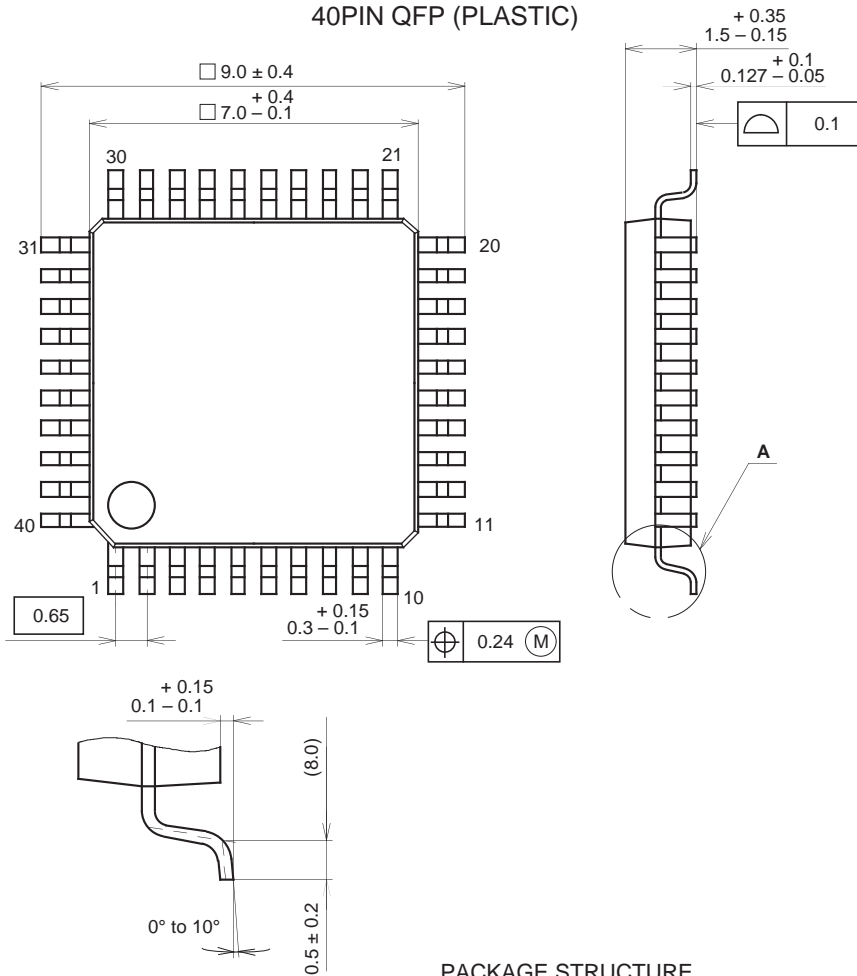


Output Impedance



Package Outline Unit : mm

40PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g