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## TDA3717

#### STEPPER MOTOR DRIVE CIRCUIT

The TDA3717 is a bipolar integrated circuit intended to control and drive the current in one winding of a stepper motor using a switch mode technique. The output drive bridge is capable of producing a bidirectional current and incorporates all required clamping diodes. The logic control inputs may by driven by TTL, CMOS, or a microprocessor control system.

#### SPECIAL FEATURES

- Bipolar output current drive enabling maximum performance to be obtained from the stepper motor.
- Full-step, half-step and quarter-step operating modes may be utilized by digital control.
- Built in clamping diodes on output drives.
- Separate supplies for internal logic and motor drive may be powered up and down in any sequence.
- Wide range of unstabilized motor supply voltage may be used 10-50 Volts.
- Wide range of output current control 20-500 mA.
- Output current levels may be selected in steps digitally or varied continuously by analog control.

#### CIRCUIT DESCRIPTION

A differential output drive is provided by means of a transistor bridge circuit which is capable of regulating a bidirectional current into a motor winding. The motor supply voltage is applied to the load by turning on two diametrically opposed output drive transistors causing the current to build up at a rate dependant on the applied voltage and the inductance of the motor winding. When the programmed current trip level is reached the monostable circuit is triggered which turns off only the negative pulling output drive transistor. Due to the inductive nature of the motor winding current cont nues to flow through the positive pulling transistor and the positive clamping diode on the opposite side of the bridge. The current will 'freewheel' since no forcing voltage is applied and only the diode and transistor voltage drops resist the flow causing a gradual reduction. After a period of time defined by the monostable circuit the supply is reestablished by turning on the negative pulling transistor causing the current to build back up to the trip level. By the above switch mode technique the load current is quickly established and maintained at the programmed level.

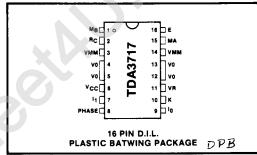


Fig. 1 Pin connections

Power dissipation in the device is reduced by cross coupling the output drives such that advantage is taken of the extra positive potential generated across the clamping diode to drive the opposite positive pulling output transistor. This will only occur during the 'freewheel' periods which are normally the greater part of the cycle.

The load current is sensed by monitoring the voltage across a low impedance resistor placed in series with the negative supply to the transistor output bridge. Current only flows through this resistor during the forcing period of the switch mode cycle and is unidirectional. At the start of the forcing period a current spike occurs due to the charge storage effect of the clamping diodes. To stop this prematurely triggering the monostable circuit a low pass RC filter is attached to the current sensing input.

Three load current trip levels can be digitally selected by the  $10~\&\,11$  inputs pins  $7~\&\,9$ . These are derived from the analog reference level (Va) on pin 11, which is normally connected direct to the 5 volt logic supply. The fourth combination of lo & li inhibits the output drive.

The 'phase' control pin 8 is a third logic input which determines the direction of the current flow in the motor winding. This input incorporates a latch with hysteresis to eliminate switching jitter.

#### **APPLICATION NOTES**

Some stepper motors are not suited to switch mode current regulation due to high core losses, a motor that has a predominant inductive load characteristic at the switching frequency is most desirable.

Power dissipation is predominatly due to the regulated load current flowing through the output drive transistors and diodes, although the power dissipated by the logic supply current should not be neglected. The upper transistor voltage drops are reduced by cross-coupling during the 'freewheel' periods and hence the power dissipation will be dependent on the duty cycle required to maintain the load current.

The maximum working ambient temperature will be dependent on the overall chip to ambient power dissipation temperature coefficient and a limitation of 145°C for the maximum working chip temperature. This chip temperature limitation is due to degradation of the plastic packaging which can occur above this limit. The overall temperature coefficient will be the sum of the chip to pin and pin to ambient coefficients.

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Typically an overall temperature coefficient of 45° C/Watt can be obtained on a P.C.B. without additional heatsinking giving a maximum working ambient temperature of 75° C when regulating 420mA giving a power dissipation of 1.5 Watts.

#### **ABSOLUTE MAXIMUM RATINGS**

			Value		Units
Electrical			Min.	Max.	
Motor Supply Voltage Motor Drive Current Logic Supply Voltage Input Voltage on Logic Inputs Analog Control Input Input Voltage	Pins 3 & 14 Pins 1 & 15 Pin 6 Pins 7,8 & 9 Pin 11 Pins 2 & 10	VMM IM VCC VR	0 —500 0 0 0	50 500 7.5 VGC 15 VGC	V mA V V V
Thermal					
Storage Temperature Operating Chip Junction Temperature		T <sub>G</sub>	<del></del> 55	145 145	°C

0 to +70°C fu BB

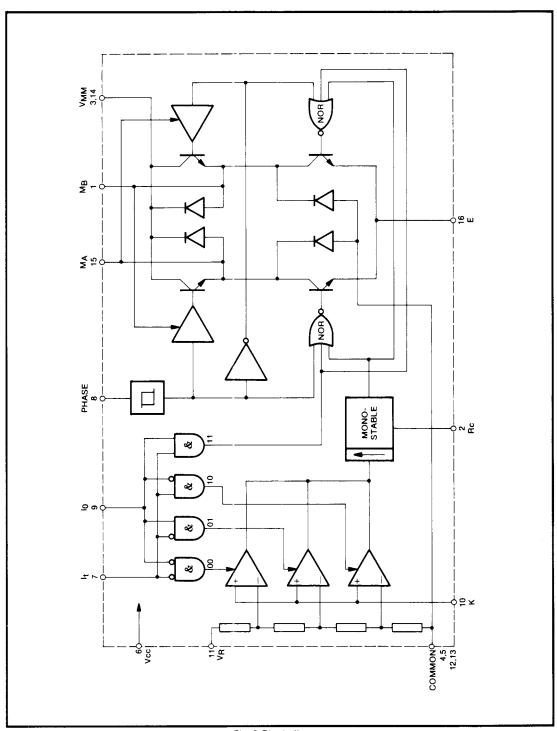


Fig. 2 Block diagram

## ELECTRICAL CHARACTERISTICS (contd)

Characteristic	Value				11-14-	Conditions	
	Symbol	Min.	Тур.	Max.	Units	Conditions	
Logic Inputs					!		
Pins 7,8 & 9 1, 10 & Phase							
Logic 1 Voltage	VIH	2.0		Vcc	V		
Logic 0 Voltage	VIL	0.0		0.8	V	V	
Input Current Low Level	IL			-0.2	mA	V <sub>1</sub> = 0.4V	
Input Current High Level	l IH			5.0	μΑ	V <sub>1</sub> = 2.4V	
Pin 8 Phase Input Hysteresis			0.6		٧		
Control Comparator							
Pin 10 Input Threshold Voltage $1_1 = 0$ , $1_0 = 0$ . $1_1 = 0$ , $1_0 = 1$ . $1_1 = 1$ , $1_0 = 0$ . $1_1 = 1$ , $1_0 = 1$ .	VER	396 236 66	416 251 78	436 266 90	mV mV mV	VR = 5V. Pin 11 Pin 10 Driving Impedance = 1Kn Inhibit—Lower Output Transistors Turned Off	
Input Current	١ĸ			-10	μΑ	Transistors 1 2 1 1	
Monostable Circuit & Timing							
Pin 2 Reset Voltage Trip Voltage Reset Charging Current Input Bias Current	VT1 VT2	2.5	1.2	5.0 —10.0	V V mA μA	Pin 2 Voltage = <sup>V</sup> T2	
Timing Period TOFF = 0.69 RT CT	TOFF	28	31	35	μS	$\label{eq:measured_mass} \left\{ \begin{array}{l} \text{Measured At Motor o/p} \\ \text{IM} = 240\text{mA}, \text{ Ton } \geq 5\mu\text{S} \\ \text{UM} = 10\text{V}, \text{dUk/dt}, \\ = 50\text{mV/}\mu\text{S} \\ \text{R}_T = 56\text{Kn}, \text{C}_t = 820\text{pF} \end{array} \right.$	
Cut Off Delay	τ <sub>D</sub>		1	2	μS	V	
Thermal Power Dissipation							
Package Thermal Resistance Chip Junction to Center Pins			11		°C/W	Measured to copper side of P.C.B. on center four pins. Note: This is not the chip to ambient temp coefficient	

### **ELECTRICAL CHARACTERISTICS**

# Test Conditions (unless otherwise stated): Vcc = 5V

Vcc = 5V Umm = 45V Chip Temperature  $\theta$  = 25°C

Input and supply voltages measured with respect to common Pins 4,5,12 & 13+.

Characteristics	Q	Value			Units	Conditions	
	Symbol	Min.	Тур.	Max.	Onits	Conditions	
Current Consumption			-				
Pin 6 Logic Supply Current 'Output Off' Logic	ICC		12.5	16.0	mA	11 = 10 = 0	
Supply Current	ICL					11 = 10 = 1	
Pin 11 Input Bias Current	IR		0.55	0.8	mA	VR = 5V	
Motor Output Drive							
Pins 1 and 15 Lower Transistor Saturation Voltage	VML			1.35	v	VE = 0V, <sup>I</sup> M = 500mA	
Lower Transistor Leakage Current	IMLL			300	μΑ	VM = 50V, VE = 0V I <sub>0</sub> = I <sub>1</sub> = 1 Current Measured at Pin 16	
Lower Diode Clamp Voltage	VMLC			-1.5	V	IM = -500mA, I0 = I1 = 1.	
Upper Transistor Forcing Saturation Voltage	VMH			-2.1	v	IM = 500mA, Measured W.R.T. UMM	
Upper Transistor Cross- Coupled Saturation Voltage	VMHX			-1.3	V		
Upper Transistor Leakage Current	IMHL			300	μА	$V_{M} = 1V, 10 = 11 = 1$	
Upper Diode Clamp Voltage	VMHC			1.25	V	M = 500mA, Measured W.R.T. UMM	
Diode Substrate Leakage Current When Clamped	ILS			2.0	, mA	IM = 500mA, VCC, VR and other inputs not connected	
Upper Diode Charge Storage			_	100	nQ	M = 500mA M = 240mA	

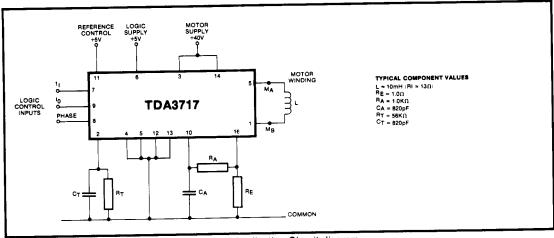


Fig. 3 Application Circuit diagram