Micro Linear

ML6696*

100BASE-X Fiber Physical Layer

GENERAL DESCRIPTION

The ML6696 implements the complete physical layer of the Fast Ethernet 100BASE-X standard for fiber media. The device provides the MII (Media Independent Interface) for interface to upper-layer silicon. The ML6696 integrates the data quantizer and the LED driver, allowing the use of low cost optical PMD components.

The ML6696 includes 4B/5B encoder/decoder, 125MHz clock recovery/clock generation, LED driver, and a data quantizer. The device also offers a power down mode which results in total power consumption of less than 20mA.
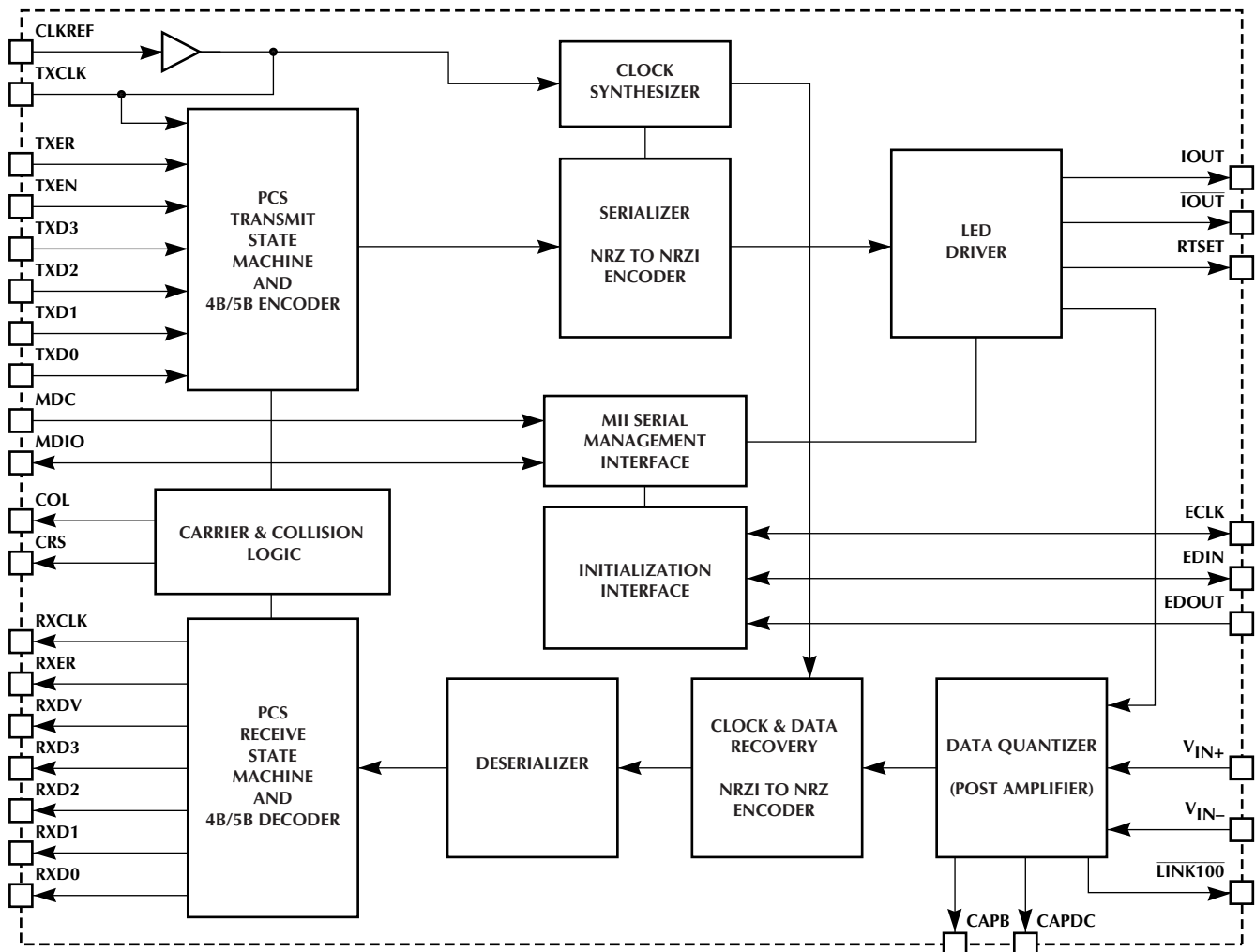
The ML6696 is suitable for the current 100BASE-FX IEEE 803.2u standard defined using 1300nm optics, as well as for the *proposed* 100BASE-SX standard defined using lower cost 820nm optics

FEATURES

■ 100BASE-FX physical layer with MII

■ Optimal 100BASE-SX solution (draft standard)

■ Integrated data quantizer (post-amplifier)

■ Integrated LED driver

■ 125MHz clock generation and recovery
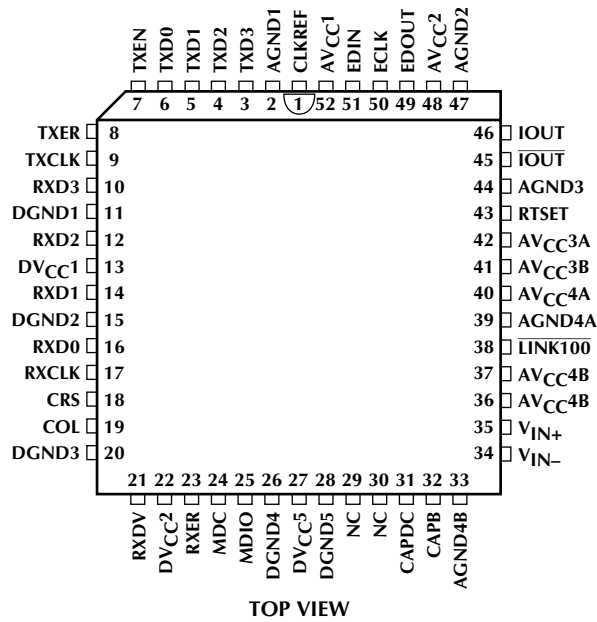
■ 4B/5B encoding/decoding

■ Power-down mode

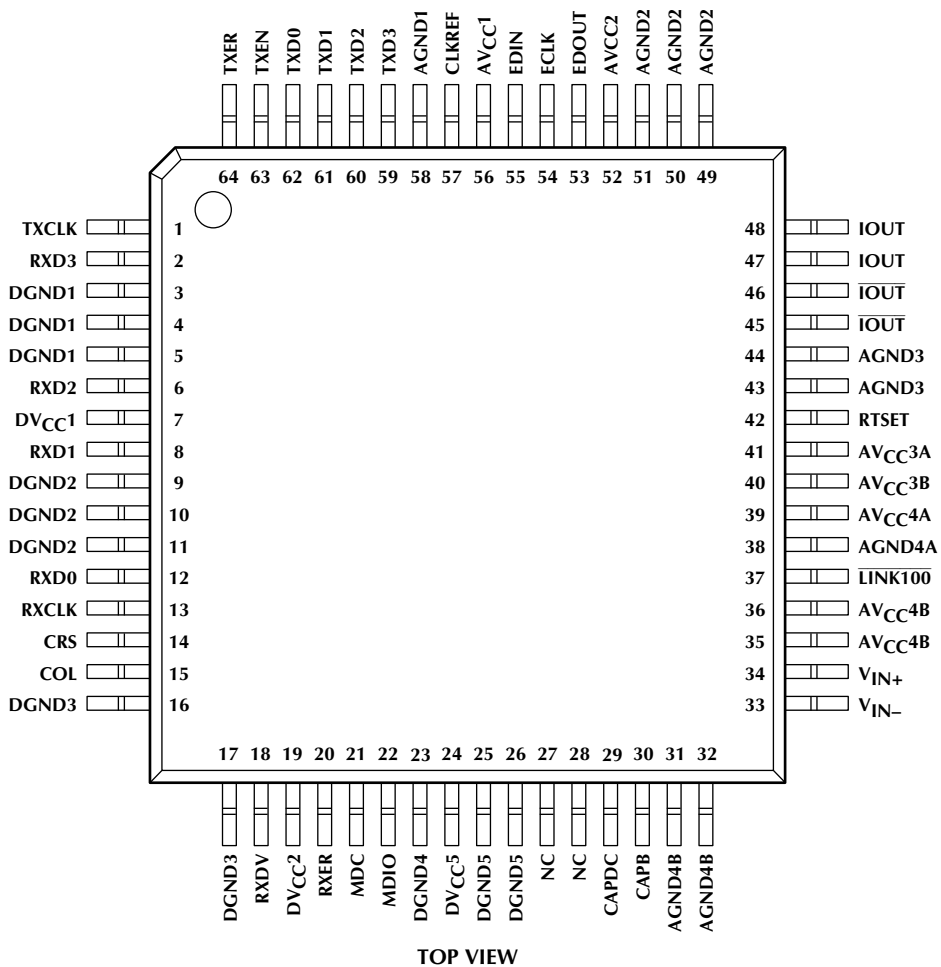* Some Packages Are Obsolete

BLOCK DIAGRAM

ML6696

PIN CONFIGURATION

ML6696
52-Pin PLCC (Q52)

Top pins (left to right): TXEN(7), TXD0(6), TXD1(5), TXD2(4), TXD3(3), AGND1(2), CLKREF(1), AV$_{CC}$1(52), EDIN(51), ECLK(50), EDOUT(49), AV$_{CC}$2(48), AGND2(47)

Left pins:
- TXER — 8
- TXCLK — 9
- RXD3 — 10
- DGND1 — 11
- RXD2 — 12
- DV$_{CC}$1 — 13
- RXD1 — 14
- DGND2 — 15
- RXD0 — 16
- RXCLK — 17
- CRS — 18
- COL — 19
- DGND3 — 20

Right pins:
- 46 — IOUT
- 45 — $\overline{IOUT}$
- 44 — AGND3
- 43 — RTSET
- 42 — AV$_{CC}$3A
- 41 — AV$_{CC}$3B
- 40 — AV$_{CC}$4A
- 39 — AGND4A
- 38 — $\overline{LINK100}$
- 37 — AV$_{CC}$4B
- 36 — AV$_{CC}$4B
- 35 — V$_{IN+}$
- 34 — V$_{IN-}$

Bottom pins (left to right): RXDV(21), DV$_{CC}$2(22), RXER(23), MDC(24), MDIO(25), DGND4(26), DV$_{CC}$5(27), DGND5(28), NC(29), NC(30), CAPDC(31), CAPB(32), AGND4B(33)

TOP VIEW

ML6696
64-Pin TQFP (H64-10)

Top pins (left to right): TXER(64), TXEN(63), TXD0(62), TXD1(61), TXD2(60), TXD3(59), AGND1(58), CLKREF(57), AV$_{CC}$1(56), EDIN(55), ECLK(54), EDOUT(53), AVCC2(52), AGND2(51), AGND2(50), AGND2(49)

Left pins:
- TXCLK — 1
- RXD3 — 2
- DGND1 — 3
- DGND1 — 4
- DGND1 — 5
- RXD2 — 6
- DV$_{CC}$1 — 7
- RXD1 — 8
- DGND2 — 9
- DGND2 — 10
- DGND2 — 11
- RXD0 — 12
- RXCLK — 13
- CRS — 14
- COL — 15
- DGND3 — 16

Right pins:
- 48 — IOUT
- 47 — IOUT
- 46 — $\overline{IOUT}$
- 45 — $\overline{IOUT}$
- 44 — AGND3
- 43 — AGND3
- 42 — RTSET
- 41 — AV$_{CC}$3A
- 40 — AV$_{CC}$3B
- 39 — AV$_{CC}$4A
- 38 — AGND4A
- 37 — $\overline{LINK100}$
- 36 — AV$_{CC}$4B
- 35 — AV$_{CC}$4B
- 34 — V$_{IN+}$
- 33 — V$_{IN-}$

Bottom pins (left to right): DGND3(17), RXDV(18), DV$_{CC}$2(19), RXER(20), MDC(21), MDIO(22), DGND4(23), DV$_{CC}$5(24), DGND5(25), DGND5(26), NC(27), NC(28), CAPDC(29), CAPB(30), AGND4B(31), AGND4B(32)

TOP VIEW

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PIN DESCRIPTION (Pin Number in Parentheses is for PLCC Version)

PIN	NAME	FUNCTION
1 (9)	TXCLK	Transmit clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz TX bit clock. Data appearing at TXD<3:0> are clocked into the ML6696 on the rising edge of this clock.
2 (10)	RXD3	Receive data TTL output. Output is valid on RXCLK's rising edge.
3, 4, 5, (11)	DGND1	Digital ground
6 (12)	RXD2	Receive data TTL output. Output is valid on RXCLK's rising edge.
7 (13)	$DV_{CC}1$	Digital positive power supply
8 (14)	RXD1	Receive data TTL output. Output is valid on RXCLK's rising edge.
9, 10, 11 (15)	DGND2	Digital ground
12 (16)	RXD0	Receive data TTL output. Output is valid on RXCLK's rising edge.
13 (17)	RXCLK	Recovered receive clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz bit clock recovered from the signal received at VIN+/-. Receive data are clocked out at RXD<3:0> on the falling edges of this clock, and should be sampled on rising edges. RXCLK is phase-aligned to CLKREF in the absence of a 100BASE-FX signal at $V_{IN+/-}$.
14 (18)	CRS	Carrier Sense TTL output. CRS goes high in the presence of non-idle signals at VIN+/-, or when the ML6696 is transmitting. CRS goes low when there is no transmit activity and receive is idle. In repeater or full-duplex mode, CRS goes high in the presence of non-idle signals at $V_{IN+/-}$ only.
15 (19)	COL	Collision Detected TTL output. COL goes high upon detection of a collision on the network, and remains high as long as the collision condition persists. COL is low when the ML6696 operates in full-duplex, repeater, or loopback modes.
16, 17 (20)	DGND3	Digital ground
18 (21)	RXDV	Receive data valid TTL output. This output is high when the ML6696 is receiving a data packet. RXDV is valid on RXCLK's rising edge.
19 (22)	$DV_{CC}2$	Digital positive power supply
20 (23)	RXER	Receive error TTL output. This output goes high to indicate error or invalid symbols within a packet, or corrupted idle between packets. RXER is valid on RXCLK's rising edge.
21 (24)	MDC	MII Serial Management Interface clock TTL input. A clock at this pin clocks serial data into or out of the ML6696's MII management registers through the MDIO pin. The maximum clock frequency at MDC is 2.5MHz.
22 (25)	MDIO	MII Serial Management Interface data TTL input/output. Serial data are written to and read from the management registers through this I/O pin. Input data is sampled on the rising edge of MDC. Output data is valid on MDC's rising edge
23 (26)	DGND4	Digital ground
24 (27)	$DV_{CC}5$	Digital positive power supply
25, 26 (28)	DGND5	Digital ground
27, 28 (29, 30)	NC	No connect
29 (31)	CAPDC	Data quantizer offset-correction loop, offset-storage capacitor input pin. The capacitor tied between this pin and AV_{CC} stores the amplified data quantizer offset voltage and also sets the dominant pole in the offset-correction loop. A 0.1µF surface mount is recommended.

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PIN	NAME	FUNCTION
30 (32)	CAPB	Data quantizer input bias bypass capacitor input. The capacitor tied between this pin and AV_{CC} filters the quantizer's internal input bias reference. A 0.1µF surface-mount capacitor is recommended.
31, 32 (33)	AGND4B	Analog ground
33 (34)	V_{IN-}	Receive quantizer negative input. This input should be tied to $AV_{CC}Q$ through an AC coupling capacitor. (0.01µF recommended)
34 (35)	V_{IN+}	Receive quantizer positive input. This input receives 100BASE-FX signals from the network optical receiver through an AC coupling capacitor. (0.01µF recommended).
35, 36 (36, 37)	$AV_{CC}4B$	Analog positive power supply
37 (38)	$\overline{LINK100}$	100BASE-FX link activity open-drain output. $\overline{LINK100}$ pulls low when there is 100BASE-FX activity at VIN+/–. This output is capable of sinking sufficient current to directly drive a status LED in series with a current limiting resistor.
38 (39)	AGND4A	Analog ground
39 (40)	$AV_{CC}4A$	Analog positive power supply
40 (41)	$AV_{CC}3B$	Analog positive power supply
41 (42)	$AV_{CC}3A$	Analog positive power supply
42 (43)	RTSET	Transmit level bias resistor. For 100BASE-FX, an external 2.32kΩ, 1% resistor connected between RTSET and AGND3 sets a precision constant bias current that gives a nominal output "on" current of 75mA at I_{OUT}.
43, 44 (44)	AGND3	Analog ground
45, 46 (45)	$\overline{IOUT}$	Transmit LED output. This pin connects through an external 15Ω resistor to AV_{CC} when the part is used to drive a network LED.
47, 48 (46)	IOUT	Transmit LED output. This open-collector current output drives NRZI waveforms into a network LED.
49, 50, 51 (47)	AGND2	Analog ground
52 (48)	$AV_{CC}2$	Analog positive power supply
53 (49)	EDOUT	Initialization Interface data out CMOS input. With EDIN low at power up, EDOUT has no function. With EDIN floating at power up, EDOUT is the serial data input for configuration data from an EEPROM. With EDIN high at power up, EDOUT is the input for configuration data from an external microcontroller. (Table 1)
54 (50)	ECLK	Initialization Interface clock CMOS input/output. With EDIN low at power up, ECLK is inactive. With EDIN floating at power up, ECLK is the ML6696's clock output for timing the configuration data from an external EEPROM. With EDIN high at power up, ECLK is the clock input for timing configuration data from an external microcontroller. (Table 1)
55 (51)	EDIN	Initialization Interface mode select and EEPROM interface data in CMOS input/output. EDIN selects one of three possible interface modes at power up. See the Initialization Interface section for more information. (Table 1)
56 (52)	$AV_{CC}1$	Analog positive power supply
57 (1)	CLKREF	Transmit clock TTL input. This 25MHz clock is the frequency reference for the internal TX PLL clock synthesizer and logic. This pin should be driven by an external 25MHz clock at TTL levels.
58 (2)	AGND1	Analog ground
59 (3)	TXD3	Transmit data TTL input. TXD<3:0> inputs accept TX data symbols from the MII. Data appearing at TXD<3:0> are clocked into the ML6696 on the rising edge of TXCLK.

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PIN DESCRIPTION (Pin Number in Parentheses is for PLCC Version) (Continued)

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
60 (4)	TXD2	Transmit data TTL input. TXD<3:0> inputs accept TX data symbols from the MII. Data appearing at TXD<3:0> are clocked into the ML6696 on the rising edge of TXCLK.	63 (7)	TXEN	Transmit enable TTL input. Driving this input high indicates to the ML6696 that transmit data are present at TXD<3:0>. TXEN edges should be synchronous with TXCLK.
61 (5)	TXD1	Transmit data TTL input. TXD<3:0> inputs accept TX data symbols from the MII. Data appearing at TXD<3:0> are clocked into the ML6696 on the rising edge of TXCLK.	64 (8)	TXER	Transmit error TTL input. Driving this pin high with TXEN also high causes the part to continuously transmit an H symbol (00100). When TXEN is low, TXER has no effect.
62 (6)	TXD0	Transmit data TTL input. TXD<3:0> inputs accept TX data symbols from the MII. Data appearing at TXD<3:0> are clocked into the ML6696 on the rising edge of TXCLK.			

ML6696

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} Supply Voltage Range ....–0.3V to 6V
Input Voltage Range
   Digital Inputs .... –0.3V to V_{CC}
   VIN+, VIN-, CLKREF, CAPB, CAPDC .... –0.3V to V_{CC}
Output Current
   IOUT, IOUT 90mA
   All Other Outputs 10mA
Junction Temperature ....0ºC to 125ºC

Storage Temperature ....–65ºC to 150ºC
Lead Temperature (Soldering, 10 sec) 260ºC
Thermal Resistance (θ_{JA})
   TQFP .... 52°C/W
   PLCC .... 40°C/W

OPERATING CONDITIONS

Temperature Range .... 0ºC to 70ºC
RTSET ....2.32kΩ ±1%
V_{CC} Supply Voltage .... 5V ±5%
   All V_{CC} supply pins *must* be within 0.1V of each other.
   All GND pins *must* be within 0.1V of each other.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ±5%, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TTL INPUTS (TXD<3:0>, CLKREF, MDC, MDIO, TXEN, TXER)						
V_{IL}	Input Low Voltage	I_{IL} = –400µA	-0.3		0.8	V
V_{IH}	Input High Voltage	I_{IH} = 100µA	2.0		V_{CC}+0.3	V
I_{IL}	Input Low Current	V_{IN} = 0.4V	-200			µA
I_{IH}	Input High Current	V_{IN} = 2.4V			100	µA
TTL OUTPUTS (RXD<3:0>, RXCLK, RXDV, RXER, CRS, COL, MDIO, TXCLK)						
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4			V
CMOS INPUTS (EDIN, EDOUT, ECLK)						
V_{ILC}	Input Low Voltage				0.2 × V_{CC}	V
V_{IHC}	Input High Voltage		0.8 × V_{CC}			V
CMOS OUTPUTS (ECLK)						
V_{OLC}	Output Low Voltage	I_{OL} = 2mA			0.1 × V_{CC}	V
V_{OHC}	Output High Voltage	I_{OL} = –2mA	0.9 × V_{CC}			V
RECEIVER (V_{IN+}, $V_{IN–}$)						
V_{ICM}	Input Common-Mode Voltage	V_{CC} = 5V		2.5		V
V_{ID}	Differential Input Voltage Range		3.5		1600	mV$_{P-P}$
R_{IDR}	Differential Input Resistance		500		1000	Ω
V_{SDA}	Signal Detect Assertion Threshold	Peak-to-Peak Non-idle Signal Level at $V_{IN+/-}$	8		12	mV$_{P-P}$
A_{HYST}	Input Hysteresis		1.5		2	dB

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DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER (IOUT, $\overline{\text{IOUT}}$)						
I_{LEDH}	IOUT High Output Current	RTSET = 2.32kΩ ±1%	67.5	75	82.5	mA
I_{LEDL}	Low Output Current	RTSET = 2.32kΩ ±1%			0.1	mA
I_{RT}	RTSET Input Current	RTSET = 2.32kΩ ±1%	486	540	594	µA
POWER SUPPLY CURRENT						
I_{CC}	Supply Current, 100BASE-FX, Transmitting	Current into All V_{CC} Pins		200	295	mA
I_{CCPD}	Supply Current, Power-Down Mode	Current into All V_{CC} Pins			20	mA

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ±5%, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER						
t_{CLK}	CLKREF – TXCLK Delay		5		11	ns
t_{TXP}	Transmit Bit Delay	Note 2			10.5	bit times
$t_{TR/F}$	I_{OUT} Rise /Fall Time	Note 3			2	ns
t_{TDC}	I_{OUT} Output Duty Cycle Disotrtion	Note 3	–0.5		0.5	ns
RECEIVER						
t_{RXDC}	Receive Bit Delay (CRS)	Note 3			15.5	bit times
t_{RXDR}	Receive Bit Delay (RXDV)	Note 4			25.5	bit times
MII INTERFACE						
X_{NTOL}	CLKREF Input Clock Frequency Tolerance	25MHz Frequency	–50		50	ppm
t_{TPWH}	TXCLK Pulse Width High		14			ns
t_{TPWL}	TXCLK Pulse Width Low		14			ns
t_{RPWH}	RXCLK Pulse Width High		14			ns
t_{RPWL}	RXCLK Pulse Width Low		14			ns
t_{TPS}	Setup Time, TXD<3:0> Data Valid to TXCLK Rising Edge	Note 5	5			ns
t_{TPH}	Hold time, TXD<3:0> Data Valid After TXCLK Rising Edge	Note 5	0			ns
t_{RCS}	Time That RXD<3:0> Data are Valid Before RXCLK Rising Edge	Note 6, 7	10			ns
t_{RCH}	Time That RXD<3:0> Data are Valid After RXCLK Rising Edge	Note 6, 7	10			ns
t_{RPCR}	RXCLK 10%-90% Rise Time				6	ns
t_{RPCF}	RXCLK 90%-10% Fall Time				6	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MII MANAGEMENT INTERFACE (MDC, MDIO)						
t_{SPWS}	Write Setup Time, MDIO Data Valid to MDC Rising Edge (1.4V Point)		10			ns
t_{SPWH}	Write Hold Time, MDIO Data Valid After MDC Rising Edge (1.4V Point)		10			ns
t_{SPRS}	Read Setup Time, MDIO Data Valid to MDC Rising Edge (1.4V Point)		100			ns
t_{SPRH}	Read Hold Time, MDIO Data Valid After MDC Rising Edge (1.4V Point)		0			ns
t_{CPER}	Period of MDC		400			ns
t_{CPW}	Pulsewidth of MDC	Positive or Negative Pulses	160			ns
EEPROM INTERFACE (ECLK, EDIN, EDOUT)						
t_{PW1}	ECLK Positive Pulsewidth	EDIN Floating (EEPROM Mode)	900			ns
t_{PW2}	ECLK Negative Pulsewidth	EDIN Floating (EEPROM Mode)	900			ns
t_{PER1}	ECLK Period	EDIN Floating (EEPROM Mode)	1800			ns
t_{DV1}	EDOUT Data Valid Time After ECLK Rising Edge	EDIN Floating (EEPROM Mode)			900	ns
t_{PER2}	ECLK Period	EDIN High (Microcontroller Mode)	5000			ns
t_{PW3}	ECLK Positive Pulsewidth	EDIN High (Microcontroller Mode)	2000			ns
t_{PW4}	ECLK Negative Pulsewidth	EDIN High (Microcontroller Mode)	2000			ns
t_{S1}	ECLK Data Setup Time	EDIN High (Microcontroller Mode)	10			ns
t_{H1}	ECLK Data Hold Time	EDIN High (Microcontroller Mode)	10			ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: From first rising edge of TXCLK after TXEN goes high, to first bit of J at the MDI.

Note 3: From first bit of J at the MDI, to CRS.

Note 4: From first bit of J at the MDI, to first rising edge of RXCLK after RXDV goes high.

Note 5: Measured between the time that TXD0-3 transition above or below the region 0.8V–2.0V, and the time that TXCLK rises above 0.8V.

Note 6: Measured between the time that RXD0-3 transition above or below the region 0.8V–2.0V, and the time that RXCLK rises above 0.8V.
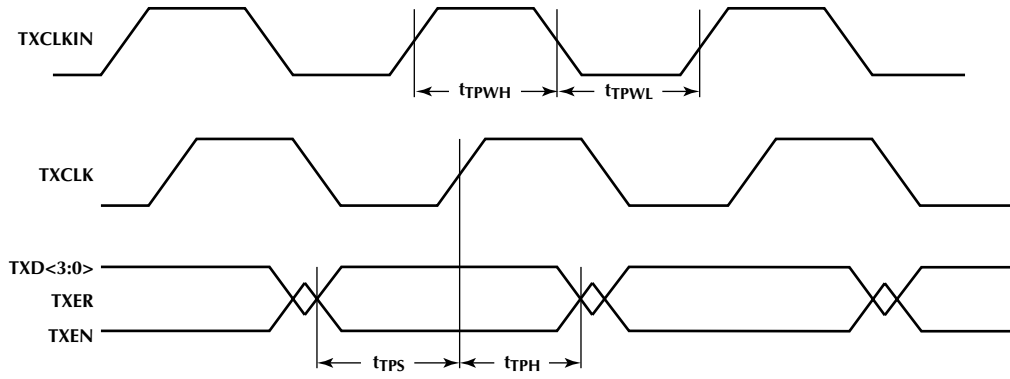
Note 7: Measured using a 15pF load to ground.

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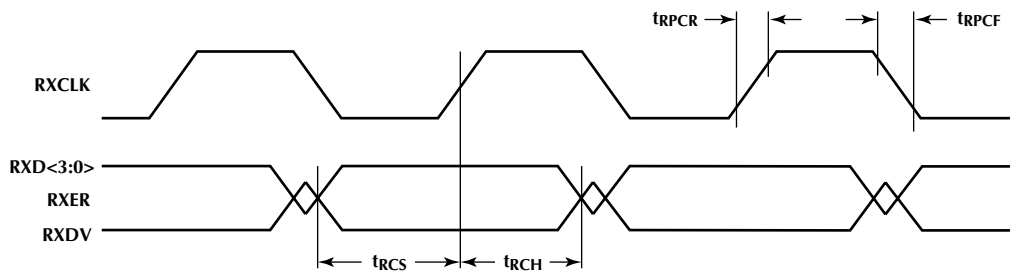
Figure 1. MII Transmit Timing
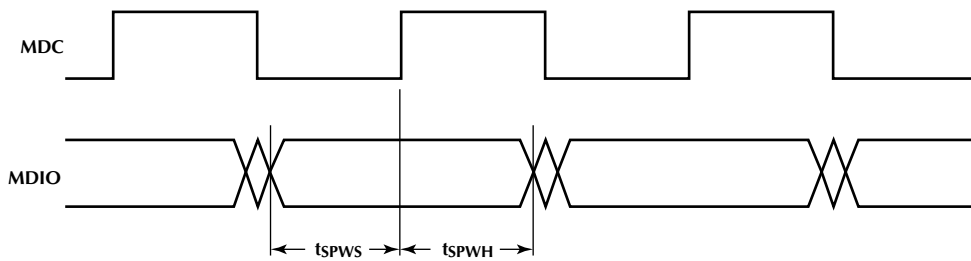

Figure 2. MII Receive Timing

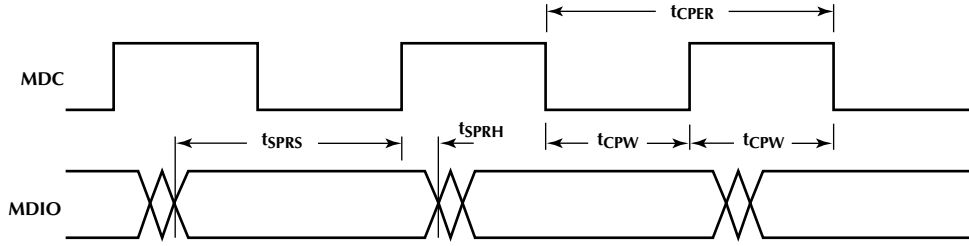**Figure 3. MII Management Interface Write Timing**

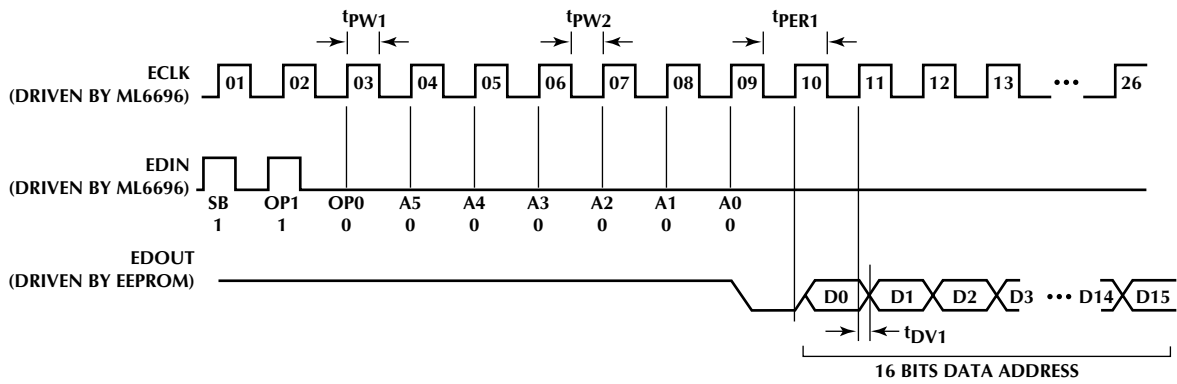**Figure 4. MII Management Interface Read Timing**
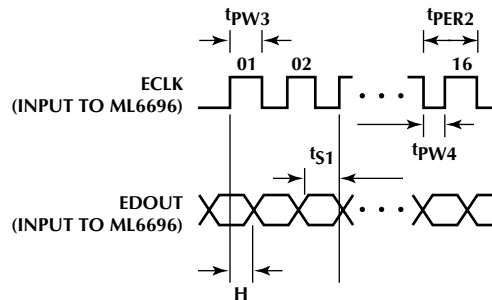

Figure 5. EEPROM Interface Timing

Figure 6. MII Management Interface Read Timing

FUNCTIONAL DESCRIPTION

FIBER OPTIC TRANSMITTER

The on-chip transmit PLL converts a 25MHz TTL-level clock at CLKREF to an internal 125MHz bit clock. TXCLK from the ML6696 clocks transmit data from the MAC into the ML6696's TXD<3:0> input pins upon assertion of TXEN. Data from the TXD<3:0> inputs are 5-bit encoded and converted from parallel to serial form at the 125MHz clock rate. The ML6696 drives corresponding NRZI data out from its LED driver. The LED driver at IOUT is a current mode switch which develops the output light by sinking current through the network LED into IOUT. RTSET's value determines the output current:

$$RTSET = \left(\frac{1.25V}{IOUT}\right) \times 140\Omega \qquad (1)$$

where IOUT is the desired output current.

Driving TXEN low will cause the ML6696's transmitter to enter the idle state and output 62.5MHz idle signal. Driving TXER high when TXEN is high causes the H symbol (00100) to appear in the transmitted data stream. The media access controller asserts TXER synchronously with TXCLK's rising edge, and the H symbol appears in place of valid symbols in the current frame.

FIBER OPTIC RECEIVER

The data quantizer accepts data at the $V_{IN+/-}$ pins that is above the internally-set 10mVpp threshold (typical).

The receive PLL extracts clock from the quantizer's output, providing jitter attenuation, and clocks the signal through the serial-to-parallel converter. The resulting 5-bit symbols are aligned and decoded, and appear at RXD<3:0>. The ML6696 asserts RXDV when it's ready to present properly decoded receive data at RXD<3:0>. The extracted clock appears at RXCLK. The receiver strips out 62.5MHz idle between data packets.

The receiver will assert RXER high if it detects errors in the receive data or idle stream.

COLLISION AND CRS

COL goes high to indicate simultaneous 100BASE-FX receive and transmit activity (a collision). CRS goes high whenever there is either receive or transmit activity in default mode, or only when there is receive activity in repeater or full-duplex mode.

CLOCK INPUT

The ML6696 requires an accurate 25MHz reference at CLKREF for internal clock generation (±50ppm, see parameter X_{NTOL}).

ML6696 PHY MANAGEMENT FUNCTIONS

The ML6696 has management functions controlled by the register locations given in Table 3 (page 12). There are two 16-bit management registers, with several unused locations. Register 0 is the basic control register (read/write). Register 1 is the basic status register (read-only). The ML6696 powers on with all management register bits set to their default values.

The ML6696's status and control register addresses and functions match those described for the MII in IEEE 802.3u section 22. IEEE 802.3u specifies the management data frame structure in section 22.2.4.4.

See IEEE 802.3u section 22.2.4 for a discussion of MII management functions and status/control register definitions.

INITIALIZATION INTERFACE

The ML6696 has an Initialization Interface to allow register programming that is not supported by the MII Management Interface. The intitialization data is loaded at power-up and cannot be changed afterwards. The pin EDIN selects one of three possible programming modes. The Initialization Register bit assignment is shown in Table 2.

EEPROM PROGRAMMING

With EDIN floating (set to a high impedance), the ML6696 reads the 16 configuration bits from an external serial EEPROM (93LC46 or similar) using the industry-standard 3-wire serial I/O protocol. After power up, the ML6696 automatically generates the address at EDIN and the clock at ECLK to read out the 16 configuration bits. The EEPROM generates the configuration bit stream at EDOUT, synchronized with ECLK. Interface timing is shown in Figure 5. It is important to note that the ML6696 expects LSBs first, whereas the 93LC46 shifts MSBs out first. Therefore, the data pattern must be reversed before programming it into the EEPROM.

MICROCONTROLLER PROGRAMMING

With EDIN high, the ML6696 expects the 16 configuration bits transfered directly at EDOUT, synchronized with the first 16 clock rising edges provided externally at ECLK after power-up. This mode is useful with a small microcontroller; one controller can program several ML6696 parts by selectively toggling their ECLK pins. Interface timing is shown in Figure 6.

ML6696 HARD-WIRED DEFAULT

With EDIN low, the ML6692 responds to MII PHYAD 00000 only. "ISODIS" bit and "REPEATER" bit are 0.

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EDIN	MODE	FUNCTION OF RELATED PINS	
		ECLK	EDOUT
Floating (EEPROM ADDR)	EEPROM	ECLK (Output clock to EEPROM)	EDOUT (Input data from EEPROM)
High	Microcontroller	ECLK (Input clock from Microcontroller)	EDOUT (Input data from Microcontroller)
Low	Hardwired	No Effect	No Effect

Table 1. ML6696 Pin Function

BIT(S)	NAME	DESCRIPTION	DEFAULT
i.15	PHY A4	PHY address bit 4	0
i.14	PHY A3	PHY address bit 3	0
i.13	PHY A2	PHY address bit 2	0
i.12	PHY A1	PHY address bit 1	0
i.11	PHY A0	PHY address bit 0	0
i.10 - i.8		Not Used	
i.7	ISODIS	Isolate bit disable (bit 0.10)	0
i.6	REPEATER	Repeater mode: when set to 1, CRS is only asserted when receiving non-idle signal at IN+/–, and ML6696 is forced to half duplex mode.	0
i.5 - i.0		Not Used	

Table 2. Initialization Interface Register

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BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
1.14	100BASE-X Full Duplex	1=Full duplex 100BASE-X capability 0=No full duplex 100BASE-X capability	RO	$\overline{i.6}$
1.13	100BASE-X Half Duplex	1=Half duplex 100BASE-X capability 0=No half duplex 100BASE-X capability	RO	1
1.12-1.3		Not used	RO	0
1.2	Link Status	1=One and only one PHY-specific link is up 0=Link is down	RO,LL	0
1.1 - 1.0		Not used	RO	0
0.15	Reset	1=Reset registers 0 and 1 to default values 0=Normal operation	R/W, SC	0
0.14	Loopback	1=PMD loopback mode 0=Normal operation	R/W	0
0.13	Manual Speed Select	1=100Mb/s 0=10Mb/s	R/W	1
0.12		Not used	RO	0
0.11	Power down	1=Power down 0=Normal operation	R/W	0
0.10	Isolate	1=Electrically isolate the ML6696 from MII 0=Normal operation	R/W	i.7
0.9		Not used	RO	0
0.8	Duplex mode	1=Full duplex select 0=Half duplex select	R/W	$\overline{i.6}$
0.7	Collision Test	1=Enable COL signal test 0=Normal operation	R/W	0
0.6 - 0.0		Not Used	RO	0

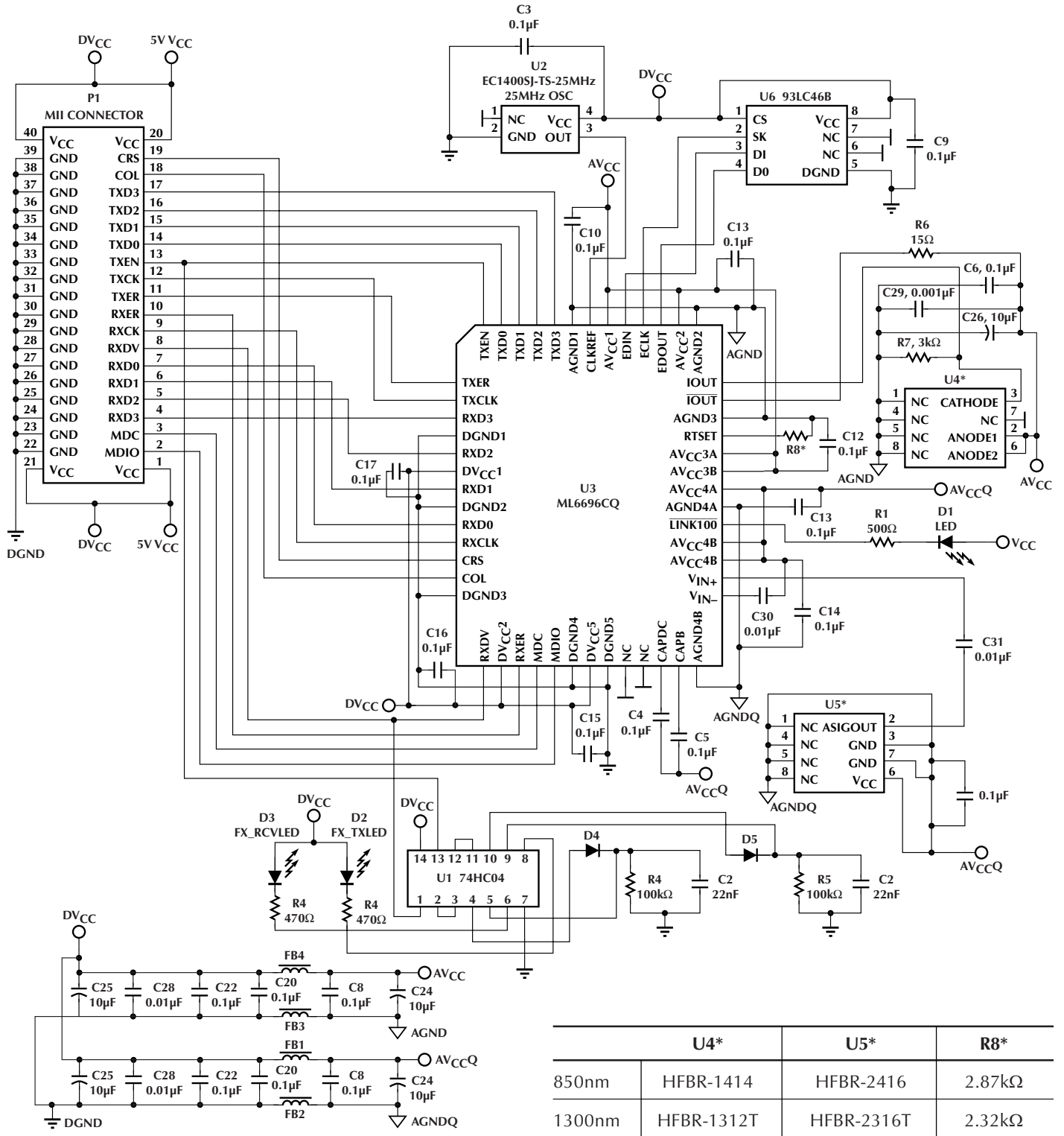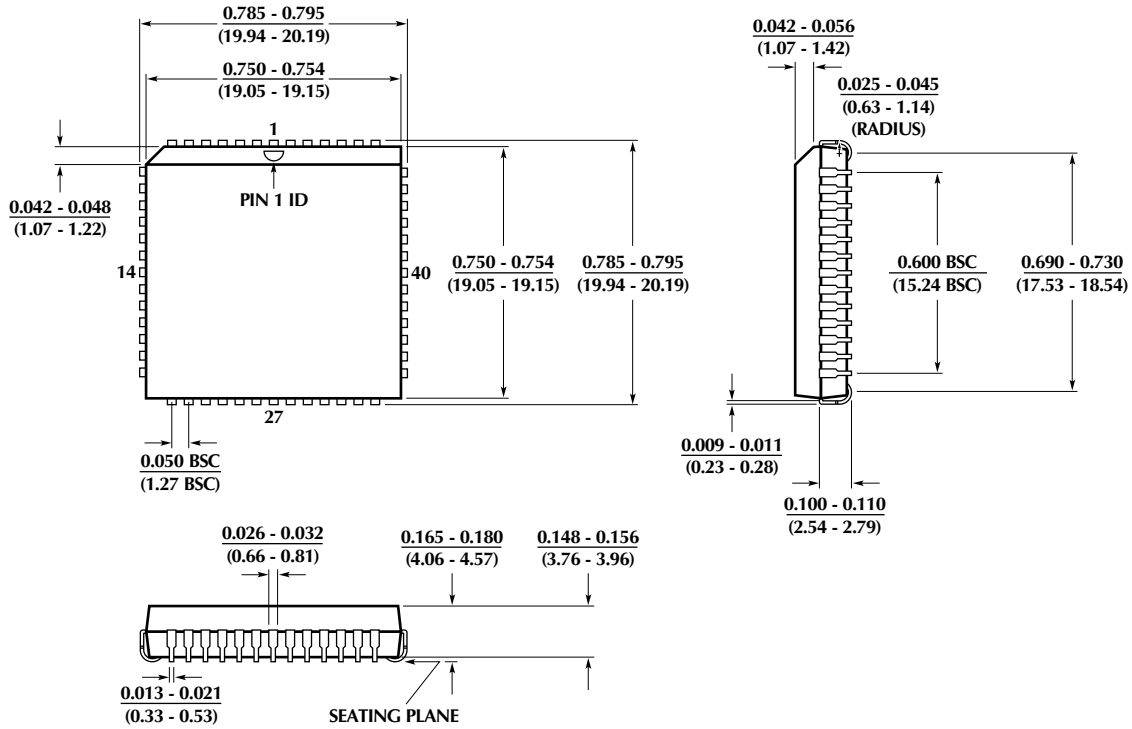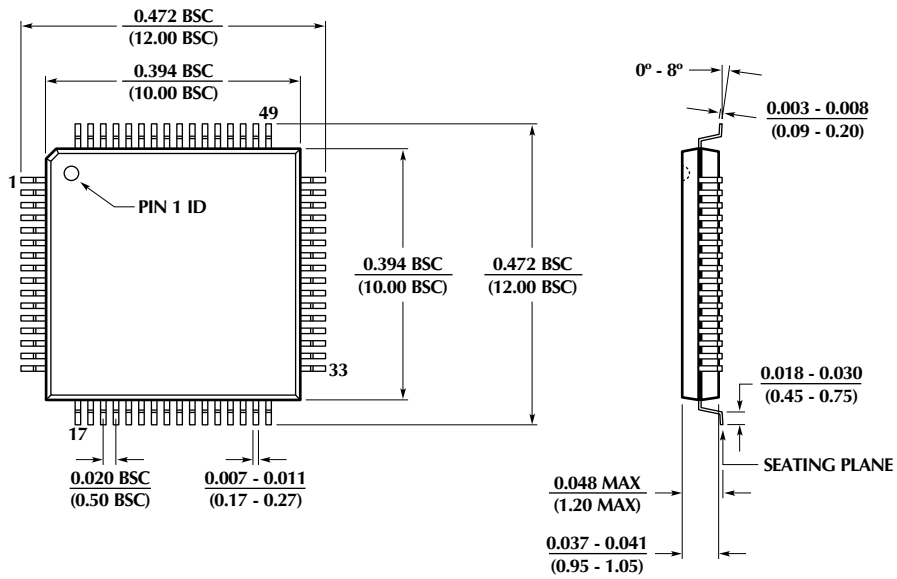**Table 3. Management Register Function Bit Locations (Registers 0, 1)**

ML6696

Figure 7. ML6696 Typical Application Schematic

	U4*	U5*	R8*
850nm	HFBR-1414	HFBR-2416	2.87kΩ
1300nm	HFBR-1312T	HFBR-2316T	2.32kΩ

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PHYSICAL DIMENSIONS inches (millimeters)

Package: Q52
52-Pin PLCC

0.785 - 0.795
(19.94 - 20.19)

0.750 - 0.754
(19.05 - 19.15)

1

PIN 1 ID

0.042 - 0.048
(1.07 - 1.22)

14

40

0.750 - 0.754
(19.05 - 19.15)

0.785 - 0.795
(19.94 - 20.19)

27

0.050 BSC
(1.27 BSC)

0.042 - 0.056
(1.07 - 1.42)

0.025 - 0.045
(0.63 - 1.14)
(RADIUS)

0.600 BSC
(15.24 BSC)

0.690 - 0.730
(17.53 - 18.54)

0.009 - 0.011
(0.23 - 0.28)

0.100 - 0.110
(2.54 - 2.79)

0.026 - 0.032
(0.66 - 0.81)

0.165 - 0.180
(4.06 - 4.57)

0.148 - 0.156
(3.76 - 3.96)

0.013 - 0.021
(0.33 - 0.53)

SEATING PLANE

Package: H64-10
64-Pin (10 x 10 x 1mm) TQFP

0.472 BSC
(12.00 BSC)

0.394 BSC
(10.00 BSC)

49

1

PIN 1 ID

0.394 BSC
(10.00 BSC)

0.472 BSC
(12.00 BSC)

33

17

0.020 BSC
(0.50 BSC)

0.007 - 0.011
(0.17 - 0.27)

0° - 8°

0.003 - 0.008
(0.09 - 0.20)

0.018 - 0.030
(0.45 - 0.75)

SEATING PLANE

0.048 MAX
(1.20 MAX)

0.037 - 0.041
(0.95 - 1.05)

Micro Linear

15

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6696CH (Obsolete)	0°C to 70°C	64-Pin TQFP (H64-10)
ML6696CQ	0°C to 70°C	52-Pin PLCC (Q52)

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