MICRO NETWORKS

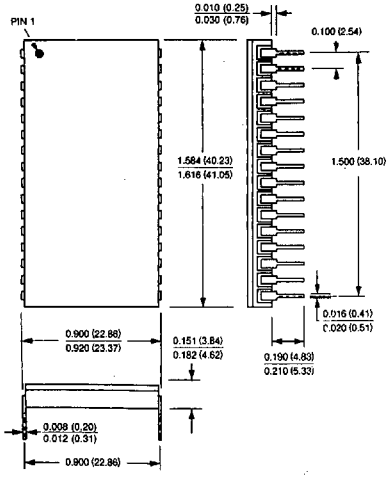
MN5284 Series

LOW-POWER
16-Bit
A/D CONVERTERS

FEATURES

- 16-Bit Resolution
- 15-Bit No Missing Codes
- 300mW Max Power Consumption
- 50μsec Max Conversion Time
- Serial and Parallel Outputs
- True-TTL and 5V-CMOS Compatible
- Small 32-Pin Side-Brazed DIP
- ±12V to ±15V Power Supply Range
- 8 User-Selectable Input Voltage Ranges

32 PIN SIDE-BRAZED DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

An outstanding combination of resolution, speed, packaging, power consumption and price may make the MN5284 Series the best high-resolution A/D converters ever put in dual-in-line packages. Featuring 16-bit resolution and a maximum 50μsec conversion time, MN5284 Series A/D's are packaged in 32-pin, side-brazed, ceramic DIP's and have an impressively low 300mW maximum power consumption when operating from ±15V and +5V supplies. ±12V supplies may also be used.

These are successive approximation type A/D's fabricated in thin-film hybrid technology. Each employs a recently developed HCT CMOS successive approximation register and a proprietary, low-power, partially segmented, bipolar DAC that is inherently monotonic. "No missing codes" to the 15-bit level and true integral linearity to the 14-bit level are guaranteed over the device's entire 0°C to +70°C specified temperature range.

Each A/D is complete with internal reference and clock and is truely compatible with either TTL or 5V-CMOS logic families. Digital input currents are specified at ±10μA max, and fanout is 2 standard TTL loads.

Originally designed for remote, lightweight, battery-operated data acquisition applications, MN5284 Series devices are extremely versatile. Their 50μsec max conversion time permits 167kHz data throughputs when used with Micro Networks MN373, High-Resolution Track-Hold Amplifier (10μsec max acquisition time to ±0.003%, 300mW power consumption). Serial and parallel data outputs and optional CSB, COB and CTC output coding permit various data transmission and processing schemes, and devices may be short cycled to any resolution with a proportionately faster conversion time. Four part numbers in the Series offer the input voltage ranges shown below.

Part Number	Unipolar Input Range	Bipolar Input Range	LSB@ 14-Bits	LSB@ 16-Bits
MN5284	0 to −20V	±10V	1.22mV	305.2μV
MN5285	0 to −16.384V	±8.192V	1mV	250μV
MN5286	0 to −10V	±5V	0.61mV	152.6μV
MN5287	0 to −8.192V	±4.096V	0.5mV	125μV

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MN5284 SERIES LOW-POWER 16-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5284, 85, 86, 87	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 30)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 31)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 17)	−0.5 to +7 Volts
Analog Input (Pin 25)	Nominal ±5Volts
Digital Inputs (Pins 22, 24)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— MN528X
Select desired input voltage range. ———

SPECIFICATIONS (T_A = +25°C, ±V_{cc} = ±15V, +V_{dd} = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges (Note 1): Unipolar (MN5284, 85, 86, 87)		0 to −20, −16.384, −10, −8.192		Volts
Bipolar (MN5284, 85, 86, 87)		±10, ±8.192, ±5, ±4.096		Volts
Input Impedance: 0 to −20V, ±10V (MN5284)		20		kΩ
0 to −16.384V, ±8.192V (MN5285)		16.384		kΩ
0 to −10V, ±5V (MN5286)		10		kΩ
0 to −8.192V, ±4.096V (MN5287)		8.192		kΩ
DIGITAL INPUTS				
Logic Levels (Note 2): Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents (V_{IH} = +5V, V_{IL} = 0V, Note 2)			±10	μA
Start Convert Command Positive Pulse Width (Note 3)	1			μsec
TRANSFER CHARACTERISTICS (Note 4)				
Resolution		16		Bits
Integral Linearity Error (Note 5): Initial (+25°C)		±0.0015	±0.003	%FSR
Over Temperature (Note 6)			±0.003	%FSR
Differential Linearity Error: Initial (+25°C)		±0.0015	±0.003	%FSR
Over Temperature (Note 6)			±0.006	%FSR
Temperature Range for Guaranteed 15-Bit No Missing Codes MN5284, 85, 86, 87	0		+70	°C
Full Scale Absolute Accuracy Error (Note 7):				
Unipolar: Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 6)		±0.1	±0.2	%FSR
Bipolar: Initial (+25°C)		±0.05	±0.15	%FSR
Over Temperature (Note 6)		±0.1	±0.25	%FSR
Unipolar Offset Error (Notes 8, 9): Initial (+25°C)		±0.025	±0.1	%FSR
Over Temperature (Note 6)		±0.05	±0.15	%FSR
Drift		±2		ppm of FSR/°C
Bipolar Zero Error (Notes 8, 10): Initial (+25°C)		±0.05	±0.12	%FSR
Over Temperature (Note 6)		±0.1	±0.2	%FSR
Drift		±5		ppm of FSR/°C
Gain Error (Notes 8, 11): Initial (+25°C)		±0.05	±0.1	%
Over Temperature (Note 6)		±0.1	±0.2	%
Drift		±5	±15	ppm/°C
DIGITAL OUTPUTS				
Logic Levels (Note 2): Logic "1" ($I_{SOURCE} \leq 400\mu A$)	+3.5			Volts
Logic "0" ($I_{SINK} \leq 3.2mA$)			+0.4	Volts
Output Coding (Note 12): Unipolar Ranges		CSB		
Bipolar Ranges		COB, CTC		
REFERENCE OUTPUT				
Internal Reference: Voltage		−9.000		Volts
Accuracy		±0.025	±0.05	%
Tempco		±5		ppm/°C
External Current			1	mA

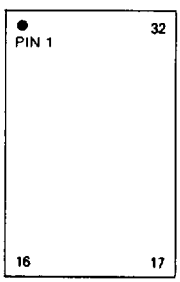
DYNAMIC CHARACTERISTICS (Note 13)	MIN.	TYP.	MAX.	UNITS
Conversion Time (16 Bits) (Note 14)		45	50	μsec
Internal Clock Frequency	320			kHz
Delay Falling Edge of Start to: Status = "1" Clock Output = "1"		75 40	150 80	nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status)		35	70	nsec
Delay LSB valid to Falling Edge of Status	40			nsec
POWER SUPPLIES				
Power Supply Range (Note 15): $\pm V_{cc}$ Supply $+V_{dd}$ Supply	±11.4 +4.75	± 15 + 5	± 16 + 5.25	Volts Volts
Power Supply Rejection: + Vcc Supply − Vcc Supply + Vdd Supply		± 0.001 ± 0.001 ± 0.001		%FSR/% Supply %FSR/% Supply %FSR/% Supply
Current Drains: + Vcc Supply − Vcc Supply + Vdd Supply		9 −5 9		mA mA mA
Power Consumption (± Vcc = ± 15V)		255	300	mW

SPECIFICATION NOTES:

1. 0 to − 16.384V and ± 8.192V input ranges correspond to 1 LSB = 1mV for 14 bits or 1 LSB = ¼mV for 16 bits. 0 to −8.192V and ± 4.096V input ranges correspond to 1 LSB = ½mV for 14 bits and 1 LSB = ⅛mV for 16 bits.
2. Digital portions of MN5284 Series A/D's are implemented with HCT CMOS logic and devices are true TTL and 5V CMOS compatible with specified logic levels and currents guaranteed over each devices entire specified temperature range.
3. Conversion is initiated on falling edge of Start Convert command; see timing diagram.
4. FSR = full scale range. A unit connected for 0 to + 10V or ± 5V operation has a 10V FSR. A ± 10V unit has a 20V FSR. A ± 8.192V unit has a 16.38V FSR etc. 1 LSB for 16 bits is equivalent to 0.00153% FSR, 1 LSB for 15 bits is equivalent to 0.00305% FSR.
5. ±0.003% FSR is equivalent to ± ½ LSB for 14 bits. ±0.0015% FSR is equivalent to ± ½ LSB for 15 bits.
6. Listed specifications apply over the 0°C to +70°C temperature range for standard products.
7. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. It refers to negative full scale accuracy for unipolar ranges and to both positive and negative full scale accuracies for bipolar ranges.
8. Initial offset and gain errors are adjustable to zero with optional external potentiometers or voltage output D/A converters.
9. Unipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 digital output code transition occurs when operating on a unipolar input range.
10. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 1000 0000 0000 0000 to 0111 1111 1111 1111 digital output code transition occurs when operating on a bipolar input range.
11. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from all 1111 1111 1111 1111 to 1111 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0000 0001 to 0000 0000 0000 0000.
12. CSB = complementary straight binary. COB = complementary offset binary. For bipolar ranges, complementary two's complement (CTC) coding is available if the MSB output is used.
13. Listed dynamic specifications are guaranteed over each device's entire specified temperature range.
14. Conversion time is defined as the width of the Status (End of conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 15 (Bit 15), for example, to pin 24 (Short Cycle) for 14-bit conversions.
15. For operation with $\pm V_{cc}$ supplies below ±12V, only 0 to -8.192V, ±8.192V, ±5V and ±4.096V input ranges should be used.

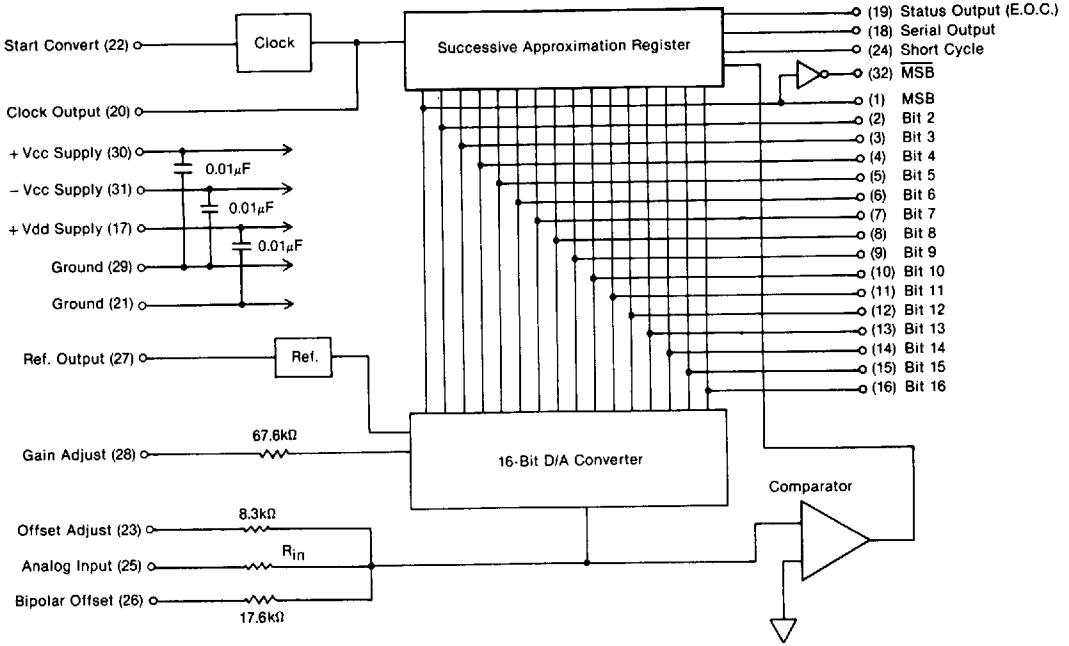
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	Bit 1 (MSB)	32	$\overline{\text{Bit 1 (MSB)}}$
2	Bit 2	31	− Vcc Supply (− 12V/ − 15V)
3	Bit 3	30	+ Vcc Supply (+ 12V/ + 15V)
4	Bit 4	29	Ground
5	Bit 5	28	Gain Adjust
6	Bit 6	27	Reference Output (− 9.0V)
7	Bit 7	26	Bipolar Offset
8	Bit 8	25	Analog Input
9	Bit 9	24	Short Cycle
10	Bit 10	23	Offset Adjust
11	Bit 11	22	Start Convert
12	Bit 12	21	Ground
13	Bit 13	20	Clock Output
14	Bit 14	19	Status Output (E.O.C.)
15	Bit 15	18	Serial Output
16	Bit 16 (LSB)	17	+ Vdd Supply (+ 5V)

BLOCK DIAGRAM



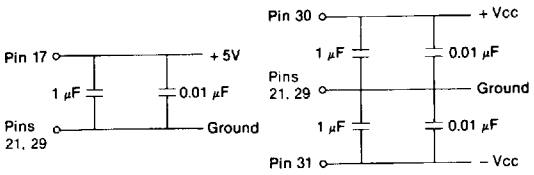
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified linearity and accuracy from MN5284 Series devices. It is critically important that power supplies be filtered, well-regulated, and free from high frequency noise. Use of noisy supplies can easily cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit or better accuracy unless great care is used in filtering any switching spikes present in the output.

MN5284's two ground pins (pins 21 and 29) are not connected to each other internal to the device. It is recommended, however, that the two pins be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large, low-impedance, analog ground plane beneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Power supply connections should be short and direct, and even though MN5284 has internal 0.01μF ceramic bypass capacitors, it is recommended that all power supplies be decoupled with additional high-frequency bypass capacitors to ground. For optimum performance and noise rejection, 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space. If the recommended ground-plane approach can not be used and separate p.c. card ground runs are used, the ±Vcc supplies should be decoupled to pin 29 and the +Vdd supply to pin 21.

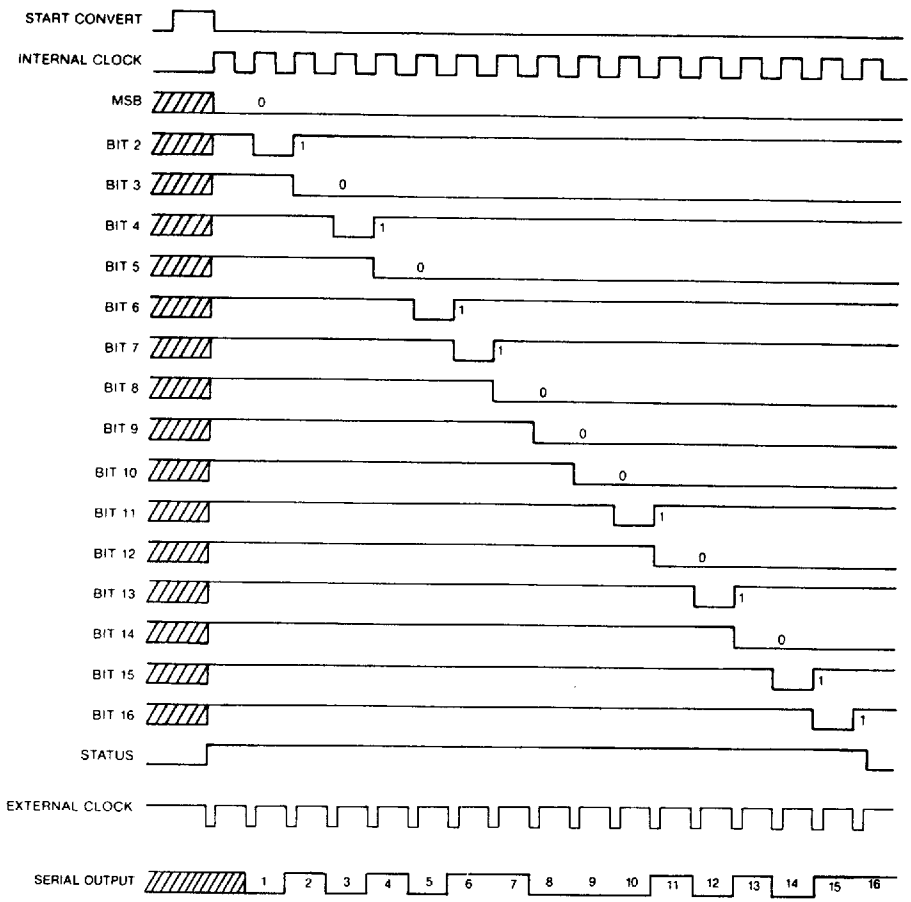
POWER SUPPLY DECOUPLING



Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 23 (Offset Adjust), 25 (Analog Input), 26 (Bipolar Offset), 27 (Reference Output), and 28 (Gain Adjust) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing these pins. Input signal lines should be as short as possible. In bipolar operation, where pin 26 is connected to pin 27, a short jumper should be used. When using external offset and gain adjustments, the adjusting pots or voltage-output DAC's should be located as close to MN5284 as possible. If using optional gain adjust, an 0.01μF ceramic capacitor should be connected between pin 28 and analog ground as close to the package as possible. Similarly, if using the Reference Output (pin 27) to drive an external load or to operate MN5284 in a bipolar mode, an 0.01μF ceramic capacitor should be connected between pin 27 and analog ground.

If short-cycling is not used, the Short-Cycle pin (pin 24) must be connected to +5V (pin 17).

TIMING DIAGRAM



SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise specified)

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (16 Bits)		45	50	µsec
Internal Clock Frequency	320			kHz
Start Convert Positive Pulse Width	1			µsec
Delay Falling Edge of Start to: Status = "1" Clock Output = "1"		75 40	150 80	nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status)		35	70	nsec
Delay LSB valid to Falling Edge of Status	40			nsec

TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command must be at least 1µsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. Output data will be valid 40nsec (minimum) prior to the falling edge of Status (E.O.C.) and will remain valid until another conversion is initiated.
5. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following Status going low at the end of the previous conversion. See External Clock.
6. Once a conversion has begun, a second start pulse will not reset the converter. See Start Convert.
7. When the converter is initially "powered up", it may come on at any point in the conversion cycle.
8. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 15 (Bit 15) to pin 24 (Short Cycle) for 14 bit conversions.

START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 1μsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

DESCRIPTION OF OPERATION — See Block Diagram. The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the analog-to-digital converter (A/D) and the digital drive for the A/D's internal digital-to-analog converter (D/A). The falling edge of a start convert pulse applied to pin 22 turns on the A/D's internal clock and resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status Output (pin 19) is set to logic "1" (see Timing Diagram). The Start Convert must now remain low for the conversion to continue.

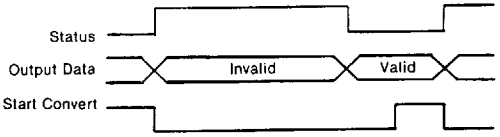
The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has gone low, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 16) also drops the Status Output to a "0" signaling that the conversion is complete and turning off the internal clock. Output data is now valid and will remain so until another conversion is started.

SHORT CYCLING — For applications requiring less than 16 bits resolution, MN5284 Series A/D's can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle pin (pin 24). For example, to truncate at 14 bits, connect pin 15 (Bit 15) to pin 24; converting will stop and the Status output will go low after bit 14 has been set. Bit 14 (the LSB for a 14-bit conversion) will be valid approximately 40nsec prior to the falling edge of status.

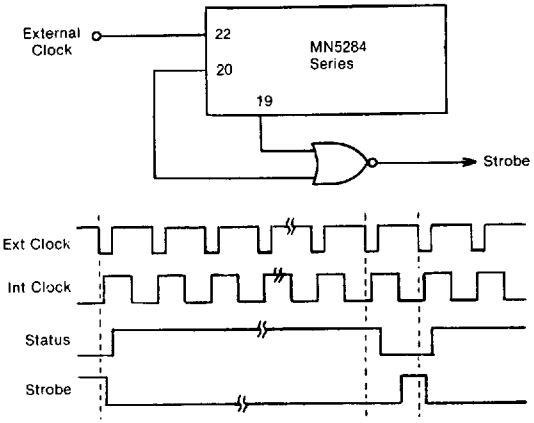
EXTERNAL CLOCK — An external clock may be connected to the Start Convert input. This external clock must consist of negative-going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 17 clock cycles. The internal clock will be disabled whenever the Start Convert input is held high. When using an external clock, a Start Convert command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after the Status output has gone low signaling the end of the previous conversion. When continuously converting in this manner, the Status output will go low for one external clock period following the completion of each conversion.

SERIAL OUTPUT — Serial data is available only during the conversion process. Format is NRZ with the MSB occuring first. Serial data is coded the same as parallel output data, and it is synchronous with the internal clock as shown in the timing diagram. Each data bit becomes valid no longer than 70nsec after each rising clock edge and remains valid for the full clock period. Therefore, falling clock edges can be used to strobe serial data into output registers.

STATUS OUTPUT — The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert signal; will remain high during conversion; and will drop to a logic "0" when conversion is complete. There is a minimum 40nsec delay between the point at which the LSB becomes valid (is set to its final value) and the status output falls to a "0". If an external latch is used to clock output data away from the MN5284, this 40nsec may or may not be long enough to satisfy the set-up time requirement of the latch. If it is not, additional delay will have to be generated. Simple gate delays can be employed or the latch can be controlled by the leading edge of the next start convert pulse. Recall that existing output data does not become invalid until the falling edge of the start pulse. See diagram below.



If continuously converting with an external clock, the Status output can be NORed with the internal clock output, as shown below, to produce a positive strobe pulse approximately ½ period wide, approximately ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion. Recall that the falling edges of the external clock pulses generate rising edges of the internal clock and that these two clocks appear 180 degrees out of phase. The delay from the rising edge of the internal clock to the rising edge of Status is typically 35nsec. See Timing Diagram and the section labeled External Clock.



INTERNAL REFERENCE — MN5284 Series devices contain an internal, low-drift −9V reference that is laser trimmed to an initial accuracy of ±0.05%. The reference is pinned out on pin 27 and can supply up to 1mA beyond the current required for bipolar operation (pin 27 connected to pin 26). If the external load is expected to vary during converter operation or if the internal reference is to be used to drive external circuitry at elevated temperatures, the reference output should be buffered externally.

DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
Unipolar Ranges	Bipolar Ranges	MSB LSB
0	+ F.S.	0000 0000 0000 0000
− 1 LSB	+ F.S. − 1 LSB	0000 0000 0000 000Ø*
− ½ F.S. + 1 LSB	+ 1 LSB	0111 1111 1111 111Ø*
− ½ F.S.	0	ØØØØ ØØØØ ØØØØ ØØØØ*
− ½ F.S. − 1 LSB	− 1 LSB	1000 0000 0000 000Ø*
− F.S. + 1 LSB	− F.S. + 1 LSB	1111 1111 1111 111Ø*
− F.S.	− F.S.	1111 1111 1111 1111

Part Number	Unipolar Input Range	Bipolar Input Range	LSB VALUE	
			16-Bits	14-Bits
MN5284	0 to − 20V	± 10V	305.2μV	1.22mV
MN5285	0 to − 16.384V	± 8.192V	250μV	1mV
MN5286	0 to − 10V	± 5V	152.6μV	0.61mV
MN5287	0 to − 8.192V	± 4.096V	125μV	0.5mV

CODING NOTES:

1. For unipolar ranges, the coding is complementary straight binary.
2. For bipolar ranges, the coding is complementary offset binary.
3. For bipolar ranges, if $\overline{MSB}$ is used instead of MSB, the coding will be complementary two's complement.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5284 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the ± 10V range, the transition from output code 0000 0000 0000 0000 to output code 0000 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of + 9.999695V (+ F.S. − 1 LSB). Subsequently, any voltage greater than + 9.999695V will give a digital output of all "0's". The transition from digital output 1000 0000 0000 0000 to 0111 1111 1111 1111 (or vice versa) will ideally occur at an input of zero volts. The 1111 1111 1111 1111 to 1111 1111 1111 1110 transition will occur at − 9.999695V. An input more negative than this level will give all "1's".

INPUT RANGE SELECTION — MN5284 Series A/D's have an internal, current-output, 16-bit D/A converter that is complementary coded and sources current at its output. Consequently, MN5284 Series A/D's are complementary coded and have unipolar input ranges that are negative (0 to − 20V, 0 to − 16.384V, etc.). Each device in the Series has one unipolar and one bipolar input voltage range. Unipolar ranges are selected by leaving pin 26 (Bipolar offset) open; bipolar ranges are selected by connecting pin 26 (Bipolar offset) to pin 7 (Reference Output).

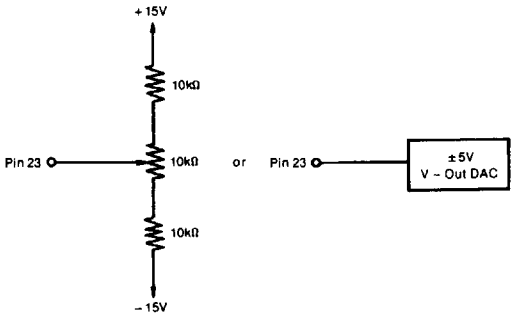
Making the bipolar-offset connection pulls a constant current from the comparator summing junction and has the effect of offsetting the device transfer function "upward" an amount equal to ½ of its full scale range (FSR). Recall that the traditional definition of unipolar offset error for a successive approximation A/D is the input-output accuracy error that occurs when the internal D/A is turned "off" or sourcing zero current (see the tutorial section of the Micro Networks catalog for details) and that for MN5284 type A/D's operating on their unipolar input range, this error occurs around zero volts (the all "0's" digital output). If one were performing optional unipolar offset adjustment, it would be done at this point. Note that making the bipolar-offset connection effectively moves this point "upward" to + ½FSR (equivalent to the positive full scale point on the bipolar input range). Now, at least according to traditional definitions, the point at which bipolar offset error occurs is the positive full scale point (still the all "0's" digital output), and if one were performing optional bipolar-offset adjustment, it would be done at this point.

To avoid potential confusion, Micro Networks does not specify bipolar offset error for MN5284 Series A/D's. We specify unipolar offset error and unipolar negative full scale accuracy (Full Scale Absolute Accuracy Error) for unipolar input ranges, and for bipolar input ranges, we specify positive and negative full scale accuracy as well as a bipolar zero error (around the zero-volt input point).

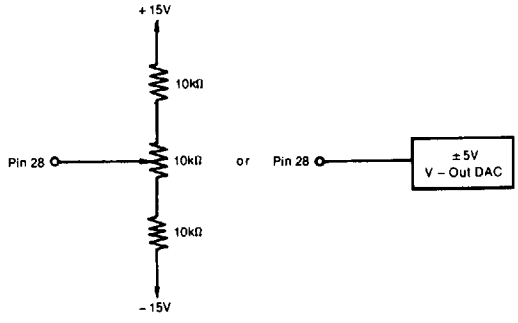
OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS — Initial offset and gain errors may be trimmed to zero using external potentiometers or voltage output DAC's as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, offset should be adjusted before gain. The gain and offset adjust points (pins 28 and 23) are purely resistive and are specifically designed to be driven with applied voltages ranging from + 5V to − 5V. Adjusting voltages can be generated by tying potentiometers to the supplies or, in microprocessor based applications, by using voltage output DAC's. If potentiometers are used, they should be multiturn devices with TCR's of 100ppm/°C or less. Fixed resistors can be ± 20% carbon composition or better. If these adjustments are not used, pin 23 should be left open and pin 28 should be decoupled to ground with a 0.01μF ceramic capacitor.

OFFSET ADJUSTMENT—Connect the offset potentiometer to pin 23 as shown. For unipolar ranges, apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "0" and the LSB "flickers" on and off. For bipolar ranges, apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "flickering". The offset adjust sensitivity is approximately ±0.04% FSR/Volt, and the total range of offset adjust, using the applied voltages of ±5V, is ±0.2% FSR.

GAIN ADJUSTMENT — Connect the gain potentiometer to pin 28 as shown, and apply the input voltage at which the 1111 1111 1111 1111 to 1111 1111 1111 1110 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off. The gain-adjust sensitivity is approximately ±0.08%/Volt, and the total range of gain adjust, using applied voltages of ±5V, is ±0.4%.



OFFSET ADJUST



GAIN ADJUST

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