Product Preview

MC13180PP/D
Rev. 2, 08/2002

2.4 GHz Low Power Wireless Transceiver IC for Bluetooth™ Applications

MOTOROLA
intelligence everywhere™

digital dna™

MC13180

Package Information
Plastic Package
Case 1314
(QFN-48)

Ordering Information

Device	Marking	Package
PC13180FC	PC13180FC	QFN-48

The MC13180 2.4 GHz Low Power Wireless Transceiver for Bluetooth™ is a part of the comprehensive Bluetooth platform from Motorola that provides a complete, low-power Bluetooth Radio System for Bluetooth Class 1 or 2 power systems. The design is based on Motorola's third-generation Bluetooth architecture that has set the industry standard for interoperability, complete functionality, and compliance with the Bluetooth specification. When combined with a specified Motorola baseband controller such as the MC71000 or MC9328MX1, a complete Bluetooth solution can be realized.

The MC13180 provides a unique combination of sensitivity, excellent C/I performance, and low power consumption. These performance parameters are extremely important to maintaining a robust link in high RF interference environments such as mobile phones, high density Bluetooth networks, 802.11b networks, microwave ovens, etc.

- Power Supply Range: 2.5 to 3.1 V
- Low Current Drain in Transmit (27 mA Peak) or Receive (37 mA Peak) Mode
- Minimum External Components
- Low IF Receiver with On-Chip Filters
- Fully Integrated Demodulator with A/D
- Direct Launch Transmitter
- Multi-Accumulator, Dual-Port, Fractional-N Synthesizer
- RSSI with A/D
- Bluetooth Class I Compatible
- Crystal Independent (12 to 15 MHz) Reference Oscillator or 12 to 26 MHz if supplied externally

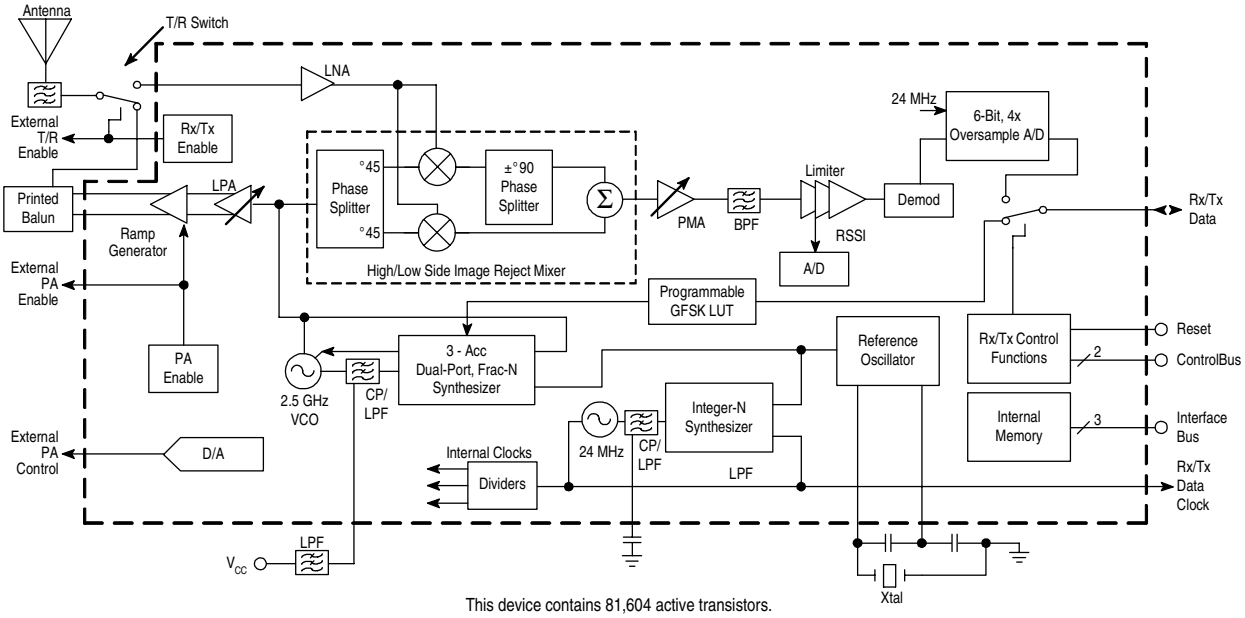


Figure 1. Simplified Block Diagram

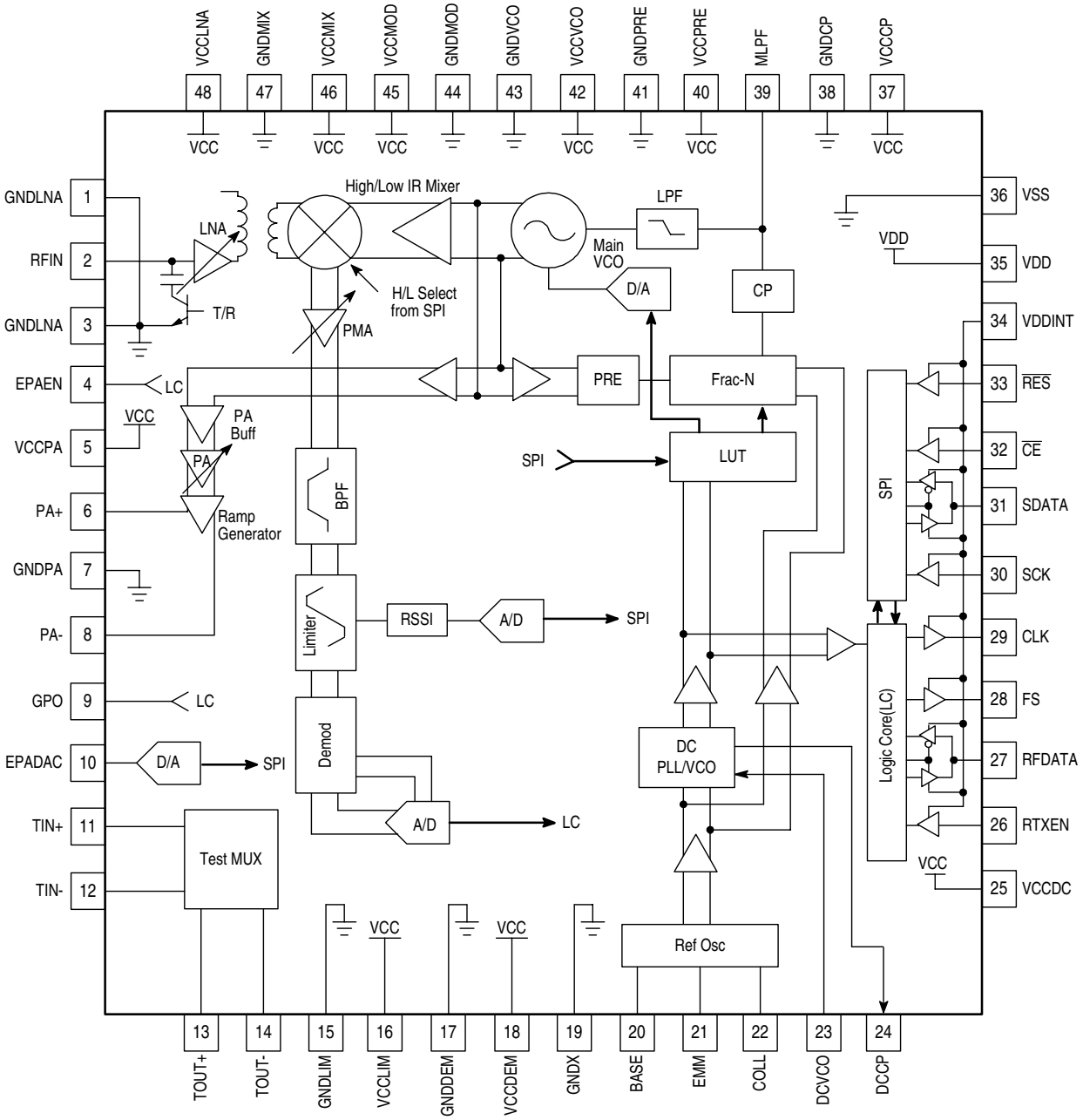


Figure 2. Device Pinout

1 Electrical Characteristics

Table 1. Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage V_{CC}RF V_{DDINT}		 3.2 3.2	V
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-60 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.
2. Meets Human Body Model (HBM) ≤2.0 kV and Machine Model (MM) ≤200 V except RF & I/O Pins = 50 V MM, RF Pins = 100 V HBM, and I/O Pins <500 V. RF pins have no ESD protection. Additional ESD data available upon request.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}RF	2.5	2.7	3.1	Vdc
Power Supply Voltage, Logic Interface ($V_{DDINT} \leq V_{CC}$RF)	V_{DDINT}	1.65	-	V_{CC}RF	Vdc
Input Frequency	f_{in}	2.4	-	2.5	GHz
Ambient Temperature Range	T_A	-20	25	85	°C
Ref Osc Frequency Range (only integral multiples of 20 kHz may be used) With Crystal External Source	f_{ref}	 12 12	 13 -	 15 26	MHz

Table 3. Digital DC Electrical Specifications

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, TA = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults in Figure 4, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN, V_{in} = 0 V or 1.8 V $\overline{RES}$, V_{in} = 0 V (Reset Mode) $\overline{RES}$, V_{in} = 1.8 V (Idle Mode)	I_{CCINT}	 - -	 0.2 0.5	 2.0 3.0	 µA mA
Radio Power Supply Current, Sleep Mode	$I_{CCRFsleep}$	-	2.0	10	µA
Radio Power Supply Current, Idle Mode	$I_{CCRFidle}$	-	3.4	4.0	mA

Table 3. Digital DC Electrical Specifications (Continued)

($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, TA = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults in Figure 4, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Radio Power Supply Current Transmit, 1 Slot Transmit, 3 Slot Transmit, 5 Slot Transmit, Continuous	 $I_{CCRFtx1}$ $I_{CCRFtx3}$ $I_{CCRFtx5}$ $I_{CCRFtxc}$	 - - - -	 22 25 26 27	 - - - 33	mA
Radio Power Supply Current Receive, 1 Slot Receive, 3 Slot Receive, 5 Slot Receive, Continuous	 $I_{CCRFrx1}$ $I_{CCRFrx3}$ $I_{CCRFrx5}$ $I_{CCRFrxc}$	 - - - -	 30 34 35 37	 - - - 47.5	mA
Output Voltage Low SDATA, CLK, FS, RFDATA ILoad = 0 µA ILoad = 100 µA	V_{OL}	 - -	 20 -	 - 0.2 x V_{DDINT}	 mV V
Output Voltage High SDATA, CLK, FS, RFDATA ILoad = 0 µA ILoad = 100 µA	V_{OH}	 - 0.8 x V_{DDINT}	 1.78 -	 - -	V
Output Voltage Low EPAEN, GPO ILoad = 0 µA ILoad = 100 µA	V_{OL}	 - -	 20 -	 - 0.2 x $V_{CC}RF$	 mV V
Output Voltage High EPAEN, GPO ILoad = 0 µA ILoad = 100 µA	V_{OH}	 - 0.8 x $V_{CC}RF$	 2.68 -	 - -	V
Input Voltage Low $\overline{RES}$, $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN	V_{IL}	-	0	0.3 x V_{DDINT}	V
Input Voltage High $\overline{RES}$, $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN	V_{IH}	0.7 x V_{DDINT}	V_{DDINT}	-	V
Input Current $\overline{RES}$, $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN, Vin = 0 V or 1.8 V	I_{in}	-	±1.0	-	µA

Table 4. EPA DAC Electrical Specifications

($V_{CC}RF$ = 3.1 Vdc, V_{DDINT} = 1.8 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults in Figure 4 except R11/7 = 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage EPADAC, ILoad = ±100 µA PADAC = 000000 PADAC = 100000 PADAC = 111111	V_{out}	 - - 2.5	 0.02 1.60 3.08	 0.4 - -	V
Resolution	RESOL	-	6	-	Bits
Linearity	INL/DNL	-	±1.0	±2.0	LSB
Average Supply Current (1-slot packet)	I_{CCDAC}	-	197	500	µA

Table 5. Digital AC Electrical Specifications

($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults in Figure 4, unless otherwise noted. See Figure 3 Test Circuit and Figure 12 Timing Diagram.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay, RTXEN to FS, receive mode	T_{propFS}	-	168	-	µs
Receiver Latency, LNA In to RFDATA, receive mode	R_XLAT	-	1.0	-	µs
Receive Disable Time	T_{RXDIS}	-	0	-	µs
Strobe Delay, RTXEN to RFDATA, transmit mode	T_{stb}	-	TXsync + 0.5	-	µs
Transmit Sync Delay (i.e., R8/15-8)	TXsync	182	184	192	µs
Hold Time, RTXEN to RFDATA, transmit mode	T_{hold}	-	4.0	-	µs
Transmit Latency, RTXEN to PAout, transmit mode	T_XLAT	-	TXsync + 2.5	-	µs
Transmit Data Rate, Bit transfer rate to RFDATA, transmit mode	T_{Bit}	-	1.0	-	µs
Transmit Disable Time	T_{TXDIS}	-	20	-	µs
CLK Duty Cycle		30	40/60	70	%

Table 6. Receiver AC Electrical Specifications

($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, Desired RF_{in} = 2.441 GHz @ f_{dev} = 157.5 kHz, Interferer f_{dev} = 160 kHz, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Modulating data for desired signal = PRBS9, Modulating data for interfering signal = PRBS15, Measured BER < 0.1%, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, T_A = 25°C, unless otherwise noted. Measurements made from LNA_{in} to Recovered Data out. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specs	Unit
Receiver Sensitivity	$SENS_{min}$					dBm
T_A = 25°C		-	-85			
T_A = -20 to 85°C		-	-80	-75	≤ -70	
Receiver Sensitivity degradation in the presence of a dirty transmitter		-	-1.5	-		dB
Maximum Usable Signal Level	$SENS_{max}$	-20	> 0	-	≥ -20	dBm
Co-Channel Interference @ -60 dBm	C/I co	-	8.0	11	≤ 11	dB
Adjacent Channel Interference						dB
Adjacent (±1 MHz) Interference @ -60 dBm	C/I 1MHz	-	-8.0	0	≤ 0	
Adjacent (±2 MHz) Interference @ -60 dBm	C/I 2MHz	-	-33	-30	≤ -30	
Adjacent (≥3 MHz) Interference @ -67 dBm	C/I ≥3MHz	-	-46	-40	≤ -40	
Image Frequency Interference @ -67 dBm	C/I image	-	-17	-9.0	≤ -9.0	dB
Adjacent Interference to In-Band Image Frequency @ -67 dBm	C/I image ±1	-	-33	-20	≤ -20	dB
Spurious Response Frequencies		-	2	5	5	
Intermodulation Performance [Note 1]		-39	-31	-	≥ -39	dBm
Receiver Spurious Emissions						dBm
30 MHz to 1.0 GHz		-	-70	-57	≤ -57	
1.0 GHz to 12.75 GHz		-	-56	-47	≤ -47	
Receiver Blocking Performance (See Figure 29) [Note 2]						dBm
30 MHz to 2.0 GHz (1.999 GHz)		-25	-9.0	-	≥ -10	
2.0 to 2.399 GHz (2.399 GHz)		-27	-16	-	≥ -27	
2.498 to 3.0 GHz (2.498 GHz)		-27	-16	-	≥ -27	
3.0 to 12.75 GHz (3.001 GHz)		-10	2.0	-	≥ -10	

NOTE: 1. Measured at $f_2 - f_1$ = 5.0 MHz in accordance to Bluetooth specification.
2. As allowed by the Bluetooth Specification, up to 5 exceptions may be taken for spurious response.

Table 6. Receiver AC Electrical Specifications (Continued)

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, Desired RF_{in} = 2.441 GHz @ f_{dev} = 157.5 kHz, Interferer f_{dev} = 160 kHz, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Modulating data for desired signal = PRBS9, Modulating data for interfering signal = PRBS15, Measured BER < 0.1%, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, T_A = 25°C, unless otherwise noted. Measurements made from LNA_{in} to Recovered Data out. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specs	Unit
RSSI Conversion Value, (R4/6 and R9/8 = 1) RF level at LNA input to maintain conversion value of: 1000 1111	RSSI	 -60 -	 -56 -70	 -52 -66		dBm
RSSI Resolution (R4/6 and R9/8 = 1)	$RSSI_{res}$	-	1.8	-		dB/bit
RSSI Dynamic Range		20	-	-		dB
RSSI Average Supply Current (R4/6 and R9/8 = 1)		-	40	-		µA

Table 7. Transmitter AC Electrical Specifications

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, T_A = -20 to 85°C, unless otherwise noted. Measurements made at PA_{out}. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specs	Unit
RF Transmit Output Power T_A = 25°C T_A = 85°C T_A = -20°C	P_{out}	 -3.5 -3.5 -3.5	 1.9 0.1 2.4	 4.0 4.0 4.0	 -6.0 to 4.0 -6.0 to 4.0 -6.0 to 4.0	dBm
-20 dBc Occupied Bandwidth	OccBW	-	930	1000	≤1000	kHz
In-Band Spurious Emissions Adjacent Channel ±2.0 MHz Offset Adjacent Channel ±3.0 MHz Offset Adjacent Channel ≥3.0 MHz Offset	 Inb2 Inb3 Inbg3	 - - -	 -59 -65 -70	 -20 -40 -40	 ≤ -20 ≤ -40 ≤ -40	dBm
In Band Spurious Emission Exceptions	Inbex	-	0	3	≤ 3	
Out of Band Spurious Emissions 30 MHz to 1.0 GHz 1.0 to 12.75 GHz (2nd Harmonic) 1.8 to 1.9 GHz 5.15 to 5.3 GHz	 Outb1 Outb2 Outb3 Outb4	 - - - -	 -57 -19 -58 -56	 -36 -5.0 -47 -47	 ≤ -36 ≤ -30 ≤ -47 ≤ -47	dBm
Peak Frequency Deviation	Dev	140	157.5	175	140 to 175	kHz
Minimum Frequency Deviation	DevMin	11.5	148	-	115	kHz
High vs Low Frequency Modulation Percentage	ModIn	80	93	-	≥ 80	%
Initial Frequency Accuracy	InitFA	-75	±5.0	-75	±75	kHz

Table 7. Transmitter AC Electrical Specifications (Continued)

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, T_A = -20 to 85°C, unless otherwise noted. Measurements made at PA_{out}. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specs	Unit
Transmitter Center Frequency Drift One-slot packet Three-slot packet Five-slot packet	 d1 d3 d5	 -25 -40 -40	 ±3.0 ±6.0 ±6.0	 25 40 40	 ±25 ±40 ±40	kHz
Maximum Frequency Drift	Dmax	-	3.0	20	20	kHz/ 50 µs
PA Output Impedance	S22	See Table 23				dB

Table 8. Receiver AC Electrical Specifications

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, T_A = -20 to 85°C, unless otherwise noted. Measurements made at PA_{out}. See Figure 3 Test Circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Maximum Usable Signal Level, T_A = -20 to 85°C	SENSmax	-	≥ 0	-	dBm
Receiver Blocking Performance, T_A = 25°C W-CDMA 1.8 GHz W-CDMA 2.2 GHz GSM 1.8 GHz	 	 - - -	 -14 -13 -13	 - - -	dBm
Co-Channel Interference @ -60 dBm, T_A = -20 to 85°C	C/I co	-	8.0	-	dB
Adjacent Interference, T_A = 25°C Adjacent (±1 MHz) Interference @ -70 dBm Adjacent (±2 MHz) Interference @ -70 dBm Adjacent (≥3 MHz) Interference @ -77 dBm	 C/I 1MHz C/I 2MHz C/I ≥3MHz	 - - -	 -8.0 -41 -47	 - - -	dB
Image Frequency Interference @ -77 dBm, T_A = 25°C	C/I image	-	-17	-	dB
Adjacent Interference to In-Band Image Frequency @ -77 dBm, T_A = 25°C	C/I image ±1	-	-33	-	dB
LNA Input Impedance	S11	See Tables 20 and 21			dB

Table 9. MC7100/MC13180 Receive Characteristics

($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, Reference Crystal = 13 MHz, Register bit settings according to specified defaults, unless otherwise noted, interfering access code at the minimum Hamming distance of 14 according to Bluetooth specifications. See Figure 3 Test Circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
False Detection Rate					%
In Presence of Noise		-	0	-	
In Presence of Interfering Access Code					
@ Actual Sensitivity		-	0	-	
@ Actual Sensitivity + 10 dB		-	0	-	
Missed Detection Rate					%
@ Actual Sensitivity		-	0	-	
@ Actual Sensitivity + 10 dB		-	0	-	
@ Actual Sensitivity - 16 dB		-	100	-	

Table 10. Reference Oscillator Receive Characteristics

($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal Frequency Range (SeeTable 19 for supported frequencies)	$f_{RefXtal}$	12	-	15	MHz
External Drive Frequency Range (See Table 19 for supported frequencies)	$f_{RefExternal}$	12	-	26	MHz
Oscillator Drive Level					V_{pp}
External Reference		0.2	-	1.0	
Crystal Reference		-	0.8	-	
Crystal Load Capacitance (Resonant Parallel)		-	13	-	pF
Maximum Crystal Equivalent Series Resistance (ESR)		-	-	100	W
Typical Crystal Adjustment Range		-	See Figure 19		
Recommended Crystal Tolerance over Temperature (-20 to 85°C)		-	±10	-	ppm
Electronic Parallel Trim Capacitance Range	C_{PT}	-	0 to 9.3	-	pF
Electronic Parallel Trim Capacitance Resolution		-	0.3	-	pF
Oscillator Bias Current					µA
(R11/0) = 0, (R11/4) = 0 or 1		-	0	-	
(R11/0) = 1, (R11/4) = 0		-	50	-	
(R11/0) = 1, (R11/4) = 1		-	200	-	
Input Impedance at Base (Reference Frequency = 12 to 26 MHz, R11/0 = 0 or 1)					
Parallel Capacitance	C_P	-	1.0 + Parallel Trim Capacitance	-	pF
Parallel Resistance	R_P	-	20	-	kΩ

Table 10. Reference Oscillator Receive Characteristics (Continued)

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Bias Voltage (Base)		-	1.2	-	V
Start-up Time (using Crystal)	T_{WAIT}	-	7.5	-	ms

Table 11. Data Clock Electrical Specifications

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Reference Frequency		-	20	4000	kHz
Data Clock Output Frequency		-	24	-	MHz
R Counter (R6/9-0) (Base 10)		3	650	1023	
N Counter (R7/10-0) (Base 10)		3	1200	2047	
Loop Filter Bandwidth		-	1.0	200	kHz
Phase Detector Gain Constant	K_{pd}	-	15.9	-	µA/rad
VCO Gain Constant	K_{VCO}	-	15	-	MHz/V
Start-up Time External Reference Crystal Reference		 - -	 1.0 7.5	 - -	ms

Table 12. SPI AC Electrical Specifications

(V_{CC}RF = 2.7 Vdc, V_{DDINT} = 1.8 Vdc, T_A = 25°C, unless otherwise noted. See Figure 13 Timing Diagram.)

Characteristic	Symbol	Min	Typ	Max	Unit
$\overline{CE}$ to SCK Setup Time Hold Time	 T_{suCE} T_{HCE}	 - -	 20 20	 - -	ns
SDATA to SCK Setup Time Hold Time	 T_{suD} T_{HD}	 - -	 20 20	 - -	ns
SCK to SDATA Propagation Delay	T_{prop}	-	20	-	ns
SCK Operating Frequency (50% Duty Cycle)	f_{max}	-	-	20	MHz
SPI Setup Time to RTXEN (See Figure 12)	T_{SUSPI}	-	20	-	ns

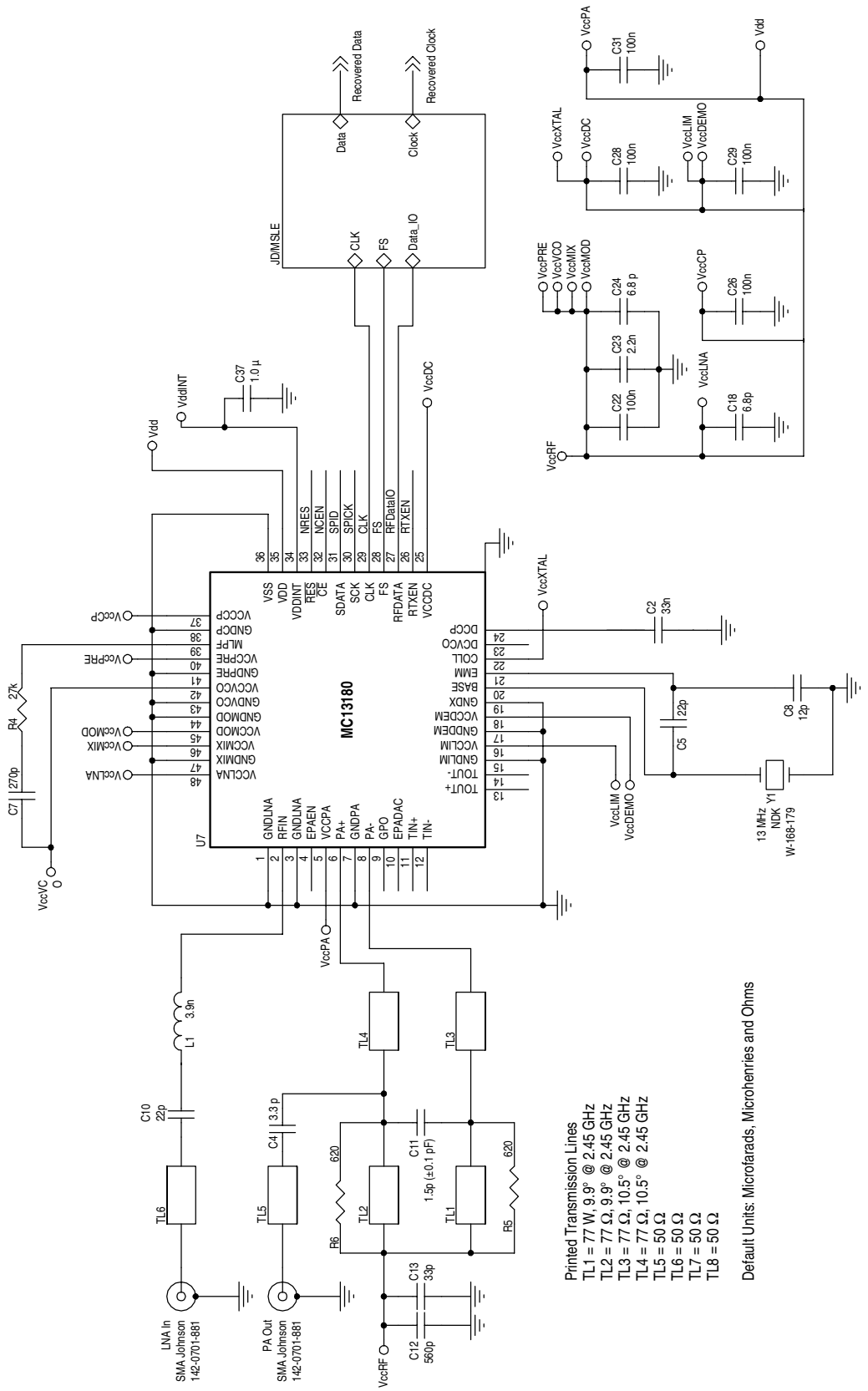


Figure 3. Test Circuit

MC13180:		Byte 1								Byte 0							
Register Address	Register Number	MSB Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
$00 Programmable Reset																	
$01	1	MSB	16 Bit Frac-N Numerator Divide Value - num														LSB
	Rx Test	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1	0
	Tx Test	1	1	0	0	0	0	0	1	1	1	0	1	0	0	1	0
$02	2	Sleep Enable	Tx Enable	Rx Enable	Narrow Bandwidth Enable	High/Low Injection Enable			General Purpose Output	MSB			Frac-N Integer Divide Valu				LSB
	Rx Test	0	0	1	0	1	1	0	1	1	0	1	1	1	0	0	1
	Tx Test	0	1	0	1	0	1	0	1	1	0	1	1	1	0	0	0
$03	3						External PA Enable Invert				General Purpose Output Invert	MSB		PA DAC Setting			LSB
		0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0
$04	4										RSSI Read Enable						
		1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1
$05	5															PA Bias Adjust	
		0	0	1	0	1	0	0	0	1	0	1	1	1	0	1	0
$06	6	External PA Enable = GPO	MSB	Xtal Trim			LSB	MSB		DC Pll R Counter							LSB
		1	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0
$07	7		Dual Port Programmable Delay For Tx PLL				MSB			DC Pll N Counter							LSB
		1	0	0	1	1	1	0	0	1	0	0	1	0	0	1	0
$08	8	MSB	Transmit Synchronization Time Delay Value						LSB	MSB	B-Dual Port Digital Multiplier Value For Tx PLL						LSB
		1	0	1	1	1	0	0	0	0	1	1	0	0	1	0	0
$09	9								RSSI Enable								
		0	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1
$0A	10																
		0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
$0B	11									External PA DAC Enable	External PA Enable		Xtal Boost Enable				Xtal Enable
		1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1
$0C	12	MSB	ROM_r2_c2						LSB	MSB			ROM_r1_c1				LSB
		1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0
$0D	13	MSB	ROM_r2_c4						LSB	MSB			ROM_r2_c3				LSB
		1	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1
$0E	14	MSB	ROM_r3_c2						LSB	MSB			ROM_r3_c1				LSB
		0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	1
$0F	15	MSB	ROM_r3_c4						LSB	MSB			ROM_r3_c3				LSB
		1	0	1	1	0	1	0	0	1	0	1	1	1	0	0	0
$10	16	MSB	ROM_r4_c3						LSB	MSB			ROM_r4_c2				LSB
		1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	0
$11	17	M-Dual Port Digital Multiplier Value for Tx PLL								MSB			ROM_r4_c4				LSB
		0	1	1	0	1	1	0	0	1	0	1	0	1	1	0	1
$12	18																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4. Register Map

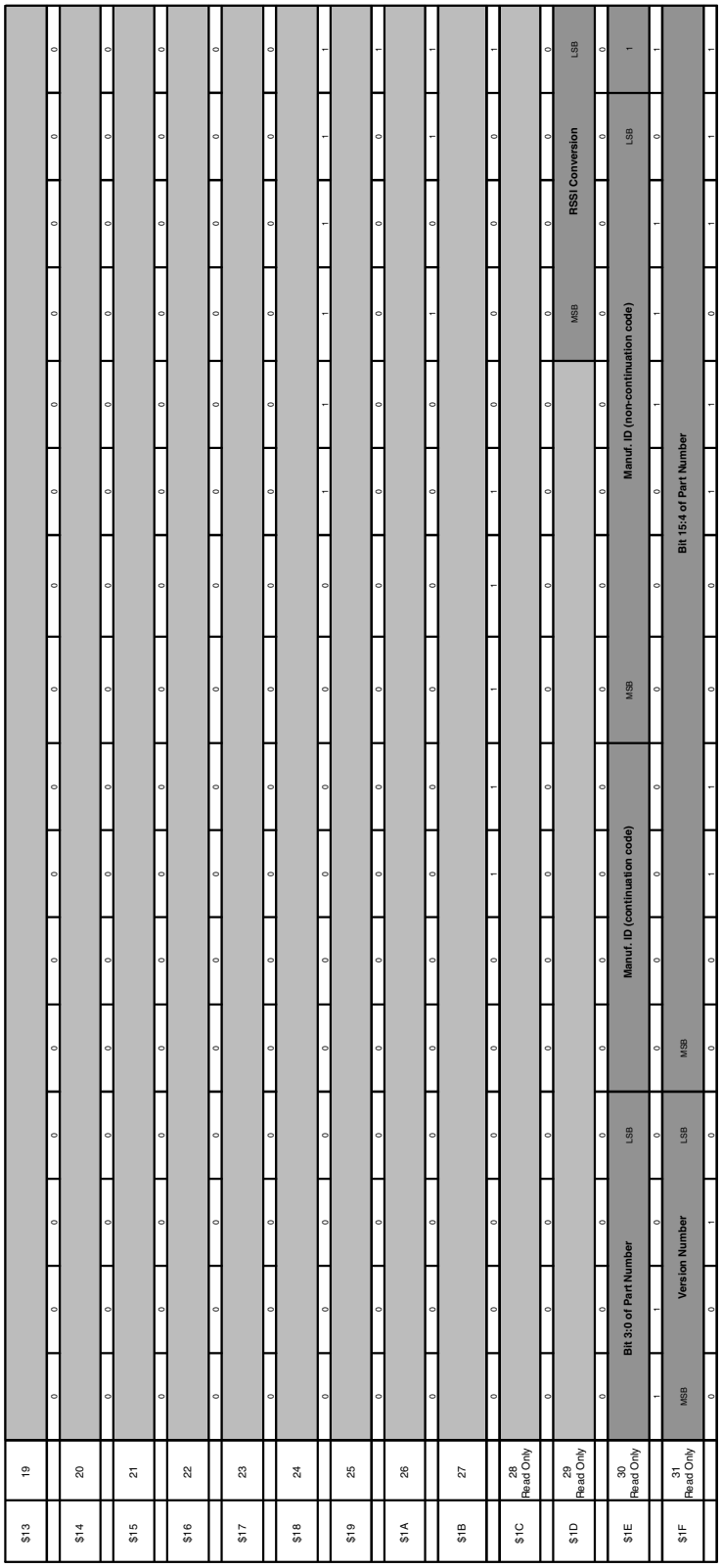
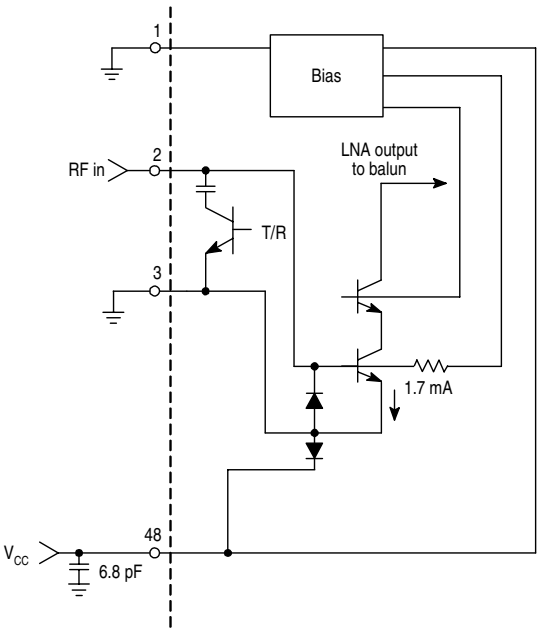
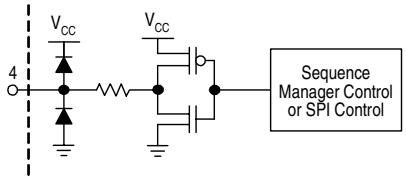


Figure 4 Register Map (continued)

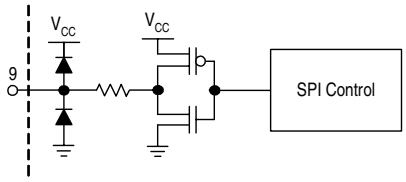
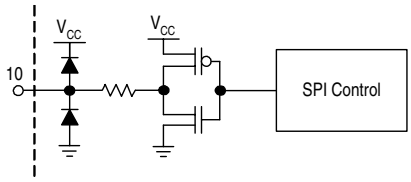
2 Pin Connections

Table 13. Pin Function Description

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
1	GNDLNA		**GNDLNA, Negative supply** GNDLNA is the ground for the LNA.
2	RFIN		**RFIN** RFIN is the RF input to the LNA. The LNA is a bipolar cascode design. The input is the base of the common emitter transistor. Minimum external matching is required to optimize the input return loss and gain. The cascode output drives the primary of an on-chip balun single-ended.
3	GNDLNA		**GNDLNA, Negative supply** GNDLNA is the ground for the LNA.
48	VCCLNA		**VCCLNA, Positive supply** VCCLNA is taken to the incoming positive battery or regulated dc voltage through a low impedance trace on the PCB. It is decoupled to GNDLNA at the pin of the IC.
4	EPAEN		**EPAEN** External PA enable is a digital output which can be used to enable an external PA. It can be controlled via SPI or placed under sequence manager control. This output can also be used to control an external T/R switch requiring complementary drive.

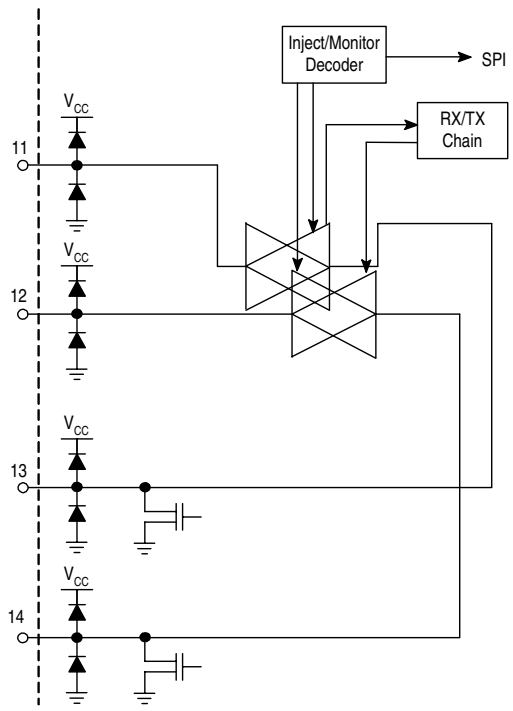
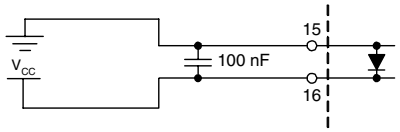
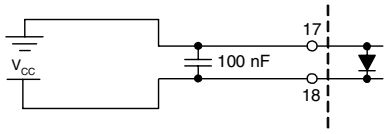
NOTE: $V_{CC} = V_{CC}RF$

Table 13. Pin Function Description (Continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
5	VCCPA	See Figure 5.	**VCCPA, Positive Supply** VCCPA pin is taken to the incoming positive battery or regulated dc voltage through a low impedance trace on the PCB. It is decoupled to GNDPA at the pin of the IC.
7	GNDPA		**GNDPA**, **Negative Supply** GNDPA pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A multi-sided PCB is implemented so that ground returns can be easily made through via holes.
6	PA+		**PA +** Positive differential PA output. An external differential-to-single-ended matching network is desired.
8	PA -		**PA -** Negative differential PA output. An external differential-to-single-ended matching network is desired.
9	GPO		**GPO** The General Purpose Output is a digital output. GPO can be controlled by the SPI. This signal can also be used to control an external T/R Switch.
10	EPADAC		**EPADAC** External PA driver. Analog output ranges from 0.02 to V_{CC}RF - 0.02. The EPADAC is linearly scaled to a maximum V_{CC} of 3.1 V.

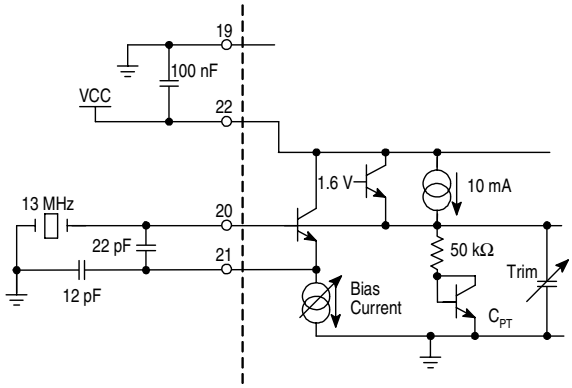
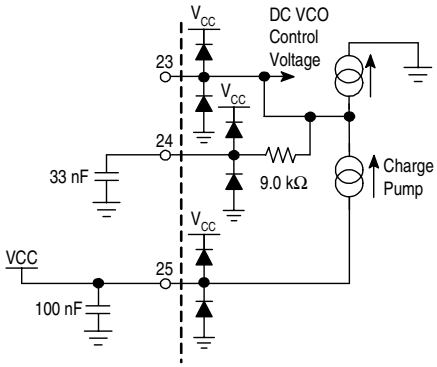
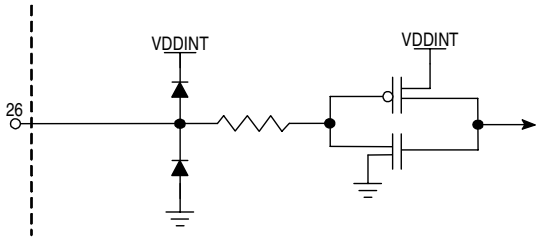
NOTE: $V_{CC} = V_{CC}RF$

Table 13. Pin Function Description (Continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
11	TIN +		**TIN +** This pin is for factory use only. It can be grounded or left open.
12	TIN -		**TIN -** This pin is for factory use only. It can be grounded or left open.
13	TOUT +		**TOUT +** This pin is for factory use only. It must be left open.
14	TOUT -		**TOUT -** This pin is for factory use only. It must be left open.
15	GNDLIM		**GNDLIM, Negative supply** GNDLIM is the ground for limiter.
16	VCCLIM		**VCCLIM, Positive supply** VCCLIM is decoupled to GNDLIM at the pin of the IC.
17	GNDDEM		**GNDDEM, Negative supply** GNDDEM is the ground for demodulator.
18	VCCDEM		**VCCDEM, Positive supply** VCCDEM is decoupled to GNDDEM at the pin of the IC.

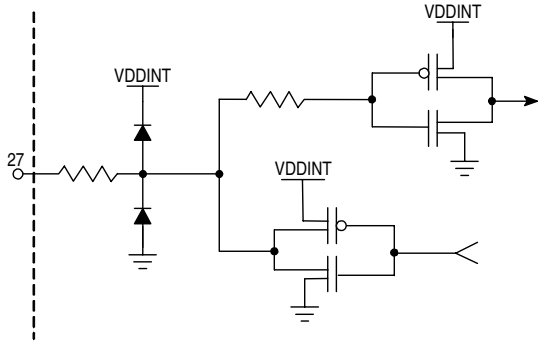
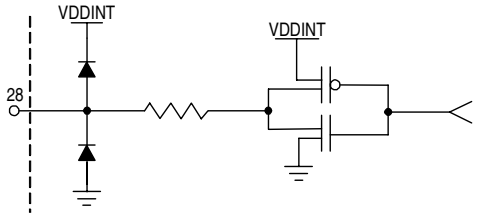
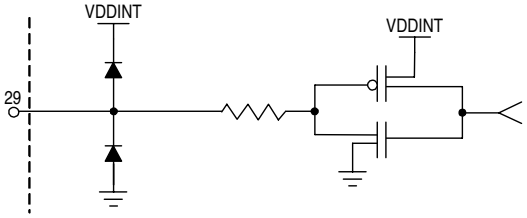
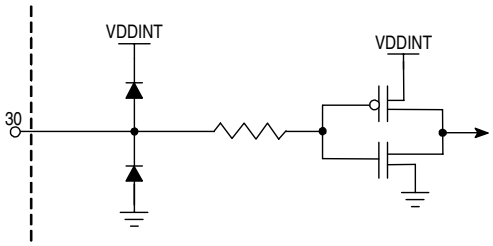
NOTE: $V_{CC} = V_{CC}RF$

Table 13. Pin Function Description (Continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
19	GNDX	 Shown for 13 MHz reference oscillator.	**GNDX** Reference oscillator ground.
20	BASE		**BASE** Reference oscillator base. The base is the reference oscillator input. An on-chip capacitor trim network is also included to allow the user to use relatively inexpensive crystals.
21	EMM		**EMM** Reference oscillator emitter. A bias current of 50 μA is supplied internally to the emitter.
22	COLL		**COLL** Reference oscillator collector. The collector is tied to VCC. The pin of the IC is bypassed to gnd.
23	DCVCO		**DCVCO** Data Clock Loop Filter VCO control voltage. This pin can be used to raise/lower the loop corner frequency in conjunction with the DCCP pin and external components.
24	DCCP		**DCCP** Data Clock Loop Filter charge pump.
25	VCCDC		**VCCDC** Data clock VCC. The pin of the IC is bypassed to gnd.
26	RTXEN		**RTXEN** When RTXEN is asserted (high), it controls the start of the Rx or Tx cycle. Digital input. The logic level is internally shifted to the V_{DD} supply.

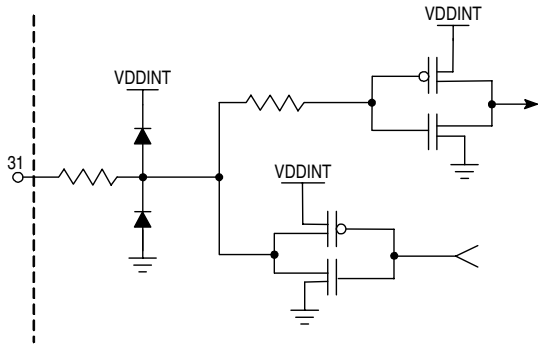
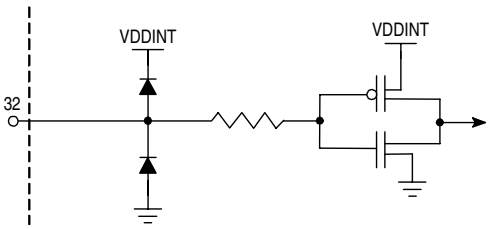
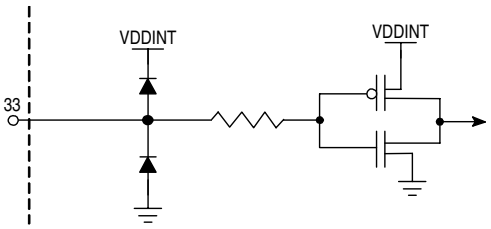
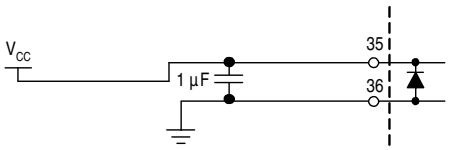
NOTE: $V_{CC} = V_{CC}RF$

Table 13. Pin Function Description (Continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
27	RFDATA		**RFDATA** This digital I/O is used for Transmit Data (input) and Received Data (output). When in transmit mode, the logic level is internally shifted to the V_{DD} supply.
28	FS		**FS** Frame-sync digital output (used for Rx only). In Receive mode, this signal brackets a 6-bit sample frame.
29	CLK		**CLK** Clock associated with RF data path. The Clock Frequency must always be programmed to 24 MHz. Digital output.
30	SCK		**SCK** SPI clock.

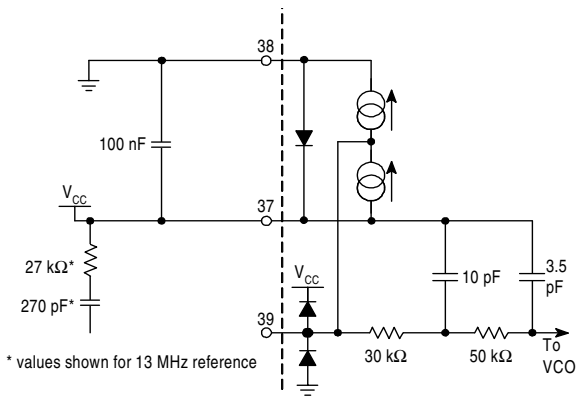
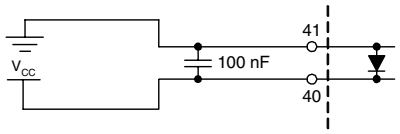
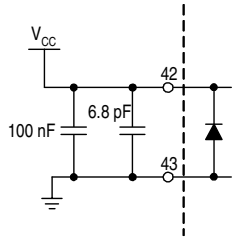
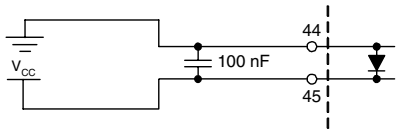
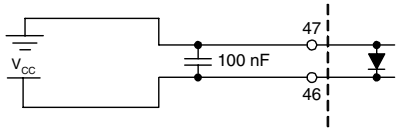
NOTE: $V_{CC} = V_{CC}RF$

Table 13. Pin Function Description (Continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
31	SDATA		**SDATA** SPI data. Digital input or output. As an input, the logic level is internally shifted to V_{DD}.
32	CE		**CE** Chip enable is active low enable to facilitate SPI transfers. Digital input. The logic level is internally shifted to the V_{DD} supply.
33	RES		**RES** Asynchronous Digital Reset (Active Low). Resets MC13180 register settings to a default value. Digital Input. The logic level is internally shifted to the V_{DD} supply.
34	VDDINT		**VDDINT** Digital interface supply voltage. 1.65 V ≤ VDDINT ≤ 3.1 V. VDDINT must, at all times, be ≤ V_{CC}.
35	VDD		**VDD** Digital core supply. The pin of the IC is bypassed to gnd. Logic Levels are internally shifted from VDDINT to/from VDD.
36	VSS		**VSS** Digital ground.

NOTE: $V_{CC} = V_{CC}RF$

Table 13. Pin Function Description (Continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
38	GNDCP		**GNDCP** Main frac-N charge pump ground.
37	VCCCP		**VCCCP** Main frac-N charge pump V_{CC}. It is decoupled to GNDCP at the pin of the IC.
39	MLPF		**MLPF** Main frac-N loop filter (Charge Pump). The filter is referenced to V_{CC}.
41	GNDPRE		**GNDPRE** Prescaler ground.
40	VCCPRE		**VCCPRE** Prescaler V_{CC}. The pin of the IC is bypassed to GNDPRE.
42	VCCVCO		**VCCVCO** VCCVCO is decoupled to GNDVCO at the pin of the IC. Extreme caution should be used when decoupling/routing to this pin.
43	GNDVCO		**GNDVCO** VCO ground.
44	GNDMOD		**GNDMOD** Modulation DAC ground.
45	VCCMOD		**VCCMOD** Modulation DAC V_{CC}. The pin of the IC is bypassed to GNDMOD.
47	GNDMIX		**GNDMIX** Mixer ground.
46	VCCMIX		**VCCMIX** Mixer V_{CC}. The pin of the IC is bypassed to GNDMIX.

NOTE: $V_{CC} = V_{CC}RF$

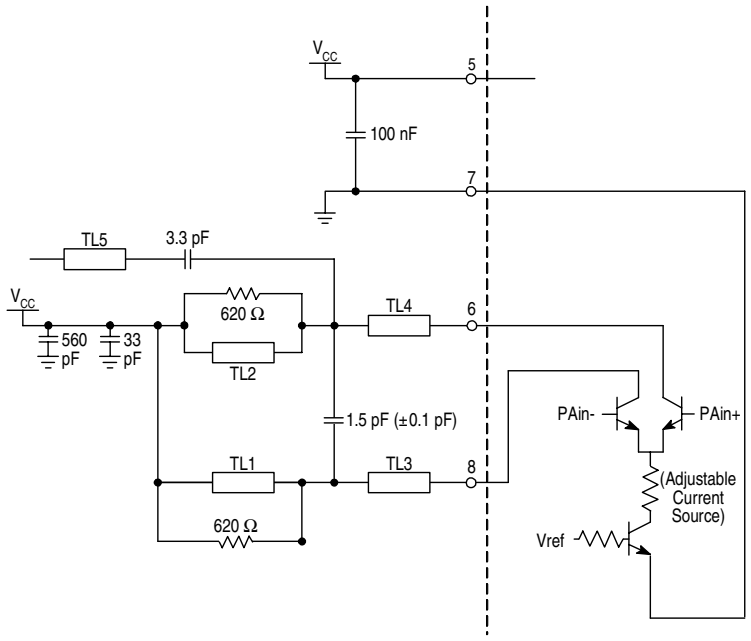


Figure 5. Equivalent Internal Circuit for Pins 5, 6, 7, and 8

3 Typical DC Performance Characteristics

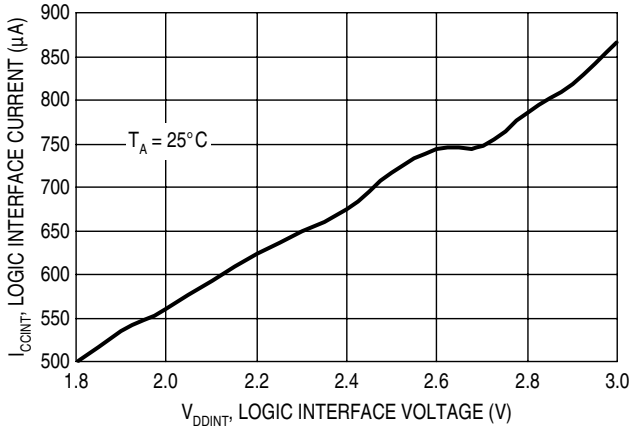


Figure 6. Logic Interface Current versus Logic Interface Voltage (Idle Mode)

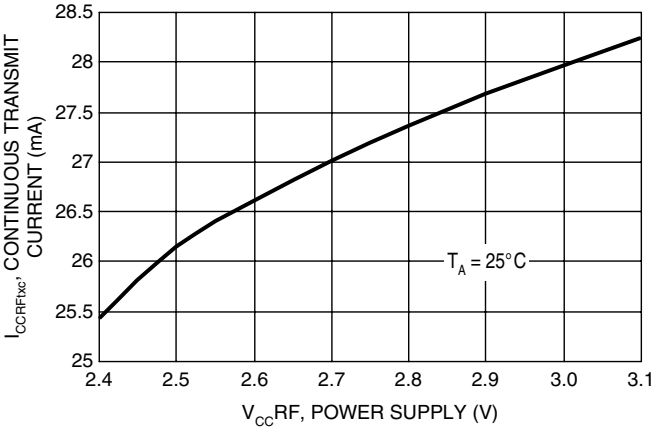


Figure 7. Continuous Transmit Current versus Power Supply

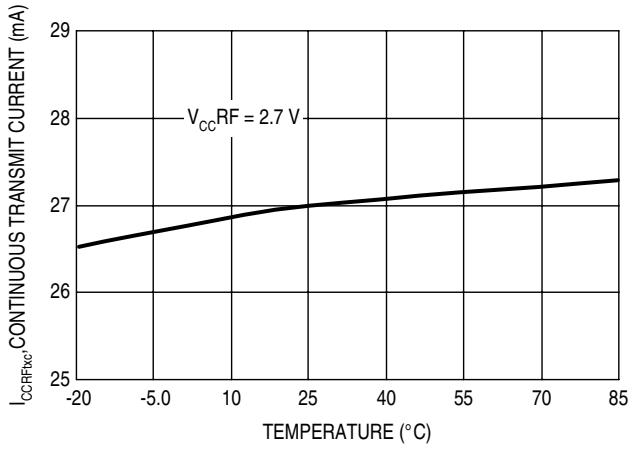


Figure 8. Continuous Transmit Current versus Temperature

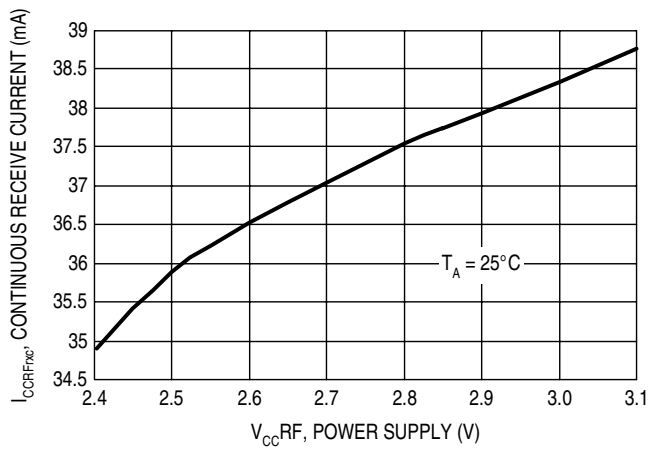


Figure 9. Continuous Receive Current versus Power Supply

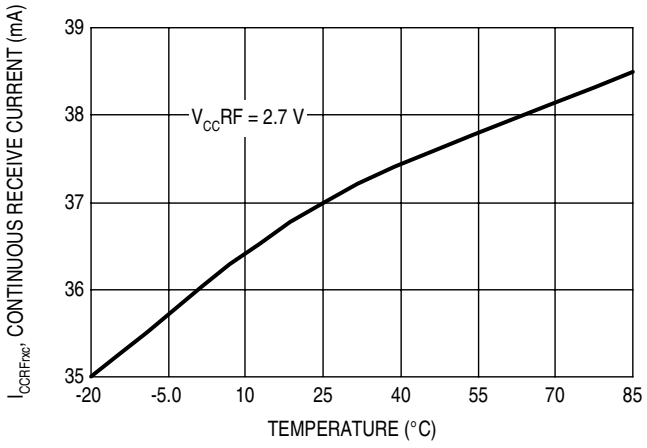


Figure 10. Continuous Receive Current versus Temperature

4 Functional Description

Note: In the following description, control bits contained in the MC13180 register map for various functions will be identified by register number and bit number(s). For example, bit R4/8 references bit 8 of register 4 while R5/9-3 identifies bits 9 through 3, inclusive, of register 5 (decimal notation). Unless otherwise noted, a default register map configuration as listed in Figure 4 is assumed.

4.1 Overview

The MC13180 is a complete RF transceiver for Bluetooth applications. The device, when coupled with an MC71000 controller or any controller containing an integrated Joint Detection/Minimum Length Sequence Estimator (JD/MLSE) digital decoder, exhibits superior RF performance with small size and low cost. Only minimal external components are required to complete the RF link of a Bluetooth system.

4.2 MC13180 States

Figure 11 illustrates the various states which the MC13180 can assume. A description of each state follows.

4.3 OFF State

In the OFF state, no power is being applied to the V_{CC}RF or V_{DDINT} of the device. During this state, all digital inputs should be held at ground to avoid forward biasing internal ESD diodes.

4.4 POWER UP State

During this state, power is applied to the device in an orderly fashion. All digital inputs should continue to be held at ground.

Since V_{DDINT} of the device must always be less than or equal to the V_{CC}RF supplied to the device, it is generally desired to first allow the V_{CC}RF to rise and stabilize, then follow with applying the V_{DDINT} supply. This prevents internal protection diodes from forward biasing.

SPI operations are not allowed during this state.

4.5 RESET State

The RESET state can be entered at any time from any state with the exception of the OFF and POWER UP states. During the RESET state, SPI operations are forbidden.

The RESET state places the entire contents of the internal register map into a known condition. All digital outputs are active and driven to a logic low. The SDATA I/O pin is configured as an input, and the RFDATA I/O pin is configured as an output. The crystal oscillator is inactive and therefore the CLK output remains at a static low level.

4.6 CONFIG State

Once the $\overline{\text{RES}}$ pin is de-asserted, the crystal oscillator and data clock PLL of the device become active. The CLK output will attempt to synthesize a clock frequency based upon the crystal oscillator frequency and values loaded into the data clock N and R registers. These values assume an initial reference frequency of 13 MHz and the data clock values are initialized from reset to synthesize 24 MHz from this reference.

During the Config state, any address location can be read or written. The Sleep Enable, Tx Enable, and Rx Enable bits of the register map must remain at a logic zero, otherwise the register map is typically loaded with user defined default values.

4.7 WAIT XTAL State

During this state, the crystal oscillator and data clock PLL are stabilizing. If an external reference oscillator is being used, the data clock PLL must still be allowed to settle. Stability will be achieved after T_{WAIT}, at which time the Idle state is entered.

4.8 IDLE State

In the Idle state, the CLK output supplies a synthesized 24 MHz output. Any SPI operation is allowed during this state. RSSI information is typically read during the Idle state.

4.9 TX CONFIG State

During this state, the contents of the register map are set for any desired transmit information, including the transmit channel setting. The Tx Enable (R2/14) bit of the register map is also asserted which places the RFDATA pin into the input state at the completion of the SPI write cycle.

4.10 TX WARM UP

The MC13180 begins a series of internal warm up sequences once the RTXEN pin is asserted. SPI operations are forbidden during this state.

4.11 TX MODE

Data presented to the RFDATA pin is transmitted to the PA output of the device. SPI operations are forbidden during this state. The TX mode is ended by de-asserting the RTXEN pin or by going into the RESET state. SPI operations are not permitted until T_{TXDIS} µs after the RTXEN pin is de-asserted.

4.12 RX CONFIG State

During this state, the contents of the register map are set for any desired receive information, including the receive channel setting. The Rx Enable (R2/13) bit of the register map is also asserted which places the RFDATA pin into the output state at the completion of the SPI write cycle.

4.13 RX WARM UP

The MC13180 begins a series of internal warm up sequences once the RTXEN pin is asserted. SPI operations are forbidden during this state.

4.14 RX MODE

Digitized and oversampled data from the desired receive channel is presented to the RFDATA pin and framed by the FS signal. Data is aligned to the rising edge of the CLK output. SPI operations are forbidden during this state. The RX mode is ended by de-asserting the RTXEN pin or by going into the RESET state. SPI operations are not permitted until T_{RXDIS} µs after the RTXEN pin is de-asserted.

4.15 SLEEP State

The Sleep state is entered by asserting the Sleep Enable (R2/15) bit of the address map. During this mode, the CLK pin is driven to a static logic low level, and the crystal oscillator is disabled. All digital outputs are driven to a logic low level.

SPI operations are permitted during this state. The Idle state is entered by de-asserting the Sleep Enable bit of the address map.

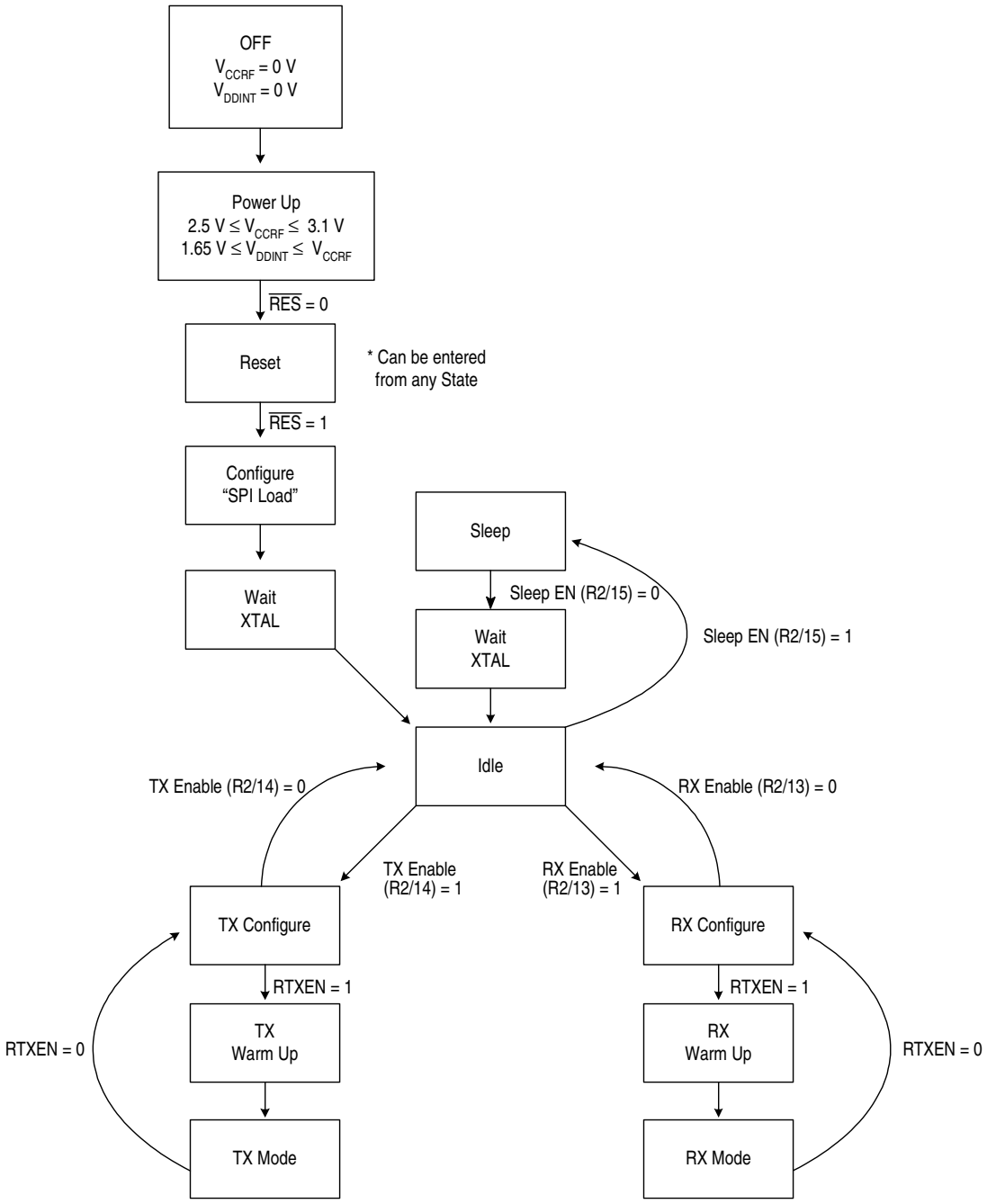


Figure 11. State Diagram

4.16 Receive Data Path

The MC13180 is placed into the receive mode from the idle mode by asserting the RTXEN pin after setting the Receive Enable bit (R2/13), clearing the Transmit Enable bit (R2/14), and clearing the Narrow Bandwidth Enable bit (R2/12) (See Figure 12). The RFDATA pin of the device is configured as an output as soon as these bit conditions are loaded into the register map. The baseband interface signals used in the receive mode are shown in Table 14. The interface signal levels are internally translated to/from V_{DDINT} to V_{DD}.

To initiate a receive cycle, the user will set the local oscillator frequency of the device in conjunction with the High/Low Injection Enable bit. Optionally, other address map values may be written or read. During this “SPI” cycle, the device's RTXEN must be de-asserted.

After time T_{SUSPI}, the RTXEN pin can be asserted. This initiates a sequence internal to the MC13180 which places it into the receive mode. Serialized, A/D data will appear at the RFDATA pin, framed by the FS pin, after T_{propFS}.

The data represents a 6-Bit, 2’s-complement digital value and is sampled four times for every data bit. Once the receive cycle is complete, the RTXEN pin is de-asserted and the MC13180 begins an internal power down sequence.

4.17 Transmit Data Path

The MC13180 is placed into the transmit mode from the idle mode by setting the Transmit Enable bit (R2/14), setting the Narrow Bandwidth Enable bit (R2/12), and clearing the Receive Enable bit (R2/13) of the address map, then asserting the RTXEN pin of the device (see Figure 12). The RFDATA pin of the device is configured as an input as soon as these bit conditions are loaded into the register map. The baseband interface signals used in the transmit mode are shown in Table 14. The interface signal levels are internally translated to/from V_{DDINT} to V_{DD}.

To initiate a transmit cycle, the user will normally set the desired channel frequency and mode bits mentioned above. Optionally, other address map values may be written or read. During this “SPI” cycle, the device's RTXEN must be de-asserted, ensuring that the device remains in idle mode.

After time T_{SUSPI}, the RTXEN pin can be asserted. This initiates a sequence internal to the MC13180 which places it into the transmit mode. Data to be transmitted must be set and stable no later than T_{stb} after the assertion of RTXEN. The RF data will be present at the PA output after RTXEN time, T_XLAT. Subsequent serial data can then continue to be presented to the MC13180 via the RFDATA pin, and the CLK of the device (divided by 24) can be used as the system clock to synchronize the data transfer.

Once the data stream has been transmitted and the time T_{hold} is met, the RTXEN pin is de-asserted and the MC13180 begins an internal power down sequence. Since RF power is still present at the PA output, no SPI operations or additional cycles can be performed for at least T_{TXDIS} µs. At this time, RF power is at a substantially low enough level as to not produce undesired emissions.

4.18 Transmit Synchronization Delay

A programmable delay exists between the rising edge of RTXEN and the first available bit of data. This delay range is TXsync and is set via SPI bits of Transmit Synchronization Time Delay Value (R8/15-8) where the value represents the delay in microseconds. Packet data is seen at the antenna approximately 2.5 µs after this delay. Refer to Figure 12 for the corresponding timing diagram. All Bluetooth packets require a minimum of four preamble bits of pattern 0101 or 1010. For minimum power consumption, set the delay to TXsync minimum. If additional settling time or preamble bits are required, manipulate the delay as necessary, up to TXsync maximum.

4.19 Main Loop Bandwidth

During a transmit cycle, Narrow Bandwidth Enable (R2/12) must be set to a logic one. During a receive cycle this bit must be set to a logic zero. Changing the loop bandwidth of the Main Loop Filter in this manner maximizes radio performance. Note that this bit is externally gated by the sequence manager.

Table 14. Data Direction and Signal Description for the MC13180 Baseband Interface

Pin Name	RX Direction	RX Mode Description
RFDATA	MC13180 → Baseband	RX data
FS	MC13180 → Baseband	Start of each 6-bit sample
RTXEN	MC13180 ← Baseband	Receive mode enable
CLK	MC13180 → Baseband	Data sample clock
Pin Name	**TX Direction**	**TX Mode Description**
RFDATA	MC13180 ← Baseband	TX data
FS	MC13180 → Baseband	Signal is unused and remains low
RTXEN	MC13180 ← Baseband	Transmit mode enable
CLK	MC13180 → Baseband	Data sample clock

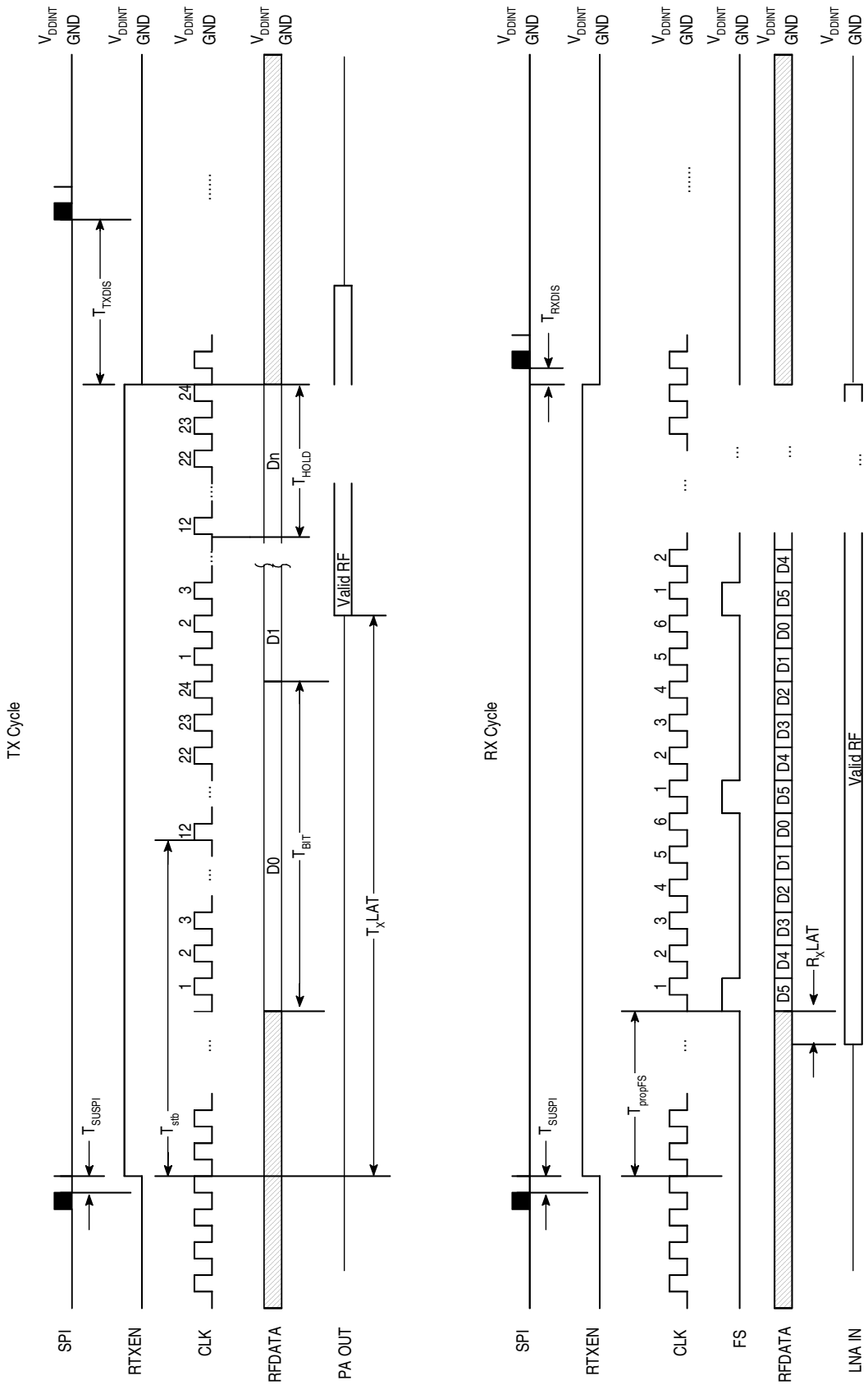


Figure 12. TX and RX Cycle Timing

4.20 Serial Peripheral Interface (SPI)

Basic functionality of the MC13180 is controlled by configuring the internal address map of the device (see Figure 4). The address map is completely read/writable and is organized as 32 addresses of 2-bytes (16-bits) each. The serial interface to this map is controlled by the $\overline{CE}$, SDATA, and SCK pins. In addition, the entire address map can be placed into a known state by either asserting the RES pin or by writing to address zero of the device. Logic interface levels are controlled by the VDDINT pin. The interface signal levels are internally translated to/from VDDINT to VDD.

The non-standard SPI uses a bi-directional SDATA pin to transfer information to/from the MC13180. Data is clocked into and out of the device on the rising edge of SCK (SCK is of RZ format). The $\overline{CE}$ pin enables the device SPI and transfers the contents of the SPI shift register to the decoded address when de-asserted. The MC13180 device address is defined to be 01 (binary). This scheme allows for up to three additional SPI devices to be cascaded together without requiring an additional chip enable line.

Figure 13 shows a SPI write operation. SPI transfers begin with the assertion of the $\overline{CE}$ pin when RES is de-asserted. The first bit clocked into the SPI is the R/W bit which equals a logic zero to indicate a SPI write operation. The next two bits are the MC13180 device address (i.e., 01). The remaining five bits of the address field represent the target address to which information will be transferred.

The data field proceeds the address field. Data is clocked into the SPI from MSB to LSB. Once the LSB has been entered, the $\overline{CE}$ pin is de-asserted and the data field contents are transferred to the MC13180's target address. A SPI write to address zero resets all register map values to their initial (reset) condition.

Figure 13 also shows a SPI read operation. The first bit clocked into the SPI is now a logic one, indicating a read operation is desired. Again, the next two bits clocked into the SPI are 01, the MC13180 device address. The next five bits of the address field will be the target address to be read.

On the falling edge of the SCK, the SDATA line becomes high impedance. This condition remains until the next rising edge of SCK, where data is driven onto the SDATA pin. Data should be sampled for reading on the falling edge of SCK.

Once all data has been shifted out of the SPI, the $\overline{CE}$ pin is de-asserted and the SDATA line becomes an input to the MC13180. Again, reading from address zero will reset the entire register map values to their initial condition.

Important Note: All SPI signals ($\overline{CE}$, SCK, and SDATA) should remain completely static during an active receive or transmit cycle to prevent digital feedthrough to the RF portions of the chip. Failure to follow this condition can cause severe performance degradation.

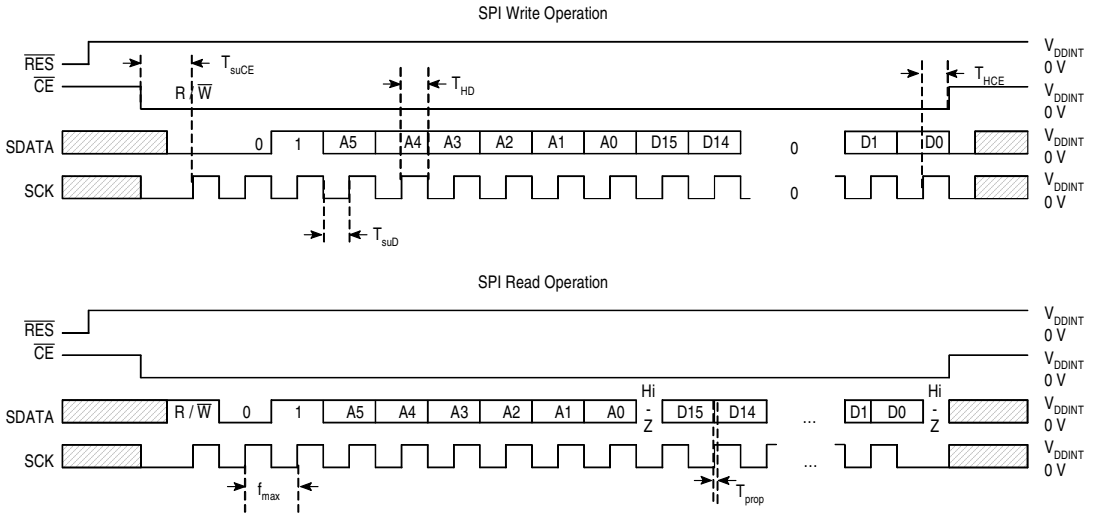


Figure 13. SPI Register Map

4.21 Crystal Oscillator

The crystal oscillator provides the reference for the data clock PLL and main PLL. It can be configured as a Colpitts type (negative resistance) oscillator and utilize an external parallel resonant crystal or may be driven from an external source. The oscillator circuit has an on-chip capacitor trim network that provides the capability to compensate for crystal and/or load capacitor tolerances. This allows the use of relatively inexpensive crystals with as much as 50 ppm tolerance. The oscillator also provides three bias current modes. Xtal Enable (R11/0) enables/disables the bias current and Xtal Boost Enable (R11/4) enables/disables a high current mode. Refer to the Reference Oscillator Electrical Characteristics for the available current modes. Table 15 gives examples of parallel trim capacitances that can be programmed to register map location Xtal Trim (R6/14-10). Typical stray capacitance is on the order of 1.0 pF.

To drive the oscillator with an external source, program the Xtal Enable (R11/0) to zero and ac-couple the external signal into the oscillator base with a 15 to 100 pF capacitor. It is also recommended to set Xtal Trim (R6/14-10) to zero to reduce the load on the external source.

Additional characteristic data is shown in Figures 14 through 19.

Table 15. Examples of Programmable XTAL Trim Capacitances

XTAL Trim (R6/14-10) Setting (MSB to left)	**Electronic Parallel Crystal Trim Capacitance (C_{PT})**
00000	0 pF
00100	1.2 pF
10000	4.8 pF
10101	6.3 pF
11111	9.3 pF

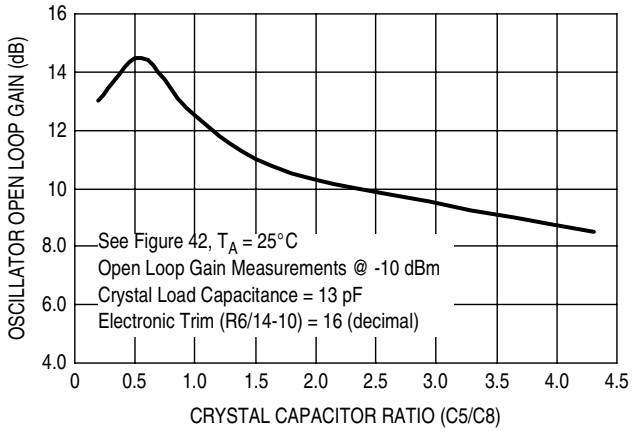


Figure 14. Oscillator Open Loop Gain versus Capacitor Ratio

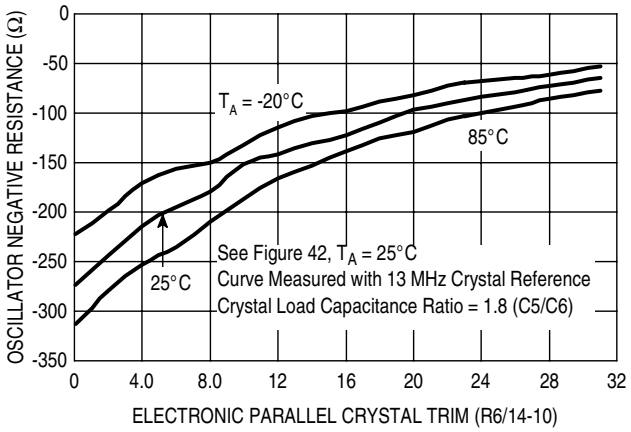


Figure 15. Oscillator Negative Resistance versus Electronic Parallel Crystal Trim (C_{PT})
(Crystal Boost Enable R11/4) = 0

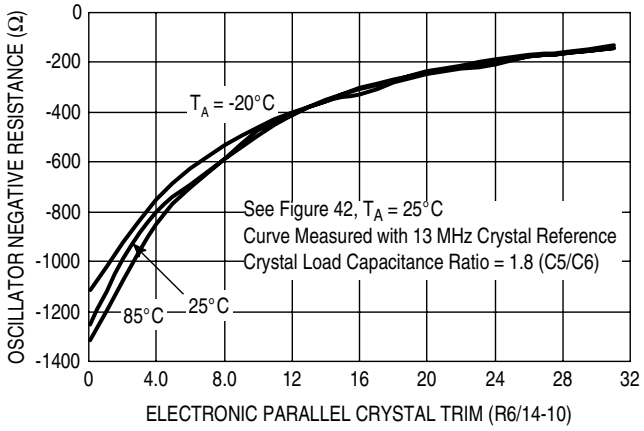


Figure 16. Oscillator Negative Resistance versus Electronic Parallel Crystal Trim (C_{PT})
(Crystal Boost Enable R11/4) = 1

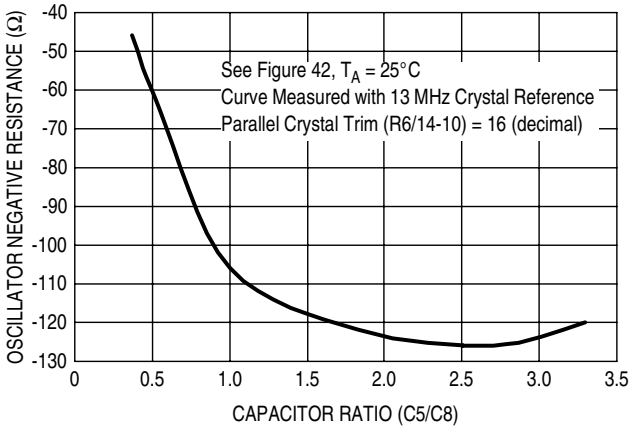


Figure 17. Oscillator Negative Resistance versus Crystal Capacitor Ratio
(Crystal Boost Enable R11/4) = 0

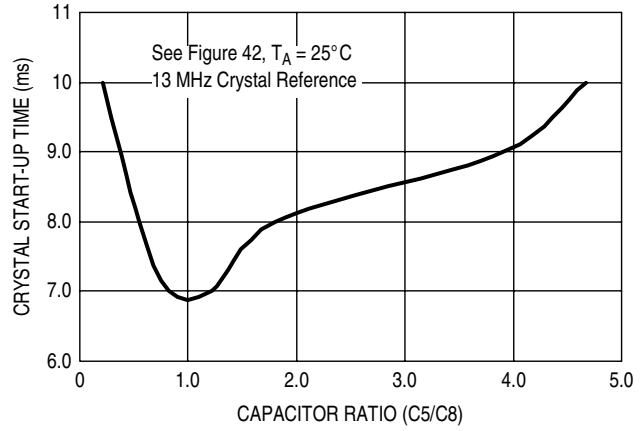


Figure 18. Crystal Start-up Time versus Capacitor Ratio

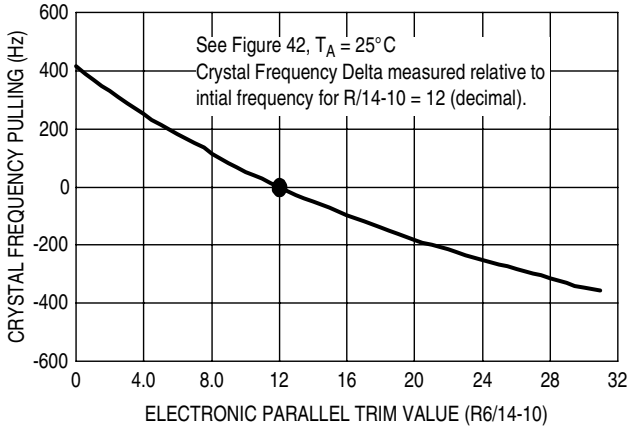


Figure 19. Crystal Frequency Pulling versus Electronic Parallel Trim Value

4.22 Data Clock Operation

The data clock phase lock loop is responsible for providing a constant 24 MHz reference for use throughout the device. The MC13180 uses a simple integer-N synthesizer to derive a 24 MHz clock (CLK) from the reference frequency. The counter values must always be set to the appropriate values to generate this 24 MHz clock frequency. The general model for the Phase Lock Loop (PLL) is illustrated in Figure 20.

For the circuit in Figure 42, the external low pass filter has a loop filter bandwidth (LBW) of 1.0 kHz. This proves to be adequate for any value of external reference frequency that is an integral multiple of 20 kHz. More details about PLL loop filters can be obtained from Motorola application note AN1253/D.

The R-counter of the synthesizer (R6/9-0) is set to a value which will set the internal reference frequency f_{ref}Internal to 20 kHz; thus R = f_{ref}External / 20 kHz. The N-counter of the synthesizer (R7/10-0) is set to multiply f_{ref}Internal to 24 MHz; thus N = 24 MHz / f_{ref}Internal. For the case of a 13 MHz external reference, R = 650_{10} and N =1200_{10}.

For applications utilizing f_{ref}External > 20 MHz, the external low pass filter with a 1.0 kHz corner frequency is still usable. However, due to the R counter limitations, the R counter is programmed to generate the f_{ref}Internal to 40 kHz (recommended). For the case of a 26 MHz external reference, $R = 650_{10}$ and $N = 600_{10}$.

The N and R counters can only divide by integer values and the greatest common divider must be found to represent f_{ref}Internal and achieve CLK. Table 16 provides the appropriate values for various f_{ref}Externals. For applications that require a faster data clock PLL response time, refer to the data clock electrical characteristics and Motorola application note AN1253/D.

Additional data clock characteristic data is shown in Figures 21 and 22.

Table 16. Data Clock R and N Counter Values for 20 kHz f_{ref}Internal with 1.0 kHz LBW

f_{ref}External (MHz)	f_{ref}Internal (kHz)	R Counter (Decimal)	N Counter (Decimal)	LBW (kHz)
12	20	600	1200	1.0
13	20	650	1200	1.0
14.4	20	720	1200	1.0
16.8	20	840	1200	1.0
19.22	20	961	1200	1.0
19.68	20	984	1200	1.0
19.88	20	994	1200	1.0
26	40	650	600	1.4

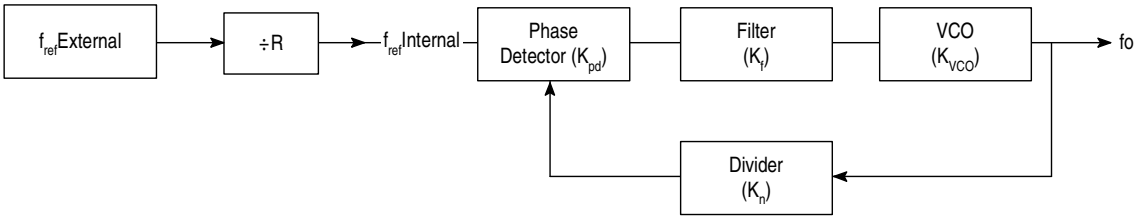


Figure 20. General Model for the PLL

Where:

K_{pd} = Phase Detector Gain Constant

K_f = Loop filter transfer function

K_{VCO} = VCO Gain Constant

K_n = Divide Ratio (1/N)

f_{ref}Internal = Input Frequency

fo = Output frequency

fo/N = Feedback frequency divided by N

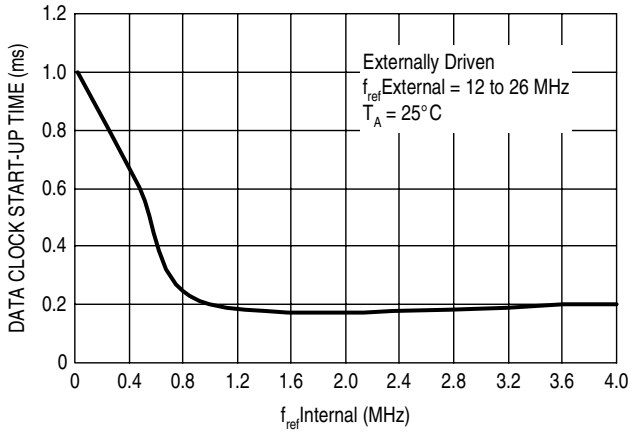


Figure 21. Data Clock Start-up Time versus f_{ref}Internal

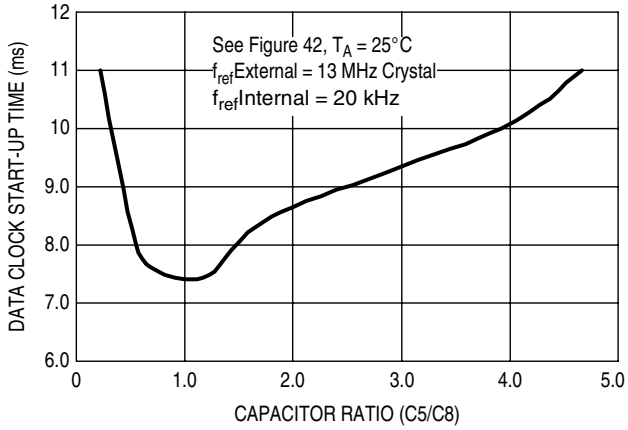


Figure 22. Data Clock Start-up Time versus Capacitor Ratio for Crystal Reference

4.23 Main Synthesizer Operation

The internal local oscillator (LO) of the MC13180 is derived from the external reference frequency by means of a 3-accumulator, fractional-N synthesizer. The external low pass filter (C7/R4 of Figure 3) has a corner frequency of approximately 140 kHz.

f_{dev} is the nominal transmit ROM frequency deviation (typically 157500 Hz).

I is the integer portion of the fractional synthesizer

R is the numerator portion of the fractional synthesizer

f_{ref}External is the external reference frequency

LO is the desired local oscillator frequency

then,

I = INT ($LO/f_{ref}External - f_{dev}/f_{ref}External$) - 3

R = REM($LO/f_{ref}External - f_{dev}/f_{ref}External$) x 2^{16}

where the INT function is the integer portion of the result and REM is the remainder portion of the result.

For Example:

f_{dev} = 157500 Hz

LO = 2.441 GHz

f_{ref}External = 13 MHz

then,

I = INT(2.441 GHz/13 MHz - 157.5 kHz/13 MHz) - 3 = 184_{10}

R = REM(2.441GHz/13 MHz - 157.5 kHz/13 MHz) x 2^{16}
= 49618_{10}

Accuracy to at least 10 decimal places is suggested.

4.24 Transmit ROM Operation

The MC13180 uses a look-up table (LUT or Transmit ROM) to shape incoming transmit data bits and produce a Gaussian filtered mask with BT=0.5. The value of the current data bit, along with knowledge of the previous two bits, determines a unique trajectory for shaping. Only four unique trajectories are required to implement this filter and due to the symmetrical nature of the Gaussian response, these trajectories can be reduced to a single quadrant. Furthermore, without compromising accuracy, this table can be reduced to only 11 values.

The output of the LUT is fed to the accumulators of the fractional synthesizer. The seven MSBs are eventually fed to the second port of the main VCO during transmit operation (see Figure 23). For receive operation, the output of the LUT is constantly held to the value contained in R1C1.

These 11 trajectory constants are listed in Table 17 (see also Figure 4, Register Map). The actual value to place in the LUT is calculated as:

LUT $RxCx_{b10} = (f_{dev}/f_{ref}External) \times 2^{16} \times (RxCx\ constant)$

This number is then rounded and converted to binary:

LUT $RxC_{xb2} = INT((LUT\ RxCx_{b10}+2)/4)$

where the INT function is the integer portion of the result.

As an example for calculating the LUT value for R4C2 and $f_{ref}External$ = 13 MHz:

LUT $R_4C_{2b10} = (157.5kHz/13.0MHz) \times 2^{16} \times 0.5229292198 = 415.2$

LUT $R_4C_{2b2} = INT((415.2+2)/4)_{b10} = INT(104.3)_{b10} = 104_{b10}$ or 011010000_{b2} or 68_{b16}

Table 19 lists all values of RxCx for supported reference frequencies.

Table 17. LUT RxCx Constants

R1C1	0.9999739537
R2C2	0.9980246857
R2C3	0.9911665663
R2C4	0.9678427310
R3C1	0.1881990082
R3C2	0.5249014674
R3C3	0.7660791186
R3C4	0.9043672052
R4C2	0.5229292198
R4C3	0.7572459756
R4C4	0.8722099597

4.25 M-Dual Port Multiplier and B-Dual Port Multiplier

For proper operation of the dual-port synthesizer, it is necessary to maintain a constant deviation injection at the input of Port 2 of the VCO. As can be seen from the Transmit ROM operation and Figure 23, the output of the LUT is fed to a digital multiplier prior to being presented to the input of the modulation DAC. Since the LUT values decrease proportionately with input reference frequency, the multiplier must scale

these values to achieve a constant deviation. This scaling is linear. Two programmable constants are used to form the equation of a line, the M & B dual-port multipliers. M-Dual Port Digital Multiplier Value (R17/15-8), determines the slope, and B-Dual Port Digital Multiplier Value (R8/7-0), determines the intercept.

M-Dual Port Digital Multiplier = (f_{ref}External) /13MHz * 108_{10}

B-Dual Port Digital Multiplier = (f_{ref}External) /13MHz * 100_{10}

Table 19 contains slope and intercept point values across all supported input reference frequencies.

4.26 Dual-Port Programmable Delay (R7/15-11)

Just as it is necessary to maintain a constant deviation at Port2 of the VCO, it is also necessary to maintain a constant phase at the FV and FR inputs of the main charge pump. The total delay from the output of the LUT to the FV input of the charge pump is given as:

LUT $\rightarrow$ FV delay = 10.5 / (f_{ref}External)

Likewise, the total delay from the LUT to the FR input of the charge pump is:

LUT $\rightarrow$ FR delay = 28 ns + Delay

where delay is the programmed delay value shown in Table 18. Therefore, for a given external reference frequency:

Delay = 10.5 / (f_{ref}External) - 28 ns.

Consult Table 18 for the closest available value.

Table 19 lists all values of the programmable delay for supported reference frequencies.

Table 18. Dual-Port Programmable Delay Values

R7/15-11 (decimal)	**Delay$_{b10}$** (ns)	**R7/15-11** (decimal)	**Delay$_{b10}$** (ns)
4	167	13	542
5	208	14	583
6	250	15	625
7	292	16	667
8	333	17	708
9	375	18	750
10	417	19	792
11	458	20	833
12	500	21	875

Table 19. Register Settings and Component Values versus Reference Frequency
(all register setting values in hex notation)

Register	Fref= 12MHz	Fref= 13MHz	Fref= 14.40MHz	Fref= 15.26MHz	Fref= 16.80MHz	Fref= 19.22MHz	Fref= 19.44MHz	Fref= 19.68MHz	Fref= 19.88MHz	Fref= 26MHz
Data Clk R (R6/9-0)	258	28A	2D0	2FB	348	3C1	3CC	3D8	3E2	28A
Data Clk N (R7/10-0)	4B0	4B0	4B0	4B0	4B0	4B0	4B0	4B0	4B0	258
R1C1 (R12/7-0)	D7	C6	B3	A9	9A	86	85	83	82	63
R2C2 (R12/15-8)	D7	C6	B3	A9	99	86	84	83	82	63
R2C3 (R13/7-0)	D5	C5	B2	A8	98	85	84	82	81	62
R2C4 (R13/15-8)	D0	C0	AD	A4	95	82	80	7F	7E	60
R3C1 (R14/7-0)	28	25	22	20	1D	19	19	19	18	12
R3C2 (R14/15-8)	71	68	5E	59	51	46	46	45	44	34
R3C3 (R15/7-0)	A5	98	89	82	76	67	66	64	63	4C
R3C4 (R15/15-8)	C2	B4	A2	99	8B	79	78	77	75	5A
R4C2 (R16/7-0)	70	68	5E	58	50	46	45	45	44	34
R4C3 (R16/15-8)	A3	96	88	80	74	66	65	63	62	4B
R4C4 (R17/7-0)	BC	AD	9C	93	86	75	74	72	71	56
M-Dual Port Multiplier (R17/15-8)	64	6C	78	7F	8C	A0	A2	A3	A5	D8
B-Dual Port Multiplier (R8/7-0)	56	64	6E	75	81	94	96	97	99	C8
Dual Port Programmable Delay (R7/15-11)	14	13	11	10	E	C	C	C	C	9

Table 19. Register Settings and Component Values versus Reference Frequency (Continued)
(all register setting values in hex notation)

R4 (kΩ)	27	27	24	22	20	18	18	18	18	13
C7 (pF)	270	270	270	330	330	390	390	390	390	560
C6 (pF)	0	0	0	0	0	4.7	4.7	4.7	4.7	10

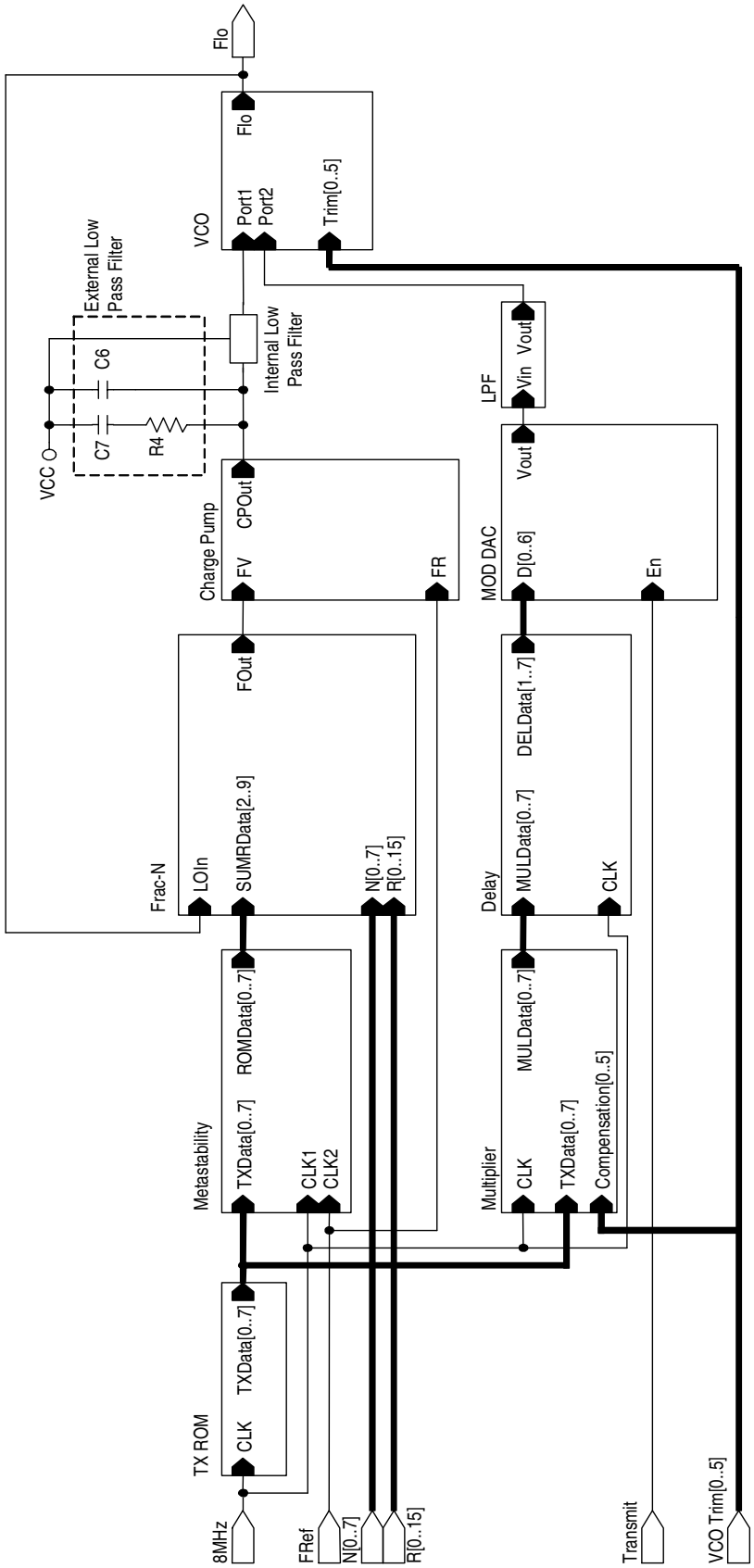


Figure 23. Main PLL Synthesizer Block Diagram

4.27 Receiver

The MC13180 receiver is intended to be used in Time Division Duplex (TDD), Frequency Hopping Spread Spectrum (FHSS) applications such as Bluetooth. The receiver uses a low intermediate frequency (IF) of 6.0 MHz, and is capable of receiving up to 1.0 Mbit/s Gaussian Frequency Shift Keyed (GFSK) serial data through the entire 2.4 GHz Industrial, Scientific and Medical (ISM) band.

The output of the receiver is a demodulated, serial bit stream of 24 Mbit/s data. This data represents a 4X over sample by a 6-bit D/A of the actual demodulated analog data recovered from the desired channel. A detailed discussion of each of the functional blocks within the receiver follows.

4.28 LNA

The first portion of the receiver chain is the Low Noise Amplifier (LNA). The LNA is a bipolar cascode design and provides gain with low noise at RF frequencies. The LNA is designed with a single-ended (unbalanced) input and is converted to a differential (balanced) output by means of an on chip, integrated balun.

For optimum performance, the LNA input impedance must be matched to the complex conjugate of the source impedance (usually 50 Ω).

The LNA of the MC13180 exhibits two distinctly different impedances depending upon whether the LNA is active or disabled. During a receive cycle, the S11 of the LNA is shown in Table 20.

Table 20. S11 for LNA During Receive

Frequency	MAG (dB)	Angle (degree)
2.45 GHz	-4.3	-138

The LNA can be matched to 50 Ω by a simple capacitor/inductor network as shown in Figure 24.

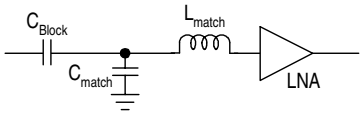


Figure 24.

When the LNA is disabled or the device is in the Idle or Transmit mode, the impedance of the LNA becomes the value shown in Table 21.

Table 21. S11 for LNA Disabled

Frequency	MAG (dB)	Angle (degree)
2.45 GHz	-8.9	42

The use of an antenna switch to interface the LNA with an antenna is the preferred circuit configuration as illustrated in Figure 42.

In this implementation, a true RF Single-Pole, Double-Throw (SPDT) switch is used to isolate the PA output from the LNA input during receive and transmit modes. A 1/4 wavelength trace is not required. As a result, this implementation has the highest performance (due to the lowest loss) and smallest size at the

penalty of increased system cost. An external switch must be used for Class 1 Bluetooth devices as the LNA input will become overloaded if not sufficiently isolated from the external PA output. The LNA provides a nominal 6.7 dB of power gain when properly matched.

The LNA is enabled approximately 150 µs after the assertion of the RTXEN pin when programmed for Receive mode. It is disabled immediately after the de-assertion of the RTXEN pin or during any Idle or Transmit mode.

4.29 High/Low Image Reject Mixer (I/R Mixer)

The mixer is used to convert the desired RF channel to a 6.0 MHz Intermediate Frequency (IF). The mixer is completely balanced on all ports, and the local oscillator (LO) is derived from the buffered output of the on-chip Voltage Controlled Oscillator (VCO).

In general, it is desired to keep all image frequencies in-band. Therefore, when receiving the 6 lowest channels, the mixer can be programmed for high-side injection and the LO will be programmed to be 6.0 MHz above the desired channel frequency. When receiving the 6 highest channels, the mixer can be programmed for low-side injection and the LO will be programmed to be 6.0 MHz below the desired channel frequency. This is illustrated in Figure 25. Selection of high or low side injection is accomplished by bit R2/11 of the register map. For all other in-band channels, the choice of high or low side injection is arbitrary, although it is recommended to use high-side injection for frequencies to 2.440 GHz and low-side injection thereafter.

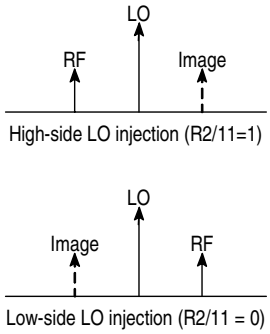


Figure 25. High-Side and Low-Side Mixer Injection

The mixer delivers approximately 15.8 dB of voltage gain and 22 dB of image rejection.

The mixer is enabled approximately 150 µs after the assertion of the RTXEN pin when programmed for Receive mode. It is disabled immediately after the de-assertion of the RTXEN pin or during any Idle or Transmit mode.

4.30 Post Mixer Amplifier (PMA)

Once the desired RF channel has been down converted to the IF frequency, the PMA is used to deliver 12 dB of additional gain prior to feeding the signal into the bandpass filter.

The PMA is enabled approximately 10 µs after the assertion of the RTXEN pin when programmed for Receive mode. It is disabled immediately after the de-assertion of the RTXEN pin or during any Idle or Transmit mode.

4.31 Bandpass Filter (BPF)

The 6.0 MHz bandpass filter is used to block undesired channels. The filter is self-adjusting and is calibrated during each receive cycle, based on an internally generated 6.0 MHz signal. The gain of the filter is fixed at 4.0 dB.

The nominal pass band for the filter is 720 kHz. This deliberately low pass band can cause significant intersymbol interference (ISI) issues for a GFSK modulated signal with a 1Mbit/s data rate. The advantages are increased sensitivity, adjacent channel interference performance and ease of manufacture. Due to this low pass band, a digitally implemented decoder scheme is utilized to eliminate ISI. This is referenced as the JD/MLSE, and is incorporated into all Motorola Bluetooth basebands.

The BPF is enabled approximately 10 µs after the assertion of the RTXEN pin while programmed for Receive mode and automatic tuning is complete after approximately 140 µs. It is disabled immediately after the de-assertion of the RTXEN pin or during any Idle or Transmit mode.

4.32 Limiter with Received Signal Strength Indicator (RSSI)

The RSSI (received signal strength indicator) is integrated into the limiter. The RSSI ADC converts the RSSI current into a 4-bit digital signal. When the RSSI enable (R4/6) and RSSI Read Enable (R9/8) are both set, the 4-bit RSSI conversion value can be read from the MC13180 register map (R29/3-0) while in Idle mode. The RSSI is updated approximately 40 µs after T_{propFS} during a receive cycle (see Figure 12). Enabling RSSI will result in additional current consumption as noted in the Receiver AC Electrical Specifications. Figure 26 shows the RSSI conversion value versus the RF level input to the LNA at various temperatures. Figure 27 shows the RSSI conversion versus the RF level at different power supplies.

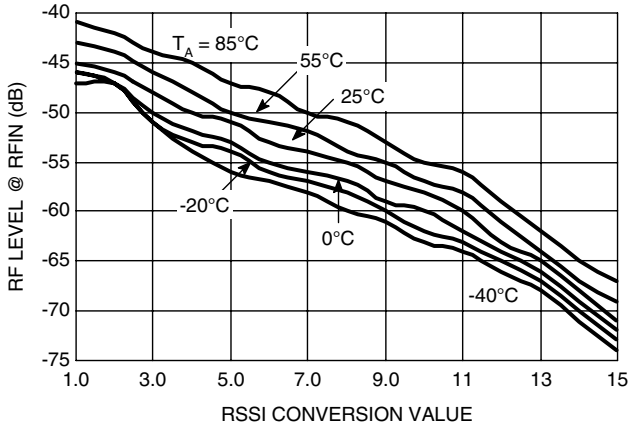


Figure 26. RF Level versus RSSI at Temperature

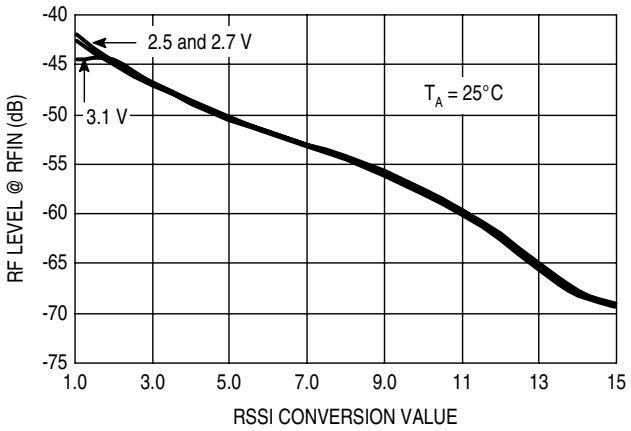


Figure 27. RF Level versus RSSI at V_{CC}RF

4.33 Demodulator

The receiver in the MC13180 downconverts the RF signal and demodulates it. The demodulator takes the IF signal from the limiter and delivers a baseband signal to an A/D converter (ADC). The 6-bit ADC uses the Redundant Sign Digit (RSD) Cyclic architecture that samples the analog input at 4.0 Msamples/s. The resulting demodulated data out of the MC13180 is a 24 Mbit/s, 2's-complement serial bit stream. The start of each 6-bit data stream is indicated by a frame sync (FS) signal. A 24 MHz clock output accompanies the demodulated data.

4.34 Receiver Characteristics

For optimum intermodulation and C/I performance, the MC13180 ground flag requires good conduction to the PCB ground layer. Refer to Figure 48 for additional information.

Figures 28 through 34 show typical performance of the receiver for various conditions.

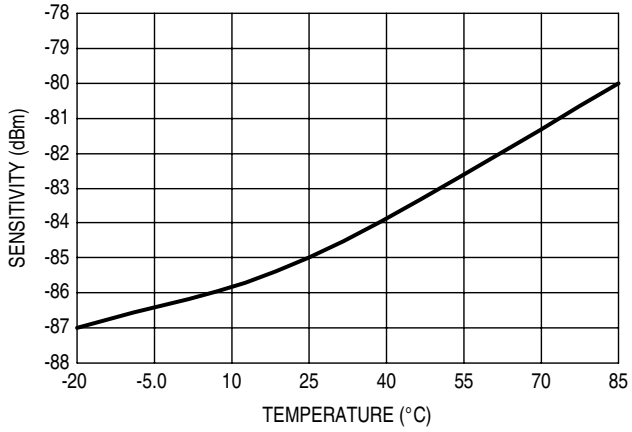


Figure 28. Receive Sensitivity versus Temperature

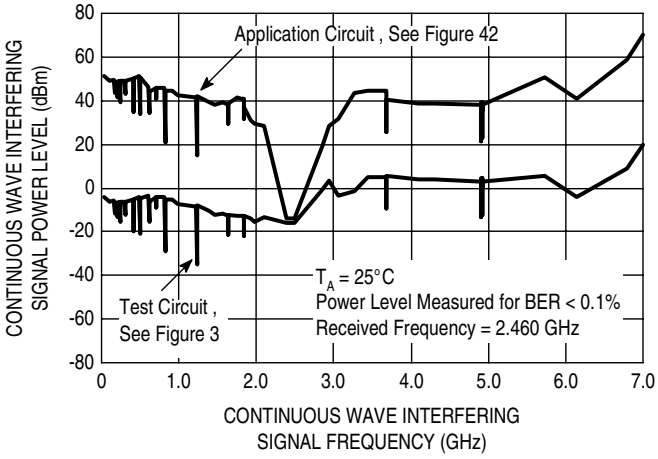


Figure 29. Blocking Performance versus Continuous Wave Interfering Signal

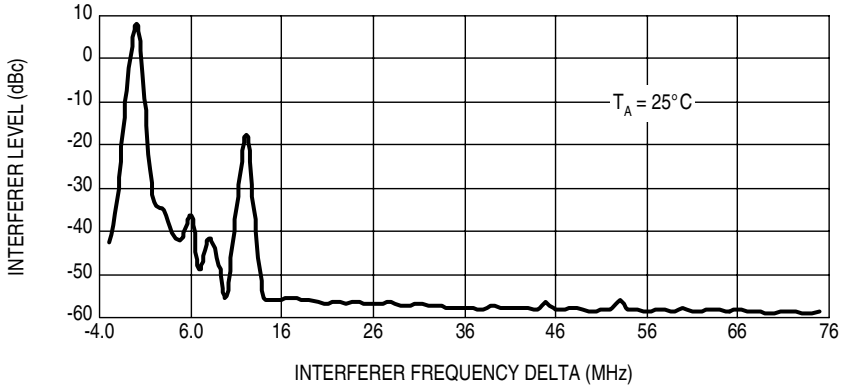


Figure 30. C/I Performance for Channel 3 (2.405 GHz, High-Side Injection)

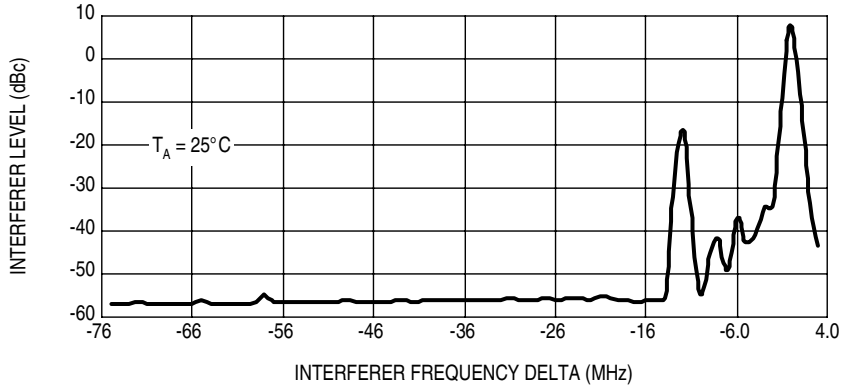


Figure 31. C/I Performance for Channel 75 (2.477 GHz, Low-Side Injection)

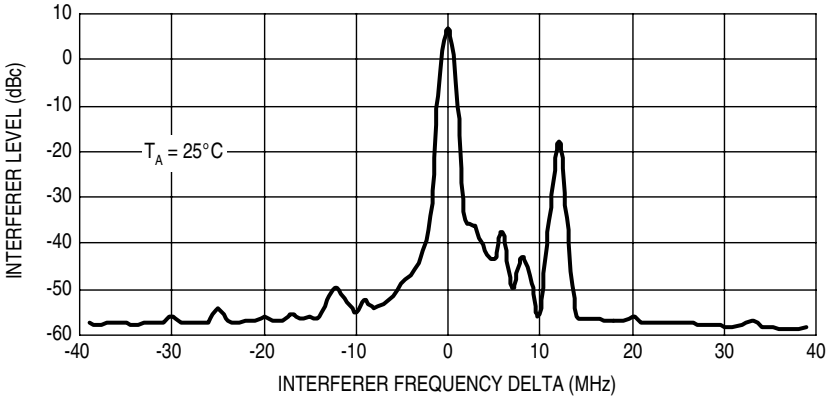


Figure 32. C/I Performance for Channel 39 (2.441 GHz, High-Side Injection)

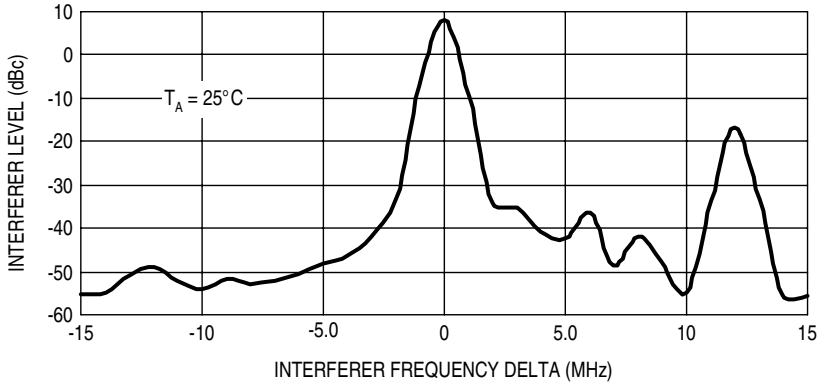


Figure 33. C/I Performance for Channel 39 (2.441 GHz, High-Side Injection)

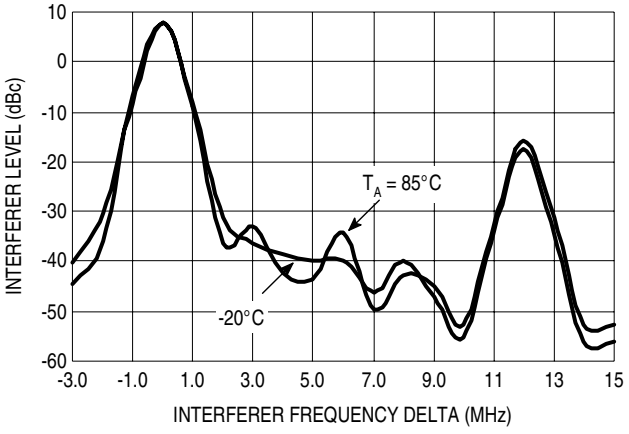


Figure 34. C/I Performance versus Temperature

4.35 Transmitter

The MC13180 uses a direct launch transmitter, taken from the output of the local oscillator (LO). During a transmit cycle the VCO of the LO is automatically trimmed. Following the LO are the output power stages, sequenced in the proper order. To minimize splattering, the output of the programmable low power

amplifier (LPA) drives a balanced ramp up/ramp down generator, which is fed to a “Balun” to provide a single-ended output for the external antenna switch. The transmit start up/warm down sequences are shown in Figure 38.

4.36 Programmable LPA

The output power of the LPA can be varied by programming PA Bias Adjust (R5/2-0) in the register map. Table 22 displays the response of RF output power, current consumption and 2nd Harmonic power level with respect to the programmable bit settings. Class 1 operations are supported through the use of an external power amplifier not shown here. Refer to Applications Information Class 1 Operation for more detail. Figures 35 and 36 provide additional LPA characteristic data.

4.37 Ramp Generator

The ramp generator has an exponential ramp up/ramp down function with a maximum settling time of 20 µs. Increasing the output power exponentially is useful to avoid splattering and minimize load pulling.

4.38 External Balun

The LPA provides a differential output that is converted to a single ended signal through the use of an inexpensive printed circuit board balun. Optionally, an external discrete balun may be used. Figures 37 and 42 show the physical dimensions and characteristics of this network.

Table 23 shows the output impedance, S22 of the PA during active and inactive cycles.

Table 22. RF Power Out versus PA Bias Adjust

PA Bias Adjust			Output Power (dBm)	Current Consumption (Continuous Transmit)(mA)	2nd Harmonic (dBc)
R5/2	R5/1	R5/0			
0	0	0	-0.9	23	-21
0	0	1	-10.8	20	-29
0	1	0	1.9	27	-19
0	1	1	-7.6	22	-24
1	0	0	5.3	33	-18
1	0	1	-3.5	27	-18
1	1	0	6.1	40	-20
1	1	1	3.5	35	-14

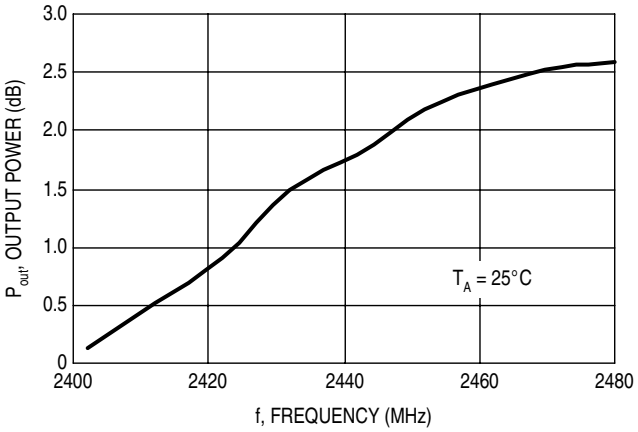


Figure 35. RF Output Power versus Carrier Frequency

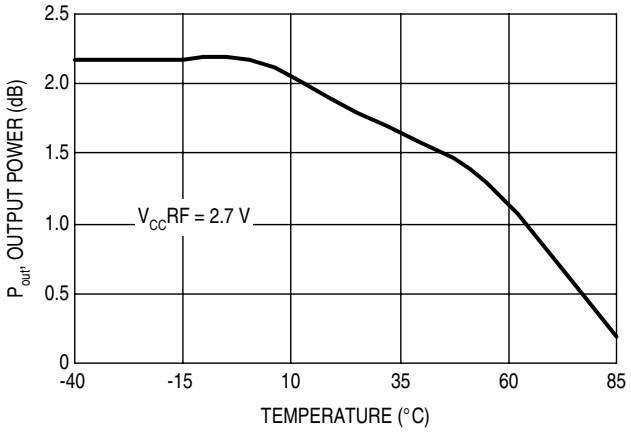


Figure 36. RF Output Power versus Temperature

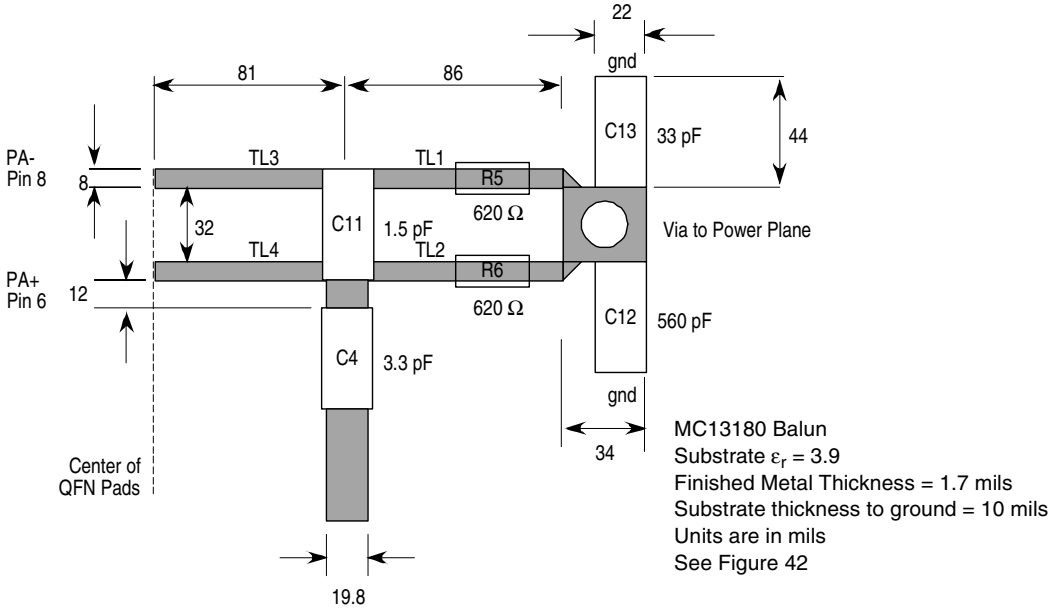


Figure 37. Balun Physical Dimensions

Table 23. S22 for PA During Transmit
(R5/2-0 = 010)(Measured Differential-Ended)

Operation Mode	Frequency (GHz)	MAG (dB)	Angle (degree)
Active	2.45	-5.5	-120
Inactive	2.45	0.2	-111

4.39 External Antenna Switch

An external antenna switch, shown in Figure 42, provides isolation between the PA output and the LNA input, and subsequently enables transmit and receive cycles. The controls to the switch are GPO and EPAEN, Pins 9 and 4, respectively, of the MC13180 device. When GPO is high, the switch is set to transmit mode. EPAEN serves as a complementary driver in this configuration. See Applications Information General Purpose Output and External Power Amplifier for further discussion.

4.40 General Purpose Output (GPO) Pin

The MC13180 General Purpose Output (GPO) is located at Pin 9 of the device. Its output is programmed for general use by setting bit R2/8 in the register map. The GPO can serve as a control line for an external antenna switch.

4.41 External Power Amplifier Enable (EPAEN) Pin

The External Power Amplifier Enable (EPAEN) output of MC13180 is located at Pin 4 of the device. EPAEN may be used in two applications. It may assist in Class 1 Operation by driving an external power amplifier; or it may serve as a complementary driver to a dual port antenna switch as seen in Figure 42. If EPAEN is not required for the desired application, it may be disabled by setting R11/6 to zero.

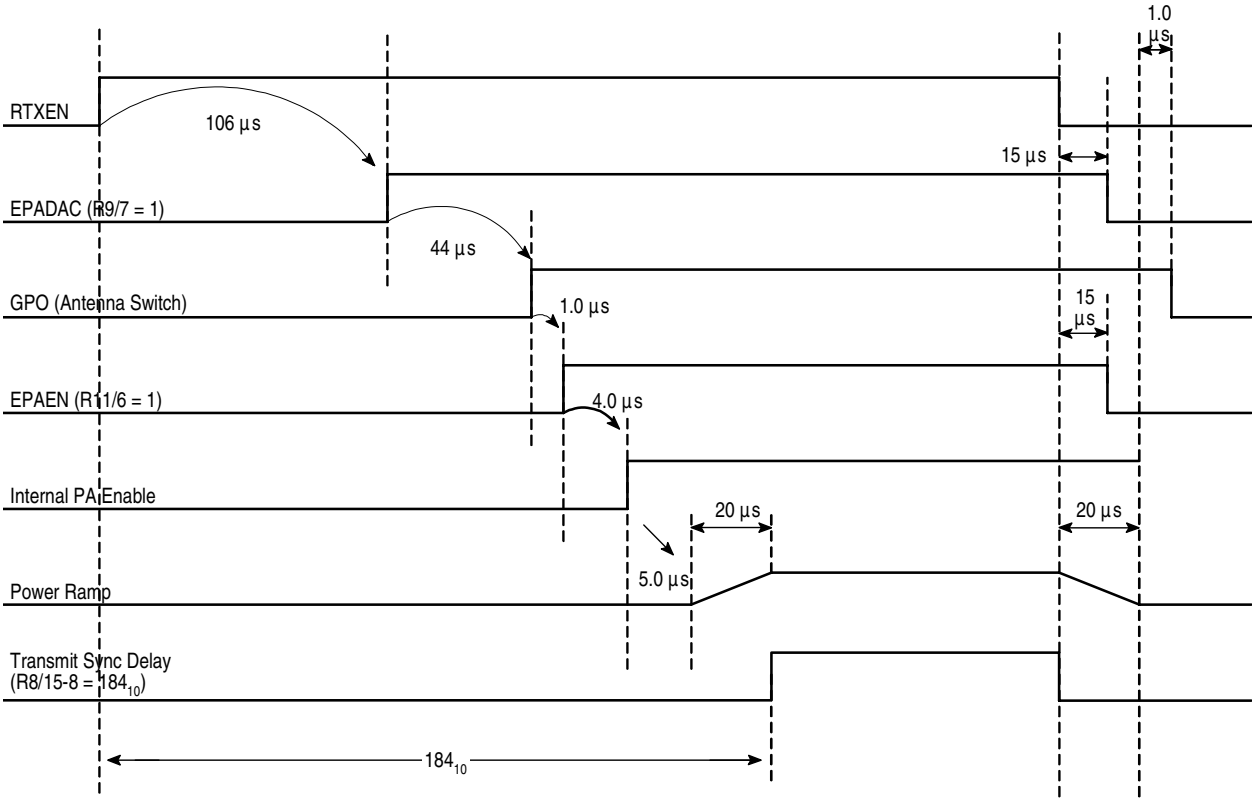


Figure 38. Ramp Generator (Transmit Cycle) Timing Diagram

5 Applications Information

5.1 General Purpose Output (GPO)

The GPO must be set to a logic one during a transmit cycle and set to a logic zero during a receive cycle via a SPI write operation, when driving an external antenna switch as shown in Figure 42. When the GPO is not actively used to drive a peripheral, R2/8 in the address register map is considered a don't care.

5.2 General Purpose Output Invert (GPO Invert)

The MC13180 General Purpose Output (GPO) Invert bit (R3/6) can be used to invert the output value of GPO located at Pin 9 of the device. The default setting for GPO Invert is zero (i.e., no inversion). When it is set to one, the GPO output pin assumes the inverted value of GPO in the register map location R2/8. This is a useful feature when an inverter is not available. It can serve as a complement to GPO Invert.

5.3 External Power Amplifier Enable (EPAEN)

The External Power Amplifier Enable (EPAEN) bit, R6/15, can be used in two applications. It may serve as a complementary driver to a dual-port antenna. This is accomplished when External PA Enable Invert, R3/10, is set to a logic one. In this configuration, EPAEN assumes the inverted value of GPO, which is the second driver for the antenna switch.

EPAEN may also assist in Class 1 operation by setting bit R11/6 to a logic high. This setting allows the MC13180 to drive an external power amplifer. Setting bits R11/6 and R3/10 to zero disables EPAEN.

5.4 External Power Amplifier DAC (EPADAC)

The Bluetooth specification for Class 1 Power implementation requires power control from 4.0 dBm (or less) to 20 dBm (max) power. The MC13180 external power amplifier digital to analog converter (EPADAC) output (Pin 10) provides a voltage reference for power control of an external power amplifier (PA), if desired.

The EPADAC output is enabled when External PA DAC Enable (R11/7) is set to one. Setting R11/7 to zero pulls the EPADAC output to ground. When enabled, the EPADAC output voltage is controlled by the PA DAC setting (R3/5-0). The minimum EPADAC output voltage is 0 Vdc and the maximum output voltage is 3.2 Vdc. The 6-bit resolution of the PA DAC setting corresponds to approximately 50 mV/bit. When using a $V_{CC}RF < 3.2$ Vdc, the maximum EPADAC output voltage is reduced to $V_{CC}RF$ (i.e., the full-scale output of the PA DAC is referenced to 3.2 V).

To obtain optimum functionality of EPADAC with an external PA, this feature should be utilized with the External PA Enable. Refer to the Applications Information section for additional usage information. The output of the EPADAC, when enabled, is gated by the MC13180 sequence manager. During a Sleep, Idle, or RX cycle, the output is set to zero volts. The programmed value of the output voltage is only achieved during an active TX cycle as shown in Figure 38.

5.5 PIN Implementation of Antenna Switch

An alternative approach to using an RF switch is to utilize a PIN diode technique as shown in Figure 39. When both PIN diodes are in the high resistance (i.e., un-biased) state, the transmitter is isolated from the antenna and LNA input. Conversely, when both PIN diodes are in the low resistance (i.e., forward-biased)

state, the λ/4 section appears as an open circuit from the transmitter output to the LNA input, and the transmitter output is coupled directly to the antenna through the bandpass filter. For receive mode, GPO is set low. For transmit mode, GPO is set high.

Some advantages to this implementation would be very low current consumption while in receive or idle mode, moderate current consumption while in transmit mode, high receiver isolation, and low cost.

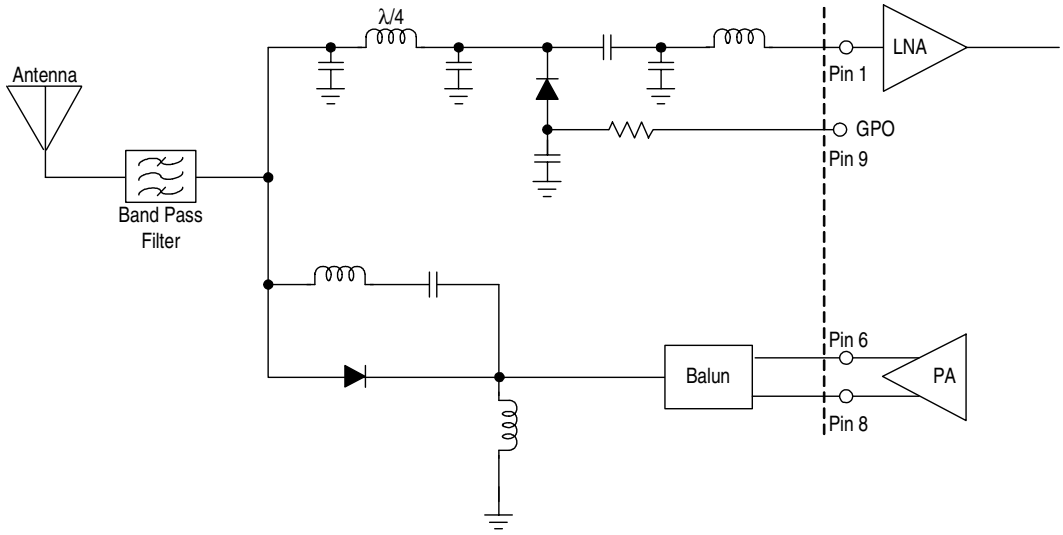


Figure 39. PIN Implementation of Antenna Switch

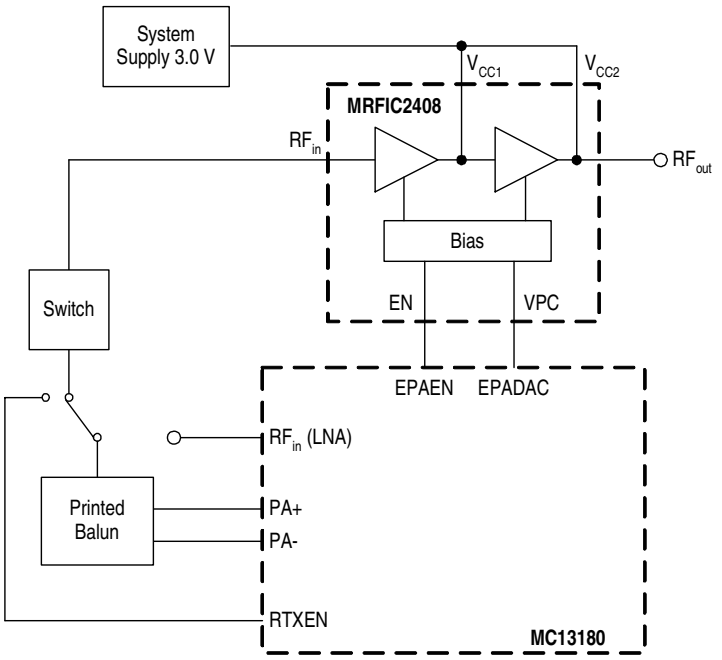
5.6 Class 1 Operation

Class 1 Operation can be realized by the MC13180 with the use of an external power amplifier (PA) such as the MRFIC2408 as shown in Figure 40. During a transmit cycle EPAEN drives the external PA Bias Enable. Figure 38 shows the transmitter warm up sequence for this mode of operation. The external PA is required to be fully powered within 5 µs. It is recommended that the antenna switch be set to the TX position before the internal PA is enabled. This option minimizes frequency pulling of the VCO, which may appear as splatter.

The power level of the external PA can be digitally controlled through the use of a digital-to-analog converter (EPADAC) internal to the MC13180. To access the DAC capability, External PA DAC Enable (R11/7), must be set to one.This line is generally decoupled with a small capacitor value (≈ 0.1 µF). Approximately 44 µs is available to fully charge this capacitor (see Figure 38).

5.7 Manufacturer Code

The format of the device identification code is shown in Figure 41. The 32-bit value is defined in the IEEE 1149.1 specification.



NOTE: MC13180 is used at 2.7 V, therefore EPAEN and EPADAC are 2.7 V lines that feed into the MRFIC2408. The MRFIC2408 is specified to operate at 3.0 V or above but is functional at 2.7 V with a slight degradation in performance.

Figure 40.

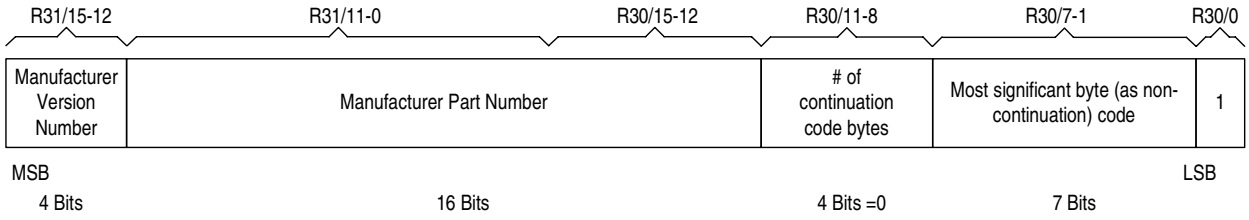


Figure 41. Manufacturer Identification Code

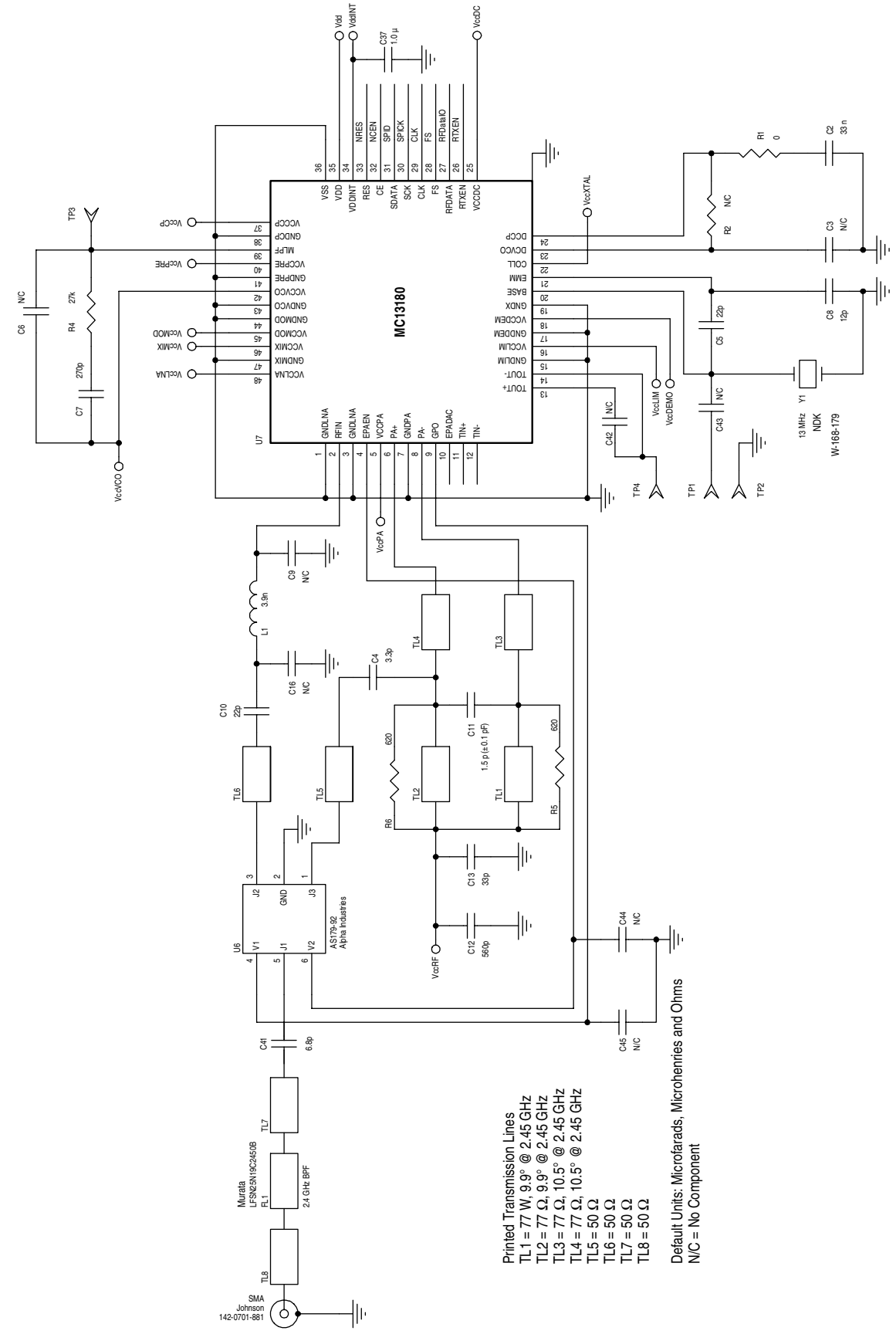
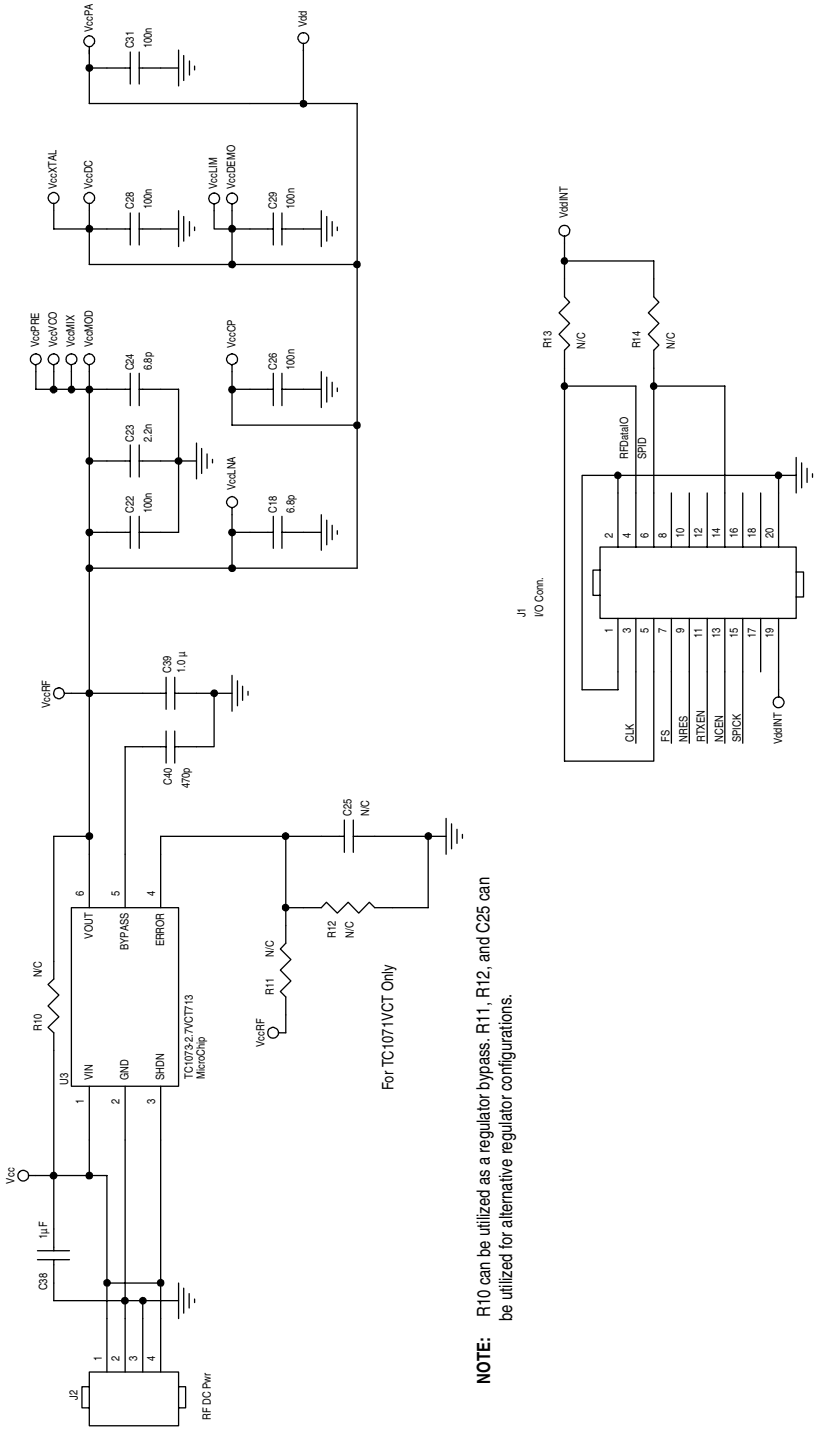


Figure 42. Application Evaluation Schematic
(Continued on Page 52)



NOTE: R10 can be utilized as a regulator bypass. R11, R12, and C25 can be utilized for alternative regulator configurations.

Figure 42 Application Evaluation Schematic (Continued)

6 Application Evaluation Printed Circuit Boards

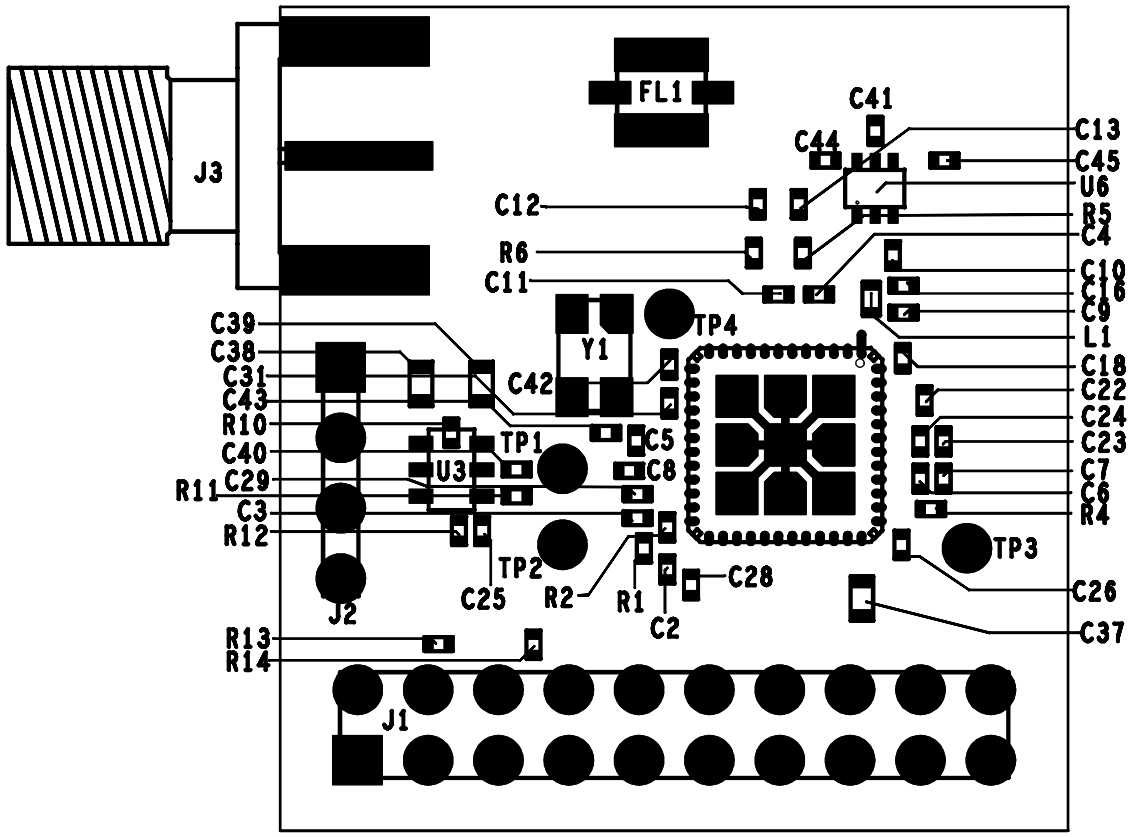


Figure 43. Application Evaluation PCB Assembly Diagram
(Not to Scale)

Table 24. Application Evaluation PCB Bill of Materials

REF	Size	Value	Part Number	Source
R1	0402	0	CR0402-16W-000	VENKEL
R2, 10, 11, 12, 13, 14	0402	N/C		
R4	0402	27 k	P27kjct-nd	Digikey
R5, R6	0402	620	P620kjct-nd	Digikey
C2	0402	33 n	PCC2140CT-ND	Digikey
C3, 6, 9, 16, 25, 42, 43, 44, 45	0402	N/C		
C4	0402	3.3 p	EVK105CH3R3JW	TAIYO YUDEN
C5, 10	0402	22 p	C0402COG500220JNE	VENKEL
C7	0402	270 p	PCC1714CT-ND	Digikey

N/C = No Component

Table 24. Application Evaluation PCB Bill of Materials (Continued)

REF	Size	Value	Part Number	Source
C8	0402	12 p	PCC120CQCT-ND	Digikey
C11	0402	1.5 p (±0.1 pF)	EVK105CH1R5BW	TAIYO YUDEN
C12	0402	560 p	C0402X7R500561JNE	VENKEL
C13	0402	33 p	C0402COG500330JNE	VENKEL
C18, 24, 41	0402	6.8 p	C0402COG5006R8JNE	VENKEL
C22, 26, 28, 29, 31	0402	100 n	C0402X7R500104JNE	VENKEL
C23	0402	2.2 n	PCC222BQCT-ND	Digikey
C37, 38, 39	0603	1.0 µ	LMK107F105ZA	TAIYO YUDEN
C40	0402	470 p	PCC471BQCT-ND	Digikey
L1	0402	3.9 n	HK1005-3N9S	TAIYO YUDEN
U7	QFN-48	Transceiver	MC13180	Motorola
U6	SC-706	RF Switch	AS179-92	Alpha Indust.
Y1	2.5 x 4 mm	13 MHz	W-168-179	NDK
FL1	2.5 X 3.2 mm	2.4 GHz	LFSN25N19C2450BAHA504	Murata
U3 (standard)	SOT-23-6	2.7 V	TC1073-2.7VCH713	Microchip
U3 (optional)	SOT-23-5	Adjustable	TC1071VCT	Microchip
J1	10 X 2	Socket	66956-010	Newark
J2	2 X 1	Connector	22-05-3021	Newark
SMA	SMA	Connector	142-0701-881	Johnson

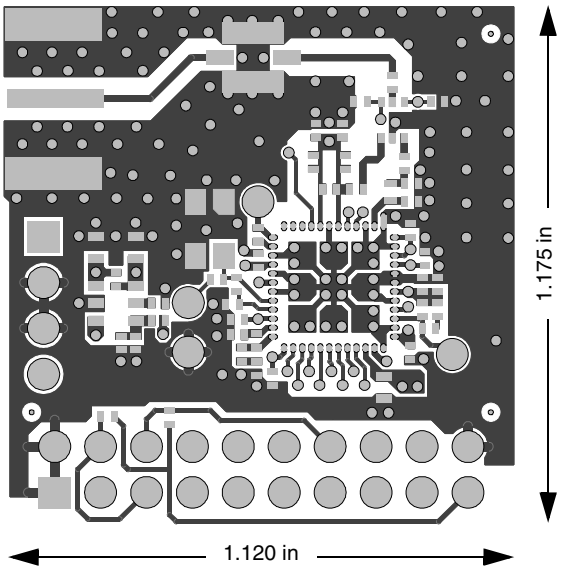


Figure 44. Top Side

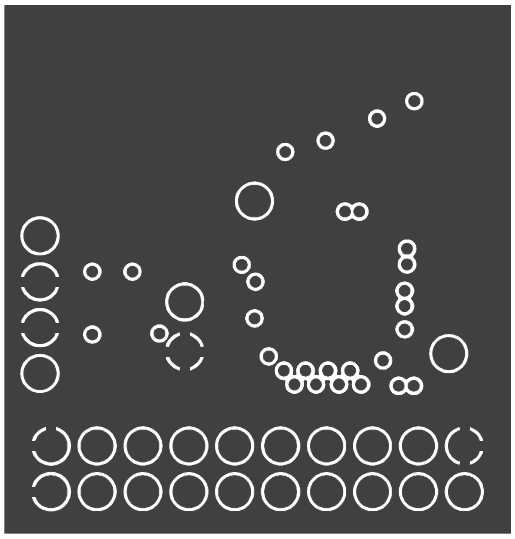


Figure 45. Ground Plane

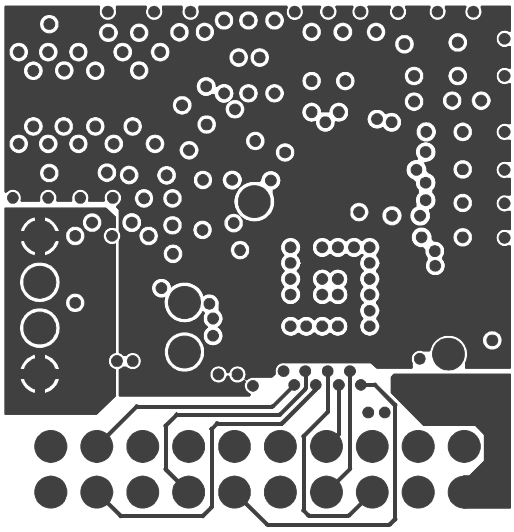


Figure 46. VCC Plane

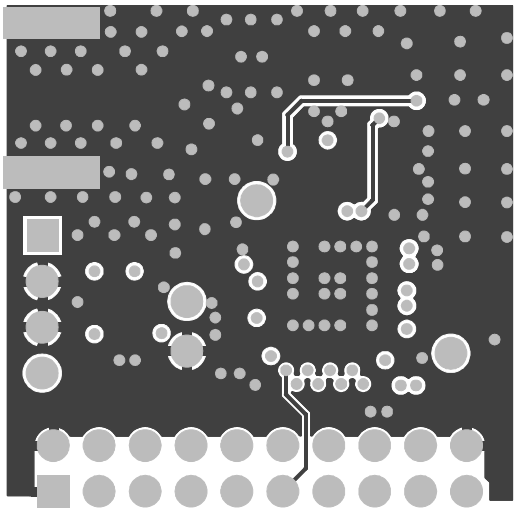
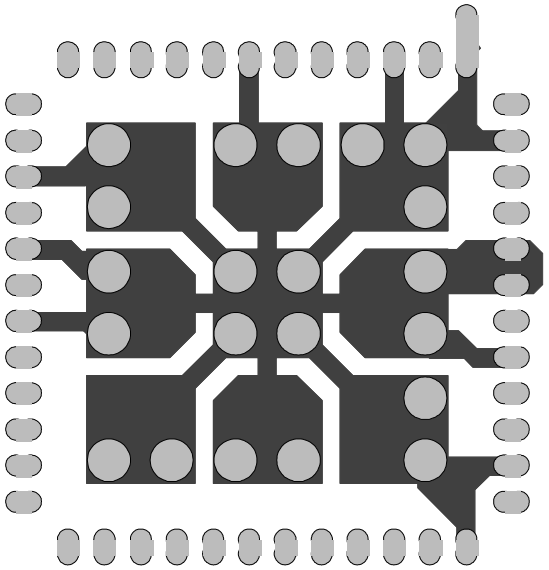


Figure 47. Bottom Plane



NOTE:
Solder Paste: SMQ92J, Indium Corp
Solder Stencil Thickness: 5 mils screen
Solder Stencil QFN Ground Flag Area: 80% of sodlerable area
Solder Stencil QFN Lead Pad Area: 100% of solderable area

The ground flag requires good condition for optimum intermodulation and C/I performance.

Figure 48. Recommended QFN Ground Flag Configuration

7 Packaging

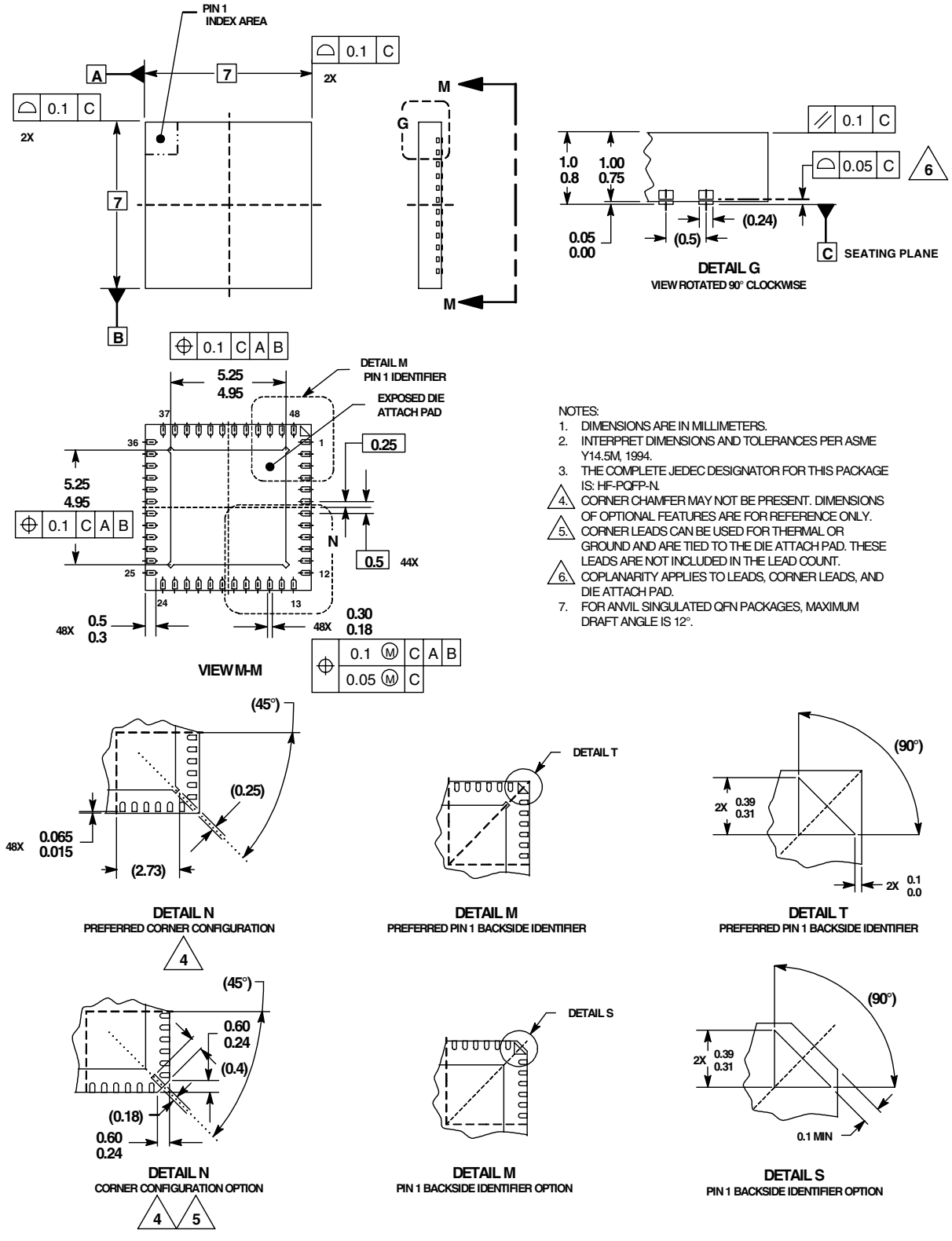


Figure 49. Outline Dimensions for QFN-48
(Case 1314-02, Issue C)

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