

# TTL ISOPLANAR MEMORY 93L422

## 256×4-BIT FULLY DECODED RANDOM ACCESS MEMORY

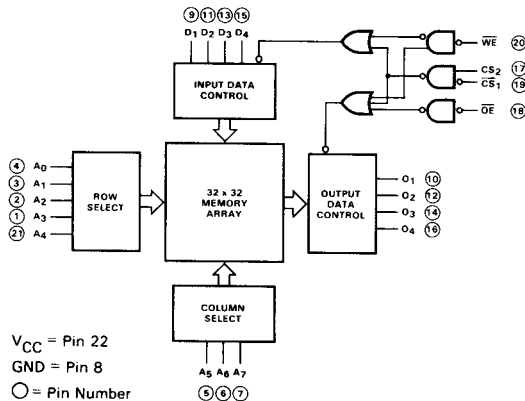
**DESCRIPTION** – The 93L422 is a 1024-bit Read/Write Random Access Memory organized 256 words by four bits per word. The 93L422 has 3-state outputs, and is designed primarily for buffer control storage and high performance main memory applications. The device has a typical address access time of 45 ns.

- ISOPLANAR TECHNOLOGY
- ORGANIZATION – 256 WORDS X 4 BITS
- 3-STATE OUTPUTS
- STANDARD 22-PIN DUAL IN-LINE PACKAGE
- TWO CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- LOW POWER DISSIPATION – 0.27 mW/BIT TYP
- TYPICAL READ ACCESS TIME – 45 ns

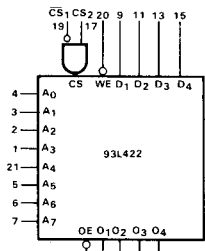
### PIN NAMES

A <sub>0</sub> – A <sub>7</sub>	Address Inputs
D <sub>1</sub> – D <sub>4</sub>	Data Inputs
$\overline{CS}_1$ , CS <sub>2</sub>	Chip Select Inputs
WE	Write Enable Input
O <sub>1</sub> – O <sub>4</sub>	Data Outputs
OE	Output Enable

### LOGIC DIAGRAM



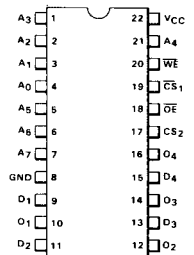
### LOGIC SYMBOL



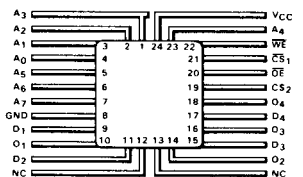
V<sub>CC</sub> = Pin 22

GND = Pin 8

### CONNECTION DIAGRAMS DIP (TOP VIEW)



### FLATPAK (TOP VIEW)



# FAIRCHILD ISOPLANAR TTL MEMORY • 93L422

**FUNCTIONAL DESCRIPTION** – The 93L422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A<sub>0</sub> thru A<sub>7</sub>.

Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, WE (pin 20). With WE held LOW and the chip selected, the data at D<sub>IN</sub> is written into the addressed location. To read, WE is held HIGH and the chip selected. Data in the specified location is presented at D<sub>OUT</sub>.

**TRUTH TABLE**

INPUTS				OUTPUTS		MODE
OE PIN 18	CS <sub>1</sub> PIN 19	CS <sub>2</sub> PIN 17	WE PIN 20	D <sub>1</sub> – D <sub>4</sub> PINS 9, 11, 13 15	93L422 3-STATE	
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	O <sub>1</sub> – O <sub>4</sub>	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage; L = LOW Voltage; X = Don't Care (HIGH or LOW); HIGH Z = High Impedance.

**ABSOLUTE MAXIMUM RATINGS** (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V <sub>CC</sub> Lead Potential to Ground Lead	–0.5 V to +7.0 V
Input Voltage (dc)*	–0.5 V to +5.5 V
Input Current (dc)*	–12 mA to +5.0 mA
Voltage Applied to Outputs (output HIGH)**	–0.5 V to +5.50 V
Output Current (dc)	+20 mA

\*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

\*\*Output Current Limit Required.

**GUARANTEED OPERATING RANGES**

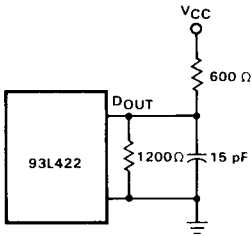
PART NUMBER	SUPPLY VOLTAGE (V <sub>CC</sub> )			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93L422XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L422XM	4.50 V	5.0 V	5.50 V	–55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

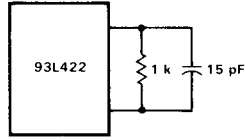
# FAIRCHILD ISOPLANAR TTL MEMORY • 93L422

## AC TEST LOAD AND WAVEFORM

### LOADING CONDITIONS



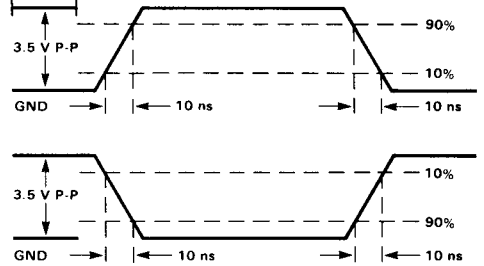
Load A



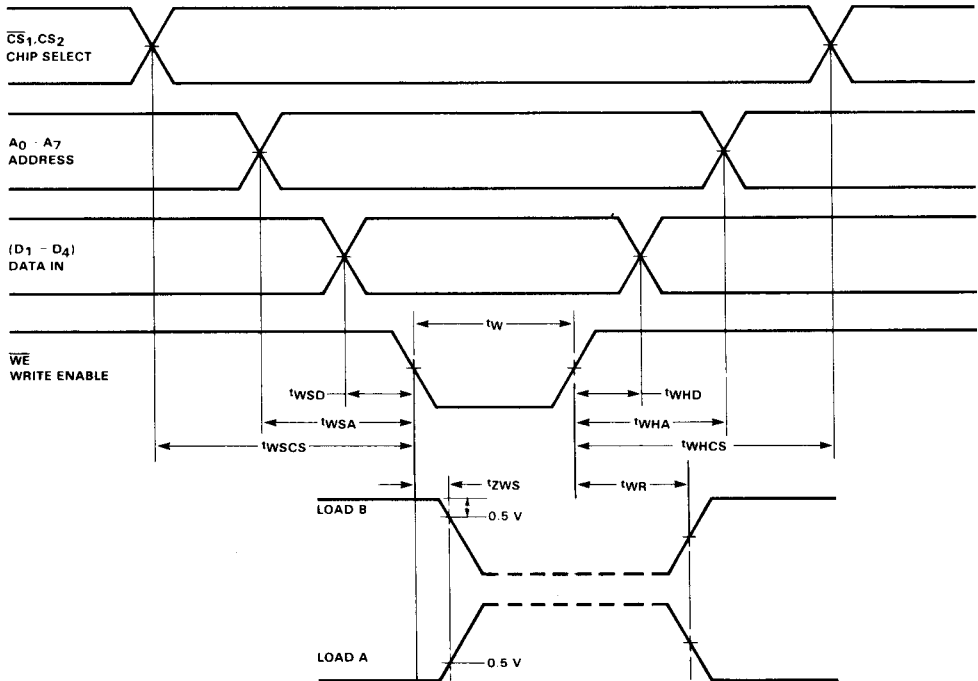
Load B

### INPUT PULSES

#### ALL INPUT PULSES



### WRITE MODE



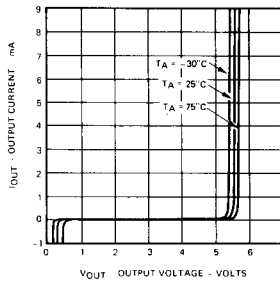
(All above measurements referenced to 1.5 V unless otherwise indicated)

NOTES:

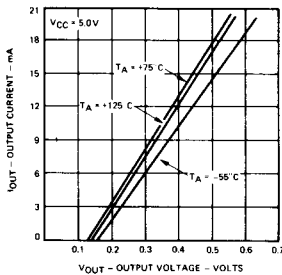
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at  $V_{CC} = 5.0\text{ V}$ ,  $T_A = +25^\circ\text{C}$ , and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:  
 $\theta_{JA}$  (Junction to Ambient) (at 400 fpm air flow) =  $50^\circ\text{C/Watt}$ , Ceramic DIP;  $65^\circ\text{C/Watt}$ , Plastic DIP; NA, Flatpak.  
 $\theta_{JA}$  (Junction to Ambient) (still air) =  $90^\circ\text{C/Watt}$ , Ceramic DIP;  $110^\circ\text{C/Watt}$ , Plastic DIP; NA, Flatpak.  
 $\theta_{JC}$  (Junction to Case) =  $25^\circ\text{C/Watt}$ , Ceramic DIP;  $25^\circ\text{C/Watt}$ , Plastic DIP;  $15^\circ\text{C/Watt}$ , Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6.  $t_W$  measured at  $t_{WSA} = \text{MIN}$ ,  $t_{WSA}$  measured at  $t_W = \text{MIN}$ .
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

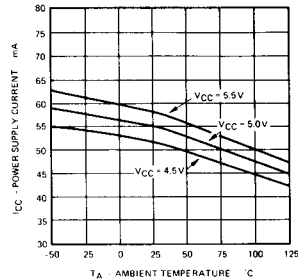
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



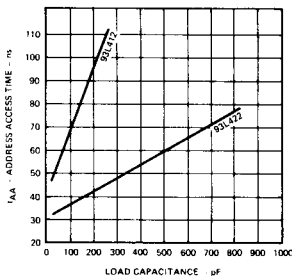
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



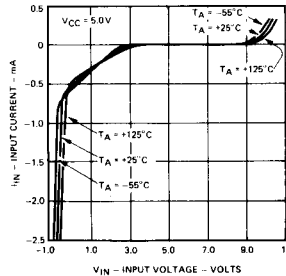
POWER SUPPLY CURRENT VERSUS TEMPERATURE



ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



# FAIRCHILD ISOPLANAR TTL MEMORY • 93L422

## DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX		
$V_{OL}$	Output LOW Voltage		0.3	0.45	V	$V_{CC} = \text{MIN}, I_{OL} = 8 \text{ mA}$
$V_{IH}$	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
$V_{IL}$	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
$I_{IL}$	Input LOW Current		-150	-300	$\mu\text{A}$	$V_{CC} = \text{MAX}, V_{IN} = 0.4 \text{ V}$
$I_{IH}$	Input HIGH Current		1.0	40	$\mu\text{A}$	$V_{CC} = \text{MAX}, V_{IN} = 4.5 \text{ V}$
				1.0	mA	$V_{CC} = \text{MAX}, V_{IN} = 5.25 \text{ V}$
$V_{CD}$	Input Diode Clamp Voltage		-1.0	-1.5	V	$V_{CC} = \text{MAX}, I_N = -10 \text{ mA}$
$I_{OFF}$	Output Current (HIGH Z)			50	$\mu\text{A}$	$V_{CC} = \text{MAX}, V_{OUT} = 2.4 \text{ V}$
				-50		$V_{CC} = \text{MAX}, V_{OUT} = 0.5 \text{ V}$
$V_{OH}$	Output HIGH Voltage	2.4			V	$V_{CC} = \text{MIN}, I_{OH} = -5.2 \text{ mA}$
$I_{OS}$	Output Current Short Circuit to Ground			-70	mA	$V_{CC} = \text{MAX}, \text{Note 7}$
$I_{CC}$	Power Supply Current		55	75	mA	$T_A = +75^\circ\text{C}$ $T_A = 0^\circ\text{C}$ $T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ $V_{CC} = \text{MAX},$ All Inputs and Outputs Open
		93L422XC	60	80		
		93L422XM	50	70		
		93L422XM	65	90		

## AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93L422XC*			93L422XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
$t_{ACS}$	Chip Select Time		20	35		20	45	ns	See Test Circuit and Waveforms
$t_{ZRCS}$	Chip Select to HIGH Z		20	35		20	45		
$t_{AOS}$	Output Enable Time		20	35		20	45		
$t_{ZROS}$	Output Enable to HIGH Z		20	35		20	45		
$t_{AA}$	Address Access Time		45	60		45	75		
WRITE MODE	DELAY TIMES								
$t_{ZWS}$	Write Disable to HIGH Z		20	40		20	45	ns	
$t_{WR}$	Write Recovery Time		25	45		25	50		
	INPUT TIMING REQUIREMENTS							ns	See Test Circuit and Waveforms
$t_W$	Write Pulse Width (to guarantee write)	45	30		55	35			
$t_{WSD}$	Data Set-Up Time Prior to Write	5	0		5	0			
$t_{WHD}$	Data Hold Time After Write	5	0		5	0			
$t_{WSA}$	Address Set-Up Time	10	0		10	0			
$t_{WHA}$	Address Hold Time	5	0		10	0			
$t_{WSCS}$	Chip Select Set-Up Time	5	0		5	0			
$t_{WHCS}$	Chip Select Hold Time	5	0		10	0			
$C_I$	Input Pin Capacitance		3	5		3	5	pF	Measure with Pulse Technique
$C_O$	Output Pin Capacitance		5	8		5	8		

\*93L422XC with the specified ac characteristics will be available starting First Quarter 1977.

