

DATA SHEET



MOS INTEGRATED CIRCUIT
μPD6372

16 BIT D/A CONVERTER

The μPD6372 is a 16-bit D/A converter for digital audio equipment.

Resistance strings system and built-in 0-point offset circuit realizes high sound quality. This CMOS LSI operates on +5 V single power supply with low current consumption.

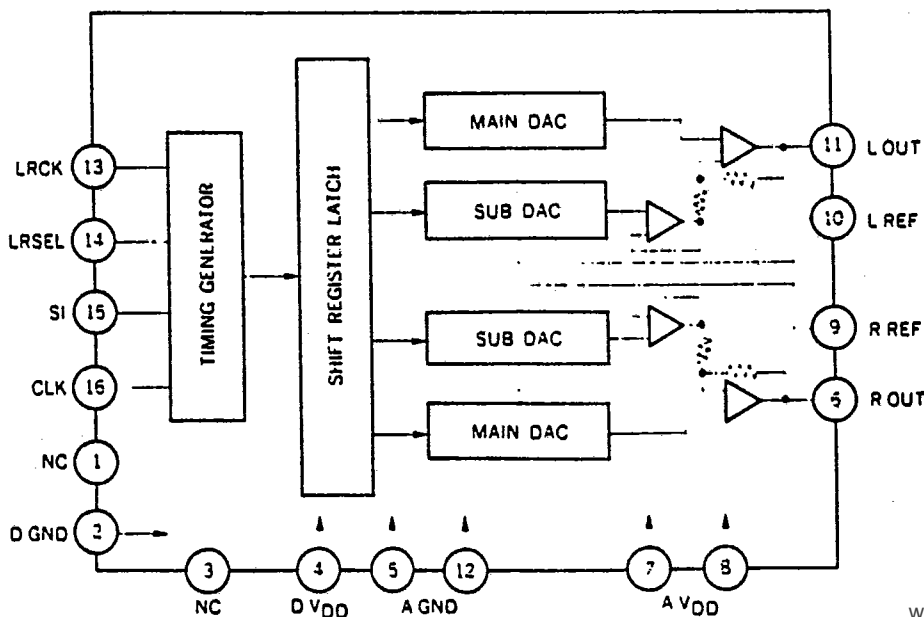
FEATURES

- +5 V single power supply
- CMOS configuration
- Built-in output operational amplifier
- Built-in 0-point offset circuit
- Resistance strings system
- 4 f_s (2 channels x 200 kHz) capability
- Built-in 2 channel DAC
- Symmetrical phase output

ORDERING INFORMATION

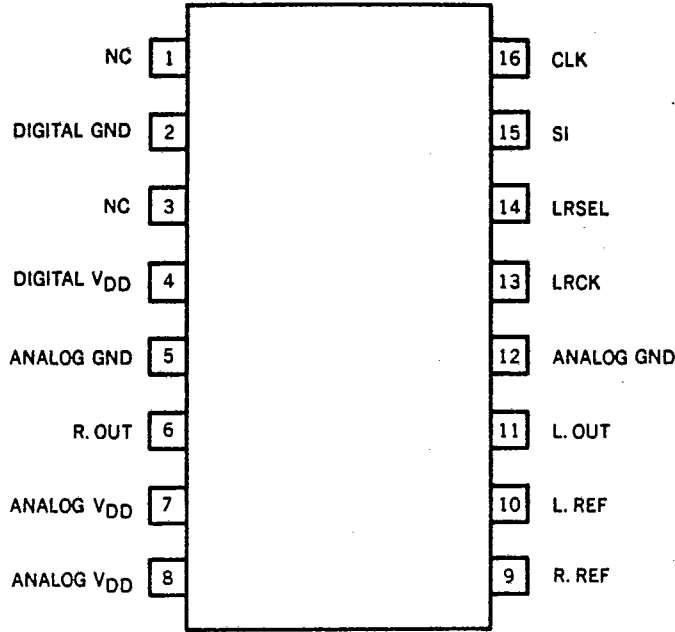
| Part Number | Package |
|-------------|------------------------------|
| μPD6372CX | 16-Pin Plastic DIP (300 mil) |
| μPD6372GS | 16-Pin Plastic SOP (300mil) |

BLOCK DIAGRAM



www.DataSheet4U.com

PIN CONNECTION (Top View)



ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

| | | | |
|-----------------------|-----------|----------------------|------------------|
| Supply Voltage | V_{DD} | -0.3 to +7.0 | V |
| Output Pin Voltage | V_{OUT} | -0.3 to $V_{DD}+0.3$ | V |
| Logic Input Voltage | V_{IN} | -0.3 to $V_{DD}+0.3$ | V |
| Operating Temperature | T_{opt} | -20 to +75 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -40 to +125 | $^\circ\text{C}$ |

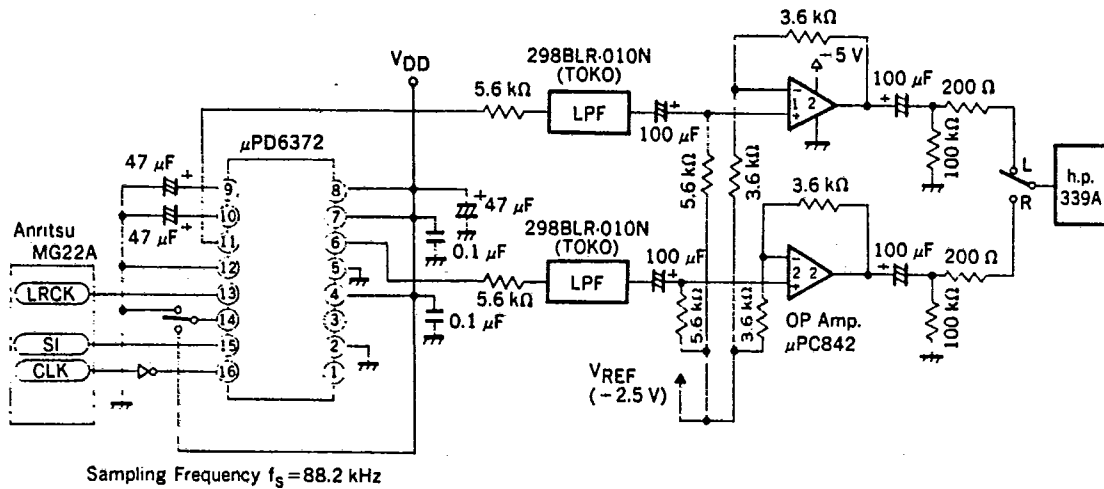
RECOMMENDED OPERATING CONDITIONS ($T_a = 25^\circ\text{C}$)

| ITEM | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|----------------------------|-----------|---------------------------------|------|------|------------------|
| Supply Voltage Range | V_{DD} | 4.5 to 5.5 | | | V |
| Digital High Level Input | V_{IH} | 0.7 $\times V_{DD}$ to V_{DD} | | | V |
| Digital Low Level Input | V_{IL} | 0 to 0.3 $\times V_{DD}$ | | | V |
| Ambient Temperature | T_a | -20 to 75 | | | $^\circ\text{C}$ |
| Load Resistance (6, 11pin) | R_L | 5 | | | $k\Omega$ |
| Sampling Frequency | f_s | | | 200 | kHz |
| Clock Frequency | f_{CLK} | | | 10 | MHz |
| Clock Pulse Width | t_{SCK} | 40 | | | ns |
| SI, LRCK Setup Time | t_{DC} | 12 | | | ns |
| SI, LRCK Hold Time | t_{CD} | 12 | | | ns |

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{DD} = +5\text{V}$)

| ITEM | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITION |
|-----------------------------|----------|------|------|------|-----------|--|
| Resolution | RES | | 16 | | Bit | |
| Total Harmonic Distortion 1 | THD_1 | | 0.04 | 0.1 | % | $f_{IN} = 1\text{ kHz}$, 0 dB |
| Total Harmonic Distortion 2 | THD_2 | | 0.1 | 0.4 | % | $f_{IN} = 1\text{ kHz}$, -20 dB |
| Full Scale Output Voltage | V_{FS} | | 2.0 | 2.3 | V_{p-p} | |
| Cross Talk | C.T | 85 | 95 | | dB | One Side Channel 0 dB, $f_{IN} = 1\text{ kHz}$ |
| S/N Ratio | S/N | 90 | | | dB | JIS-A |
| Dynamic Range | D.R | 92 | | | dB | $f_{IN} = 1\text{ kHz}$, -60 dB |
| Supply Current | I_{DD} | | 6.0 | 12 | mA | $f_{IN} = 1\text{ kHz}$, 0 dB |

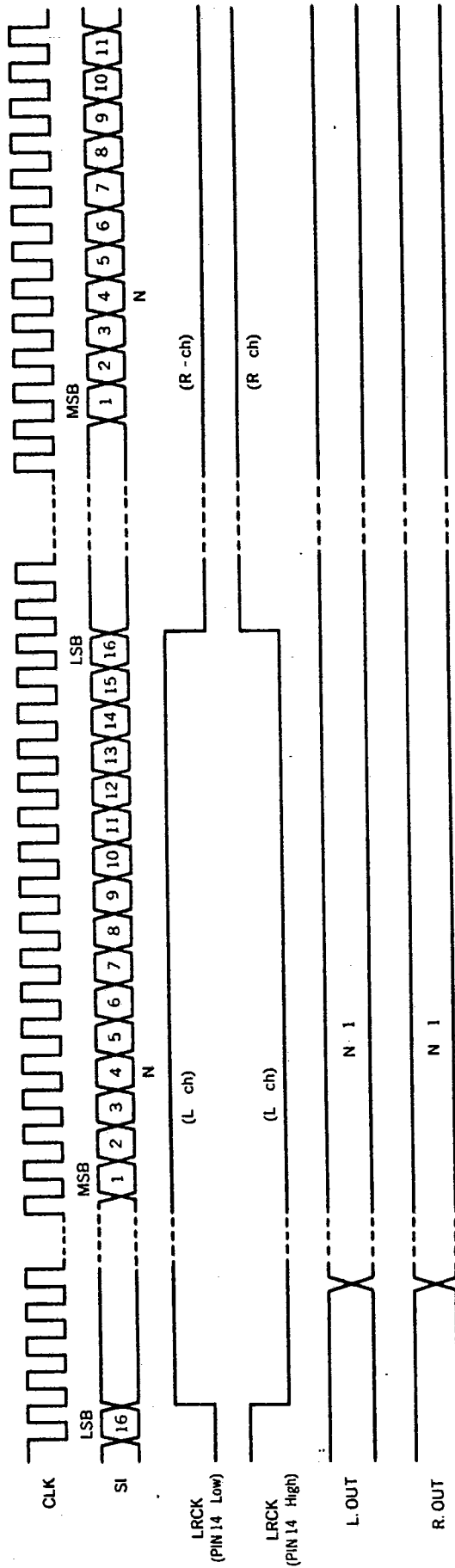
TEST CIRCUIT



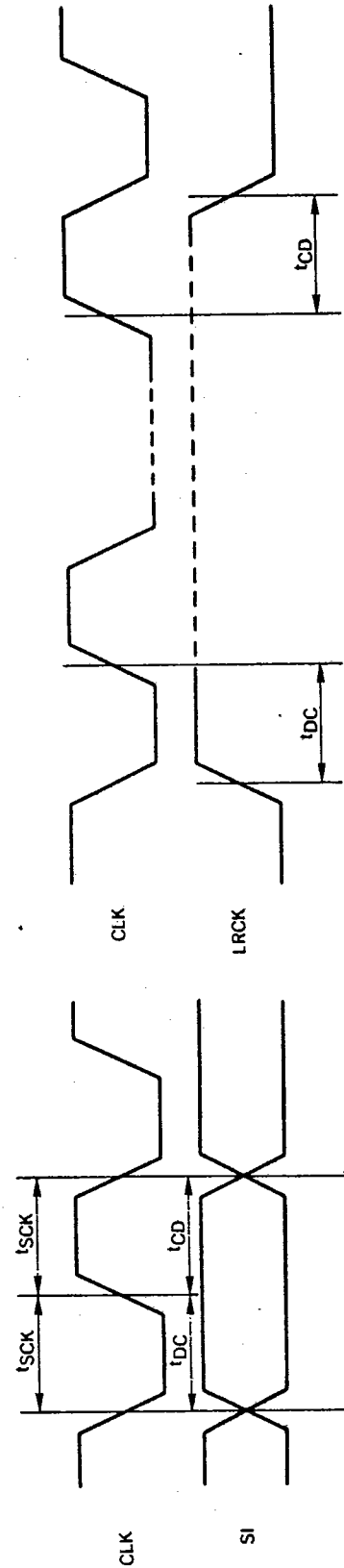
TERMINAL FUNCTION

| TERMINAL NO. | SYMBOL | TERMINAL NAME | DESCRIPTION | Input/Output |
|--------------|--------|------------------------|--|--------------|
| 1 | NC | Non Connection | - | |
| 2 | D.GND | Digital GND | Ground terminal for the logic circuit | |
| 3 | NC | Non Connection | - | |
| 4 | D.VDD | Digital VDD | Power supply terminal for the logic circuit | |
| 5 | A.GND | Analog GND | Ground terminal for the analog circuit | |
| 6 | R.OUT | R-ch OUTPUT | Output terminal for the right analog signal | Output |
| 7 | A.VDD | Analog VDD | Power supply terminal for the analog circuit | |
| 9 | R.REF | R-ch Voltage Reference | Operational Amplifier reference bias terminal. Normally connected to A.GND via a capacity. | |
| 10 | L.REF | L-ch Voltage Reference | | |
| 11 | L.OUT | L-ch OUTPUT | Output terminal for the left analog signal | Output |
| 12 | A.GND | Analog GND | Output terminal for the left analog signal | |
| 13 | LRCK | Left/Right Clock | Input terminal for left/right identification signal. | Input |
| 14 | LRSEL | Left/Right Selection | Left/right selection terminal for LRCK signal. At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input. At "Low" of LRCK signal, set LRSEL pin at "High" for L-ch DATA input. | Input |
| 15 | SI | Series Input | Input terminal for L-ch and R-ch serial data. | Input |
| 16 | CLK | Clock | Input terminal for read clock of serial input data | Input |

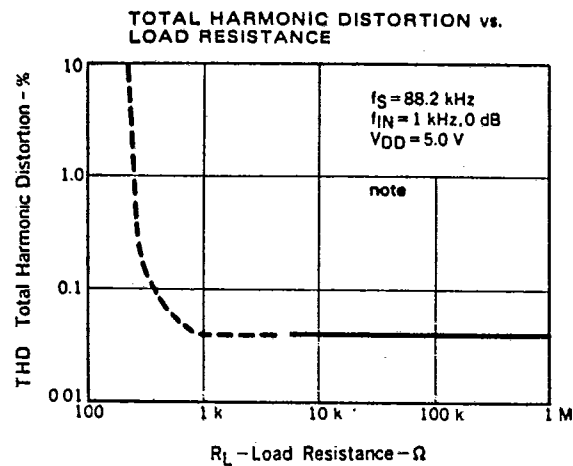
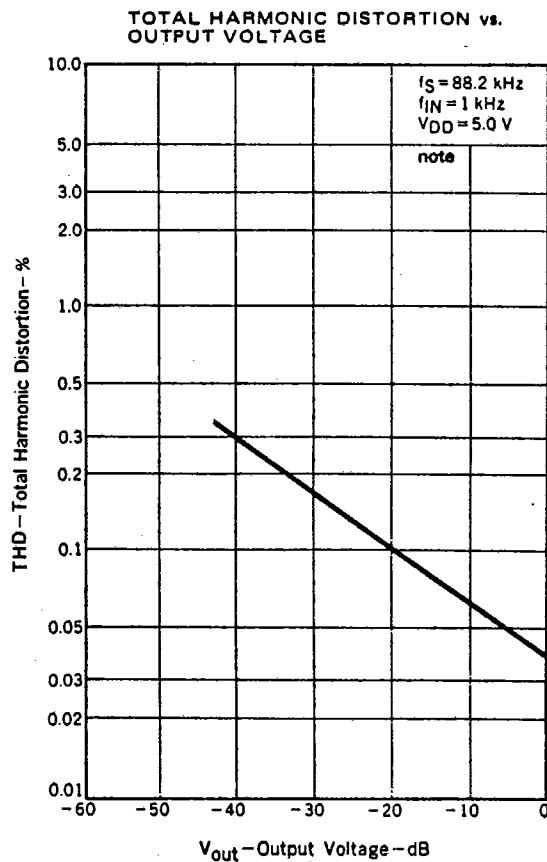
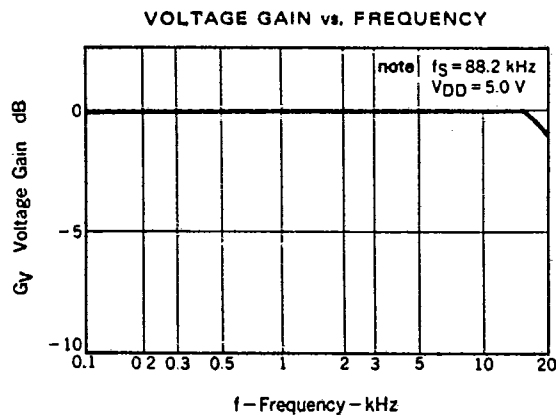
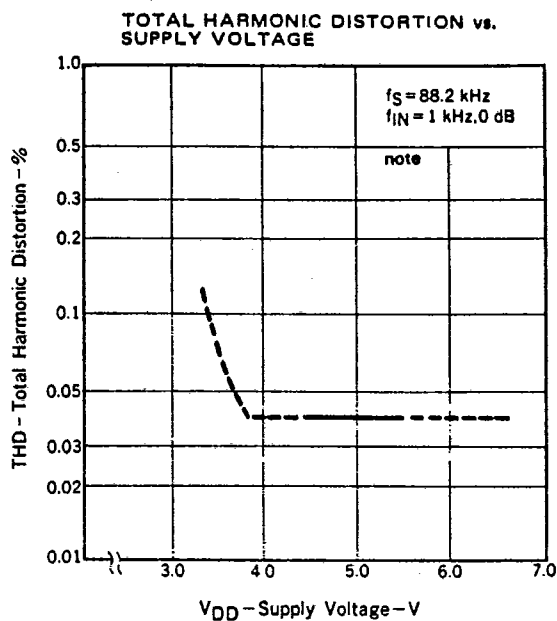
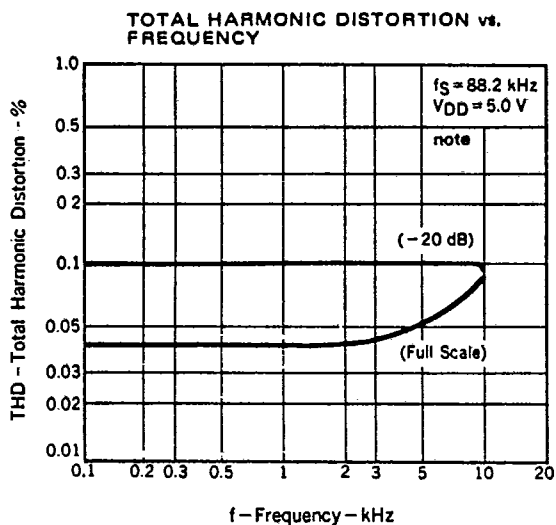
TIMING CHART



(NOTICE) At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input.
 At "Low" of LRCK signal, set LRSEL pin at "High" for L ch DATA input.

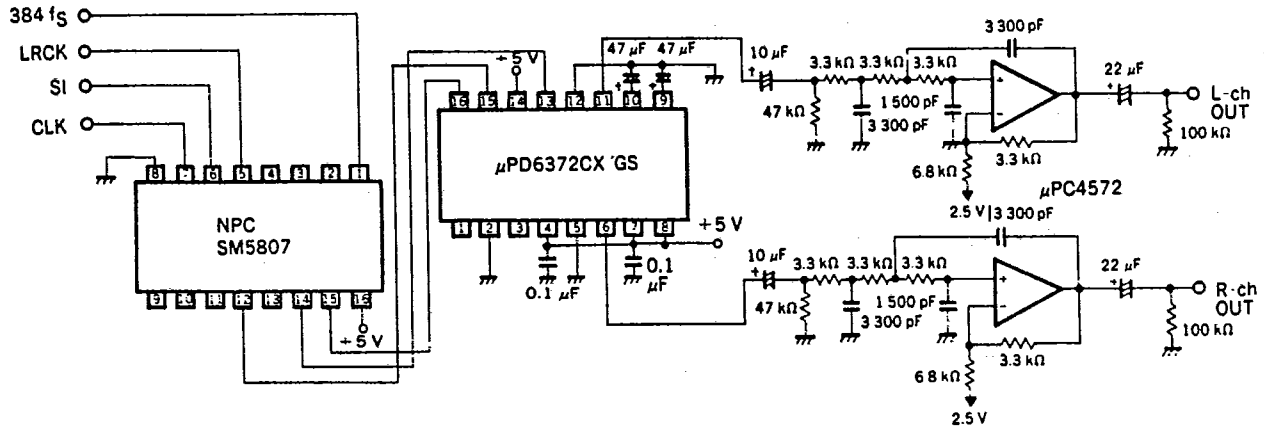


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

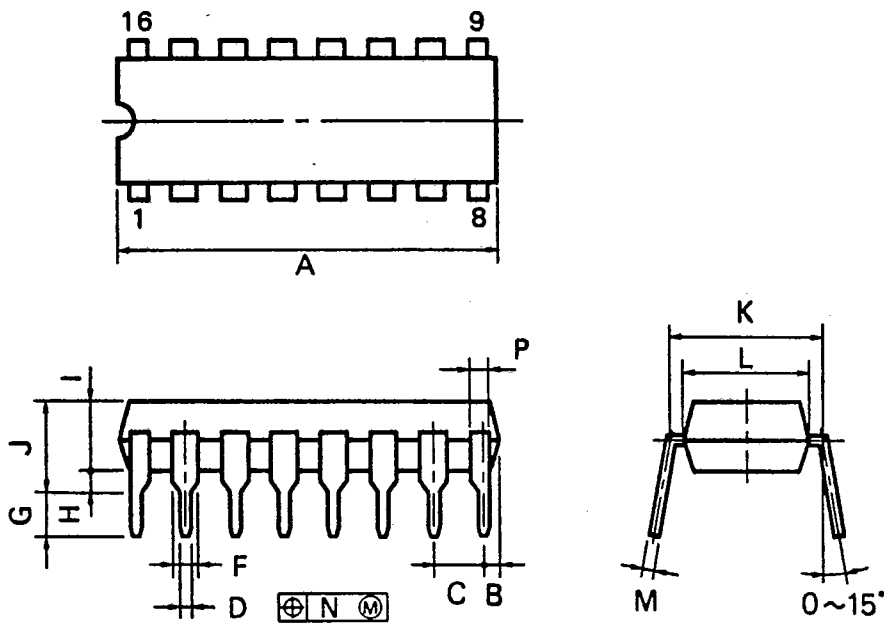


note. 20 kHz Low Pass Filter
: 298BLR-010N (TOKO)

APPLICATION CIRCUIT



16 PIN PLASTIC DIP (300 mil)



P16C-100-300B

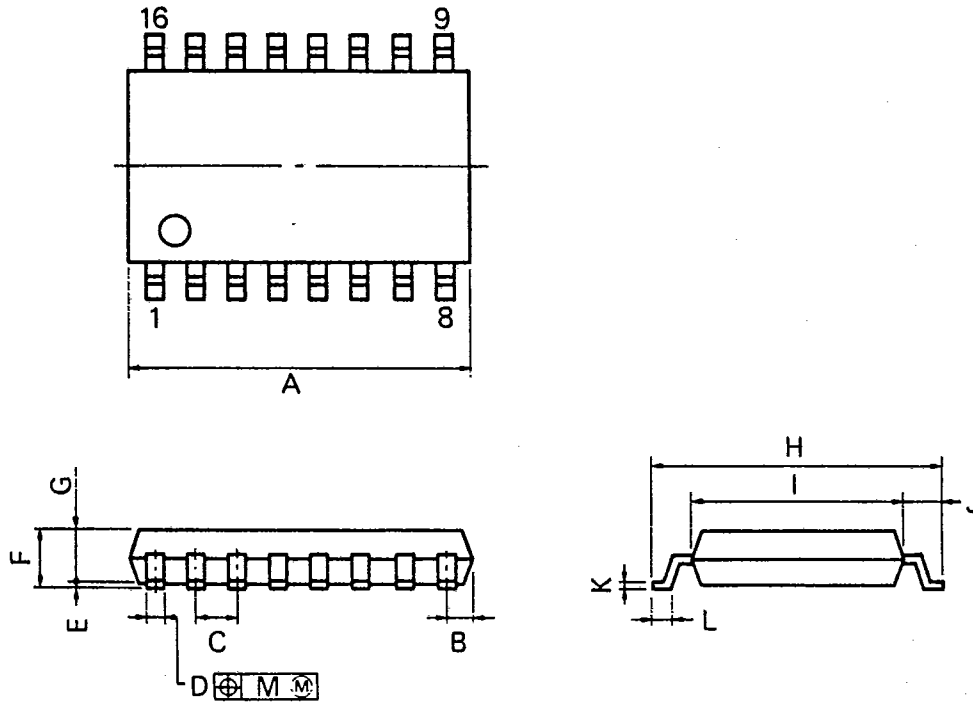
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|------|-----------------------|-------------------------|
| A | 20.32 MAX. | 0.800 MAX. |
| B | 1.27 MAX. | 0.050 MAX. |
| C | 2.54 (T.P.) | 0.100 (T.P.) |
| D | 0.50 ^{+0.10} | 0.020 ^{+0.004} |
| F | 1.1 MIN. | 0.043 MIN. |
| G | 3.5 ^{+0.3} | 0.138 ^{+0.012} |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 7.62 (T.P.) | 0.300 (T.P.) |
| L | 6.5 | 0.256 |
| M | 0.25 ^{+0.10} | 0.010 ^{+0.003} |
| N | 0.25 | 0.01 |
| P | 1.1 MIN. | 0.043 MIN. |

T-51-09-16

16 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P16GM-50-3008-1

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 10.46 MAX. | 0.412 MAX. |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40 ^{0.010} / _{0.009} | 0.016 ^{0.004} / _{0.003} |
| E | 0.1 ^{0.01} | 0.004 ^{0.004} |
| F | 1.8 MAX. | 0.071 MAX. |
| G | 1.55 | 0.061 |
| H | 7.7 ^{0.3} | 0.303 ^{0.012} |
| I | 5.6 | 0.220 |
| J | 1.1 | 0.043 |
| K | 0.20 ^{0.010} / _{0.009} | 0.008 ^{0.004} / _{0.003} |
| L | 0.6 ^{0.2} | 0.024 ^{0.008} / _{0.009} |
| M | 0.12 | 0.005 |