Am8152A/Am8152B

Video System Controller (VSC)

FINAL

DISTINCTIVE CHARACTERISTICS

- Am8152A with Video Dot Clock Rate up to 80 MHz
  Am8152B with Video Dot Clock Rate up to 40 MHz
- Four-level current driven (75Ω) differential video output
- Digital Video output
- On-board crystal driven oscillator
- Proportional Spacing Support (2–17 dots)
- 9-bit dot data parallel input, with expansion capability to seventeen bits
- Trailing blanks (0–3 dots)
- Double Width Characters
- Attribute Support: Character Blink, Underline, Overstrike, Reverse, and Highlight
- Buffered and Synchronized Character Clock Outputs
- Background color selection
- Buffered and Synchronized Vertical and Horizontal Sync Outputs

GENERAL DESCRIPTION

The Am8152A/Am8152B Video System Controller (VSC) provides the interface between a CRT controller and a CRT monitor. The basic chip functions are:

- Support proportional and non-proportional character display
- Correctly synchronize and mix character attributes with video signals
- Output the video information in a four-level analog or digital format
- Serialize parallel video data

The VSC consists of a parallel-to-serial converter which provides a video bit stream to on-chip attribute logic. This logic, under control of the attribute inputs, operates on the bit stream to generate grey scale video. Video outputs from the VSC are of two forms — analog and digital. The digitally encoded outputs implement four video levels: Blank, Black, Grey and White. Identical information is available in analog form via differential outputs (current driven) into a nominal 75Ω impedance.

The Am8152A/Am8152B also supports proportional spacing using a bit width programmable character clock. Character ROM pixel information is selectable from two to seventeen pixels per character. Up to three blank pixels can be appended to the character ROM input thereby facilitating right justification of text.

The difference between the Am8152A and the Am8152B is that the Am8152A operates up to 80 MHz, while the Am8152B operates up to 40 MHz. When using the PLL, the lower operating frequency limit is 20 MHz.

The Am8152A/Am8152B is fabricated using AMD's advanced bipolar process with internal ECL logic. The device is available in conventional 48-pin dual in-line package as well as the surface mounted 68-pin PLCC package.

BLOCK DIAGRAM

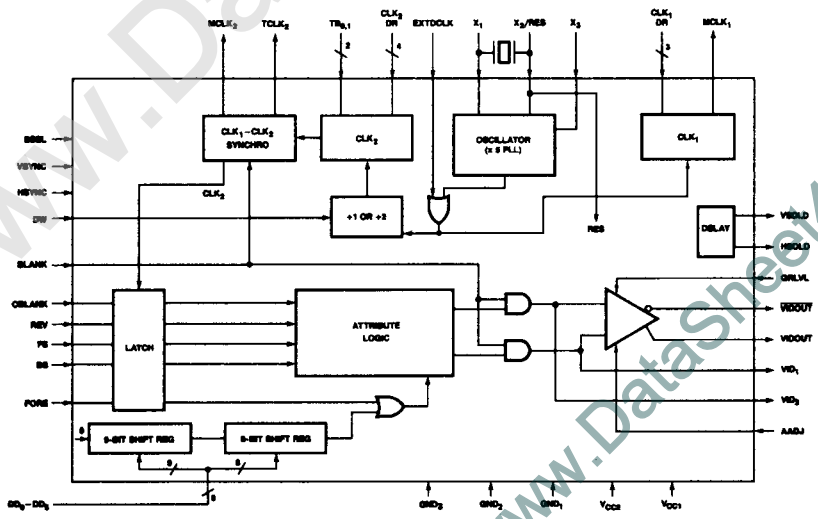

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Figure 1.

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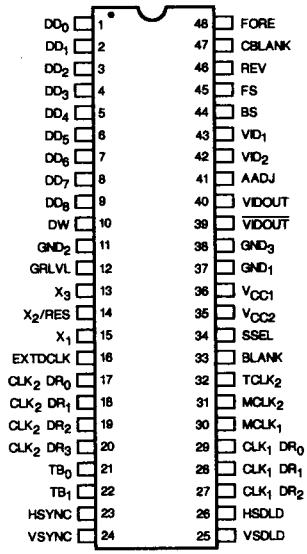
Issue Date: October 1986

CONNECTION DIAGRAM
Top View



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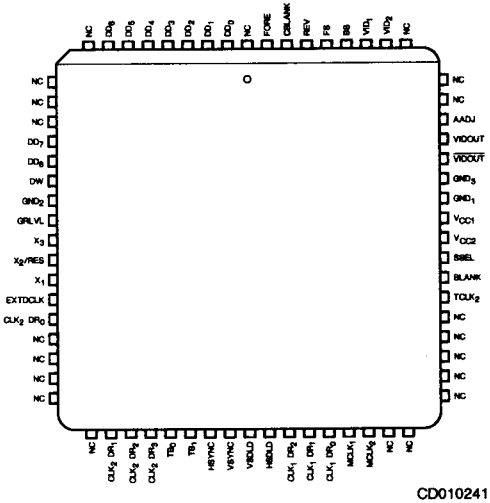

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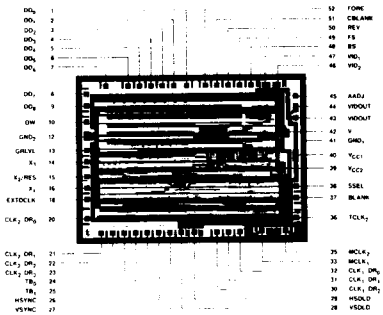
Note: Pin 1 is marked for orientation

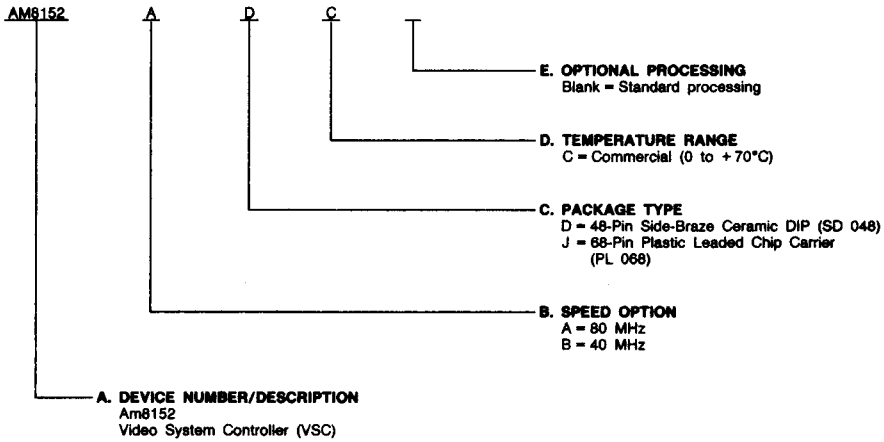
METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM8152A AM8152B	DC, JC

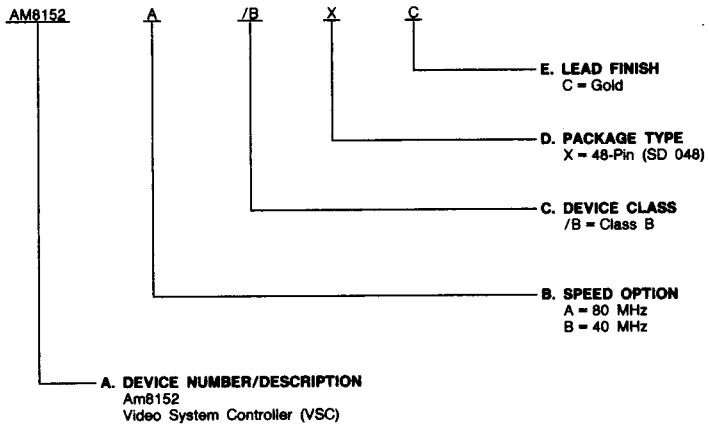
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM8152A	/BXC
AM8152B	/BXC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consists of Subgroups:
1, 2, 3, 7, 8, 9, 10, 11

3

PIN DESCRIPTION

$MCLK_1$ Clock$_1$ (non-TTL compatible) (Output)
$MCLK_1$ is a system clock. It is intended to drive the Am8052 CLK_1, $MCLK_1$ output is nominally a square wave divided down from the internal dot clock frequency according to the CLK_1 DR DR_{0-2} (CLK_1 Divide Ratio) inputs.

CLK_1 DR Clock$_1$ Divide Ratio (Input)
CLK_1 DR DR_{0-2} are three inputs which control the $MCLK_1$ divide ratio. The three inputs may be programmed to divide the $MCLK_1$ signal by two, four, six, ..., sixteen. (See Table 1)

$MCLK_2$ Clock$_2$ (non-TTL compatibe) (Output)
$MCLK_2$ is the character clock. Its function is to drive the Am8052 CLK_2. $MCLK_2$ output is a nominal square wave divided down from the internal dot clock frequency according to the sum of the CLK_2, DR_{0-3} and TB_{0-1} inputs.

CLK_2 DR Clock$_2$ Divide Ratio (Input)
CLK_2 DR DR_{0-3} are four inputs which control an internal divider to divide the dot clock frequency by a value from two to seventeen. The TB inputs are added. (See Table 2)

$TCLK_2$ TTL Clock$_2$ (Output)
$TCLK_2$ is a TTL-compatible version of $MCLK_2$.

X_1, X_2/RES X_1, X_2/RESET (X_2 is non-TTL compatible, reset is TTL compatible) (Input)
X_1, X_2/RES are the external crystal inputs when the on-chip oscillator of the VSC is being used. The external crystal frequency is multiplied by five to produce the on-chip dot clock. If the external dot clock flow-through mode is used, the X_1 should be tied Low and X_2/RES may be used as a reset input to synchronize multiple VSCs. Note that the reset signal must be synchronous to the external dot clock.

X_3 X_3 (non-TTL compatible) (Input)
X_3 is used as an input to the on-chip voltage-controlled oscillator. When the on-chip oscillator of VSR is being used, X_3 should be connected to ground by an appropriate capacitor. If the external dot clock flow-through mode is used, X_3 and X_1 should be tied to ground.

VSYNC Vertical Sync (Input)
VSYNC is an input that must be synchronous to either $MCLK_1$ or $MCLK_2$, dependent on the SSEL input. If SSEL is High, VSYNC must be synchronous to $MCLK_1$.

VSDLD Vertical Sync Delayed (Output)
VSDLD is the delayed output of VSYNC, synchronous to $MCLK_1$ or $MCLK_2$, depending on the setting of SSEL.

HSYNC Horizontal Sync (Input)
HSYNC is an input that must be synchronous to either $MCLK_1$ or $MCLK_2$, dependent upon the SSEL input. If SSEL is Low, HSYNC must be synchronous to $MCLK_2$; if SSEL is High, HSYNC must be synchronous to $MCLK_1$.

HSDLD Horizontal Sync Delayed (Output)
HSDLD is the delayed output of HSYNC, synchronous to $MCLK_1$ or $MCLK_2$, depending upon the setting of SSEL.

SSEL Sync Select (Input)
The SSEL line determines if the VSYNC, HSYNC and BLANK are going to be synchronized to the $MCLK_1$ or $MCLK_2$ signals. A High on SSEL also will resynchronize $MCLK_2$ and $MCLK_1$ during blanking. SSEL is kept LOW for applications which do not involve proportional spacing and HIGH for proportional spacing.

BLANK Blank (Input)
BLANK is an input normally synchronous to $MCLK_1$, although it may be synchronous to $MCLK_2$ in non-proportional spacing applications. The active pulse width of BLANK will usually overlap the active portions of HSYNC and VSYNC. While BLANK is active, $TCLK_2$/$MCLK_2$ may be forced to synchronize to the $MCLK_1$ clock. When BLANK goes inactive, the rising edges of $MCLK_1$ and $TCLK_2$/$MCLK_2$ will be synchronized in order to prevent "dot walk" in proportional spacing applications. BLANK active also forces the video output level to "blank" regardless of DD, FORE or other inputs.

CBLANK Character Blank (Input)
CBLANK forces video output levels (VID_1, VID_2, VIDOUT and $\overline{\text{VIDOUT}}$) to switch to the background color level.

FORE Foreground Video (Input)
The FORE video input is "OR'ed" with the dot data output by the parallel-to-serial shift register to switch to the foreground color level (e.g., to implement underlines). FORE is latched with CLK_2 and cannot be used to insert serial data.

REV Reverse (Input)
The REV input causes the foreground color levels to be transposed with the background color level for the total character period (including any trailing blanks).

FS Foreground Shift (Input)
The FS input causes the shift in the video output levels to produce a highlight effect. (See Table 3.)

TB_0, TB_1 Trailing Blanks (Input)
The TB inputs are added to the CLK_2, DR_{0-3} inputs to calculate the total period (in DOT Clock periods) of $MCLK_2$. If the total period is greater than 17, then zeroes will be shifted out of the shift register. If the total period is less than 17 dot clocks, the user must insure that the shift register is filled with zeroes. The maximum CLK_2 period is 19 dot clock periods; therefore, the combination of CLK_2 DR = 17 and TB = 3 is not allowed. The first character after video blanking must be four or more pixels, trailing blanks included, or an extra pixel will be outputted.

DD_0 – DD_8 Dot Data (Inputs)
The DD inputs accept parallel character dot matrix information for serial conversion for video output. DD_0 is shifted out first.

BS Background Select (Input)
The BS input specifies the color level of the background video. This input can be overridden by BLANK active.

VIDOUT, $\overline{\text{VIDOUT}}$ Video Output (non-TTL compatible)
VIDOUT and $\overline{\text{VIDOUT}}$ outputs in a differential mode the composite blank and video dot levels to a nominal 75Ω load impedance from switched current sources.

VID_1, VID_2 Video Digital (Output)
VID_1 and VID_2 are digitally encoded outputs of the video out. VID_1 is the least significant bit. Encoding is as follows:

	VID_2 (VIDEO)	VID_1 (HIGHLIGHT)
Blank Level	0	0
Black	0	1
Grey	1	0
White	1	1

GRLVL Grey Level (Input)
The GRLVL input adjusts the current level output, via the VIDOUT and $\overline{\text{VIDOUT}}$ outputs, of the grey video level. There are two pre-selected grey levels: for GRLVL HIGH, grey is brighter; for GRLVL LOW, grey is darker. GRLVL is not latched with $MCLK_2$ but is sampled on a pixel-by-pixel basis.

DW Double Width (Input)
The DW input, when active HIGH, causes the dot clock supplied to the $TCLK_2/MCLK_2$ clock divide circuitry and the video shift register to be divided by two. This function is used to facilitate doubling the width of a character cell matrix in the horizontal direction. The trailing blank information is also widened during a double width character.

EXTDCLK External Dot Clock (Input)
EXTDCLK is an external, TTL-compatible dot clock input for use in multiple Am8152A/Am8152B configurations. This signal replaces the internal oscillator function. To enable EXTDCLK, both X_1 and X_3 must be grounded.

AADJ Analog Outputs Current Adjust (non-TTL compatible) (Inputs)
Analog output current adjust is used for setting the analog video output current to 13.3 mA. This is done by connecting AADJ to GND_3 via an applicable 1% resistor.

V_{CC1}, V_{CC2}
V_{CC} should be connected to +5 V.

GND_1, GND_2, GND_3
GND_{1-3} should be connected to Ground.

CLK_1 DR 2	1	0	A	B
L	L	L	1	1
L	L	H	2	2
L	H	L	3	3
L	H	H	4	4
H	L	L	5	5
H	L	H	6	6
H	H	L	7	7
H	H	H	8	8

Table 1

Note: A, B are measured in EXTDCLK periods.

CLK_2 Period

$(CLK_2\ DR_{0-3} + TB_{0-1}) + 2$	C	D
2	1	1
3	1	2
4	2	2
5	2	3
6	3	3
7	3	4
8	4	4
9	4	5
10	5	5
11	5	6
12	6	6
13	6	7
14	7	7
15	7	8
16	8	8
17	8	9
18	9	9
19	9	10

Note: C and D are measured in EXTDCLK periods.

Table 2

CLK_2, DR_{0-3} and TB_{0-1} are a 4-bit and 2-bit binary number respectively. For A, B, C, D refer to the Reset Timing Diagram.

3

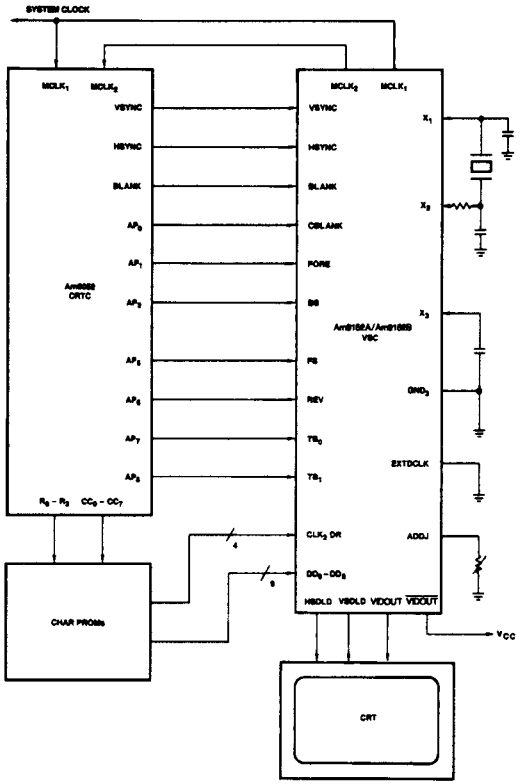


Figure 2. Am8152A/Am8152B Application with Am8052 CRT Controller

FUNCTIONAL DESCRIPTION

The Am8152A Video System Controller (VSC) supports both black and white and color video applications for CPUs, CRT controllers, and terminals. The essential functions of the VSC are to support proportional and non-proportional character display, to synchronize and mix character attributes with video, and to output the video in a four level analog or 2-bit digital serial format.

PARALLEL PIXEL LOADING

Pixel information that must be serialized for video transmission is loaded into the serial shift register via inputs $DD_0 - DD_8$. Information is loaded on both edges of the $MCLK_2$ character clock, as shown in Figure 3. The information set up on DD(0:7) prior to the falling edge of $MCLK_2$ is loaded into positions $VID_9 - VID_{16}$. Note that DD_8 information is ignored. Information set up on DD(0:8) prior to the rising edge of $MCLK_2$ is loaded into positions $VID_0 - VID_8$. Thus, up to 17 bits of pixel information can be loaded into the shift register. Note that if the character width is nine pixels or less the information captured on the falling edge of the $MCLK_2$ is not used.

CLK_2DR (0:3) and TB (0:1) determine the divide ratio for the character clock. The sum of both values specifies the character clock period in dot clocks. During the trailing blank, the VSC shifts out what was loaded into the shift register. Therefore, it is the responsibility of the user to insure that the pixels output during the trailing blank dot period are set to the blank level. If the total is greater than 17, this occurs automatically.

VIDEO OPERATION

Parallel video data is obtained from the character ROM inputs; bits are shifted out serially and mixed with attribute information such as underline, shifted underline, and any other video sources. Video is internally encoded into one of four levels: White, Grey, Black and Blank. White is the highest analog current level, and Blank is the lowest. This information is then output through two ports. (See Figure 5). One port provides a differential current source output into a 75Ω impedance, and the second port outputs encoded TTL video on two pins.

There are two distinct blank inputs to the Am8152A/Am8152B. BLANK is the CRTC's horizontal and vertical retrace period input which causes a blank output level to the display. CBLANK is an attribute input to selectively blank a character cell by forcing the video information for the particular character cell period to switch to the selected background color level. (See Table 3).

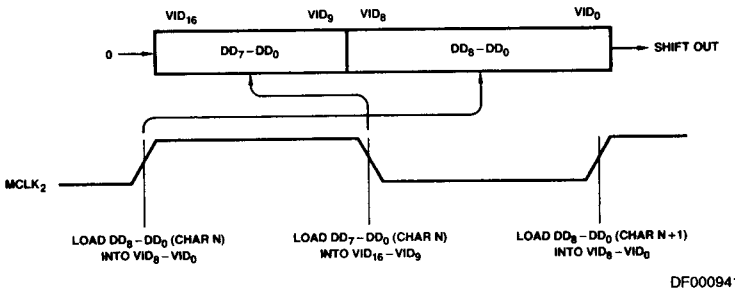


Figure 3. Shift Register Loading

CRYSTAL SPECIFICATION

The crystal used with the VSC may have the following specifications:

AT cut
Series Resonant
Shunt Capacitance: 7 pf maximum

VIDEO INPUTS/OUTPUTS

Video information may be input in a number of different ways. Table 3 depicts all the combinations of video outputs achievable with each of the various inputs. The background color is determined by a separate pin input allowing either a black or white background. Using the REVERSE VIDEO (REV) input, a grey background can also be selected. The foreground then becomes black or white according to the signal on the foreground SHIFT line. Foreground and video sums can be modified depending on the combination of background, foreground shift, and reverse inputs. The user may apply any of his video inputs to the foreground to obtain a desired effect.

TABLE 3. Am8152A/Am8152B VIDEO ATTRIBUTES

INPUTS				Am8152A/Am8152B VIDEO ATTRIBUTES
BS	FS	REV	$\overline{\text{CBLANK}}$ (DD (0 : 8) + FORE)	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

TB4

SYSTEM TIMING

The CPU clock ($MCLK_1$) output is derived from an on-board oscillator by an externally programmable divide ratio. The internal oscillator is capable of operating at a frequency of up to 80 MHz in the Am8152A and 40 MHz in the Am8152B. In crystal oscillator multiplier mode, the crystal should be an AT cut operating in series resonant mode using the fundamental frequency.

The character clock ($MCLK_2$) output to the CRTC is frequency modulated according to the chosen number of dots per character cell. The duty cycle of $MCLK_2$ is 50% (±1 dot clock period) and is derived from the internal dot clock whose divide ratio is set by the width of the character ROM plus the number of trailing blanks. A double width input further modifies $MCLK_2$, doubling the character width. During an active BLANK input, $MCLK_2$ is internally resynchronized to $MCLK_1$ if SSEL is HIGH. This action aligns character cells at the left-end side of the display, thereby eliminating "Dot Walk." The Vertical and Horizontal Sync (VSYNC, HSYNC) inputs from the CRT controller are buffered and delayed by one $MCLK_1$ or $MCLK_2$ clock period.

DOT CLOCK GENERATION WITH PLL

When using the internal oscillator of the VSC, care should be used in laying out the grounds and supplies for the part in order to minimize the jitter of the PLL. Under optimal conditions this jitter is less than 1 ns. If the jitter does occur it is normally less than 4 ns and can, over the operating range, be reduced to less than 1 ns by varying the duty cycle on X_1. The following table shows the worst-case jitter observed on typical parts over the operating range and the percentage Dot Clock at various Dot Clock frequencies.

Dot Clock Frequency (MHz)	Worst Case Jitter Observed (ns)	% Dot Clock
25	3.9	10
40	7.4	30
60	4.4	26
80	6.7	54

PROPORTIONAL/VARIABLE SPACING

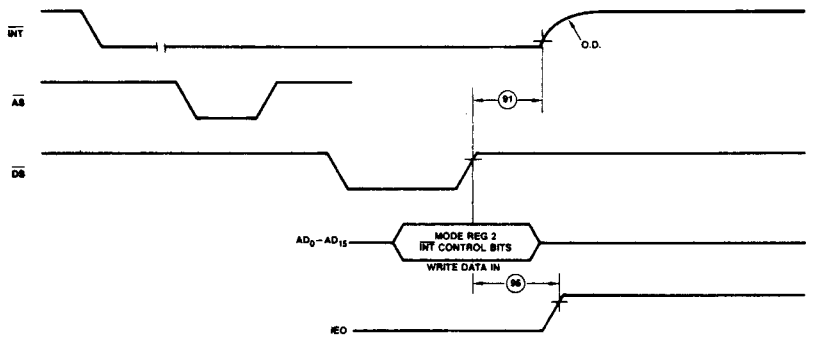
Proportional spacing is achieved by programming, on a character-by-character basis, a number from two to nineteen dot clock periods per character. The character ROM pixel information is selectable from two to seventeen per character. Up to three trailing blank pixels can be concatenated to the character ROM input, making it easier to provide a straight right margin for right justification of text.

SWITCHING CHARACTERISTICS (Cont'd.)

Am8052 Non-Vectored $\overline{INT}$ Timing

No.	Parameter Symbol	Parameter Description	4 MHz		6 MHz		8 MHz*		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
91	t_D	$\overline{DS}$ ↑ to $\overline{INT}$ (Write) (Note 1)		100		90		80	ns
95	t_D	$\overline{DS}$ ↑ to IEO ↑ (Write) (Note 2)		100		90		80	ns

Notes: 1. This parameter describes the termination of an interrupt request via a write to the appropriate bit in Mode Register 2:
IUSS → 1 IUSV → 1
IES → 0 IEV → 0
IPS → 0 IPV → 0
2. This is the release of IEO LOW due to the slave mode reset of the IUS bit in Mode Register 2.
* Commercial products only.



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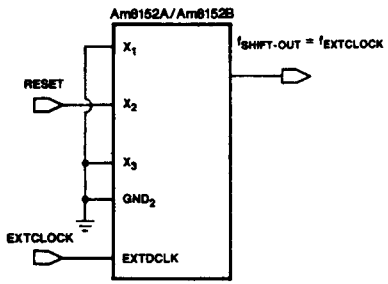
Am8052 Non-Vectored $\overline{INT}$ Timing

DOTCLOCK GENERATION MODE

EXTERNAL DOT CLOCK FLOW THROUGH MODE



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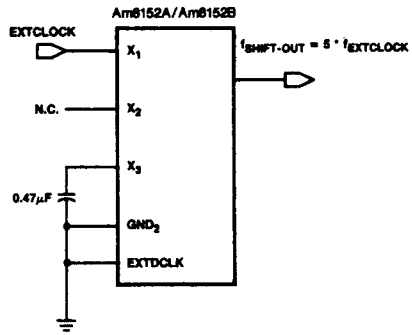
EXTERNAL CLOCK MULTIPLIER MODE



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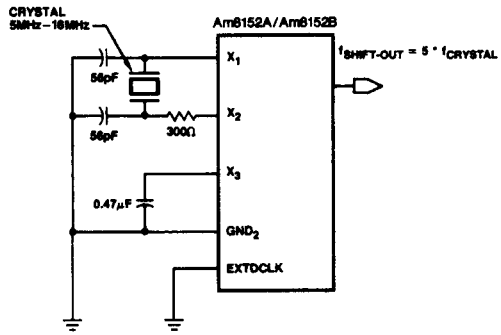
CRYSTAL OSCILLATOR MULTIPLIER MODE



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs for
High Output State ..... −0.5V to +V_{CC}
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current into Outputs (See Note 2) 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +5.0 V ±5%

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +5.0 V ±10%

Operating ranges define those limits over which the functionality of the device is guaranteed.

Am8152A/Am8152B

DC CHARACTERISTICS over operating range unless otherwise specified; Included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted.
COM'L T_A = 0 to +70°C, V_{CC} = 5.0 V ±5%
MIL T_C = −55 to +125°C, V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions				Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min	$MCLK_1$, $MCLK_2$	I_{OH} = −0.1 mA		4.0		Volts
			TTL Output	I_{OH} = −1.0 mA	MIL	2.4		Volts
				I_{OH} = −2.6 mA	COM'L			
V_{OL}	Output LOW Voltage	V_{CC} = Min	$MCLK_1$, $MCLK_2$	I_{OL} = 0.1 mA			0.3	Volts
			TTL Output	I_{OL} = 16 mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage				2.0		Volts
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA					−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4 V		All Inputs (Except RES, EXTDCLK)			−0.4	mA
				RES, EXTDCLK			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 2.7 V		All Inputs (Except RES)			+50	µA
				RES			+600	µA
I_I	Input HIGH Current at Max Input Voltage	V_{CC} = Max, V_{IN} = 5.5 V					+1.0	mA
I_{SC}	Output Short Current Current (Notes 1, 2)	V_{CC} = Max		$MCLK_1$, $MCLK_2$		−50	−250	mA
				Others		−40	−130	mA
I_{CC}	Power Supply Current	V_{CC1} = Max, V_{CC2} = Max	Over Operating Ranges				415	mA

ANALOG ELECTRICAL CHARACTERISTICS (Notes 2 – 6)

The following conditions apply unless otherwise specified:
COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5%
MIL T_C = −55 to +125°C, V_{CC} = 5.0 V ±10%

Grey Level	VID_2	VID_1		VIDOUT		$\overline{VIDOUT}$	
				Min (%)	Max (%)	Min (%)	Max (%)
X	I	I	I_{White}	0	0	100	100
I	I	O	I_{Grey1}	37	45.5	54.5	63
O	I	O	I_{Grey2}	45	54	46	55
X	O	I	I_{Black}	89.5	93	7	10.5
X	O	O	I_{Blank}	100	100	0	0

Notes:
1. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
2. The absolute maximum rating for VIDOUT, $\overline{VIDOUT}$ and AADJ is 22 mA. Shorting VIDOUT, $\overline{VIDOUT}$, or AADJ to ground will destroy the device.
3. Test condition: Normal I_{white} for $\overline{VIDOUT}$ = 13.3 mA.
4. Positive Current flowing into VIDOUT/$\overline{VIDOUT}$.
5. $\overline{VIDOUT}$ output currents normalized to I_{white}
VIDOUT output currents normalized to I_{blank}.
6. VIDOUT and $\overline{VIDOUT}$ typically will not drift by more than 2% over the operating conditions.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted.

COM'L $T_A = 0$ to 70°C, $V_{CC} = 5.0$ V ±5%
MIL $T_C = -55$ to +125°C, $V_{CC} = 5.0$ V ±10%

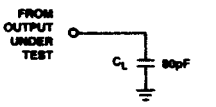
Number	Description	Am8152A		Am8152B		Units
		Min	Max	Min	Max	
† 1	$MCLK_1$ Period (Note 7)	100		165		ns
† 2	$MCLK_2$ Period (Note 7)	70		165		ns
† 3	$MCLK_1$ HIGH (See Notes 5, 7) (See Figure 4)	38		70		ns
† 4	$MCLK_1$ LOW (See Notes 3, 5, 7) (See Figure 4)	37.5		70		ns
† 5	$MCLK_2$ HIGH (See Notes 6, 7) (See Figure 4)	23		70		ns
† 6	$MCLK_2$ LOW (See Notes 3, 6, 7) (See Figure 4)	20		70		ns
† 7	Data to $MCLK_2/TCLK_2$ RE (See Note 1, 7)	25		30		ns
8	$MCLK_2/TCLK_2$ to Data Not Valid	0		0		ns
9	VSYNC/HSYNC to $MCLK_1$ RE Setup (SSEL = HIGH)	25		30		ns
† 10	VSYNC/HSYNC to $MCLK_2$ RE Setup (SSEL = LOW) (Note 7)	25		30		ns
11	$TCLK_2$ RE to $MCLK_2$ RE Delay		8		8	ns
12	$TCLK_2$ FE to $MCLK_2$ FE Delay		12		15	ns
13	$MCLK_1$ to VSLD, HSLD (SSEL = HIGH) (See Note 2)		$6 + T_D$		$6 + T_D$	ns
14	$TCLK_2$ to VSLD, HSLD (SSEL = LOW) (See Note 2)		$6 + T_D$		$6 + T_D$	ns
† 15	DD(0 - 7) to $TCLK_2$ FE (See Note 7)	25		30		ns
16	$TCLK_2$ RE to VID_1 VID_2 VAL (See Note 2)		$6 + T_D$		$6 + T_D$	ns
17	BLANK FE to $MCLK_2$ RE Setup (SSEL = LOW)	22		25		ns
18	BLANK FE to $MCLK_1$ FE Setup (SSEL = HIGH)	20		25		ns
19	BLANK RE to $MCLK_1$ RE Setup (SSEL = HIGH)	22		25		ns
20	BLANK RE to $MCLK_2$ RE Setup (SSEL = LOW)	22		25		ns
† 22	VID_1 to VID_2 Skew (See Note 7)	−5	+5	−7	+7	ns
† 24	EXTDCLK to $MCLK_1$ (See Note 7)		20		25	ns
† 25	EXTDCLK to $TCLK_2$ (See Note 7)		18		25	ns
26	EXTDCLK to $MCLK_2$		23		25	ns
27	EXTDCLK to VID_1/VID_2		18		20	ns
28	EXTDCLK to HSDLD/VSDLD (SSEL HI)		18		20	ns
29	EXTDCLK to HSDLD/VSDLD (SSEL LO)		18		20	ns
† 30	EXTDCLK to Data in Setup (See Note 7)	12		18		ns
31	EXTDCLK to Data Not Valid Hold	18		20		ns
† 32	EXTDCLK to H/V SYNC Setup (See Note 7)	14		18		ns
† 33	EXTDCLK Period (See Note 7)	12.5		25		ns
† 34	EXTDCLK LOW Cycle (See Note 7)	5		7		ns
† 35	EXTDCLK HIGH Cycle (See Note 7)	5		7		ns
† 36	Reset Pulse Width (High) (See Note 7)	15		20		ns
† 37	Reset Low to EXTDCLK Setup	8.0		10		ns
† 38	EXTDCLK Period in PLL Mode (See Note 7)	12.5	50	25	50	ns

Notes:
1. Data includes CBLANK, FORE, REV, FS, DD_0–DD_8, TB0, TB1, BS, CLK_1DR, CLK_2DR, DW.
2. First Pixel of character. T_D is the dot clock period.
3. Max undershoot on these outputs is guaranteed to be −0.3V.
4. T_D is the dot clock period.
5. Guaranteed to 100ns $MCLK_1$ cycle time.
6. Guaranteed to 70ns $MCLK_2$ cycle time (even divide ratio only).
7. These parameters are guaranteed by device characterization or tested using bench top equipment.

† = Not included in Group A tests.

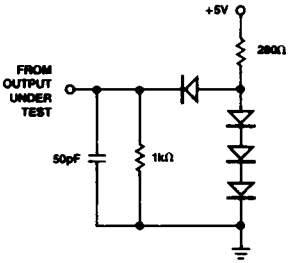
SWITCHING TEST CIRCUIT

$MCLK_1/MCLK_2$ OUTPUT



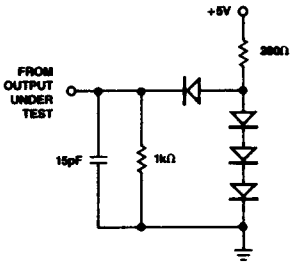
TC000561

TTL OUTPUTS EXCEPT $TCLK_2$



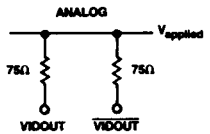
TC000701

$TCLK_2$ OUTPUT



TC001531

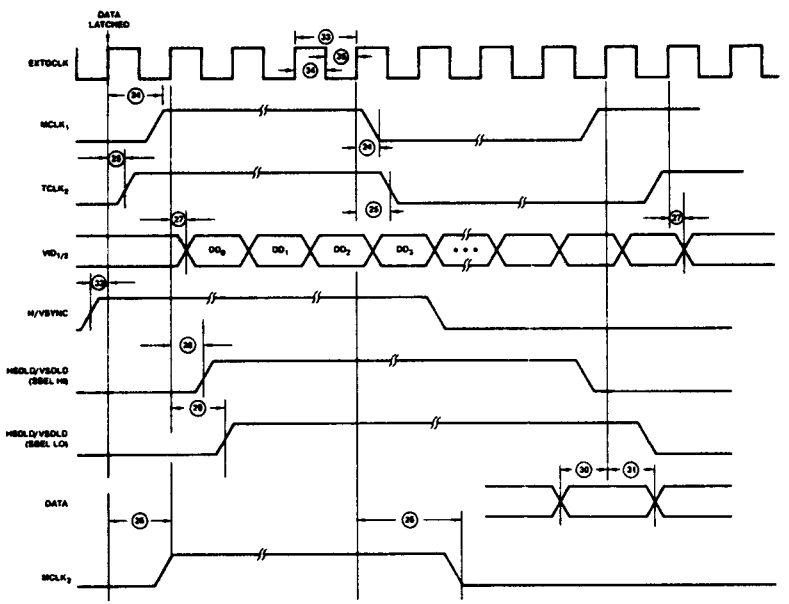
ANALOG OUTPUTS



TC000551

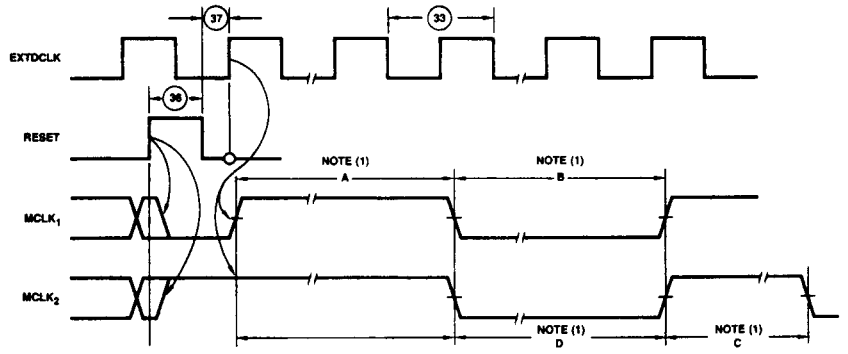
Am8152A/Am8152B TIMING

(PARAMETERS MEASURED WITH RESPECT TO EXTDCLK)



WF003213

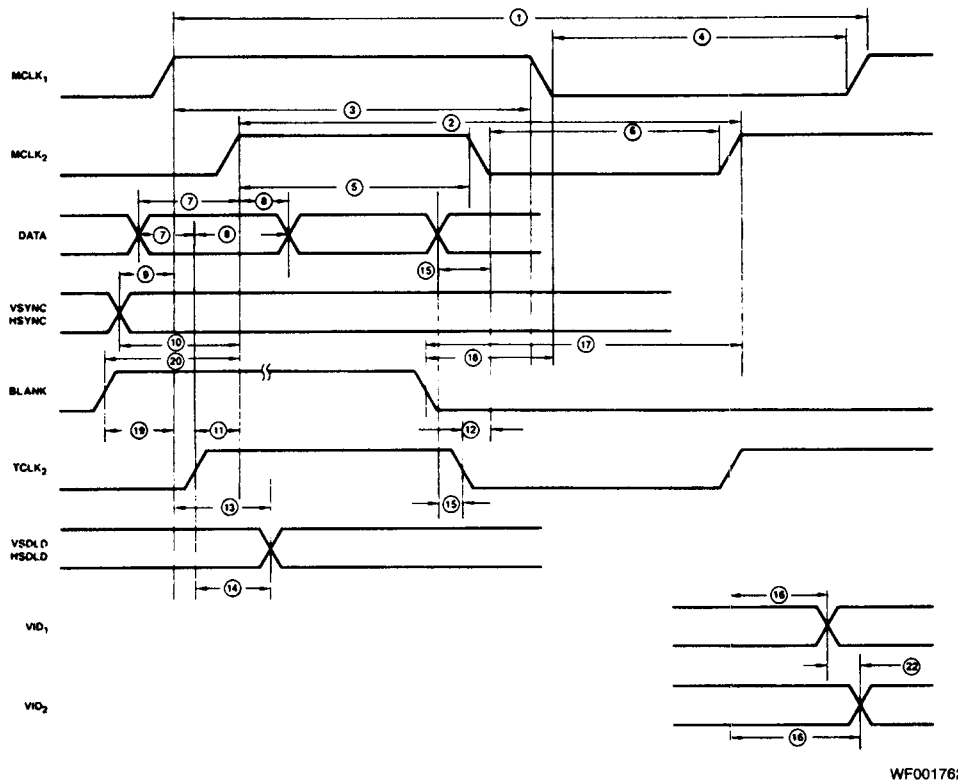
RESET TIMING FOR Am8152A/Am8152B



WF003192

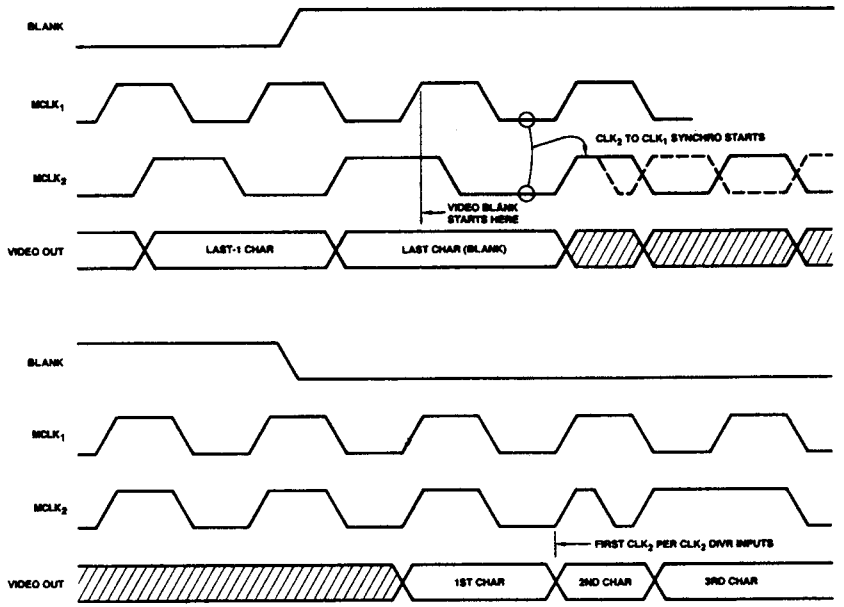
Note 1. See Pin Description section.

SWITCHING TIMING DIAGRAM — $MCLK_1/MCLK_2$

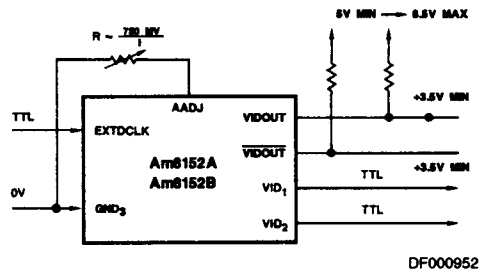


WF001762

VSC CLK_2 SYNCHRONIZATION (ONLY OCCURS IF SSEL IS HIGH)



WF001752



DF000952

Figure 5. Analog Video Outputs and Digital Video Outputs for Am8152A/Am8152B