LXT384/6/8 Twisted Pair Interface — Without Component Changes

Application Note

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Application Note

Contents

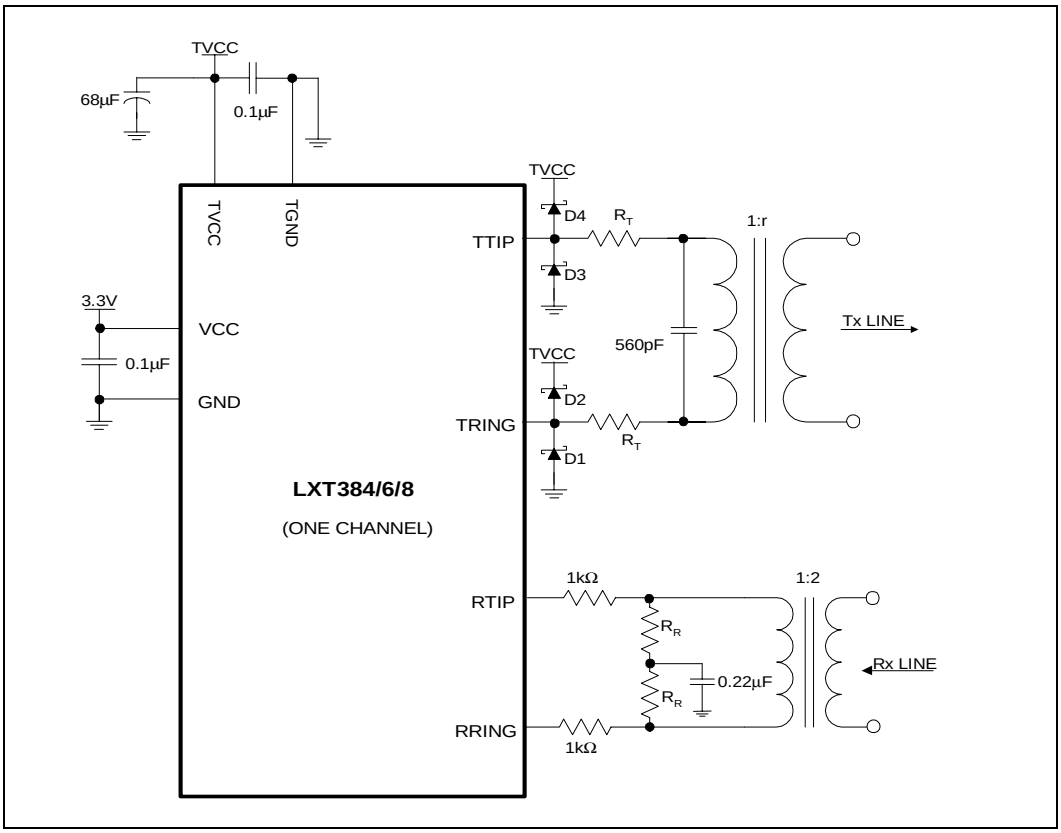
Figures

Tables

1.0 General Description

In today's global economy, a critical consideration when designing telecommunications systems is compatibility with the various international standards. Ideally, one should be able to design a system that can be sold in the different international markets with minimal or no hardware changes. By doing so, the manufacturer reduces the cost associated with maintaining different system versions. The designer of T1/E1 line interfaces is often faced with this same challenge. Meeting all the electrical specifications using the same line interface circuitry for T1 and E1 can be a difficult task. This application note proposes two universal T1/E1 twisted pair line interface solutions using Intel's series of 3.3V T1/E1 LIUs.

Figure 1. LXT384/6/8 Line Interface Circuitry



2.0 LXT384/6/8 T1/E1 LIU Family

Intel's family of 3.3V T1/E1 LIUs includes the following members:

- LXT384: Eight channel T1/E1 LIU with clock recovery and digital jitter attenuator (hardware/ software mode).
- LXT386: Four channel version of the LXT384.
- LXT388: Dual LIU with four receivers. Feature set is identical to the LXT384 with the addition of simultaneous receive and transmit jitter attenuator and DPM (Driver Performance Monitoring).

These devices have identical receive and transmit circuits. The following discussion applies to all three devices unless otherwise noted.

3.0 LXT 384/6/8 Standard Line Interface Circuitry

Figure 1 shows the line interface circuitry as recommended in the LXT384/6/8 data-sheets.

In the transmit section, the R_T resistors change from E1 to T1. In T1 mode, series resistors are only supported when the transmitter power supply (TVCC) is set to 5V.

In the receive section, the R_R resistors are selected so that the input impedance offered by the receive circuitry matches the characteristic line impedance. Therefore, R_R is such that:

$$Z_L = r^2 (2 R_R)$$

Where Z_L is the line characteristic impedance and r is the transformer turns ratio (in this case r = 2). Consequently, to obtain optimum impedance matching and receive return loss performance, the designer typically changes R_R when the line impedance changes. This is the case going from a T1 100Ω line impedance to an E1 120Ω line impedance.

In the following section we will show that simple solutions exist for supporting T1/E1 twisted pair interfaces without component changes. Transmit and receive interfaces are addressed in separate sections. The performance tradeoffs for each of the suggested configurations is discussed. Test data is provided along with the recommended configurations.

Note that E1 coaxial cable interface is not addressed in this application note as most of the modern designs use twisted pair interfaces. In many applications, support for coaxial cable can be added with external baluns. For more information on supporting E1 coaxial and twisted pair interface in the same design, please refer to the LXT384 FAQ and the “LXT380 Design Assistant” at www.developer.intel.com/design/network.

4.0 Universal T1/E1 Interface

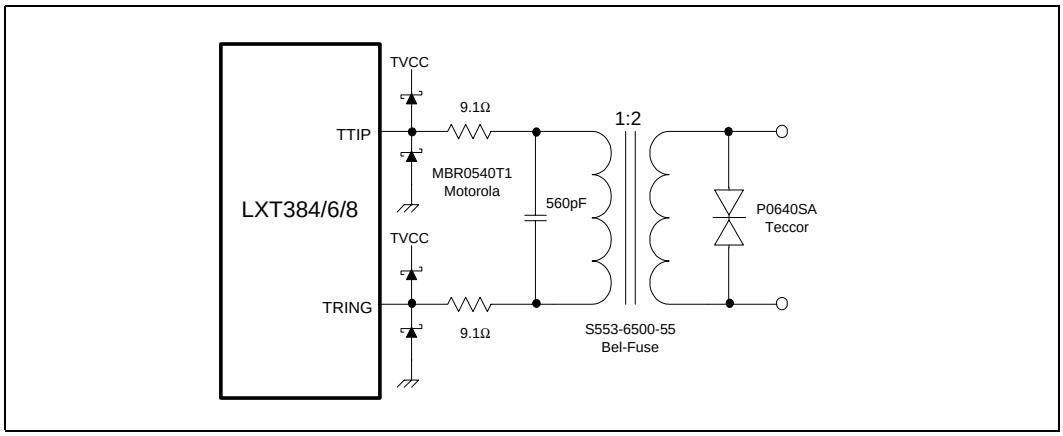
4.1 Transmit Interface

Two different T1/E1 transmit interface options are proposed in this section: a *high transmit return loss* interface and a *low power* interface.

4.1.1 High Transmit Return Loss Interface

Transmit return loss is a measure (in dB) of the matching between the line impedance and the transmit interface impedance. High transmit return loss minimizes reflections and ensures quality transmission over harsh cable environments. The configuration illustrated in Figure 2 can be used for both T1 and E1 operation while maintaining excellent transmit return loss performance.

Figure 2. High Tx Return Loss Interface

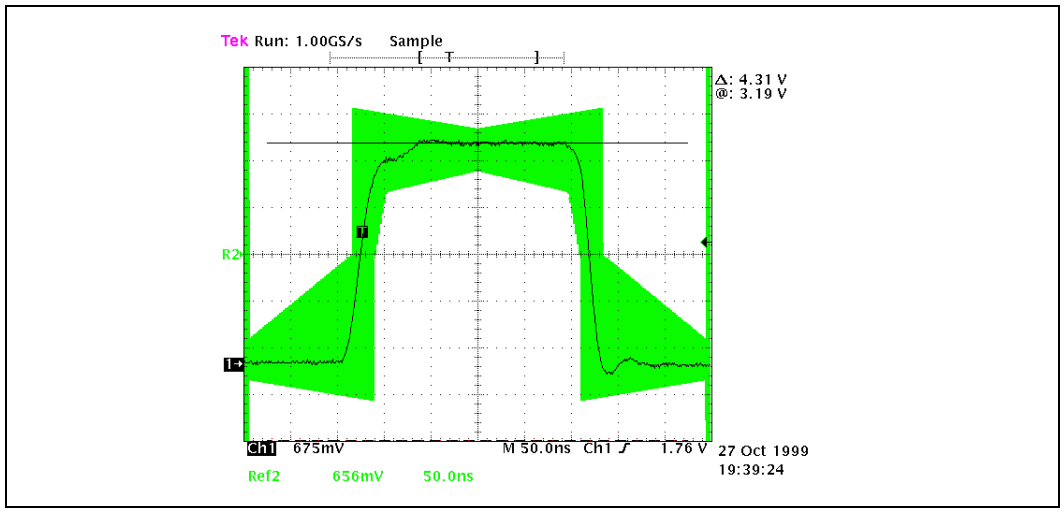


For T1 operation, this configuration coincides with the standard recommended interface. Its performance is therefore well characterized in the product data-sheet. For E1, twisted pair operation, the transmit series resistors are slightly lower than the recommended value (R_T = 11 Ω). The transient voltage suppressor and Schottky diodes were added for surge protection. Although Intel recommends this protection for increased reliability, they are not mandatory for normal operation.

4.1.1.1 Pulse Template Measurement

The output voltage in E1 mode using this configuration is slightly higher than nominal. We measured a typical value of 3.2 V which is within the ITU-T G.703 specified range: 2.7V < Vo < 3.3V. Figure 3 shows the resulting output pulse as measured using the LXT384 evaluation board. Note: in typical applications, long pcb traces, protection elements, EMI filters and connectors will add resistive loss that effectively reduces the output level at the measurement point. In these application, the increased output amplitude may actually result in additional margin to the pulse template specifications.

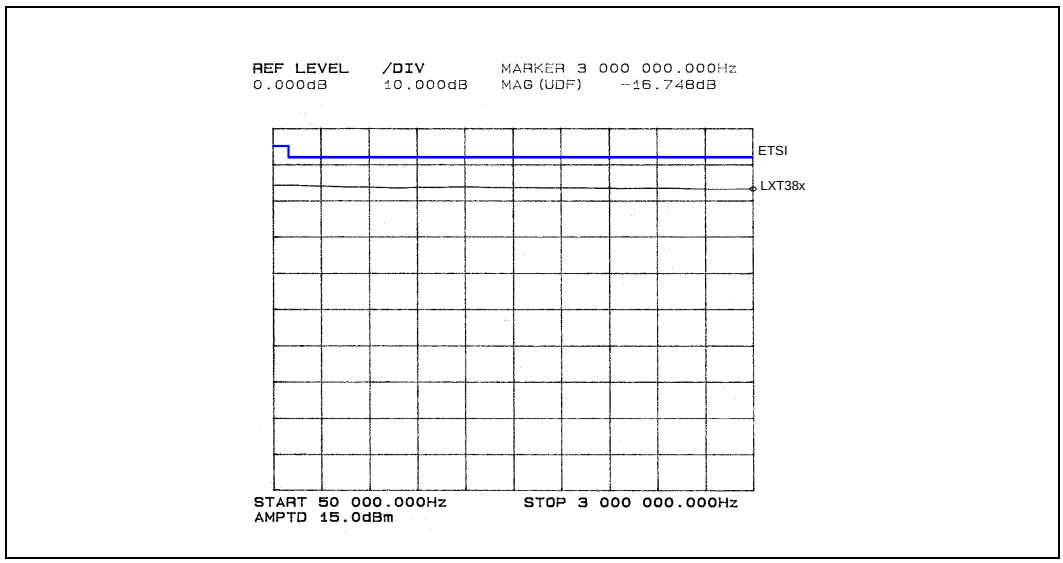
Figure 3. E1, Twisted Pair Cable Output



4.1.1.2 Transmit Return Loss Measurement

This configuration offers excellent transmit return loss performance exceeding the requirements in ETS300166 by a comfortable margin. Please refer to Figure 4.

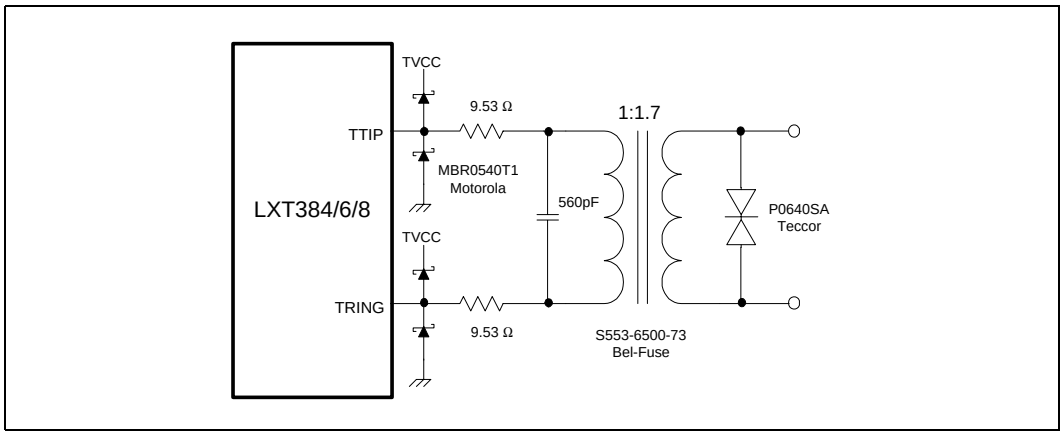
Figure 4. E1 Twisted Pair, Tx Return Loss



4.1.1.3 Low Power Interface

Figure 5 represent a low power solution for T1/E1 twisted pair cable interface. By using a transformer with a lower turns ratio, we effectively reduce the current consumption through the TVCC pins (TVCC = 5V).

Figure 5. Low Power Interface



4.1.1.4 Pulse Template Measurement

Since this configuration is not standard in the LXT38x datasheets, both T1 and E1 pulse template measurements were performed. Figure 6 through Figure 16 illustrate the measurements.

Figure 6. E1, Twisted Pair Cable Output

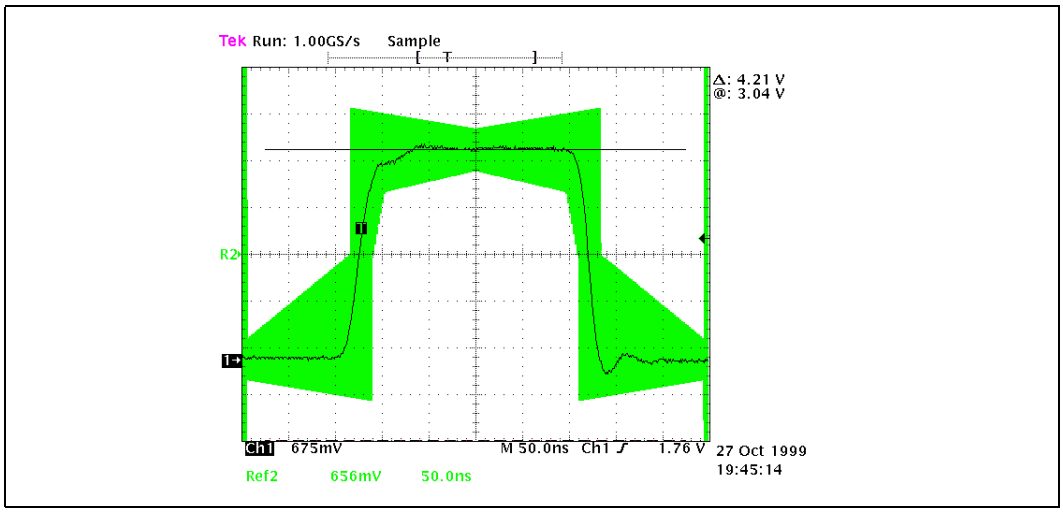


Figure 7. T1, LEN = 011 @ 0 ft. Cable

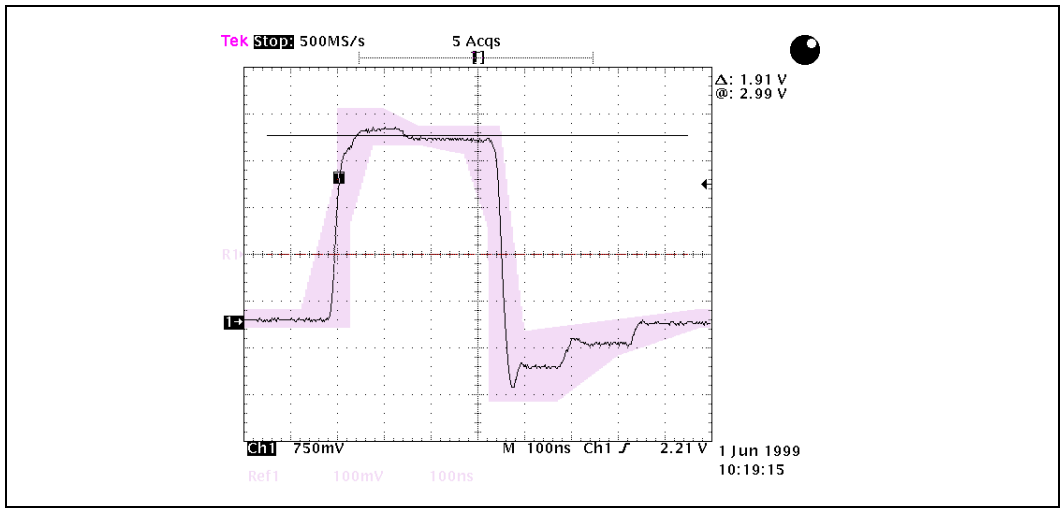


Figure 8. T1, LEN = 011 @ 131 ft. Cable

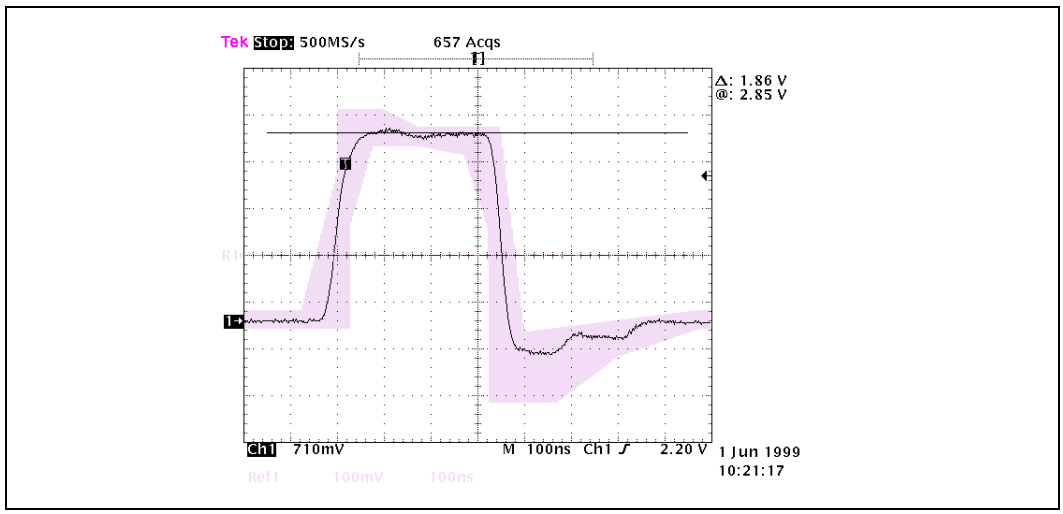


Figure 9. T1, LEN = 100 @ 131 ft. Cable

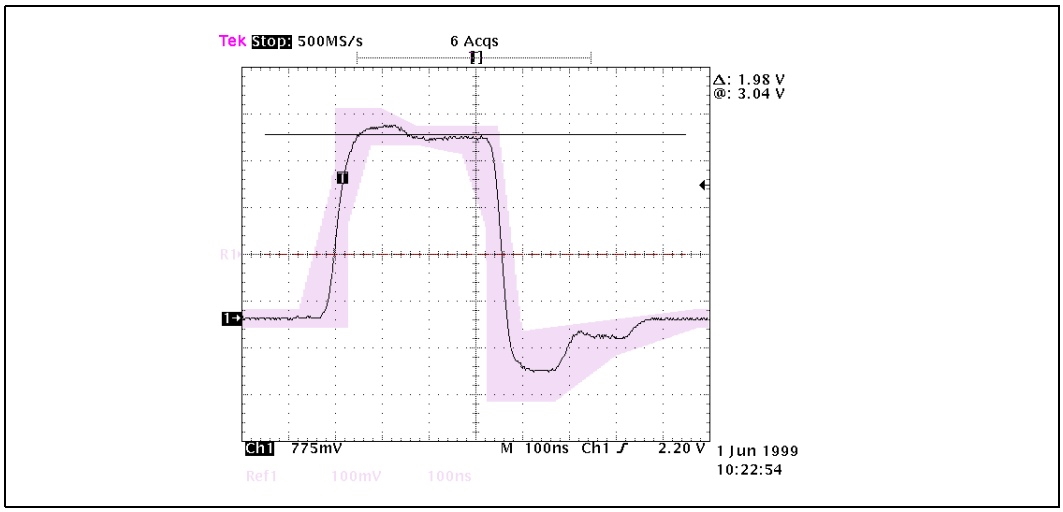


Figure 10. T1, LEN = 100 @ 262 ft. Cable

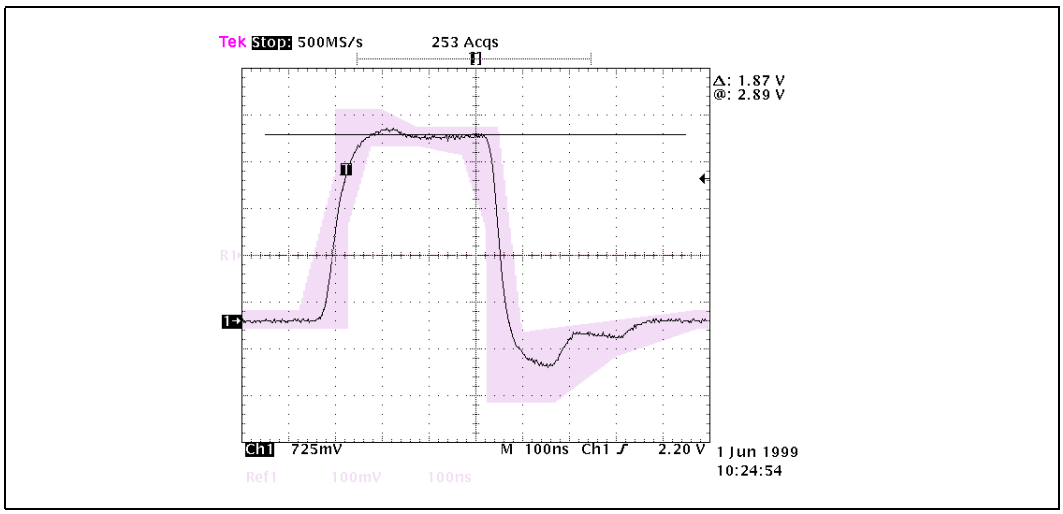


Figure 11. T1, LEN = 101 @ 262 ft. Cable

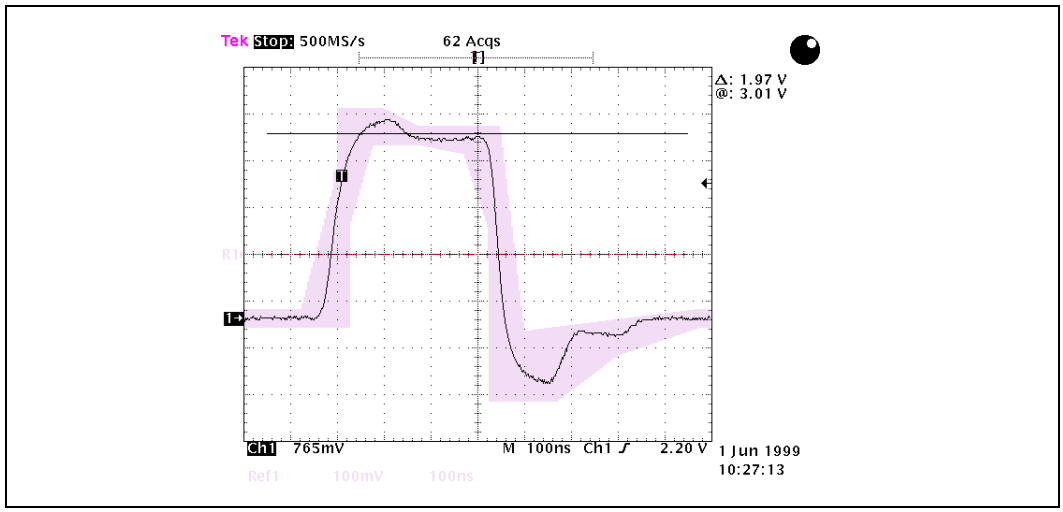


Figure 12. T1, LEN = 101 @ 393 ft. Cable

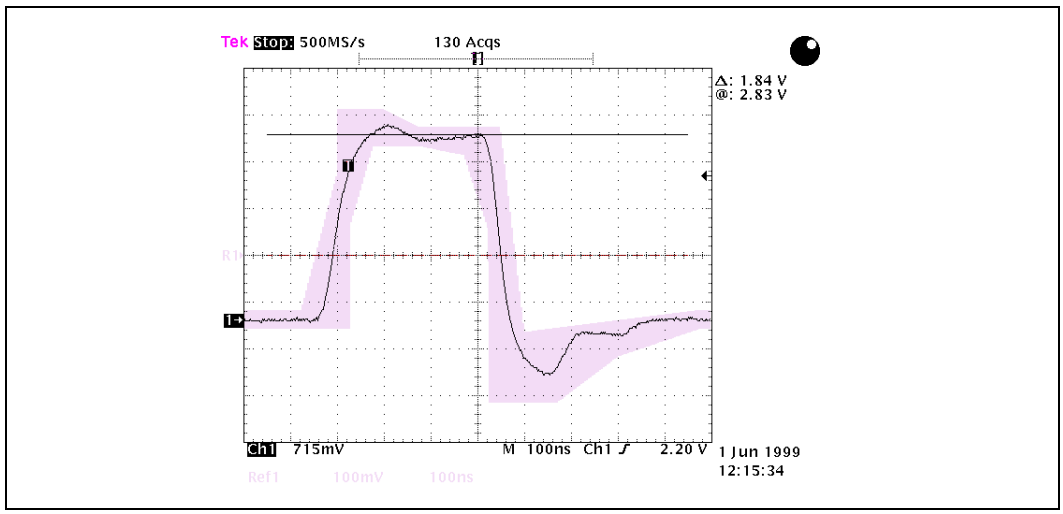


Figure 13. T1, LEN = 110 @ 393 ft. Cable

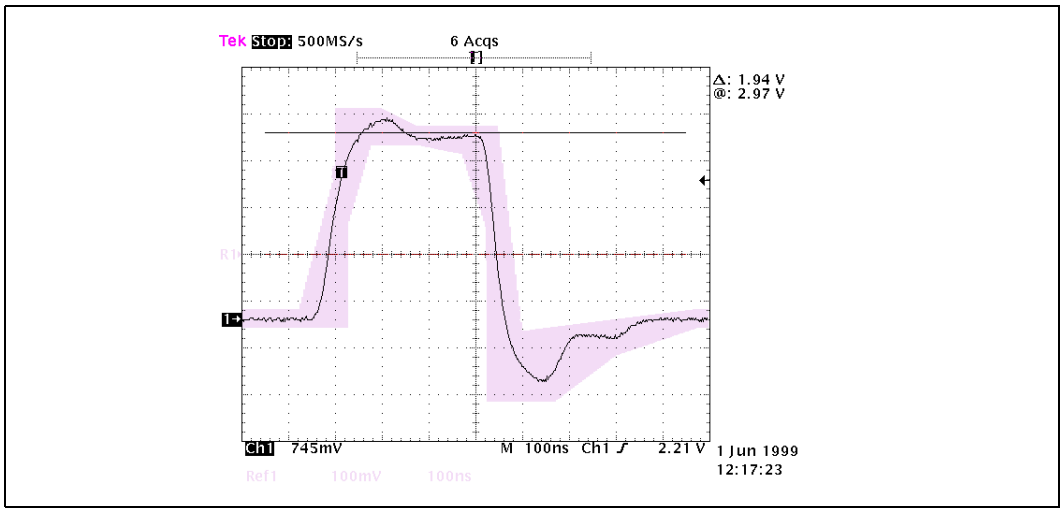


Figure 14. T1, LEN = 110 @ 524 ft. Cable

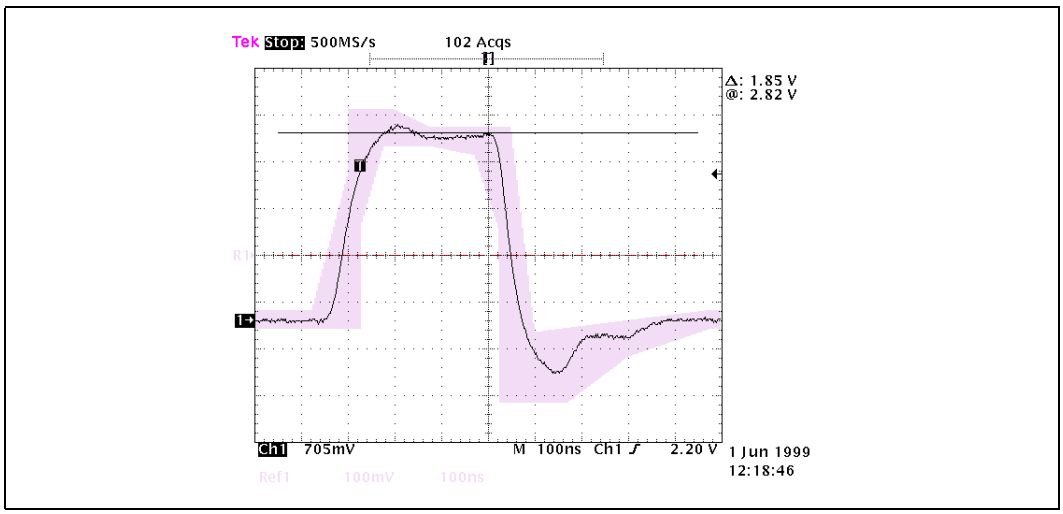


Figure 15. T1, LEN = 111 @ 524 ft. Cable

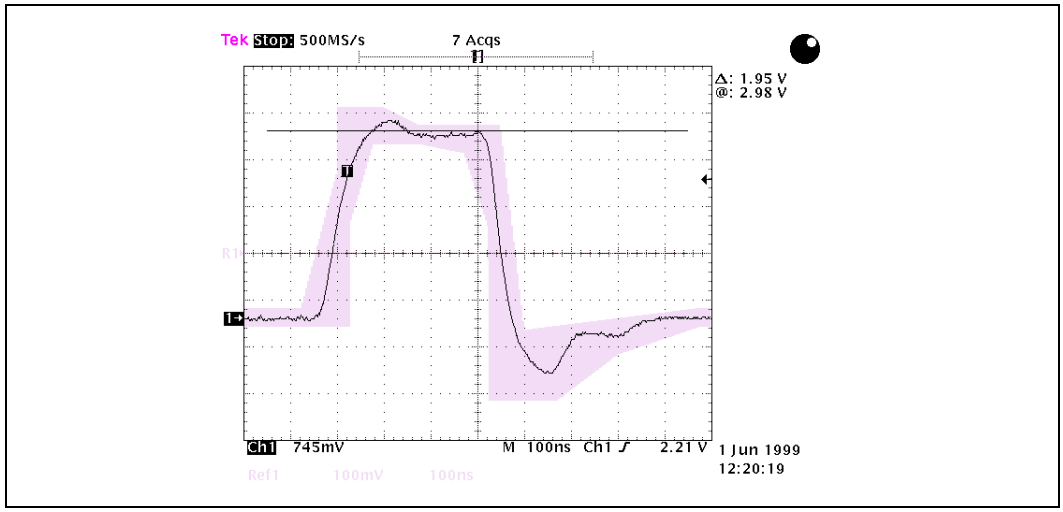
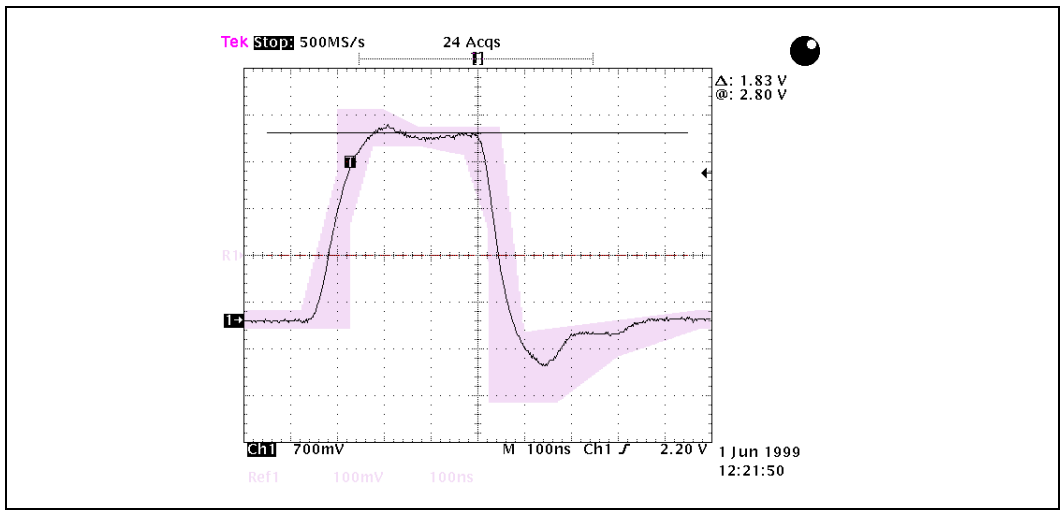


Figure 16. T1, LEN = 111 @ 655 ft. Cable



4.1.1.5 Transmit Return Loss Measurement

Although transmit return loss performance in this configuration is not as good as the performance offered by the configuration described in the previous section, it is still enough to meet the requirements of ETS 300166. Note that there are no return loss specification for T1. In this application note, the corresponding E1 limits are used as a reference for the T1 measurements. Figure 17 and Figure 18 show the transmit return loss measurements.

Figure 17. T1 Twisted Pair, Tx Return Loss

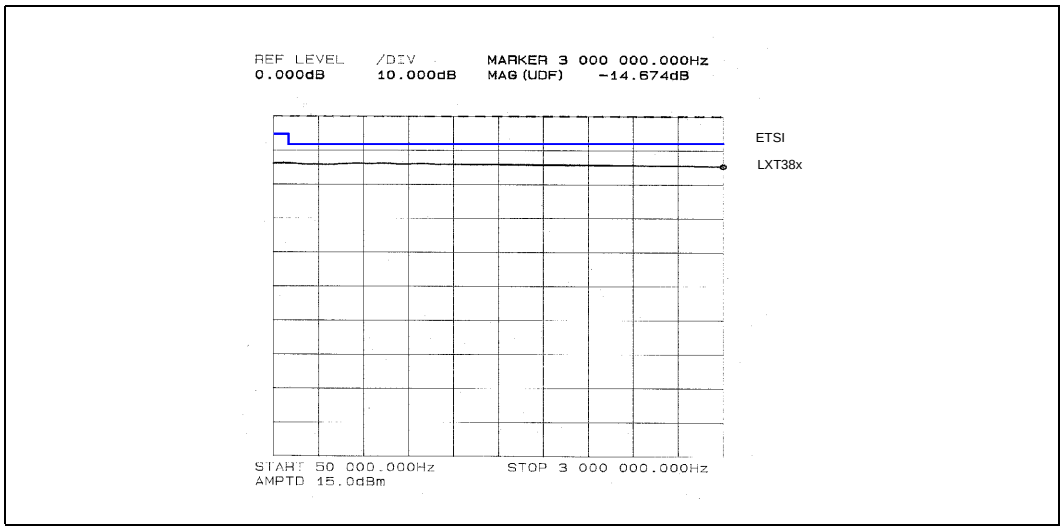
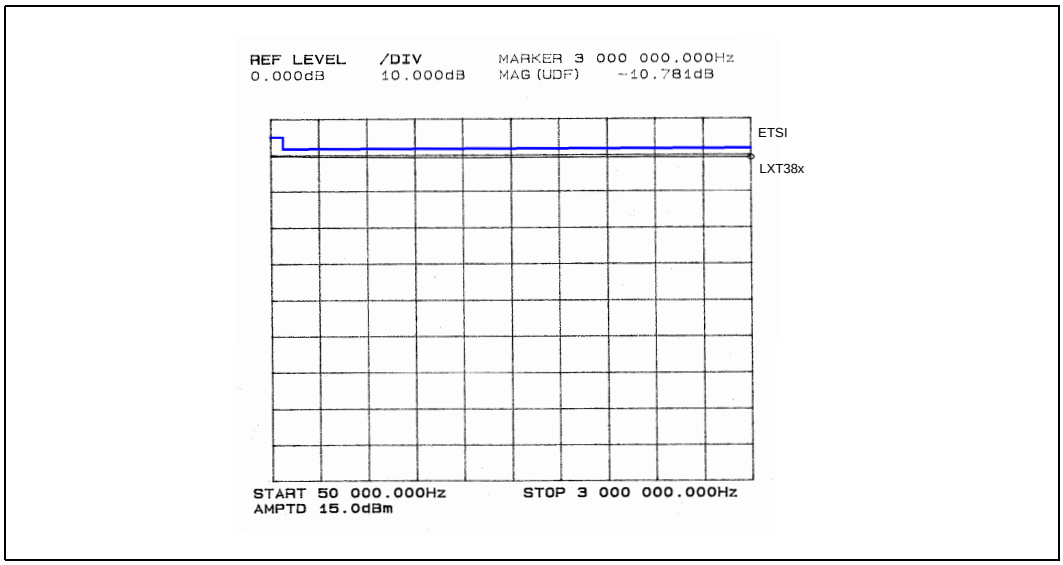


Figure 18. E1 Twisted Pair, Tx Return Loss



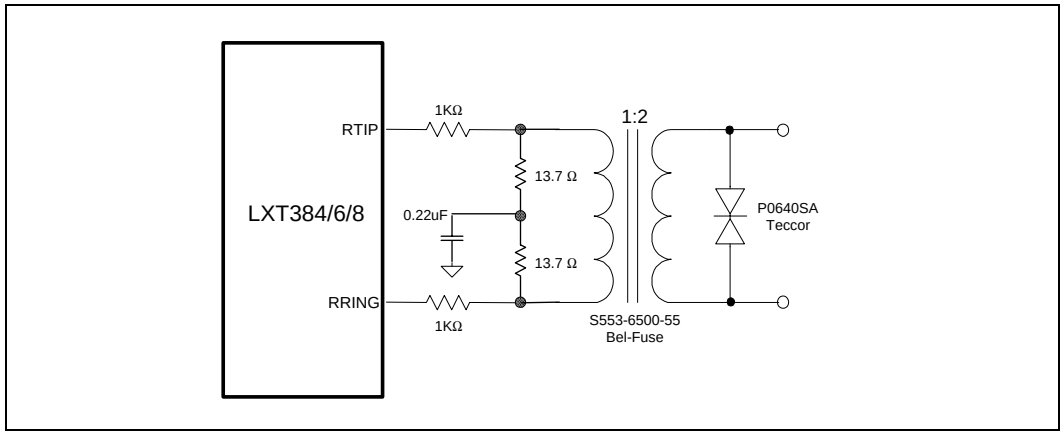
4.2 Transmit Interface Summary

As we saw in the previous sections, the two proposed transmit interfaces offer different tradeoffs between transmit return loss, pulse template and power consumption performance. Therefore, the right interface for a given application is going to depend on which of these parameters is the most critical for the design. Table 1 summarizes the performance characteristics of both interfaces.

4.2.1 Receive Interface

As we saw in the standard receive interface description, the receive termination resistors R_R are usually modified to match different line impedances. While this practice yields optimum receive return loss performance, it is not necessary to exactly match the line impedance in order to meet the receive return loss requirements with a comfortable margin. The receive interface we are about to propose takes advantage of this fact. Since the T1 and E1 twisted pair characteristic impedances (100Ω and 120Ω) are relatively close, we can use a compromise 110Ω equivalent impedance to terminate both interfaces. Please refer to Figure 19.

Figure 19. T1/E1 Receive Interface



The reflected impedance *Z* is:

$Z = r^2 (2 R_R) = 2^2 \times (2 \times 13.7) = 109.6\ \Omega$

With this termination impedance, we can easily meet G.703 receive return loss requirements as shown in Figure 20. On the other hand, the T1 receive return loss is still well above 20 dB in the same frequency range. Note that these measurements also take into account the capacitive loading effect of the protection sidactor.

Figure 20. E1 Twisted Pair, Tx Return Loss

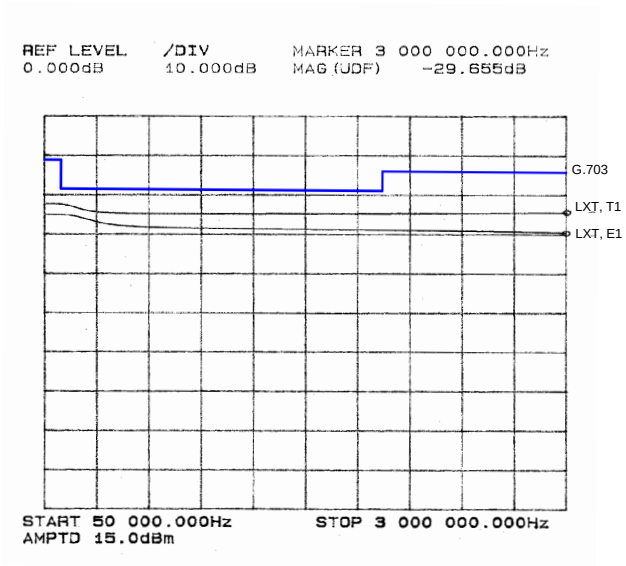


Table 1. Transmit Interface Performance Summary

	Per Channel I_{TVCC} max.[1,2]		Tx Return Loss typ.	
	T1	E1	T1 f = 772 KHz	E1 f = 1024 KHz
High Return Loss Option Figure 2	62 mA	34 mA	21 dB	16 dB
Low Power Option Figure 5	51 mA	27 mA	14 dB	11 dB

1. Add total I_{VCC} for total power consumption calculations.
2. TVCC = 5V +/- 5%

5.0 Conclusions

The previous sections we proposed simple solutions for T1/E1 twisted pair operation without component changes using the LXT38X series of 3.3V T1/E1 LIUs. These devices offer the flexibility to support different tradeoffs between power consumption and transmission performance. As a result, the designer can choose the interface circuit that better suits his requirements while meeting the applicable standards with a comfortable margin.