HD49227FS — Preliminary

RAM Controller for DATA/DAT

Description

The HD49227FS is a RAM controller developed for DATA/DAT applications. It performs signal-processing functions required for DATA/DAT formats.

Features

- Signal-processing functions for DATA/DAT formats are built in.
- Single 5-V power supply.

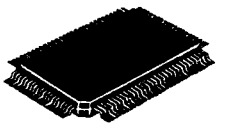
Functions

- Control of buffer memory for transfers between DAT block and the host interface
- Error correction, using the HD49224A layered error correction unit (L.ECU)

Ordering Information

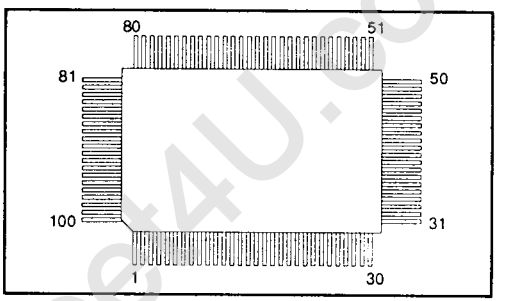
Type No.	Package
HD49227FS	FP-100A

HD49227FS



FP-100A

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TTO0	26	TFRSYR	51	TTO5	76	LOC4
2	TTI7	27	TSIN	52	MD6	77	LOC3
3	TTI6	28	TSPINTN	53	TWEN	78	LOC2
4	TTI5	29	TGRINTN	54	MD5	79	LOC1
5	TTI4	30	TWAITN	55	TTO4	80	LOC0
6	TTI3	31	TCSSCIN	56	TMA9	81	TDOE
7	TTI2	32	TCSGUREN	57	TMA8	82	TLOE
8	GND	33	TCA0	58	GND	83	GND
9	TTI1	34	TCA1	59	MD4	84	TDLD
10	TTI0	35	TCPURDN	60	TMA7	85	TCORS
11	TTMD2	36	TCPUWRN	61	TMA6	86	TCS0ECU
12	TTMD1	37	CD7	62	MD3	87	TDLCK
13	TTMD0	38	CD6	63	TMA5	88	TCX0ECU
14	TRESETN	39	CD5	64	TMA4	89	W
15	GND	40	CD4	65	GND	90	T
16	TCK24M	41	V_{CC}	66	MD2	91	V_{CC}
17	TEF	42	CD3	67	TMA3	92	TSCIORN
18	TMPXP	43	CD2	68	TMA2	93	TSCIOWN
19	TBCKP	44	CD1	69	MD1	94	TSCICSN
20	TSOUT	45	CD0	70	TMA1	95	TSCACKN
21	TMPXR	46	MD8	71	TMA0	96	TSCEOPN
22	TBCKR	47	GND	72	MD0	97	TSCDRQ
23	GND	48	TCASILN	73	GND	98	TTO3
24	THGRSY	49	TRASN	74	TCASN	99	TTO2
25	TFRSYP	50	MD7	75	LOC5	100	TTO1

Pin Functions

Pin No.	Pin Symbol	I/O	Function	Connects to	Polarity High	Polarity Low	Input Spec.	Pull-U/D
1	TTO0	O	Test pin					
2	TTI7	I	Test pin	GND	Test	Norm	CMOS	D
3	TTI6	I	Test pin	GND	Test	Norm	CMOS	D
4	TTI5	I	Test pin	GND	Test	Norm	CMOS	D
5	TTI4	I	Test pin	GND	Test	Norm	CMOS	D
6	TTI3	I	Test pin	GND	Test	Norm	CMOS	D
7	TTI2	I	Test pin	GND	Test	Norm	CMOS	D
8	GND							
9	TTI1	I	Test pin	GND	Test	Norm	CMOS	D
10	TTI0	I	Test pin	GND	Test	Norm	CMOS	D
11	TTMD2	I	Test pin	GND	Test	Norm	CMOS	D
12	TTMD1	I	Test pin	GND	Test	Norm	CMOS	D
13	TTMD0	I	Test pin	GND	Test	Norm	CMOS	D
14	TRESETN	I	Reset input	RESET	Norm	Reset	CMOS	D
15	GND							
16	TCK24M	I	Clock input	Signal-processing section			CMOS	D
17	TEF	I	Erasure flag input signal	HD49211BFS (play)	Erasure	Correct	CMOS	D
18	TMPXP	I	Left/right channel switching signal	HD49211BFS (play)	Right	Left	CMOS	D
19	TBCKP	I	Serial bit clock	HD49211BFS (play)			CMOS	D
20	TSOUT	I	Serial input from HD49211BFS	HD49211BFS (play)	1	0	CMOS	D
21	TMPXR	I	Left/right channel switching signal	HD49211BFS (record)	Right	Left	CMOS	D
22	TBCKR	I	Serial bit clock	HD49211BFS (record)			CMOS	D
23	GND							
24	THGRSY	I	Group sync signal	System microcontroller	Start		CMOS	D
25	TFRSYP	I	Frame sync signal for play	Signal processing section			CMOS	D
26	TFRSYR	I	Frame sync signal for record	Signal processing section			CMOS	D
27	TSIN	O	Serial output to HD49211BFS	HD49211BFS (record)	1	0		
28	TSPINTN	OD	Group end interrupt signal	System microcontroller		Int.		U
29	TGRINTN	OD	Interface microcontroller interrupt signal	Interface microcontroller		Int.		U
30	TWAITN	OD	Interface microcontroller's wait signal	Interface microcontroller		Wait		U
31	TCSSCIN	I	Chip select signal when interface microcontroller accesses host interface	Interface microcontroller	Norm	Select	CMOS	U
32	TCSGUREN	I	Chip select signal when interface microcontroller accesses HD49227FS	Interface microcontroller	Norm	Select	CMOS	U

Notes: I/O: I = input O = output I/O = input/output OD = open-drain output with pull-up resistor
Pull-U/D: U = pull-up resistor D = pull-down resistor

Pin Functions

Pin No.	Pin Symbol	I/O	Function	Connects to	Polarity High	Polarity Low	Input Spec.	Pull-U/D
33	TCA0	I	Interface microcontroller's address 0	Interface microcontroller			TTL	D
34	TCA1	I	Interface microcontroller's address 1	Interface microcontroller			TTL	D
35	TCPURDN	I	Interface microcontroller's read command	Interface microcontroller	Norm	Read	TTL	U
36	TCPUWRN	I	Interface microcontroller's write command	Interface microcontroller	Norm	Write	TTL	U
37	CD7	I/O	Interface microcontroller data bus 7	Interface microcontroller	1	0	TTL	U
38	CD6	I/O	Interface microcontroller data bus 6	Interface microcontroller	1	0	TTL	U
39	CD5	I/O	Interface microcontroller data bus 5	Interface microcontroller	1	0	TTL	U
40	CD4	I/O	Interface microcontroller data bus 4	Interface microcontroller	1	0	TTL	U
41	V_{CC}							
42	CD3	I/O	Interface microcontroller data bus 3	Interface microcontroller	1	0	TTL	U
43	CD2	I/O	Interface microcontroller data bus 2	Interface microcontroller	1	0	TTL	U
44	CD1	I/O	Interface microcontroller data bus 1	Interface microcontroller	1	0	TTL	U
45	CD0	I/O	Interface microcontroller data bus 0	Interface microcontroller	1	0	TTL	U
46	MD8	I/O	Buffer memory	Buffer memory	1	0	TTL	U
47	GND							
48	TCASILN	O	Buffer memory CAS (for erasure flag)	Buffer memory	Norm	CASIL		
49	TRASN	O	Buffer memory RAS	Buffer memory	Norm	RAS		
50	MD7	I/O	Buffer memory data bus 7	Buffer memory	1	0	TTL	U
51	TTO5	O	Test output (CASILIN for 512-kword mode)	Monitor				
52	MD6	I/O	Buffer memory data bus 6	Buffer memory	1	0	TTL	U
53	TWEN	O	Buffer memory write enable	Buffer memory	Norm	Write		
54	MD5	I/O	Buffer memory data bus 5	Buffer memory	1	0	TTL	U
55	TTO4	O	Test output (OEN for 512-kword mode)	Monitor				

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Pull-U/D: U = pull-up resistor D = pull-down resistor

Pin Functions

Pin No.	Pin Symbol	I/O	Function	Connects to	Polarity High	Polarity Low	Input Spec.	Pull-U/D
56	TMA9	O	Buffer memory address 9 (CASIN for 512-kword mode)	Buffer memory				
57	TMA8	O	Buffer memory address 8	Buffer memory				
58	GND							
59	MD4	I/O	Buffer memory data bus 4	Buffer memory	1	0	TTL	U
60	TMA7	O	Buffer memory address 7	Buffer memory				
61	TMA6	O	Buffer memory address 6	Buffer memory				
62	MD3	I/O	Buffer memory data bus 3	Buffer memory	1	0	TTL	U
63	TMA5	O	Buffer memory address 5	Buffer memory				
64	TMA4	O	Buffer memory address 4	Buffer memory				
65	GND							
66	MD2	I/O	Buffer memory data bus 2	Buffer memory	1	0	TTL	U
67	TMA3	O	Buffer memory address 3	Buffer memory				
68	TMA2	O	Buffer memory address 2	Buffer memory				
69	MD1	I/O	Buffer memory data bus 1	Buffer memory	1	0	TTL	U
70	TMA1	O	Buffer memory address 1	Buffer memory				
71	TMA0	O	Buffer memory address 0	Buffer memory				
72	MD0	I/O	Buffer memory data bus 0	Buffer memory	1	0	TTL	U
73	GND							
74	TCASN	O	Buffer memory CAS (for data)	Buffer memory	Norm	CAS		
75	LOC5	I/O	HD49224A location address 5	HD49224A	1	0	CMOS	D
76	LOC4	I/O	HD49224A location address 4	HD49224A	1	0	CMOS	D
77	LOC3	I/O	HD49224A location address 3	HD49224A	1	0	CMOS	D
78	LOC2	I/O	HD49224A location address 2	HD49224A	1	0	CMOS	D
79	LOC1	I/O	HD49224A location address 1	HD49224A	1	0	CMOS	D
80	LOC0	I/O	HD49224A location address 0	HD49224A	1	0	CMOS	D
81	TDOE	O	HD49224A data output enable	HD49224A	Data out	Norm		
82	TLOE	O	HD49224A location address output enable	HD49224A	Loc. out	Norm		
83	GND							
84	TDLD	O	HD49224A data load timing	HD49224A	Data load	Norm		

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Pin Functions

Pin No.	Pin Symbol	I/O	Function	Connects to	Polarity High	Polarity Low	Input Spec.	Pull-U/D
85	TCORS	O	HD49224A correction start timing signal	HD49224A	Start	Norm		
86	TCS0ECU	O	HD49224A chip select signal	HD49224A	Erasure flag input	Data input		
87	TDLCK	O	HD49224A data latch clock signal	HD49224A				
88	TCX0ECU	O	HD49224A rec/play switching signal	HD49224A	Record	Play		
89	W		Test pin	V_{CC}	Norm	Test		
90	T		Test pin	V_{CC}	Norm	Test		
91	V_{CC}							
92	TSCIORN	O	Host interface read signal	Host interface	Norm	Read		
93	TSCIOWN	O	Host interface write signal	Host interface	Norm	Write		
94	TSCICSN	O	Host interface chip select signal (CPU access)	Host interface	Norm	Select		
95	TSCACKN	O	Host interface acknowledge signal (DMA)	Host interface	Norm	Ack.		
96	TSCEOPN	O	Host interface end signal (DMA)	Host interface	Norm	End		
97	TSCDRQ	I	Host interface data request signal (DMA)	Host interface	Req.	Norm	CMOS	D
98	TTO3	O	Test pin	Monitor				
99	TTO2	O	Test pin	Monitor				
100	TTO1	O	Test pin	Monitor				

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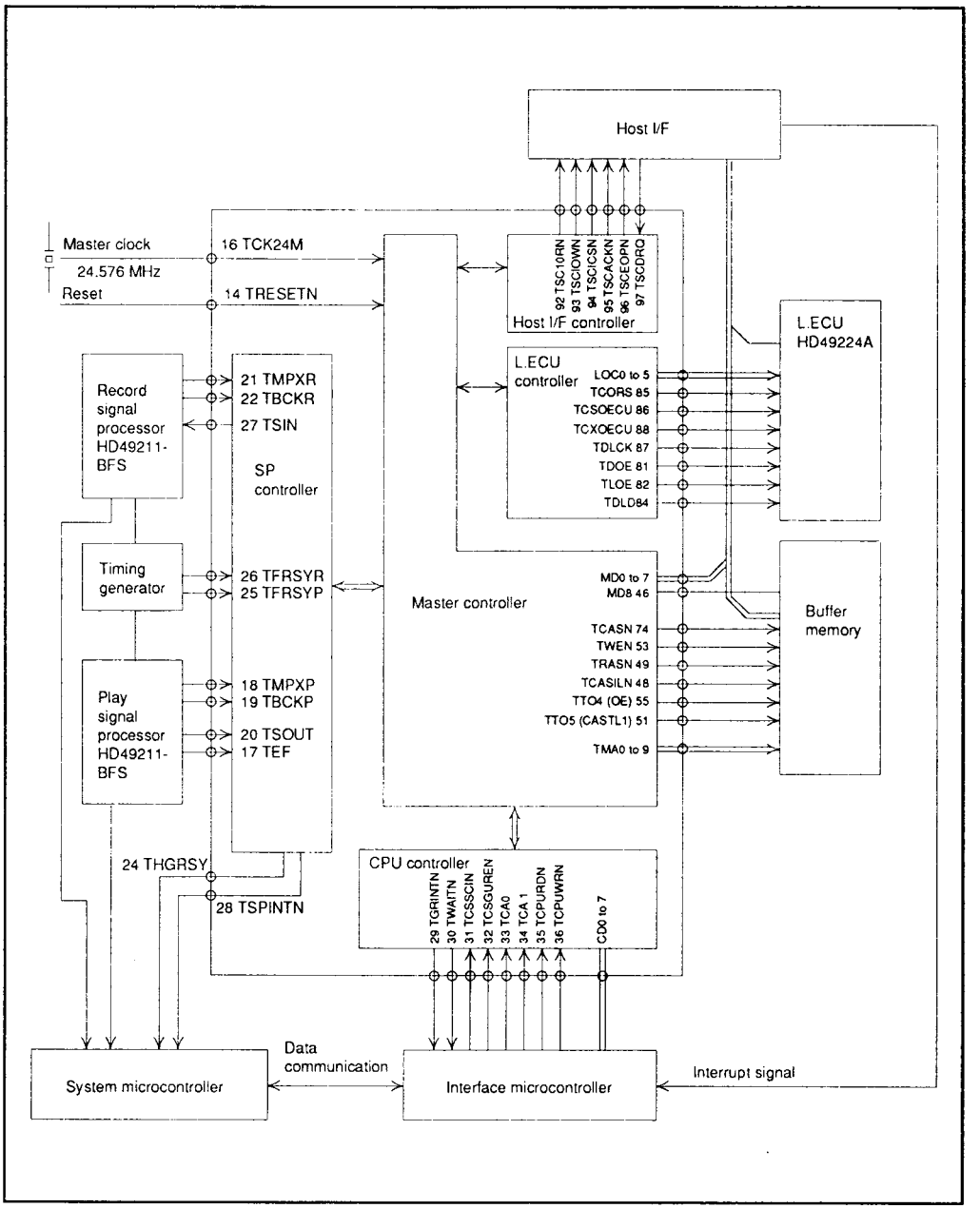
Block Diagram



Absolute Maximum Ratings

(Ta = 25° C)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +6.7	V
Pin voltage	V_{TI}	–0.3 to Vcc + 0.3	V
Pin voltage	V_{TO}	–0.3 to Vcc + 0.3	V
Output current	I_O	–16 to +16	mA
Total output current	I_{OT}	–70 to +70	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{bias}	–20 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics

(GND = 0 V, Ta = 25° C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IHT}	2.2	—	—	V	TTL level
	V_{IHC}	Vcc × 0.7	—	—	V	CMOS level
	V_{ILT}	—	—	0.8	V	TTL level
	V_{ILC}	—	—	Vcc × 0.3	V	CMOS level
Output voltage	V_{OH}	3.5	—	—	V	I_{OH} = –2 mA
	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA
Input leakage current	I_{LI}	—	—	1.0	µA	V_{IN} = 0 to Vcc
Output leakage current	I_{LO}	—	—	1.0	µA	output = "H : Z"
Current dissipation	I_{CC}	—	—	100	mA	Vcc = 5 V, no load
Pull-up current	$-I_{PU}$	80	—	550	µA	V_{IN} = 0 V
Pull-down current	I_{PD}	80	—	550	µA	V_{IN} = Vcc