SONY

CXA2549M

RF Amplifier for CD Players

Description

The CXA2549M is an IC developed for compact disc players. This IC incorporates an RF amplifier, focus error amplifier, APC circuit and RF level control circuit. (The voltage-converted optical pickup output is supported.)

Features

- Low power consumption (45 mW at ±2.5 V)
- High-band RF amplifier
- APC circuit
- RF level control circuit
- Both single power supply and dual power supply operations possible.
- Compatible with pickup for LC and PD

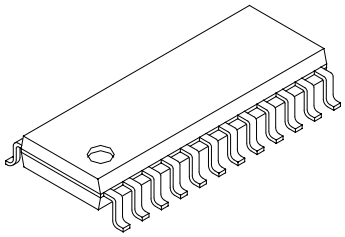
Applications

Compact disc players

Structure

Bipolar silicon monolithic IC

24 pin SOP (Plastic)



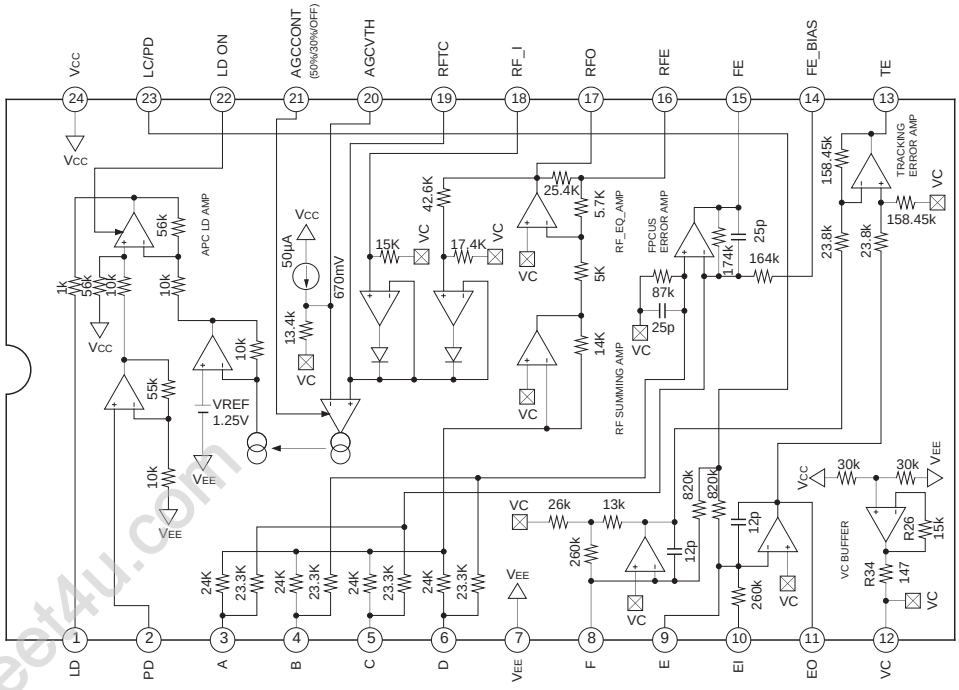
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	650	mW

Operating Conditions

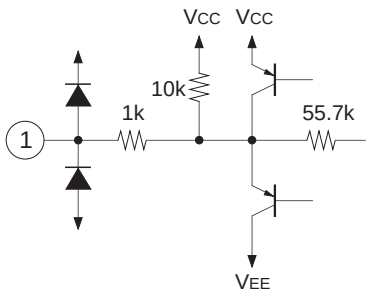
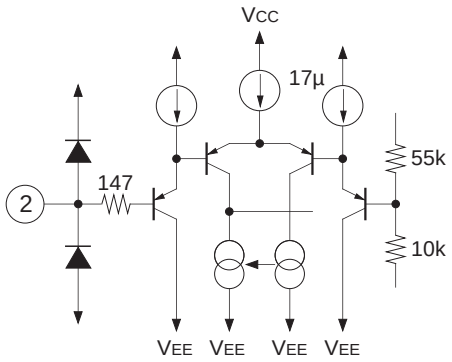
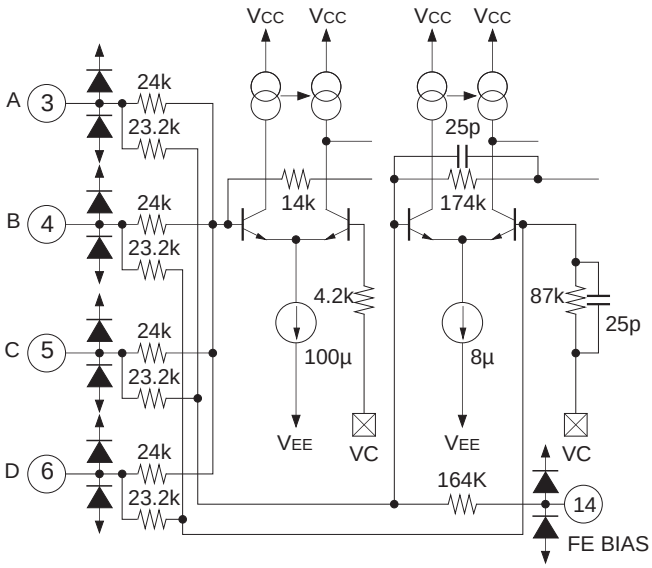
Supply voltage	V_{CC}—V_{EE}	4.5 to 5.5	V

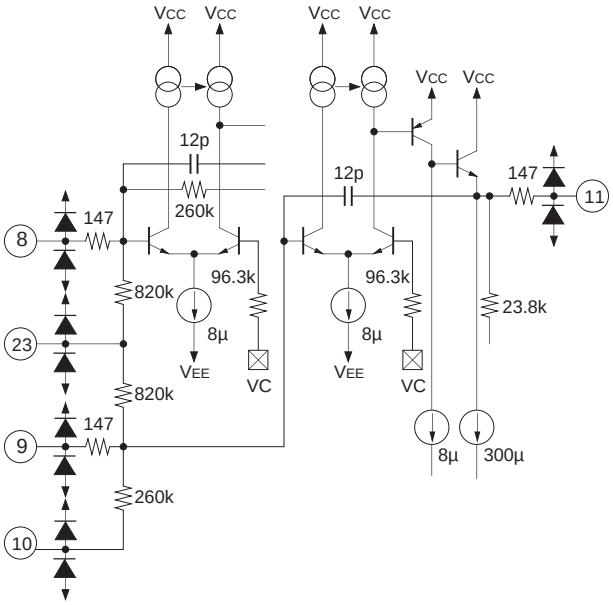
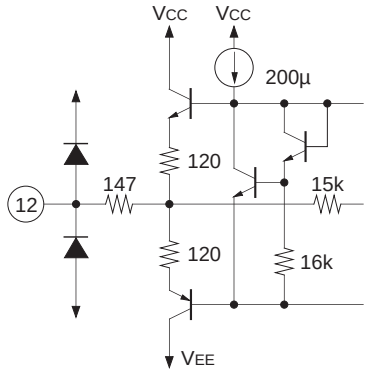
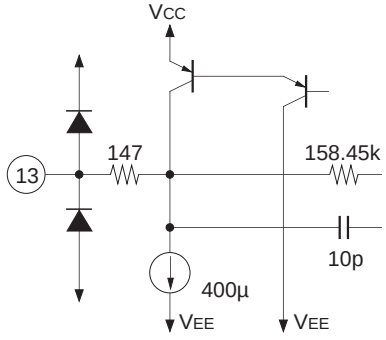
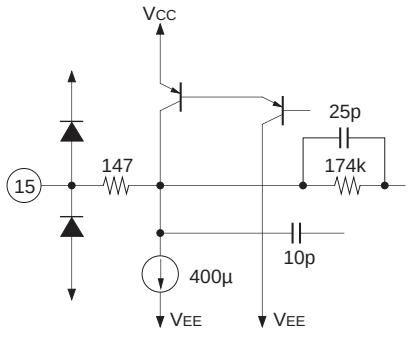
Block Diagram and Pin Configuration

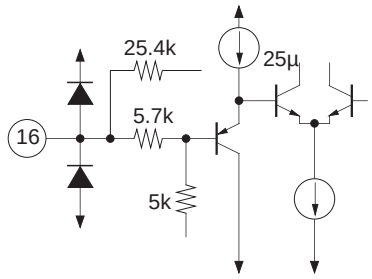
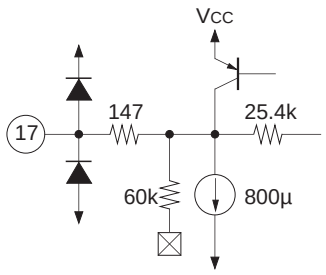
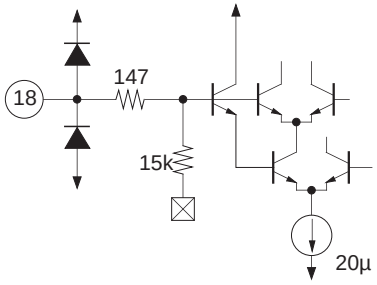
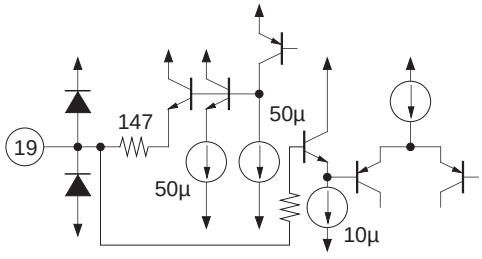
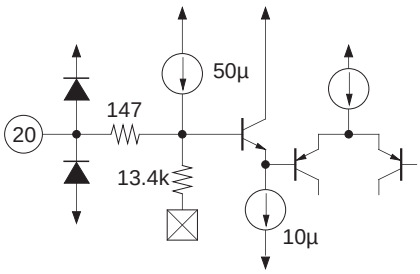


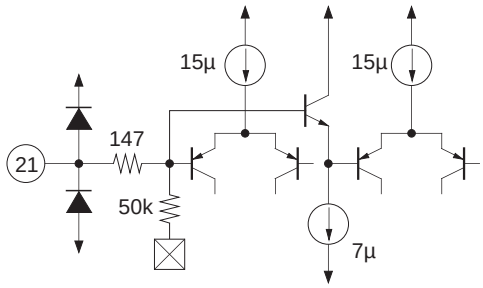
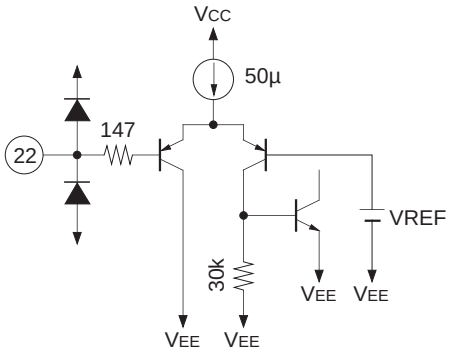
E97428-TE

Pin Description

Pin No.	Symbol	IO	Equivalent circuit	Description
1	LD	O		Output pin of APC amplifier.
2	PD	I		Input pin of APC amplifier.
3 4 5 6 14	A B C D FE BIAS	I I I I I		Input pin of RF and FE amplifiers for Pins 3, 4, 5 and 6; focus bias adjustment for Pin 14.
7	VEE	—		VEE.

Pin No.	Symbol	IO	Equivalent circuit	Description
8 9 10 11 23	F E EI EO LC/PD	I I — — I		Input pin of tracking error amplifier for Pins 8 and 9. An external resistor for V-I conversion should be connected because these pins are for current input. Gain adjustment of input signal from Pin 9 for Pins 10 and 11. Pin 23 is a bias for LC when connected to Vcc and for PD IC when left open.
12	VC	O		DC voltage output pin of (Vcc+VEE)/2. Connect to GND when dual power supply (±2.5 V) is used; connect a smoothing capacitor when single power supply (+5 V) is used.
13	TE	O		Output pin of tracking error amplifier. The F-E signal is output.
15	FE	O		Output pin of focus error amplifier.

Pin No.	Symbol	IO	Equivalent circuit	Description
16	REF	—		Equalizing pin of RF amplifier. Frequency response can be adjusted by connecting CR to this pin.
17	RFO	O		Output pin of RF amplifier.
18	RF_I	I		Input pin of RF amplifier output RFO with capacitance coupled.
19	RFTC	—		External time-constant pin for RF level control.
20	AGCVTH	—		Variable pin of reference level for RF level control. The reference level can be varied by the external resistor.

Pin No.	Symbol	IO	Equivalent circuit	Description
21	AGCCONT	I		RF level control ON (limit level of 50 % / 30 %)/ OFF switching pin. 50 % for V_{CC}, 30 % for open or VC and OFF for V_{EE}.
22	LD ON	I		ON/OFF selection pin of APC amplifier. ON for V_{CC} and OFF for V_{EE}.
24	V_{CC}	—		V_{CC}

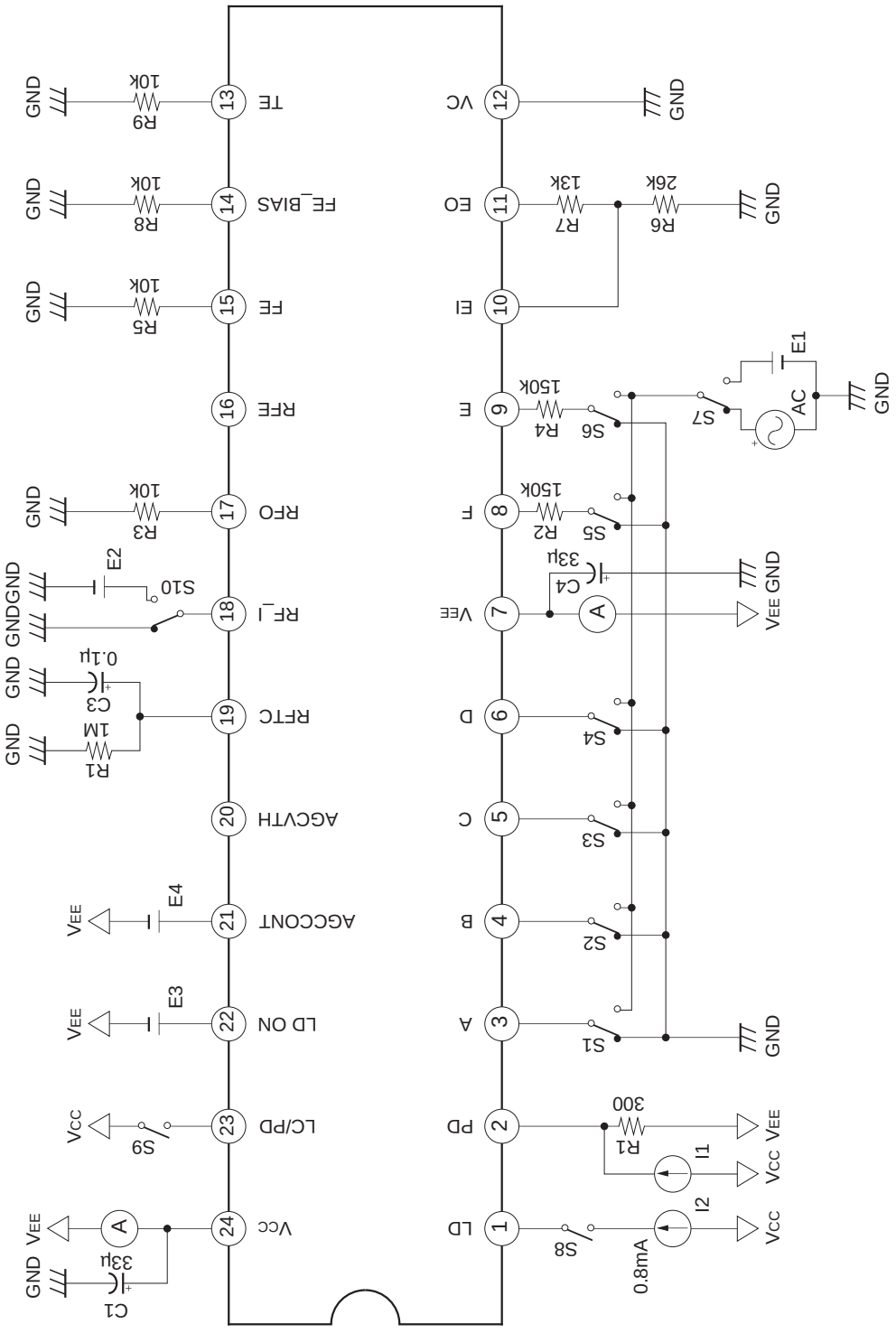
Electrical Characteristics

±2.5 V power supply (V_{CC}=2.5 V, V_{EE}=–2.5 V, VC=GND)

Measurement No.	Measurement item		Symbol	SW conditions										Bias conditions					Measurement pin	Description of I/O waveform and measurement method		Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8	9	10	E1	E2	E3	E4	I1							
1	Current consumption		ICC																24	Input GND		5.59	8.6	11.61	mA
2			IEE																7	Input GND		–11.61	–8.6	–5.59	mA
3	RF amplifier	Offset voltage 1	V17-1																17	Input GND	Output DC measurement	–35	—10	15	mV
4		Voltage gain	V17-2	O	O	O	O												17	Input 1 kHz 100 mVp-p.	Output AC measurement	19.9	22.9	25.9	dB
5		Maximum output amplitude H	V17-3	O	O	O	O			O				280 mV					17		Output DC measurement	2.2	—	—	V
6		Maximum output amplitude L	V17-4	O	O	O	O			O				–280 mV					17		Output DC measurement	—	—	–2	V
7	FE amplifier	Offset voltage	V15-1																15	Input GND	Output DC measurement	–30.0	0	30.0	mV
8		Voltage gain 1	V15-2	O		O													15	Input 1 kHz 100 mVp-p.	Output AC measurement	20.3	23.3	26.3	dB
9		Voltage gain 2	V15-3		O		O												15	Input 1 kHz 100 mVp-p.	Output AC measurement	20.3	23.3	26.3	dB
10		Voltage gain difference	V15-4																15	V15-4=V15-2–V15-3		–3.0	0	3.0	dB
11		Maximum output amplitude L	V15-5	O		O				O				310 mV					15		Output DC measurement		—	–1.9	V
12		Maximum output amplitude H	V15-6		O		O			O				310 mV					15		Output DC measurement	1.9	—		V
13	TE amplifier	Offset voltage 1	V13-1																13	input GND	Output DC measurement	–25	10	45	mV
14		Voltage gain 1	V13-2					O											13	Input 1 kHz 140 mVp-p.	Output AC measurement	21.9	24.9	27.9	dB
15		Voltage gain 2	V13-3						O										13	Input 1 kHz 140 mVp-p.	Output AC measurement	21.9	24.9	27.9	dB
16		Voltage gain difference	V13-4																13	V13-4=V13-2–V13-3		–3.0	0	3.0	dB
17		Maximum output amplitude H	V13-5					O		O				270 mV					13		Output DC measurement	1.9	—	—	V
18		Maximum output amplitude L	V13-6						O	O				270 mV					13		Output DC measurement	—	—	–1.9	V
19	APC	Output voltage 1	V1-1													2.0 V	1.3 V	230 µA	1		Output DC measurement	—	–1.7	–0.3	V
20		Output voltage 2	V1-2													2.0 V	1.3 V	410 µA	1		Output DC measurement	–1.5	0	1.1	V
21		Output voltage 3	V1-3													2.0 V	1.3 V	590 µA	1		Output DC measurement	0.6	2.0	—	V
22		Output voltage 4	V1-4													0.5 V	1.3 V	0 µA	1	LD OFF	Output DC measurement	2.1	2.3	—	V
23		Maximum output amplitude	V1-5								O					2.0 V	1.3 V	0 µA	1	I1=0.8mA	Output DC measurement	—	—	0	V
24	RF level control	50 % limit	V1-6	O	O	O	O			O				50 mV		2.0 V	3.8 V/1.3 V	700 µA	1	Level control : 50 % (E4 : 3.8 V) –Level control OFF (E4 :1.3 V)		–2950	–2350	–1150	mV
25		30 % limit	V1-7	O	O	O	O			O				50 mV		2.0 V	3.3 V/1.3 V	700 µA	1	Level control : 30 % (E4 : 3.3 V) –Level control OFF (E4 :1.3 V)		–1620	–1120	–120	mV
26		–50 % limit	V1-8										O		800 mV	2.0 V	3.8 V/1.3 V	170 µA	1	Level control : –50 % (E4 : 3.8 V) –Level control OFF (E4 : 1.3 V)		1550	2350	2800	mV
27		–30 % limit	V1-9										O		800 mV	2.0 V	1.8 V/1.3 V	170 µA	1	Level control : –30 % (E4 :1.8 V) –Level control OFF (E4 : 1.3 V)		598	1098	1598	mV
28	Center output voltage		V12-1																12		Output DC measurement	–100	—	100	mV

∗ O in the SW conditions represents the ON state.

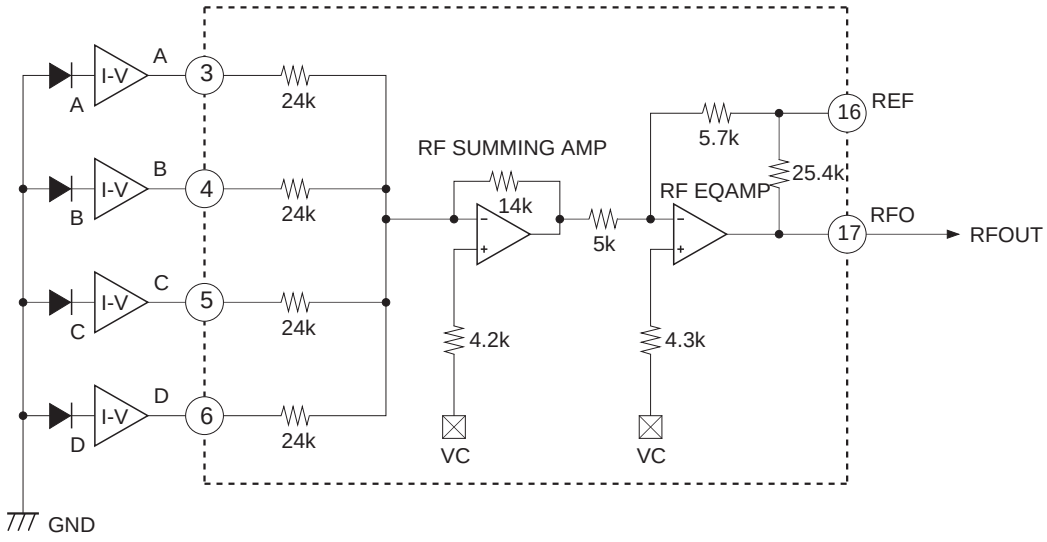
Electrical Characteristics Measurement Circuit



Description of Functions

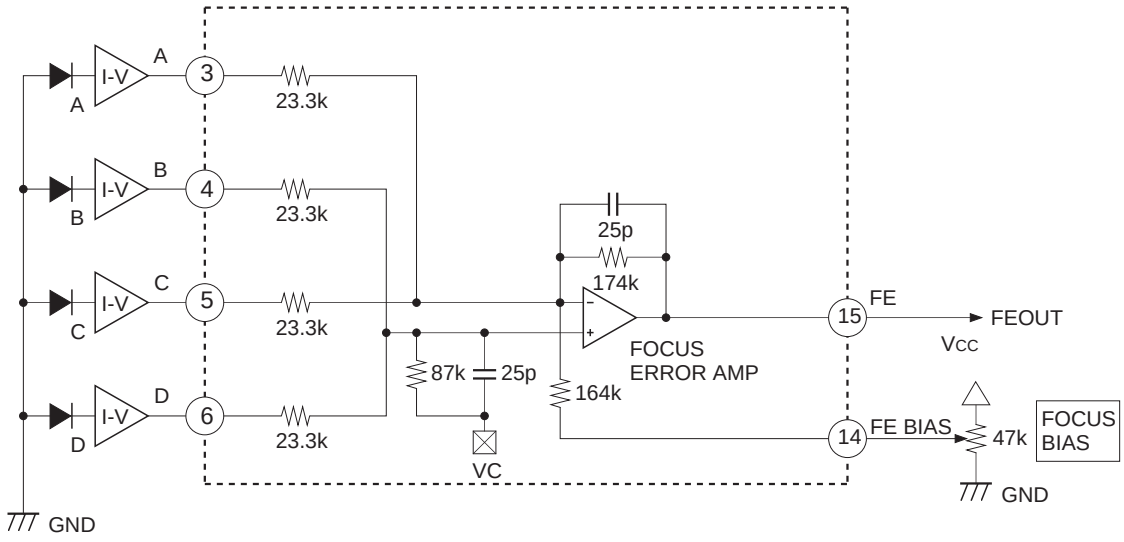
RF Amplifier

Each signal current from the photodiodes A, B, C and D is I-V converted, and input to Pins 3, 4, 5 and 6. These signals are added by the RF summing amplifier and equalized by the RF equalizing amplifier and then output to Pin 17. When the RF signal is equalized, an equalizing circuit is added to Pin 16.



Focus Error Amplifier

The operation of (B+D)–(A+C) is performed and the signal is output to Pin 15. Pin 14 is used for bias adjustment of the focus error signal.

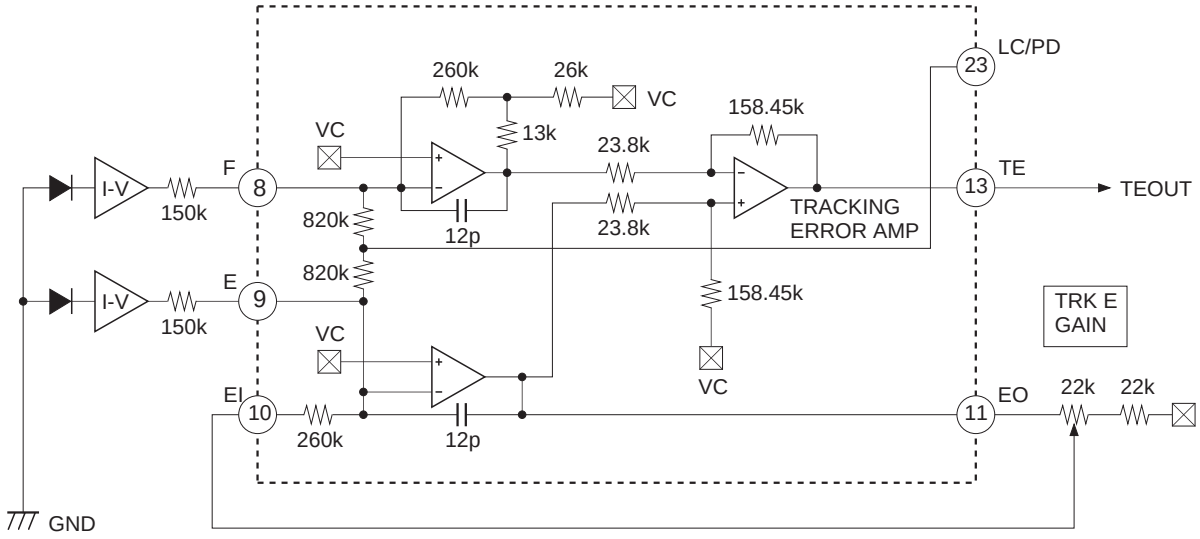


Tracking Error Amplifier

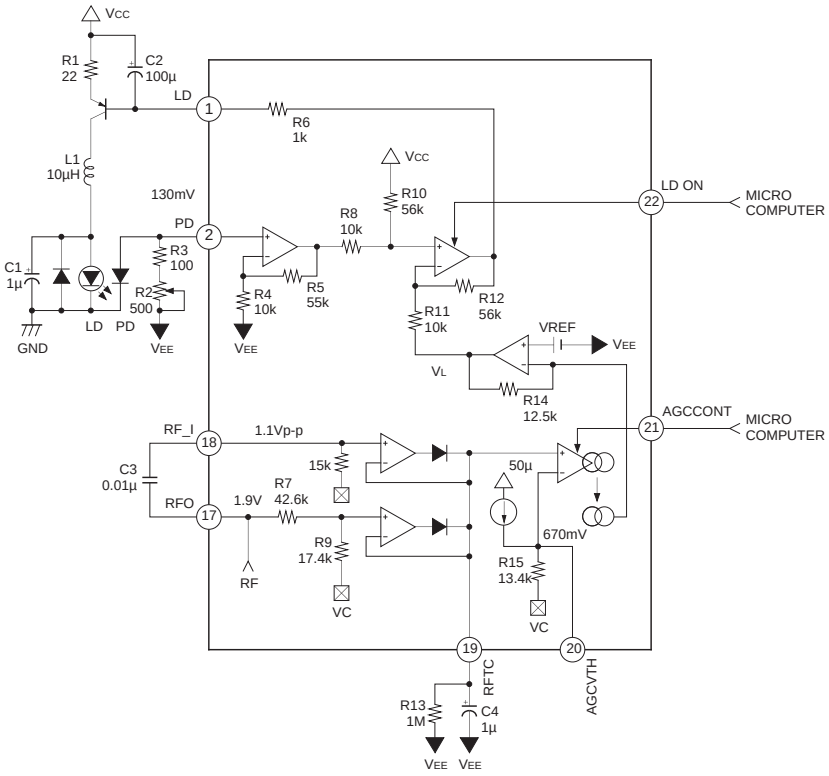
Each signal current from the photodiodes E and F is I-V converted and input to Pins 8 and 9 via an input resistor which determines the gain. The signal is amplified by the gain amplifier, operated by the tracking error amplifier and then the (F-E) signal is output to Pin 13.

The E input gain can be adjusted by Pin 11.

Pin 23 can be used as a bias for LC when connected to V_{CC} and as a bias for PD IC when left open.



APC & Laser Power Control



• APC

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics.

The APC circuit is used to maintain the optical power output at a constant level.

The laser diode current is controlled according to the monitor photo diode output.

APC is set to ON by connecting the LD ON pin to V_{CC} ; OFF by connecting it to V_{EE}.

• Laser Power Control (LPC)

The RF level is stabilized by attaching an offset to the APC VL and controlling the laser power in sync with the RF level fluctuations.

The RFO and RF_I levels are compared and the larger of the two is smoothed by the RFTC's external CR.

This signal is then compared with the reference level.

The laser power is controlled by attaching an offset to VL according to the results of comparison with the reference level.

Set the reference level to 670 mV. (center voltage reference)

When the reference level is changed, connect the external resistor to the AGCVTH pin (Pin 20). The reference level can be lowered by connecting the resistor between Pin 20 and the center output voltage or between Pin 20 and V_{CC}.

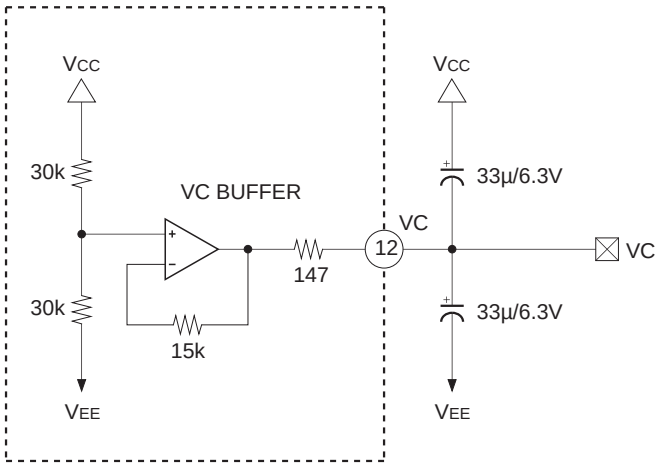
The AGCCONT pin (Pin 21) is used to switch the level of the laser power control circuit ; OFF, ON (laser power limit of 30 %) and ON (laser power limit of 50 %)

∗ For the laser power limit, 50 % is recommended for PD IC ; 30 % for LC.

AGCCONT	LPC	LPC limit	VL variable range
L (V_{EE})	OFF	—	Approximately 1.27 V
M (VC or OPEN)	ON	30 %	Approximately 1.27 V±350 mV
H (V_{CC})	ON	50 %	Approximately 1.27 V±570 mV

Center Voltage Generation Circuit

This circuit provides the center potential when this IC is used at single power supply. The maximum current is approximately ±3 mA. The output impedance is approximately 147 Ω. Connect this circuit to GND when used at dual power supply.



Notes on Operation

1. Power supply

   The CXA2549M can be used either at dual power supply or single power supply. The table below shows the connection of power supply for each case.

	V_{CC}	V_{EE}	VC
Dual power supply	+power supply	–power supply	GND
Single power supply	Power supply	GND	OPEN

2. Laser Power Control

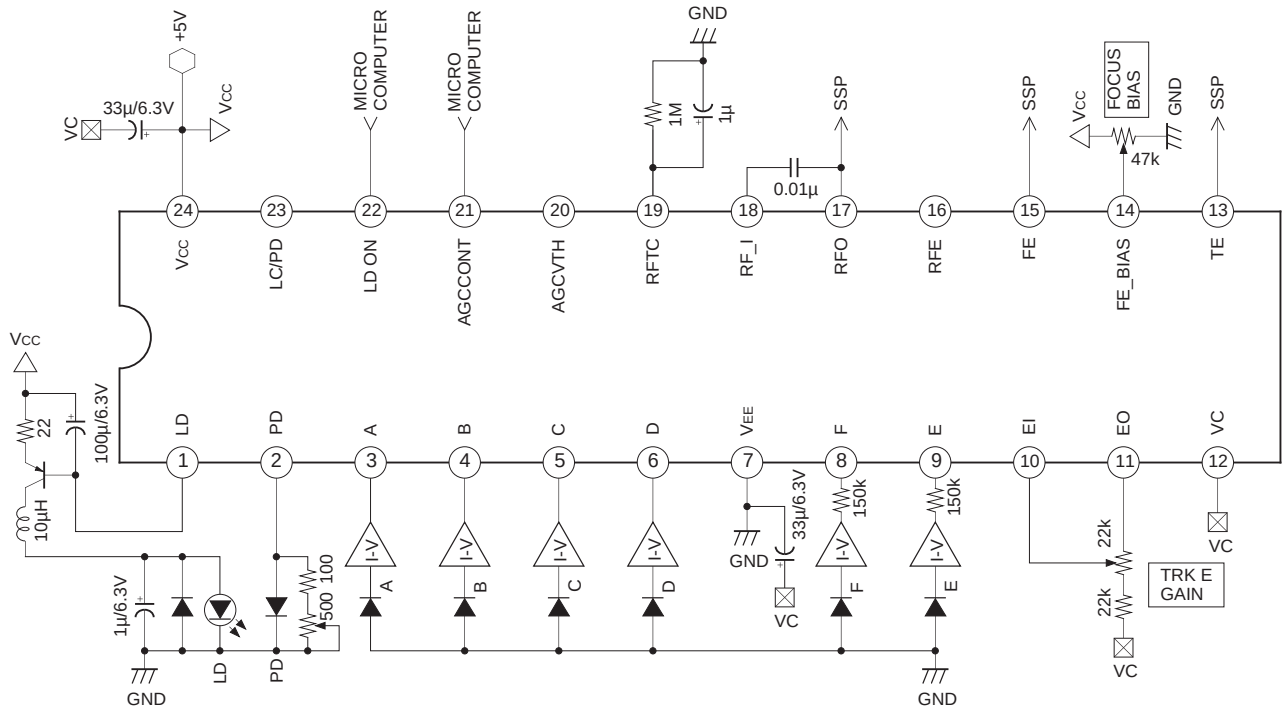
   The RF level is stabilized by attaching an offset to the APC VL and controlling the laser power in sync with the RF level fluctuations. Therefore, use this circuit in the state where the focus servo is applied.

   The laser life is shortened by increasing the laser power when the less light is reflected from the disc. It is recommended that the typical laser power value is set lower to maintain the laser life.

   Take care of the laser maximum ratings when using the laser power control circuit.

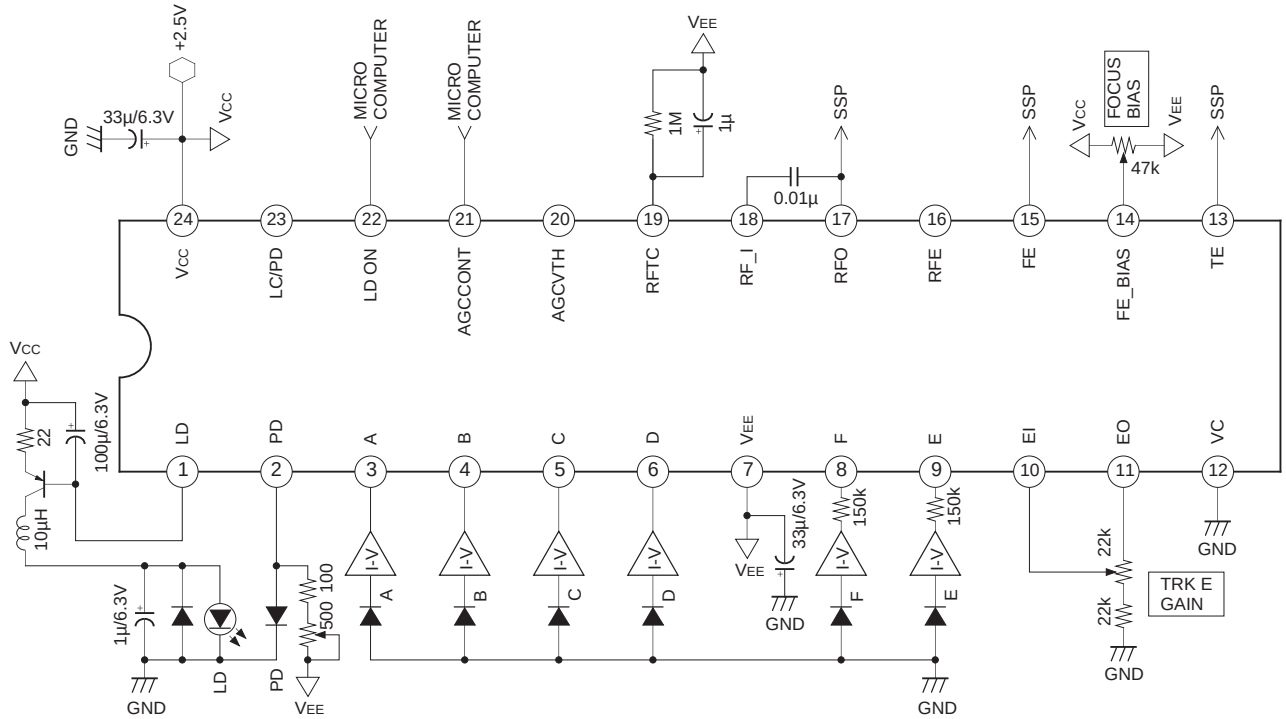
Application Circuit

• For single power supply +5 V



∗ Connect Pin 23 to VCC when LC is used.

• For dual power supply +2.5 V

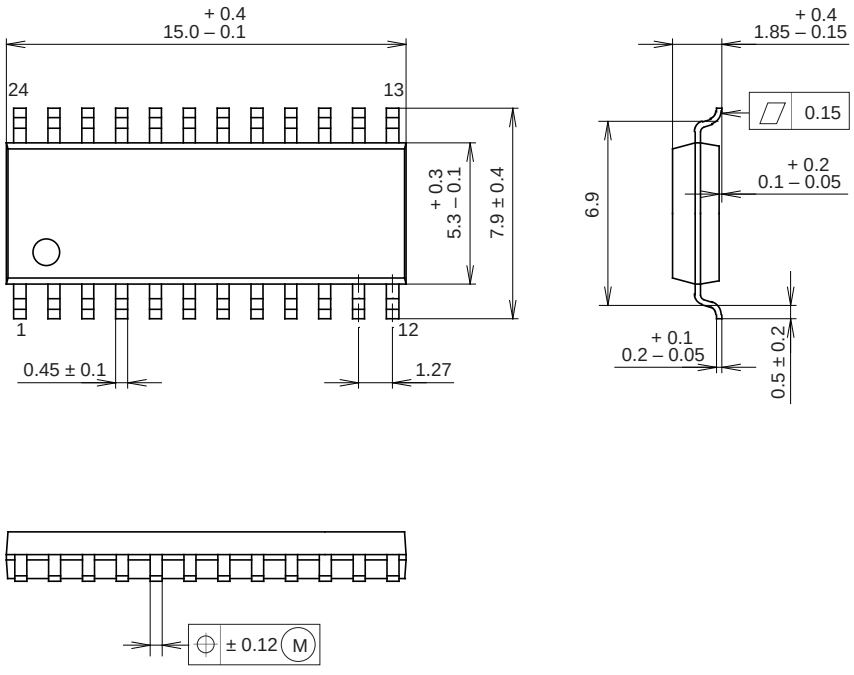


∗ Connect Pin 23 to VCC when LC is used.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

24PIN SOP (PLASTIC)



SONY CODE	SOP-24P-L01
EIAJ CODE	*SOP024-P-0300-A
JEDEC CODE	

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g