OptiMOS® Chip data sheet

Feature

- N-Channel
- Enhancement mode
- 175°C operating temperature
- Avalanche rated
- d*v*/d*t* rated
- Integrated gate resistance

for easy parallel connection

V_{DS}	75	V
$R_{DS(on)}$	4.2	mΩ
Die size	7 x 6	mm^2
Thickness	175	µm

Ordering Code

unsawn wafer on foil	on request
sawn wafer on foil	Q67061-S7146
surf tape	on request

DESCRIPTION

- Assembly by epoxy die bonding or soldering
- AQL 1.5 for visual inspection according to failure catalog A67207-A7001-A001 issue C on 100% measured wafer
- Storage of chips and wafer according technical guideline 14 Doc. No. A66003-R14-T1-B-35

Maximum Ratings, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current [1)2)] T_C=25°C	I_D	227	A
Avalanche energy, single pulse[1)] I_D=80A, V_{DD}=25V, R_{GS}=25Ω	E_{AS}	1070	mJ
Repetitive avalanche energy, limited by T_{jmax} [1)2)]	E_{AR}	50	mJ
Gate source voltage	V_{GS}	±20	V
Additional gate resistance	R_G	5 ±20%	Ω
Operating and storage temperature	T_j , T_{stg}	-55... +175	°C

[1] Defined by design. Not subject to production test.

[2] Calculated with R_{thJC} = 0.3 K/W

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

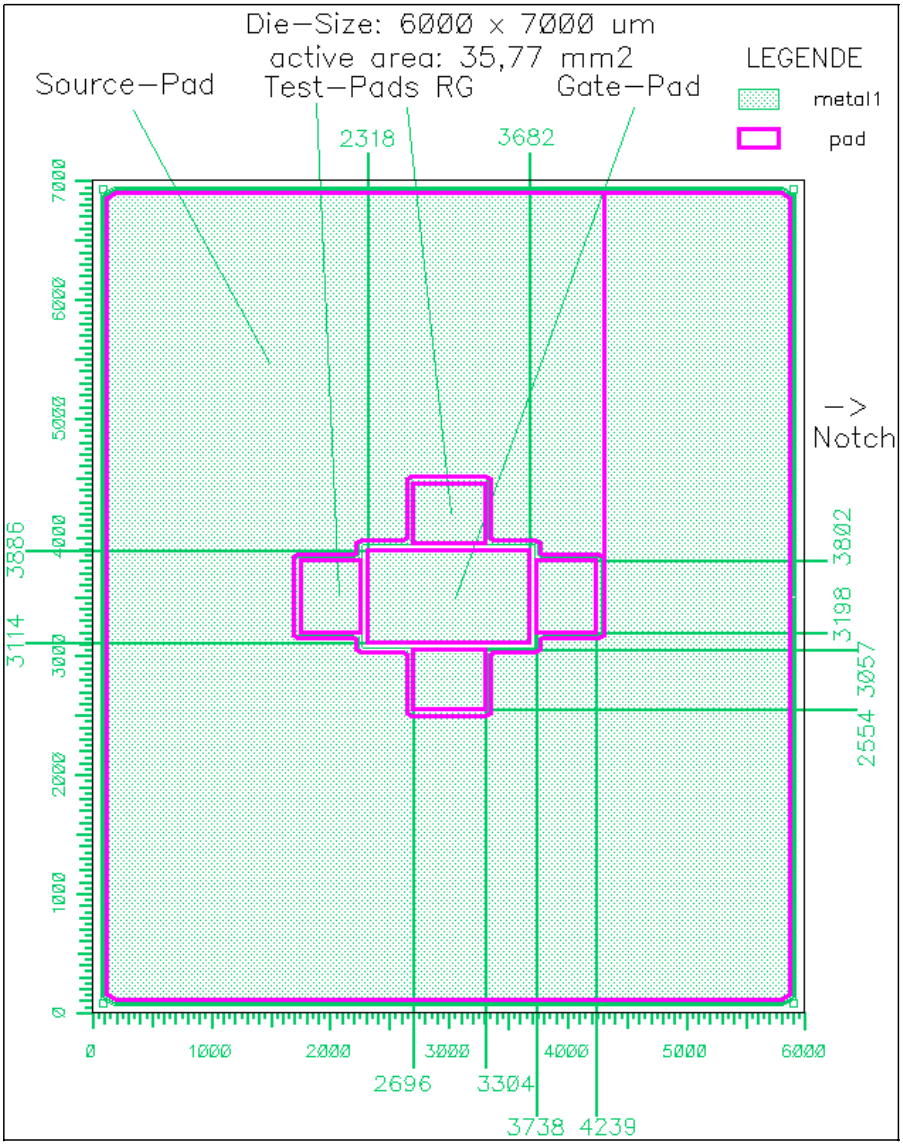
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage V_{GS}=0V, I_D=1mA	$V_{(BR)DSS}$	75	-	-	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 250 µA	$V_{GS(th)}$	2.1	3	4	
Zero gate voltage drain current	I_{DSS}				µA
V_{DS}=75V, V_{GS}=0V, T_j=25°C		-	0.01	1	
V_{DS}=75V, V_{GS}=0V, 125°C, 1)		-	1	100	
Gate-source leakage current V_{GS}=20V, V_{DS}=0V	I_{GSS}	-	1	100	nA
On-state resistance1) V_{GS}=10V, I_D=134A	$R_{DS(on)}$	-	3.7	4.2	mΩ
Dynamic Characteristics1)					
Gate to source charge V_{DD}=60V, I_D=80A	Q_{gs}	-	27	36	nC
Gate to drain charge V_{DD}=60V, I_D=80A	Q_{gd}	-	82	123	
Gate charge total V_{DD}=60V, I_D=80A, V_{GS}=0 to 10V	Q_g	-	189	251	
Reverse Diode1)					
Inverse diode forward voltage V_{GS}=0V, I_F=80A	V_{SD}	-	0.9	1.3	V

1Defined by design. Not subject to production test.

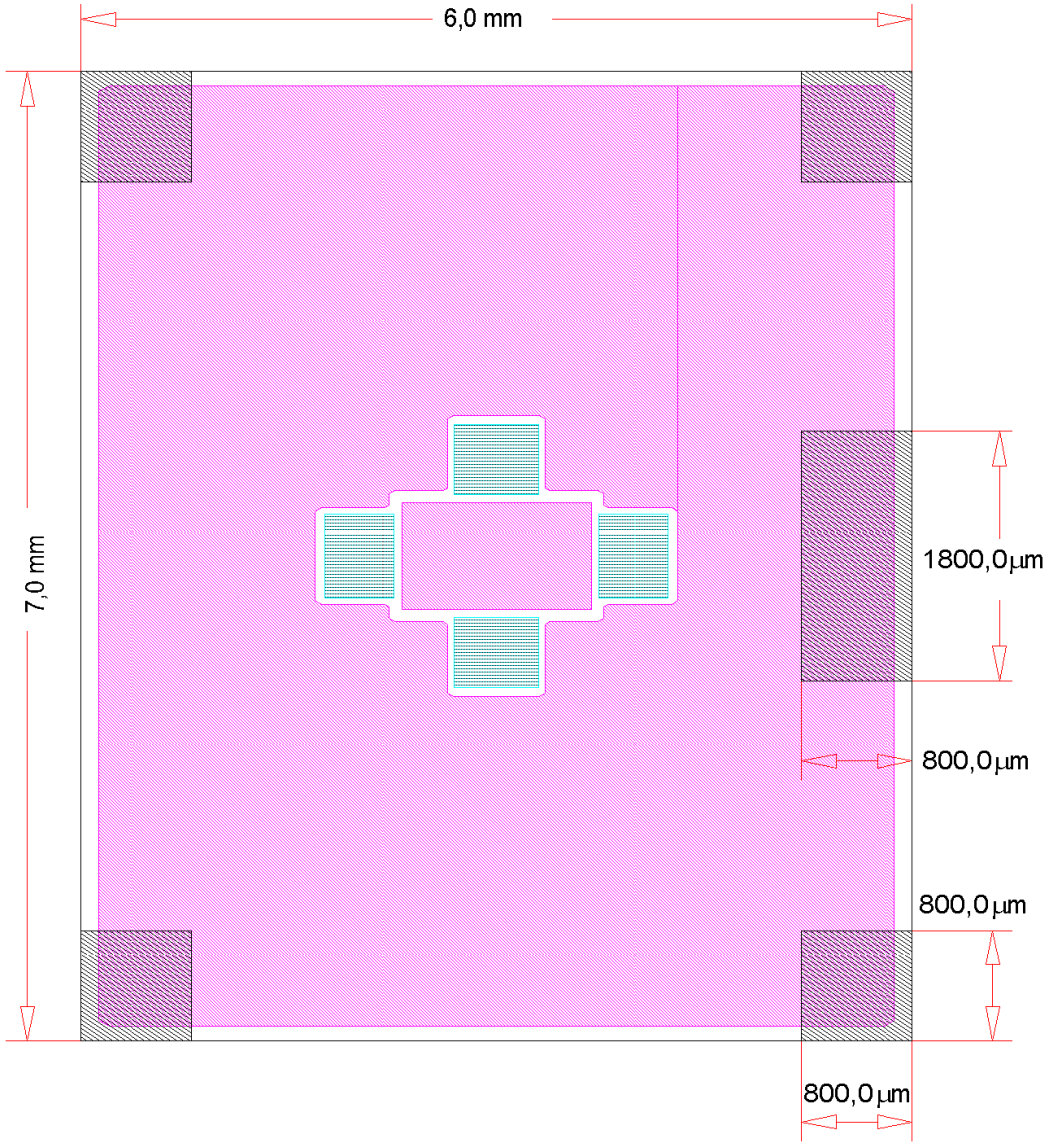
CHIP Parameters

Saw street width	-
Passivation frontside	Nitride
Metalization frontside	5µ AlSiCu
Metalization gate pad	AlSiCu
Metalization backside	Ni-Ag System
Die bond	applicable: soft or glue
Wire bond	Al wedge-wedge

Chip - Layout:



Additional information for bonding:



Area for testing purposes: bonding here is not recommended

Area of integrated gate resistance covered with Al metallization: no contact with gate bond wires allowed in order to prevent short circuit of gate resistance

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Further information
Please notice that the part number is BSIPC42S2N08, for simplicity the device is referred to by the term SIPC42S2N08 throughout this documentation.