

■ OVERVIEW

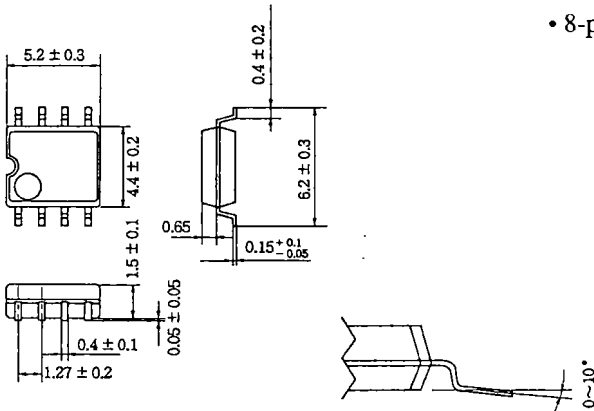
The SM5610 series are C-MOS ICs for quartz crystal oscillating module. Each IC has a high frequency oscillating circuit and dividers with low current consumption.

There are many kinds of type, capacitor for oscillation on chip or not, output frequency: f_0 (fundamental), $f_0/2$, $f_0/4$, or $f_0/8$, and I/O level TTL or CMOS (Refer to the SERIES TABLE).

■ FEATURES

- Operating voltage (4V - 6V)
- Built-in feed back resistance of oscillation circuit
- 3-state function
- Low current consumption
- Chip form, 8-pin SOP
- Molybdenum gate C-MOS
- For fundamental wave use

■ PACKAGE DIMENSION

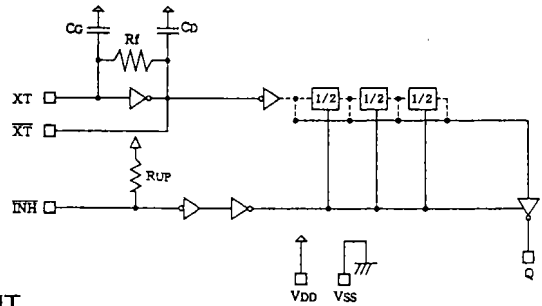


■ PIN COORDINATES

UNIT: μm

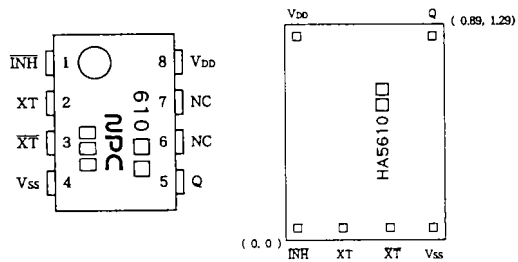
NAME	X	Y
INH	145	140
XT	345	140
$\overline{\text{XT}}$	545	140
V _{SS}	745	140
Q	745	1150
V _{DD}	145	1155

■ BLOCK DIAGRAM



■ PIN OUT

• 8-pin SOP (TOP VIEW)



CHIP SIZE: 0.89 × 1.29mm
CHIP THICKNESS: 400 ± 30 μm

■ PIN DESCRIPTION

NAME	FUNCTION
XT	Input terminal for oscillating
$\overline{\text{XT}}$	Output terminal or oscillating
INH	"L" High impedance On-chip pull-up resistance
V _{DD}	Power supply
V _{SS}	Ground
Q	Output (Selected by master slice) f_0 , $f_0/2$, $f_0/4$, or $f_0/8$

f_0 : Fundamental frequency

■ SERIES TABLE

VERSIONS	Output frequency	Output duty level	Output current
SM5610K1	f_0	TTL	16mA
K3	$f_0/2$	TTL	16mA
K5	$f_0/4$	TTL	16mA
K7	$f_0/8$	TTL	16mA
H1	f_0	CMOS	4mA
H3	$f_0/2$	CMOS	4mA
H5	$f_0/4$	CMOS	4mA
H7	$f_0/8$	CMOS	4mA
N1	f_0	CMOS	16mA
N3	$f_0/2$	CMOS	16mA
N5	$f_0/4$	CMOS	16mA
N7	$f_0/8$	CMOS	16mA

Note: SOP package is named SM5610 □ □ S.

■ ABSOLUTE MAXIMUM RATING ($V_{SS}=0V$)

ITEM	SYMBOL	CONDITIONS	UNIT
Supply voltage	V_{DD}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{DD}+0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{DD}+0.5$	V
Storage temperature	T_{STG1}	-65 to +150 (chip)	°C
	T_{STG2}	-40 to +125 (SOP)	
Output current	I_{OUT}	N, K series 25	mA
		H series 10	
* Power dissipation	P_w	200	mW
* Soldering temperature	T_{SLD}	255	°C
* Soldering time	t_{SLD}	10	S

Note: * mark is useful at SOP package

■ RECOMMENDED OPERATIONAL CONDITIONS ($V_{SS}=0V$)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Operating voltage	V_{DD}	4.0	5.0	6.0	V
Input voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating temperature	T_{OPR}	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

(V_{SS}=0V, Ta=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT	
				MIN	TYP	MAX		
H-level output voltage	V _{OH}	SM5610K, N	Q pin, Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA	3.9	4.2	V	
				V _{DD} =4.0V, I _{OH} =14.4mA	3.4	3.7		
		SM5610H		V _{DD} =4.5V, I _{OL} =4.0mA	3.9	4.2		
				V _{DD} =4.0V, I _{OL} =3.6mA	3.4	3.7		
L-level output voltage	V _{OL}	SM5610K, N	Q pin, Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA		0.3	0.4	V
				V _{DD} =4.0V, I _{OH} =14.4mA		0.3	0.4	
		SM5610H		V _{DD} =4.5V, I _{OL} =4.0mA		0.3	0.5	
				V _{DD} =4.0V, I _{OL} =3.6mA		0.3	0.5	
Output leak current	I _Z	Q pin, Fig. 1, INH="L", V _{DD} =6.0V		V _{OH} =V _{DD} V _{OL} =V _{SS}			10	μA
H-level input voltage	V _{IH}	INH pin		V _{DD} =5±0.5V	2.0			V
				V _{DD} =5±1.0V	2.2			
L-level input voltage	V _{IL}	INH pin		V _{DD} =5±1.0V			0.8	V
Current consumption	I _{DD1}	Load circuit 1 (SM5610N, H) Load circuit 2 (SM5610K), Fig. 2, INH=OPEN, CL=15pF		V _{DD} =5V, Ta=25°C		15	20	mA
				V _{DD} =5.5V			30	
				V _{DD} =6.0V			35	
	I _{DD2}	Load circuit 1 (SM5610N, H) Load circuit 2 (SM5610K), Fig. 2, INH=OPEN, CL=50pF		V _{DD} =5V, Ta=25°C		21	26	
				V _{DD} =5.5V			36	
				V _{DD} =6.0V			41	
INH pin pull-up resistance	R _{UP}	Fig. 3			50		250	kΩ
Feedback resistance	R _F	Fig. 4		V _{DD} =5±0.5V	1.0		5.0	MΩ
				V _{DD} =5±1.0V	0.9		5.5	
Internal capacitor	C _G	Design value			19	27	35	pF
	C _D				19	27	35	

■ SWITCHING CHARACTERISTICS

V_{SS} = 0V, Ta= -40 to +85°C unless otherwise noted.

1. K series

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT	
				MIN	TYP	MAX		
Output rise time	T _{R1}	Load circuit 2, Fig. 2 0.4 to 2.4V	C _L =15pF	V _{DD} =5±0.5V	1.5	3.0	ns	
				V _{DD} =5±1.0V		3.5		
	C _L =50pF		V _{DD} =5±0.5V	3.0	6.0			
			V _{DD} =5±1.0V		7.0			
Output fall time	T _{F1}	Load circuit 2, Fig. 2 2.4V to 0.4V	C _L =15pF	V _{DD} =5±0.5V	1.5	3.0	ns	
				V _{DD} =5±1.0V		3.5		
	C _L =50pF		V _{DD} =5±0.5V	3.0	6.0			
			V _{DD} =5±1.0V		7.0			
Output duty cycle	DUTY	Load circuit 2, Fig. 2, C _L =15pF, Ta=25°C, V _{DD} =5.0V		45		55	%	
Output disable delay time	T _{PLZ}	Fig. 2, Ta=25°C, V _{DD} =5±1.0V, Load C _L ≤50pF					100	ns
Output enable delay time	T _{PZL}						100	
Maximum operating frequency	f _{MAX}	Load circuit 2, Fig. 2, V _{DD} =5±1.0V			30			MHz

SM5610

2. H series

V_{SS} = 0V, T_a = -40 to +85°C unless otherwise noted.

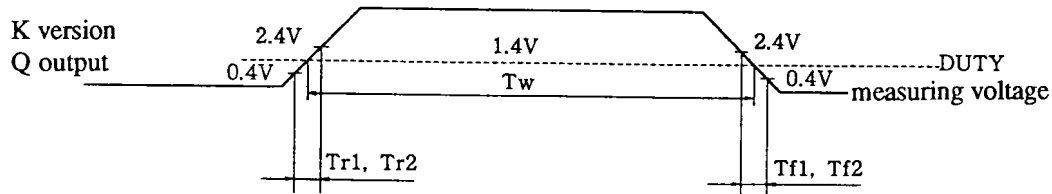
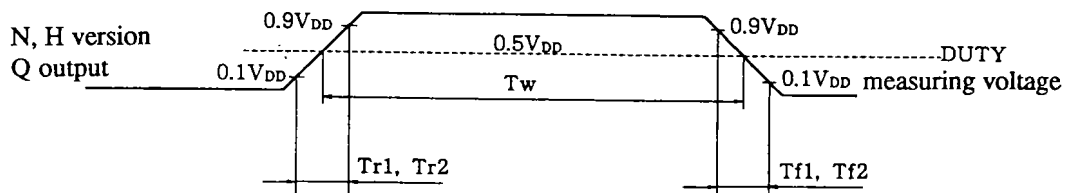
ITEM	SYMBOL	CONDITIONS			LIMITS			UNIT
					MIN	TYP	MAX	
Output rise time	T _{r1}	Load circuit 1, Fig. 2 0.1V _{DD} to 0.9V _{DD}	C _L =15pF	V _{DD} =5±0.5V	5.0	10	ns	
				V _{DD} =5±1.0V		12		
	C _L =50pF		V _{DD} =5±0.5V	13	26			
			V _{DD} =5±1.0V		30			
Output fall time	T _{f1}	Load circuit 1, Fig. 2 0.9V _{DD} to 0.1V _{DD}	C _L =15pF	V _{DD} =5±0.5V	5.0	10	ns	
				V _{DD} =5±1.0V		12		
	C _L =50pF		V _{DD} =5±0.5V	13	26			
			V _{DD} =5±1.0V		30			
Output duty cycle	DUTY	Load circuit 1, Fig. 2, C _L =15pF, T _a =25°C, V _{DD} =5.0V			45	55	%	
Output disable delay time	T _{PLZ}	Fig. 2, T _a =25°C, V _{DD} =5±1.0V, Load C _L ≤50pF				100	ns	
Output enable delay time	T _{PZL}					100		
Maximum operating frequency	f _{MAX}	Load circuit 1, Fig. 2, V _{DD} =5±1.0V			30		MHz	

3. N series

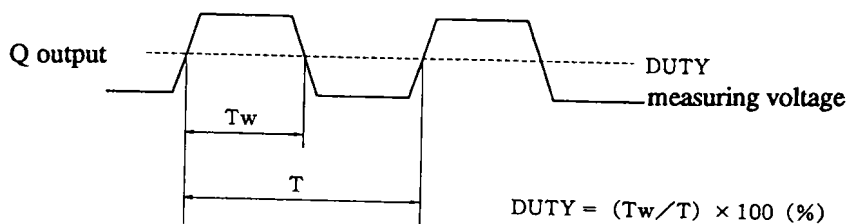
V_{SS} = 0V, T_a = -40 to +85°C unless otherwise noted.

ITEM	SYMBOL	CONDITIONS			LIMITS			UNIT
					MIN	TYP	MAX	
Output rise time	T _{r1}	Load circuit 1, Fig. 2 0.1V _{DD} to 0.9V _{DD}	C _L =15pF	V _{DD} =5±0.5V	1.5	3.0	ns	
				V _{DD} =5±1.0V		3.5		
	C _L =50pF		V _{DD} =5±0.5V	3.0	6.0			
			V _{DD} =5±1.0V		7.0			
Output fall time	T _{f1}	Load circuit 1, Fig. 2 0.9V _{DD} to 0.1V _{DD}	C _L =15pF	V _{DD} =5±0.5V	1.5	3.0	ns	
				V _{DD} =5±1.0V		3.5		
	C _L =50pF		V _{DD} =5±0.5V	3.0	6.0			
			V _{DD} =5±1.0V		7.0			
Output duty cycle	DUTY	Load circuit 1, Fig. 2, C _L =50pF, T _a =25°C, V _{DD} =5.0V			45	55	%	
Output disable delay time	T _{PLZ}	Fig. 2, T _a =25°C, V _{DD} =5±1.0V, Load C _L ≤50pF				100	ns	
Output enable delay time	T _{PZL}					100		
Maximum operating frequency	f _{MAX}	Load circuit 1, Fig. 2, C _L =50pF, V _{DD} =5±1.0V			30		MHz	

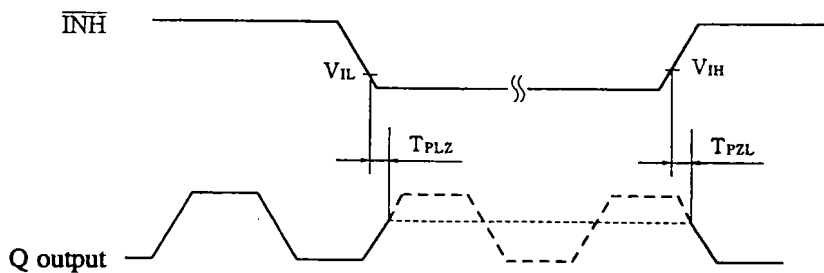
■ WAVEFORMS FOR SWITCHING TIME



■ DUTY FACTOR



■ OUTPUT DISABLE TIME



INH input waveform Tr = Tf 10 ns or less

■ FUNCTION

CONTROL	Output terminal
INH	Q
H (OPEN)	Output ($f_0/f_0/2$; $f_0/4$ or $f_0/8$)
L	High impedance

f_0 : Fundamental frequency