



MICROCHIP PIC16F631/677/685/687/689/690

PIC16F631/677/685/687/689/690 Rev. A Silicon/Data Sheet Errata

The PIC16F631/677/685/687/689/690 parts you have received conform functionally to the Device Data Sheet (DS41262C), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC16F631/677/685/687/689/690 silicon.

1. Module: EUSART (PIC16F687/689/690 only)

1.1 WUE Bit is not clearing.

After a wake-up due to a Break character, the WUE bit is not automatically cleared.

Work around

Clear the WUE bit after waking up.

1.2 Auto-baud captures the incorrect baud rate after a break.

The SPBRGH:SPBRG registers are not being initialized correctly. If WUE and ABDEN are set at the same time and a Break character followed by a Sync character are received, then the calculated baud rate will be random.

Work around

Set WUE and wait for the wake-up to occur.

Clear SPBRGH:SPBRG after waking up with the break.

Set ABDEN to begin the auto-baud process.

1.3 Auto-baud calculates a baud rate value that is +2.

The SPBRGH:SPBRG are not initialized correctly when ABDEN is set. This causes the measured baud rate to be high by two counts.

Work around

Clearing the SPBRGH:SPBRG registers will correctly initialize the baud rate counter. After the auto-baud has been completed, the baud rate will now be +1. The firmware should now subtract 1 from the baud rate generator to produce the correct baud rate.

1.4 Delay after auto-baud before transmit is allowed.

After the auto-baud Sync character has been received and the RCIF flag is set, there is approximately 17 ms of delay before the transmitter is enabled.

Work around

After the RCIF flag is set indicating the baud rate has been measured, read the SPBRG register and write the value back to SPBRG. This will terminate the delay, and enable the transmitter module.

1.5 Auto-baud sequence cannot be aborted in some cases.

If an auto-baud is started but no edges are received, there is no way to leave Auto-Baud mode.

Work around

Use the Watchdog Timer to reset the entire device.

1.6 Clearing SPEN does not reset EUSART state machine correctly.

When SPEN is cleared, the entire EUSART is frozen. When SPEN is set, the EUSART resumes where it left off. This can cause some unexpected behavior.

Work around

To reset the EUSART, toggle TXEN and CREN after clearing SPEN. This will reset the transmit and receive state machines.

1.7 Extra character transmitted after auto-baud.

If TXEN is high when ABDEN is set, it will be cleared as soon as the auto-baud process begins, and reset as soon as the auto-baud process completes. When TXEN is reset, the character in the transmit queue will be transmitted.

Work around

Before starting auto-baud, clear TXEN. This will reset the transmit state machine correctly. After the auto-baud is complete and the firmware has brought TXEN high, no character will be transmitted.

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1. Module: SSP (PIC16F687/689/690 only)

In any of the I²C™ modes, the SSP module will fail to recognize the first Start bit received after a transition from module disable to module enable. Subsequent Stop bits and Start bits are detected properly.

Work around

Enable the SSP module in SSPMSK Access mode before changing the mode to the desired I²C operation.

EXAMPLE 1: CODE EXAMPLE

```
MOVLW  B'00111001'  ;Module enable, clock
MOVWF  SSPCON        ;enable, SSPMSK access.
                          ;Optionally load
                          ;address mask value
                          ;into SSPMSK register.
MOVLW  B'00110110'  ;Module enable, clock
MOVWF  SSPCON        ;enable, 7-bit address
                          ;I2C slave.
```

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Clarifications/Corrections to the Data Sheet:

1. Module: 20-Pin QFN Pin Diagram Title

Change Title: **PIC16F690** Pin Diagram (QFN) to **PIC16F631/677/685/687/689/690** Pin Diagram (QFN), for the 20-pin QFN, on page 7.

REVISION HISTORY

Rev A Document (7/2005)

Original release of this document.

Clarifications/Corrections to the Data Sheet:

Added Modules 1 through 7:

Module 1: Device V_{DD} Range

Module 2: 4x4 QFN Package Marking

Module 3: Table 1-1: Pinout Description – PIC16F685

Module 4: Register 10-5: EECON1

Module 5: Table 11-2: Registers Associated with Capture, Compare and Timer1

Module 6: Section 12.0 EUSART

Module 7: Section 14.2.2 MCLR

Rev B Document (8/2005)

Silicon Section:

Added Module 1: EUSART (PIC16F687/689/690 only).

Clarifications/Corrections to the Data Sheet:

Added Modules 8 and 9:

Module 8: SSP Module Overview

Module 9: Electrical Specifications.

Rev C Document (11/2005)

Silicon Section:

Added Module 2: SSP (PIC16F687/689/690 only)

Rev D Document (01/2006)

Clarifications/Corrections to the Data Sheet:

Replaced the 20-Lead QFN package diagram in Module 2: 4x4 QFN Package Marking.

Rev E Document (7/2006)

Data Sheet Clarifications/Corrections Section: Removed Items 1 through 9, which have been incorporated into the data sheet. Added Item 1, 20-pin QFN Pin Diagram Title change.

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