DATA SHEET

BLV98CE
UHF power transistor

Product specification

March 1993

Philips
Semiconductors

PHILIPS

UHF power transistor BLV98CE

FEATURES

- Internal input matching to achieve high power gain
- Implanted ballasting resistors an for optimum temperature profile
- Gold metallization ensures excellent reliability

DESCRIPTION

NPN silicon planar epitaxial transistor in an SOT-171 envelope, intended for common emitter, class-AB operation in radio transmitters for the 960 MHz communications band. The transistor has a 6-lead flange envelope, with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

RF performance up to T_h = 25 °C in a common emitter class-AB circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_P (dB)	η_c (%)
c.w. class-AB	960	24	15	> 7.5	> 50

PINNING - SOT171A

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	b	base
4	c	collector
5	e	emitter
6	e	emitter

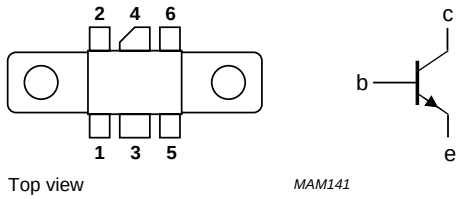


Fig.1 Simplified outline and symbol.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector base voltage	open emitter	–	50	V
V_{CEO}	collector emitter voltage	open base	–	27	V
V_{EBO}	emitter base voltage	open collector	–	3.5	V
I_C	collector current	DC or average	–	1.5	A
I_{CM}	collector current	peak value f > 1 MHz	–	4.5	A
P_{tot}	total power dissipation	f > 1 MHz T_{mb} = 25 °C	–	40	W
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	200	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{thj\text{-}mb}$	from junction to mounting base (RF)		–	4.4	K/W
$R_{th\ mb\text{-}h}$	from mounting base to heatsink		–	0.4	K/W

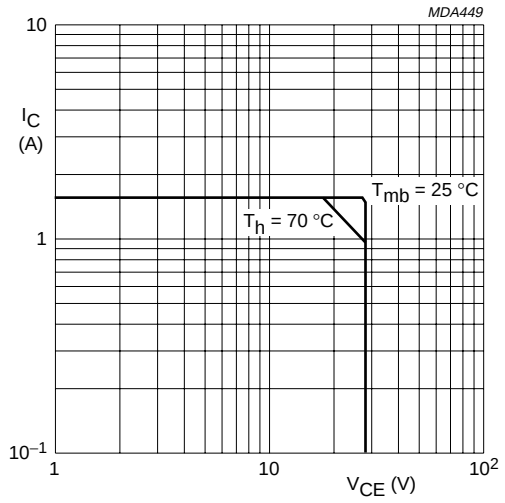
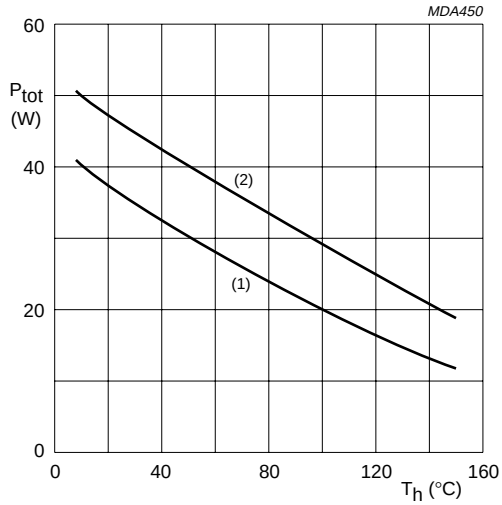


Fig.2 DC SOAR.



(1) DC or RF operation

(2) short-term operation during mismatch

Fig.3 Power/temperature derating.

CHARACTERISTICS

at T_j = 25 °C unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter I_C = 25 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base I_C = 50 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector I_E = 5 mA	3.5	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0 V_{CE} = 27 V	–	–	5	mA
h_{FE}	DC current gain	I_C = 1 A V_{CE} = 20 V	15	–	–	
C_c	collector capacitance at f = 1 MHz	$I_E = I_e$ = 0 V_{CB} = 24 V	–	23	–	pF
C_{re}	feedback capacitance at f = 1 MHz	I_C = 0 V_{CE} = 24 V	–	14	–	pF
C_{cf}	collector-flange capacitance		–	2	–	pF

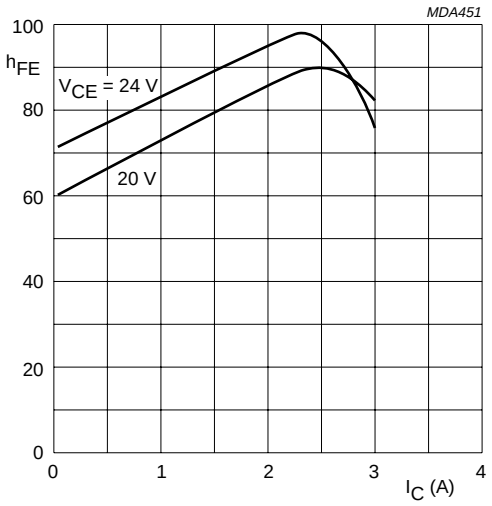


Fig.4 DC current gain as a function of collector current; typical values.

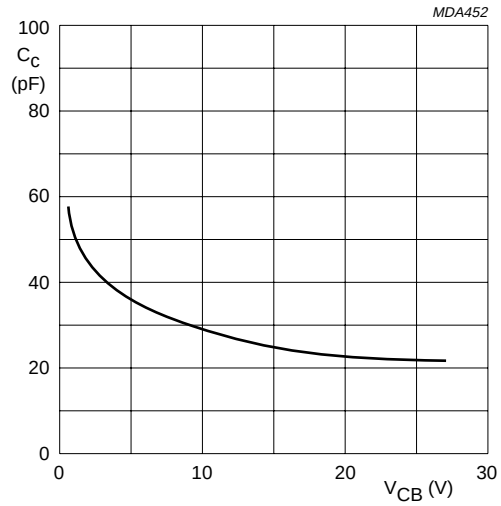


Fig.5 Output capacitance as a function of V_{CB}; typical values.

APPLICATION INFORMATION

RF performance in a common emitter test circuit.
T_h = 25 °C, $R_{th\ mb\text{-}h}$ = 0.4 K/W unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (mA)	P_L (W)	G_P (dB)	η_c (%)
c.w. class-AB	960	24	30	15	> 7.5 typ. 8.5	> 50 typ. 55

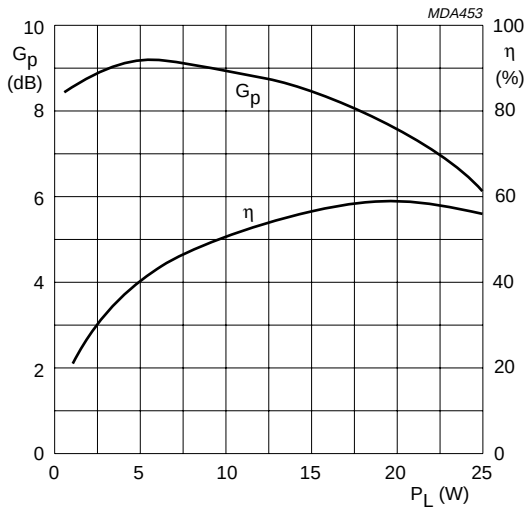


Fig.6 Power gain and efficiency as a function of load power; typical values.

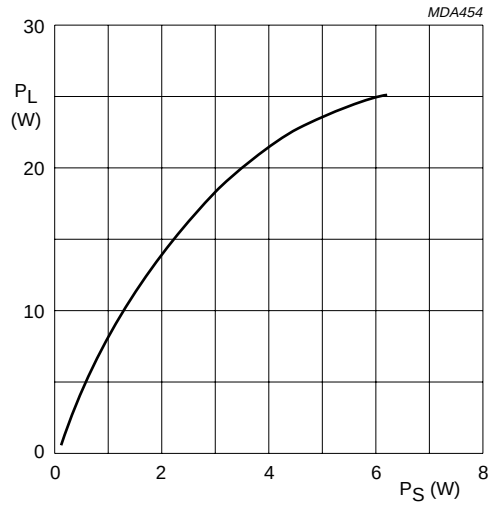


Fig.7 Load power as a function of input power; typical values.

Ruggedness in class-AB operation

The BLV98CE is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions: V_{CE} = 24 V, $I_{C(ZS)}$ = 30 mA, f = 960 MHz at rated output power.

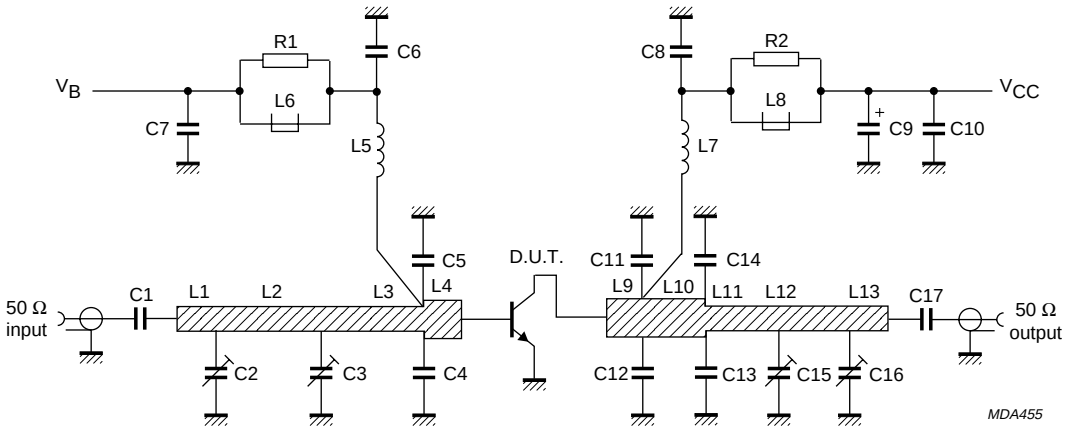


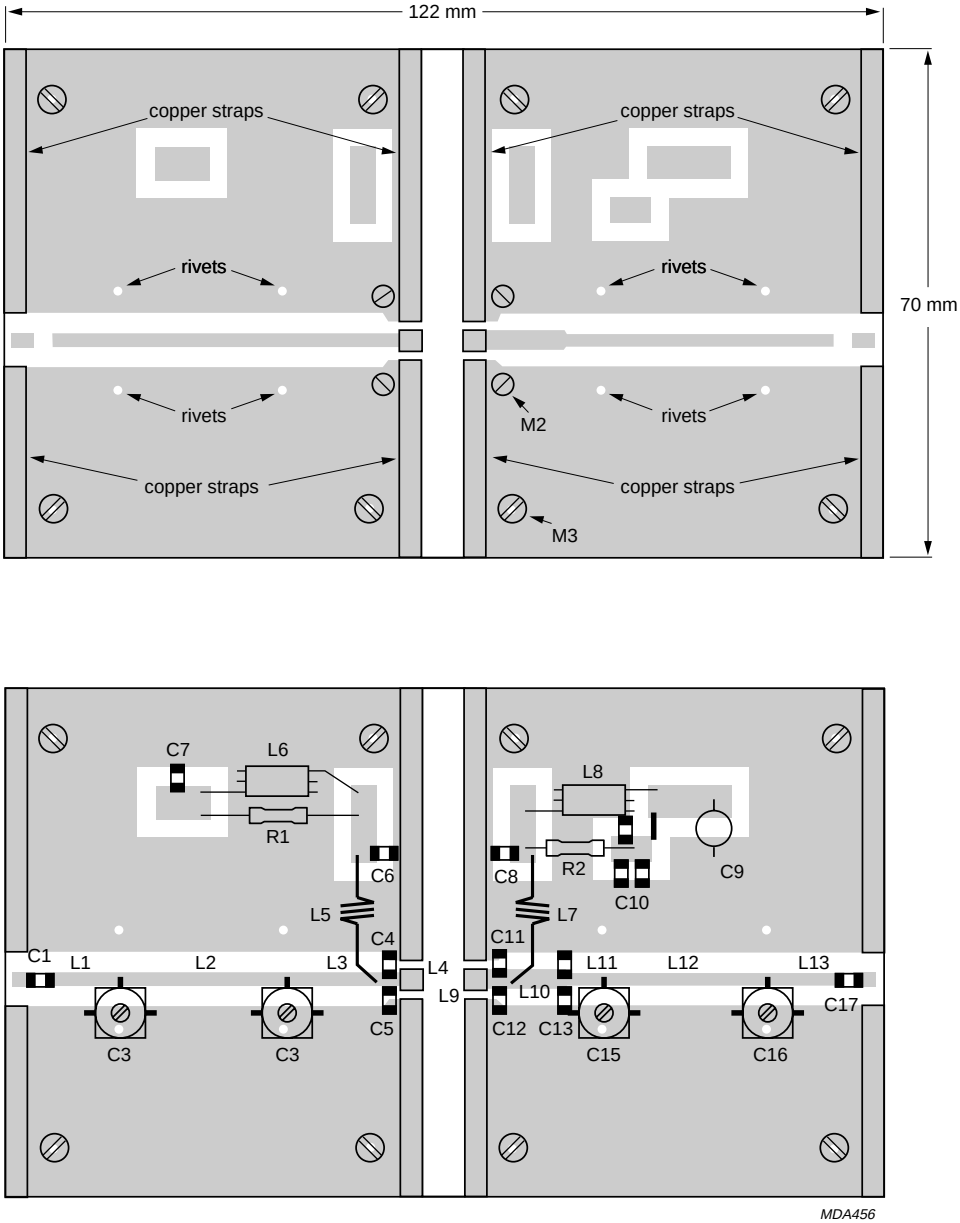
Fig.8 Test circuit BLV98CE class-AB.

List of components (Fig.8)

DESIGNATION	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C7, C8,C17	multilayer ceramic chip capacitor	330 pF		
C2, C3, C15, C16	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C4, C5	multilayer ceramic chip capacitor note 1	4.3 pF		
C9	35 V solid aluminium capacitor	2.2 μF		2222 128 50228
C10	multilayer ceramic chip capacitor	3 × 100 nF in parallel		
C11, C12	multilayer ceramic chip capacitor note 1	5.6 pF		
C13, C14	multilayer ceramic chip capacitor note 2	5.1 pF		
L1, L13	microstrip note 3	50 Ω	9.0 × 2.4 mm	
L2, L12	microstrip note 3	50 Ω	23.0 × 2.4 mm	
L3	microstrip note 3	50 Ω	16.0 × 2.4 mm	
L4	microstrip note 3	43 Ω	3.0 × 3.0 mm	
L5	3 turns enamelled 0.8 mm copper wire		int. dia. 3 mm length 5 mm leads 2 × 5 mm	
L6, L8	grade 3B ferroxcube wide-band RF choke			4312 020 36642
L7	4 turns enamelled 0.8 mm copper wire		int. dia. 4 mm length 5 mm leads 2 × 5 mm	
L9	microstrip note 3	43 Ω	3.5 × 3.0 mm	
L10	microstrip note 3	43 Ω	11.0 × 3.0 mm	
L11	microstrip note 3	50 Ω	4.5 × 2.4 mm	
R1, R2	0.4 W metal film resistor	10 Ω		2322 151 71009

Notes

1. ATC capacitor type 100A or capacitor of the same quality.
2. ATC capacitor type 100B or capacitor of the same quality.
3. The microstrips are on a double copper-clad PCB with PTFE fibre-glass dielectric (ε_r = 2.2); thickness $^1/_{32}$ inch.



The circuit and components are located on one side of the PTFE fibre-glass board, the other side being fully metallized, to serve as an earth. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the emitters, to provide a direct contact between the component side and the ground plane.

Fig.9 Printed circuit board and component layout for 960 MHz test circuit.

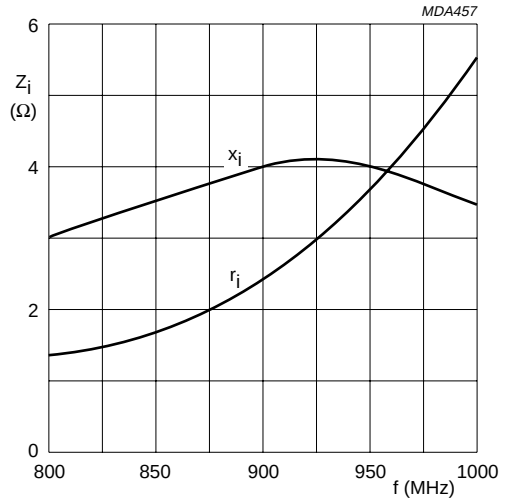


Fig.10 Input impedance; series components; V_{CE} = 24 V; P_L = 15 W; $R_{th\ mb\text{-}h}$ = 0.4 K/W; typical values.

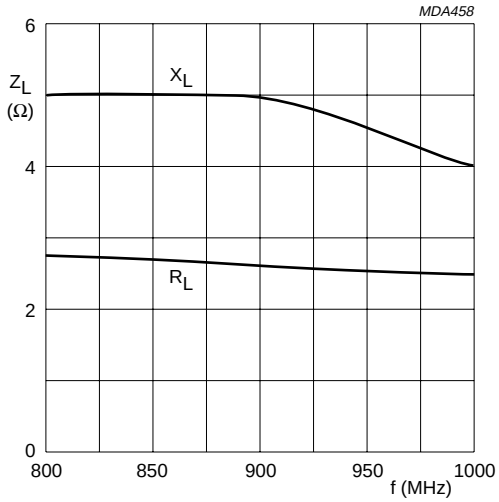


Fig.11 Load impedance; series components; V_{CE} = 24 V; P_L = 15 W; $R_{th\ mb\text{-}h}$ = 0.4 K/W; typical values.

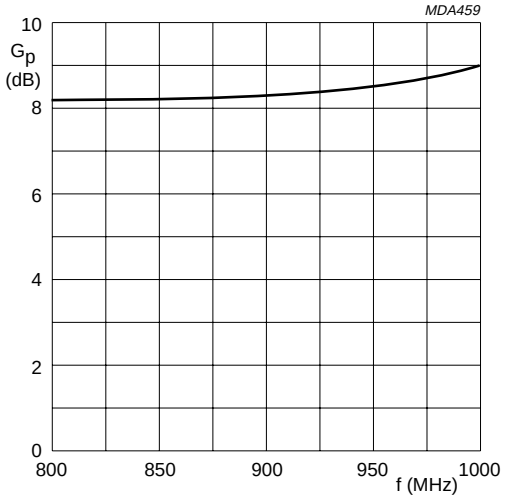
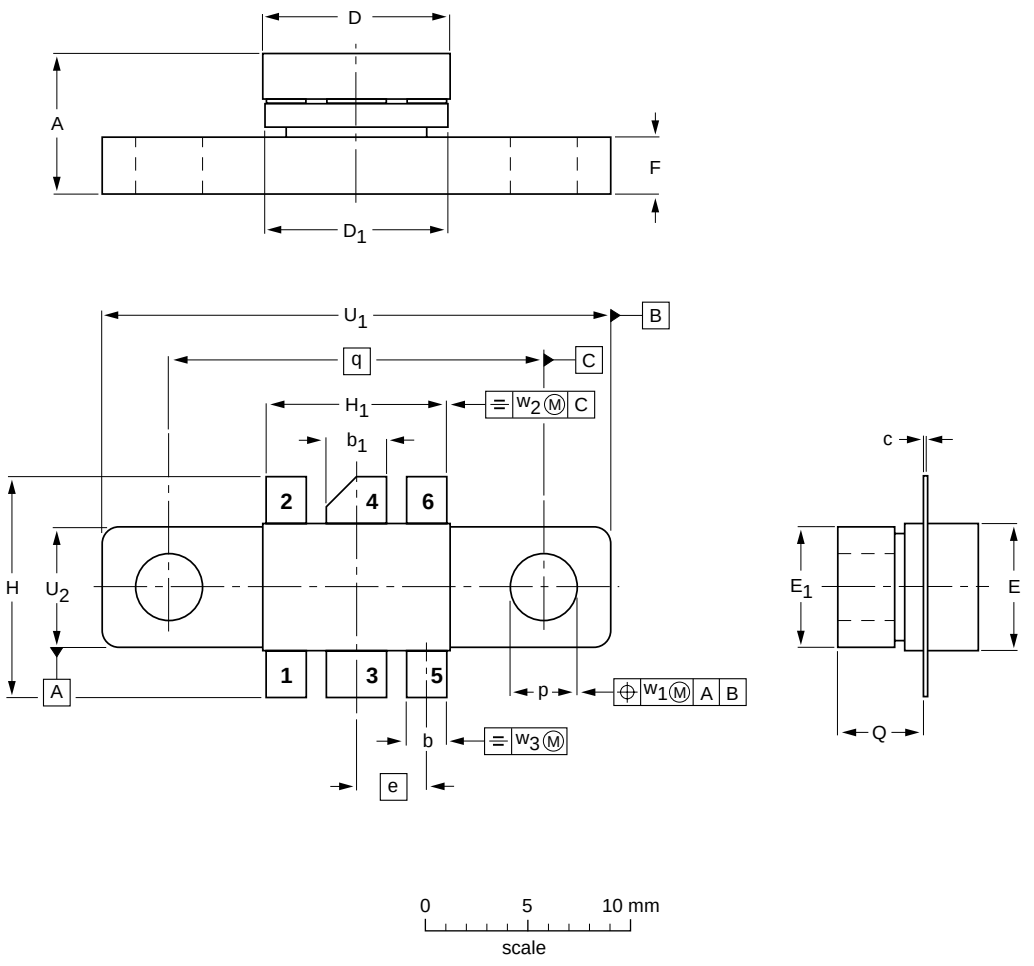


Fig.12 Power gain; class-AB operation; V_{CE} = 24 V; P_L = 15 W; $R_{th\ mb\text{-}h}$ = 0.4 K/W; typical values.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 6 leads **SOT171A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.81 6.07	2.15 1.85	3.20 2.89	0.16 0.07	9.25 9.04	9.30 8.99	5.95 5.74	6.00 5.70	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	6.00 5.70	0.51	1.02	0.26
inches	0.268 0.239	0.085 0.073	0.126 0.114	0.006 0.003	0.364 0.356	0.366 0.354	0.234 0.226	0.236 0.224	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.236 0.224	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						97-06-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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