

Version :0.1

TECHNICAL SPECIFICATION

MODEL NO. : PD035VX1

Customer's Confirmation

Customer _____

By _____

PVI's Confirmation

Confirmed By _____

Prepared By _____

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1. Application

This data sheet applies to a color TFT LCD module, PD035VX1. PD035VX1 module applies to projector which require high quality flat panel display.

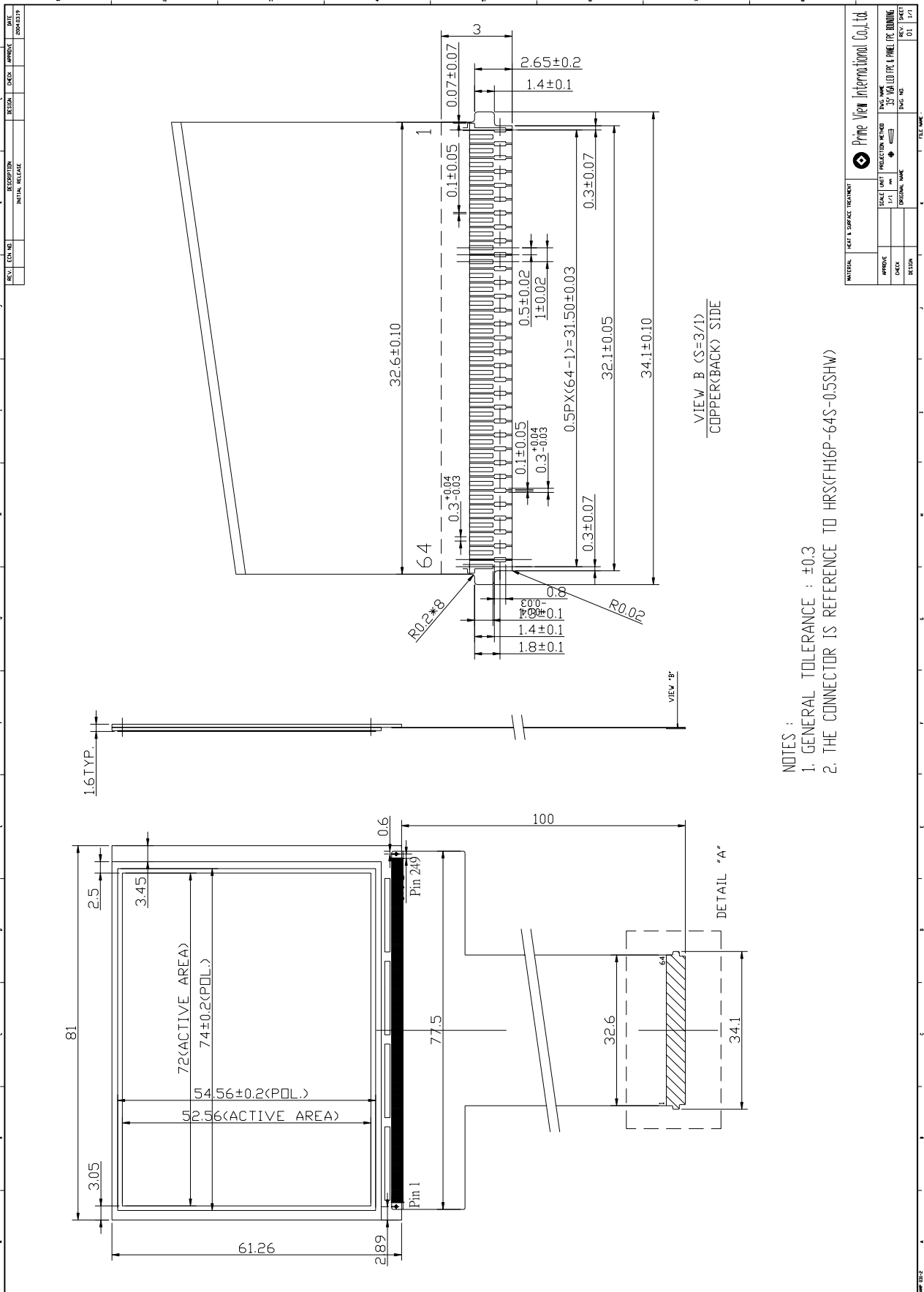
2. Features

- . Amorphous silicon TFT LCD panel
- . Pixel in stripe configuration
- . Display Colors : 262,144 colors
- . Optimum Viewing Direction : 6 o'clock
- . TTL transmission interface

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5(diagonal)	inch
Display Format	640×(R, G, B)×480	dot
Display Colors	262,144	
Active Area	72(H)×52.56(V)	mm
Pixel Pitch	0.1125(H)×0.1095(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	81(W)×61.26 (H)×1.8 (typ.) (D)	mm
Weight	TBD	g
Surface treatment	TBD	
Display mode	Normally white	

4. Mechanical Drawing of TFT-LCD Module



NOTES :
 1. GENERAL TOLERANCE : ±0.3
 2. THE CONNECTOR IS REFERENCE TO HRS(FH16P-64S-0.5SHW)

MATERIAL		SCALE		DATE	
SHEET & DRAWING TREATMENT		PROJECTION METHOD		DRAWING NO.	
APPROVE	SCALE	UNIT	PROJECTION METHOD	DWG. MARK	DWG. NO.
CHECK	1/1	mm	1st	25° VIA LED P.C. BOARD	REV. SHEET
DESIGN					01 / 01

5.Input / Output Terminals
TFT-LCD Panel Driving

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output 1	Note5-1
2	VSS1	I	Ground	
3	VDD1	I	Power Supply	
4	CLK	I	Horizontal Shift Clock	
5	VSS1	I	Ground	
6	R/L	I	Left/Right Selection	Note 5-1
7	R0	I	Red Data (LSB)	
8	R1	I	Red Data	
9	R2	I	Red Data	
10	R3	I	Red Data	
11	R4	I	Red Data	
12	R5	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0	I	Green Data (LSB)	
15	G1	I	Green Data	
16	G2	I	Green Data	
17	G3	I	Green Data	
18	G4	I	Green Data	
19	G5	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0	I	Blue Data (LSB)	
22	B1	I	Blue Data	
23	B2	I	Blue Data	
24	B3	I	Blue Data	
25	B4	I	Blue Data	
26	B5	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note5-2
28	REV	I	Data invert control	Note5-3
29	POL	I	Polarity selection	Note5-4
30	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note5-1
31	VSS2	I	Ground	
32	V1	I	Gamma Voltage 1	Note5-5
33	V2	I	Gamma Voltage 2	Note5-5
34	V3	I	Gamma Voltage 3	Note5-5
35	V4	I	Gamma Voltage 4	Note5-5
36	V5	I	Gamma Voltage 5	Note5-5
37	V6	I	Gamma Voltage 6	Note5-5
38	V7	I	Gamma Voltage 7	Note5-5
39	VSS2	I	Ground	
40	V8	I	Gamma Voltage 8	Note5-5
41	V9	I	Gamma Voltage 9	Note5-5
42	V10	I	Gamma Voltage 10	Note5-5
43	V11	I	Gamma Voltage 11	Note5-5
44	V12	I	Gamma Voltage 12	Note5-5
45	V13	I	Gamma Voltage 13	Note5-5
46	V14	I	Gamma Voltage 14	Note5-5
47	VSS2	I	Ground	
48	VDD2	I	Voltage for analog circuit	Note5-5
49	VCOM	I	Common Voltage	
50	XON	I	NC	
51	OE	I	Output Enable	Note5-6
52	U/D	I	Up/Down Selection	Note 5-7
53	CKV	I	Vertical Shift Clock	Note5-8
54	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note5-7
55	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note5-7
56	VGG	I	Gate On Voltage	Note5-9
57	VSS1	I	Ground	
58	VCC	I	Voltage for logic circuit	
59	VSS1	I	Ground	
60	VEE	I	Gate Off Voltage	Note5-10
61	NC	-	No connection	
62	NC	-	No connection	
63	NC	-	No connection	
64	NC	-	No connection	

Note 5-1: Select left or right shift

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to right
0	Hi-Z	Input	Right to left

Note 5-2: Latch the polarity of outputs and switch the new data to outputs

At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

Note 5-3: Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)

When “REV=1”, these data will be inverted.

EX: “00”→”3F”, “07”→”38”, “15”→”2A”

Note 5-4: Polarity selector for dot-inversion control. Available at the rising edge of LD.

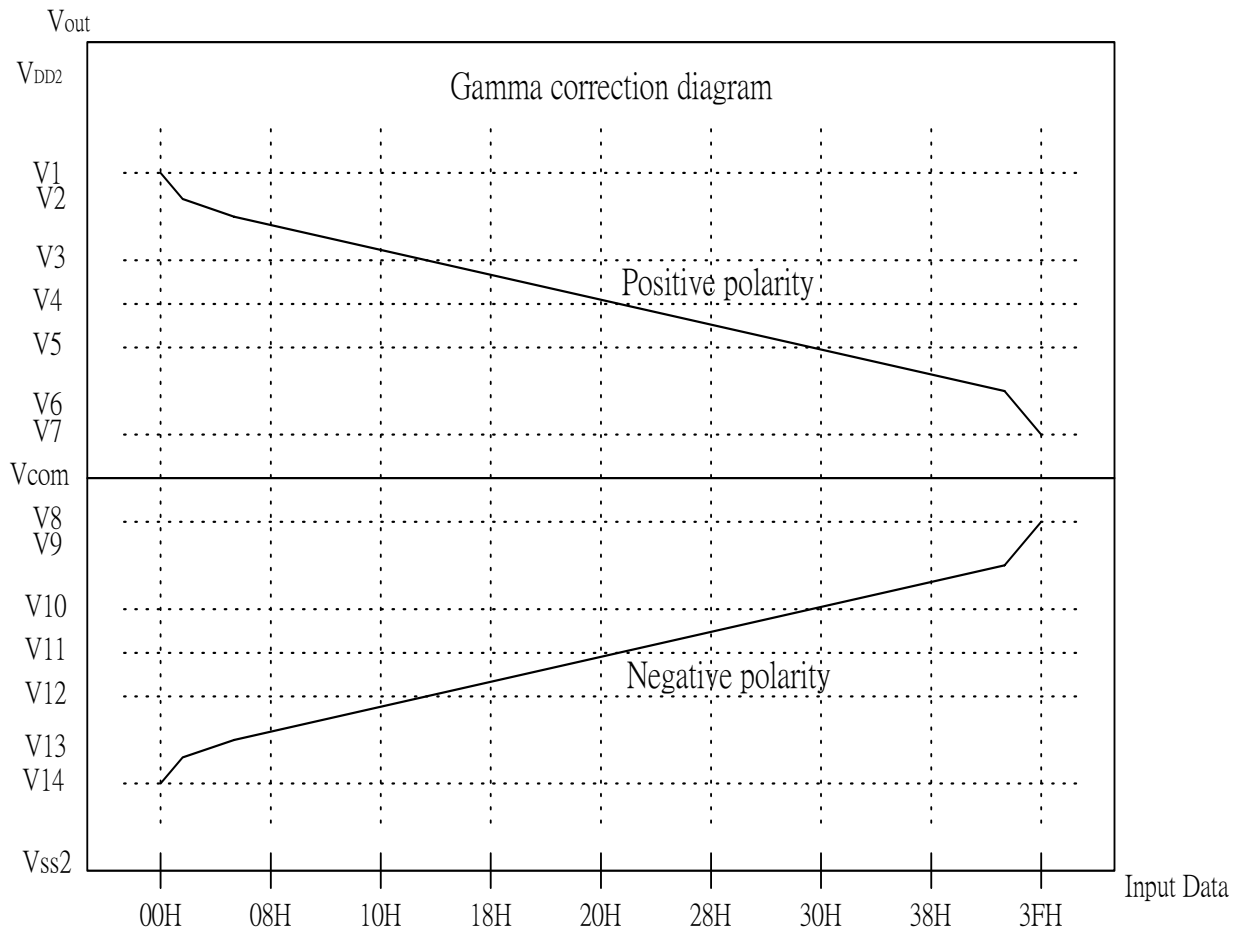
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;

When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-5:

1) Relationship between input data and output voltage

The figure below shows the relationship between the input data and the output voltage with the polarity. The range of V1~V7 is for positive polarity, and V8~V14 for negative polarity. Please refer to the following pages to get the related resistor values and voltage calculation method.



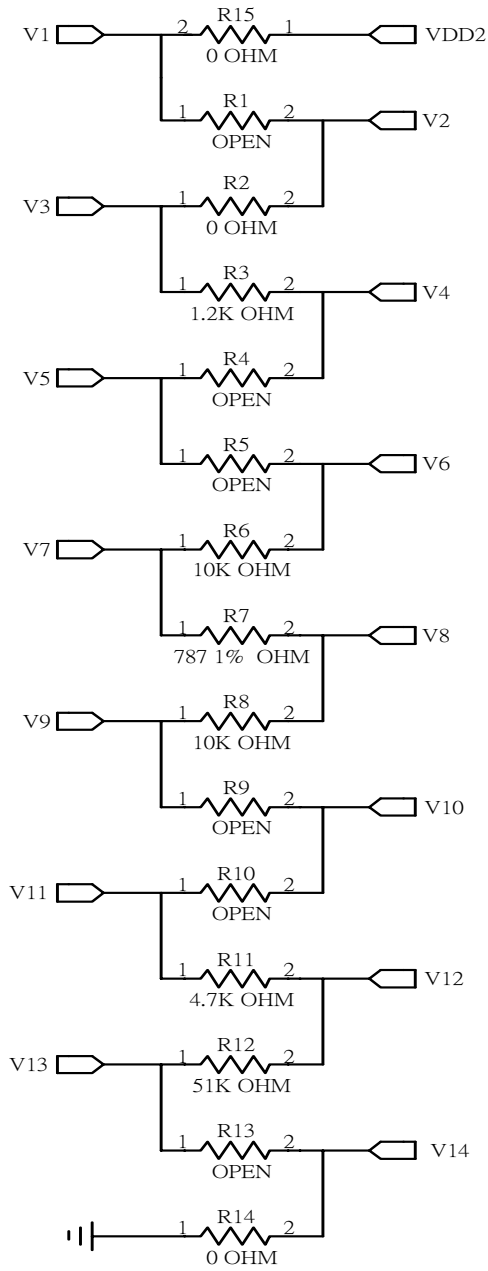
2) Output voltage and input data

Output Voltage to Panel VS Input Data

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	$V2=V3+(V1-V3) \times 58 / 64.4$	$V13=V14+(V12-V14) \times 6.4 / 64.4$
02H	$V3+(V1-V3) \times 52 / 64.4$	$V14+(V12-V14) \times 12.4 / 64.4$
03H	$V3+(V1-V3) \times 46.4 / 64.4$	$V14+(V12-V14) \times 18 / 64.4$
04H	$V3+(V1-V3) \times 41.2 / 64.4$	$V14+(V12-V14) \times 23.2 / 64.4$
05H	$V3+(V1-V3) \times 36.4 / 64.4$	$V14+(V12-V14) \times 28 / 64.4$
06H	$V3+(V1-V3) \times 32 / 64.4$	$V14+(V12-V14) \times 32.4 / 64.4$
07H	$V3+(V1-V3) \times 27.6 / 64.4$	$V14+(V12-V14) \times 36.8 / 64.4$
08H	$V3+(V1-V3) \times 23.6 / 64.4$	$V14+(V12-V14) \times 40.8 / 64.4$
09H	$V3+(V1-V3) \times 19.6 / 64.4$	$V14+(V12-V14) \times 44.8 / 64.4$
0AH	$V3+(V1-V3) \times 16.4 / 64.4$	$V14+(V12-V14) \times 48 / 64.4$
0BH	$V3+(V1-V3) \times 13.2 / 64.4$	$V14+(V12-V14) \times 51.2 / 64.4$
0CH	$V3+(V1-V3) \times 10.4 / 64.4$	$V14+(V12-V14) \times 54 / 64.4$
0DH	$V3+(V1-V3) \times 7.6 / 64.4$	$V14+(V12-V14) \times 56.8 / 64.4$
0EH	$V3+(V1-V3) \times 4.8 / 64.4$	$V14+(V12-V14) \times 59.6 / 64.4$
0FH	$V3+(V1-V3) \times 2.4 / 64.4$	$V14+(V12-V14) \times 62 / 64.4$
10H	V3	V12
11H	$V4+(V3-V4) \times 19.6 / 22$	$V12+(V11-V12) \times 2.4 / 22$
12H	$V4+(V3-V4) \times 17.6 / 22$	$V12+(V11-V12) \times 4.4 / 22$
13H	$V4+(V3-V4) \times 15.6 / 22$	$V12+(V11-V12) \times 6.4 / 22$
14H	$V4+(V3-V4) \times 13.6 / 22$	$V12+(V11-V12) \times 8.4 / 22$
15H	$V4+(V3-V4) \times 12 / 22$	$V12+(V11-V12) \times 10 / 22$
16H	$V4+(V3-V4) \times 10.4 / 22$	$V12+(V11-V12) \times 11.6 / 22$
17H	$V4+(V3-V4) \times 8.8 / 22$	$V12+(V11-V12) \times 13.2 / 22$
18H	$V4+(V3-V4) \times 7.6 / 22$	$V12+(V11-V12) \times 14.4 / 22$
19H	$V4+(V3-V4) \times 6.4 / 22$	$V12+(V11-V12) \times 15.6 / 22$
1AH	$V4+(V3-V4) \times 5.2 / 22$	$V12+(V11-V12) \times 16.8 / 22$
1BH	$V4+(V3-V4) \times 4 / 22$	$V12+(V11-V12) \times 18 / 22$
1CH	$V4+(V3-V4) \times 3.2 / 22$	$V12+(V11-V12) \times 18.8 / 22$
1DH	$V4+(V3-V4) \times 2.4 / 22$	$V12+(V11-V12) \times 19.6 / 22$
1EH	$V4+(V3-V4) \times 1.6 / 22$	$V12+(V11-V12) \times 20.4 / 22$
1FH	$V4+(V3-V4) \times 0.8 / 22$	$V12+(V11-V12) \times 21.2 / 22$

Output Voltage to Panel VS Input Data(continued)

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	$V5+(V4-V5) \times 12 / 12.8$	$V11+(V10-V11) \times 0.8 / 12.8$
22H	$V5+(V4-V5) \times 11.2 / 12.8$	$V11+(V10-V11) \times 1.6 / 12.8$
23H	$V5+(V4-V5) \times 10.4 / 12.8$	$V11+(V10-V11) \times 2.4 / 12.8$
24H	$V5+(V4-V5) \times 9.6 / 12.8$	$V11+(V10-V11) \times 3.2 / 12.8$
25H	$V5+(V4-V5) \times 8.8 / 12.8$	$V11+(V10-V11) \times 4 / 12.8$
26H	$V5+(V4-V5) \times 8 / 12.8$	$V11+(V10-V11) \times 4.8 / 12.8$
27H	$V5+(V4-V5) \times 7.2 / 12.8$	$V11+(V10-V11) \times 5.6 / 12.8$
28H	$V5+(V4-V5) \times 6.4 / 12.8$	$V11+(V10-V11) \times 6.4 / 12.8$
29H	$V5+(V4-V5) \times 5.6 / 12.8$	$V11+(V10-V11) \times 7.2 / 12.8$
2AH	$V5+(V4-V5) \times 4.8 / 12.8$	$V11+(V10-V11) \times 8 / 12.8$
2BH	$V5+(V4-V5) \times 4 / 12.8$	$V11+(V10-V11) \times 8.8 / 12.8$
2CH	$V5+(V4-V5) \times 3.2 / 12.8$	$V11+(V10-V11) \times 9.6 / 12.8$
2DH	$V5+(V4-V5) \times 2.4 / 12.8$	$V11+(V10-V11) \times 10.4 / 12.8$
2EH	$V5+(V4-V5) \times 1.6 / 12.8$	$V11+(V10-V11) \times 11.2 / 12.8$
2FH	$V5+(V4-V5) \times 0.8 / 12.8$	$V11+(V10-V11) \times 12 / 12.8$
30H	V5	V10
31H	$V7+(V5-V7) \times 26.8 / 27.6$	$V10+(V8-V10) \times 0.8 / 27.6$
32H	$V7+(V5-V7) \times 26 / 27.6$	$V10+(V8-V10) \times 1.6 / 27.6$
33H	$V7+(V5-V7) \times 25.2 / 27.6$	$V10+(V8-V10) \times 2.4 / 27.6$
34H	$V7+(V5-V7) \times 24.4 / 27.6$	$V10+(V8-V10) \times 3.2 / 27.6$
35H	$V7+(V5-V7) \times 23.6 / 27.6$	$V10+(V8-V10) \times 4 / 27.6$
36H	$V7+(V5-V7) \times 22.4 / 27.6$	$V10+(V8-V10) \times 5.2 / 27.6$
37H	$V7+(V5-V7) \times 21.2 / 27.6$	$V10+(V8-V10) \times 6.4 / 27.6$
38H	$V7+(V5-V7) \times 20 / 27.6$	$V10+(V8-V10) \times 7.6 / 27.6$
39H	$V7+(V5-V7) \times 18.4 / 27.6$	$V10+(V8-V10) \times 9.2 / 27.6$
3AH	$V7+(V5-V7) \times 16.8 / 27.6$	$V10+(V8-V10) \times 10.8 / 27.6$
3BH	$V7+(V5-V7) \times 14.8 / 27.6$	$V10+(V8-V10) \times 12.8 / 27.6$
3CH	$V7+(V5-V7) \times 12.8 / 27.6$	$V10+(V8-V10) \times 14.8 / 27.6$
3DH	$V7+(V5-V7) \times 10.4 / 27.6$	$V10+(V8-V10) \times 17.2 / 27.6$
3EH	$V7+(V5-V7) \times 6.4 / 27.6$	$V10+(V8-V10) \times 21.2 / 27.6$
3FH	V7	V8

3) Typical Application Circuit (When $V_{DD2} = +9.5V$)


Note 5-6: When OE is connected to high “1”, the driver outputs are disabled (Gate output = V_{EE}).
Under this condition, the operation of registers will not be affected.

Note 5-7: Select up or down shift

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

Note 5-8: Gate driver shift clock

Note 5-9: Gate on voltage, $V_{GG}=27V$.

Note 5-10: Gate off voltage, $V_{EE}=-10V$.

6. Absolute Maximum Ratings:
 $V_{SS1}=V_{SS2}=GND=0V, T_a=25^{\circ}C$

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{DD1}	-0.3	2	V	
	V_{CC}	-0.3	5	V	
	V_{DD2}	-0.5	12.0	V	
	V_{GG}	-0.3	40.0	V	
	$V_{GG}-V_{EE}$	-	40.0	V	
	V_{EE}	-20	0.3	V	
Storage Temperature	T_{ST}	-10	80	$^{\circ}C$	
Operating Temperature	T_{OP}	0	80	$^{\circ}C$	

7. Electrical Characteristics
7-1) Recommended Operating Conditions:
 $V_{SS1}=V_{SS2}=GND = 0V, T_a = 25^{\circ}C$

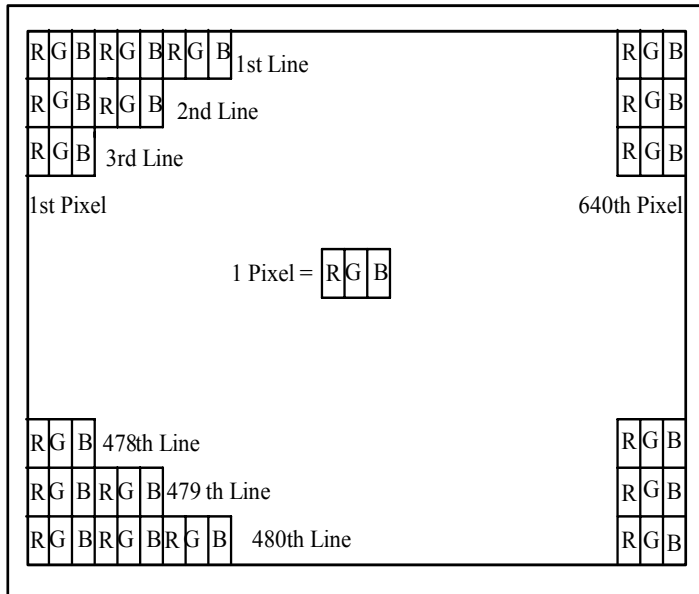
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	V_{DD1}	3.0	3.3	3.6	V	
	V_{DD2}	9	9.5	10		
Supply Voltage for Gate Driver	V_{GG}	-	27	-	V	
	V_{EE}	-	-10	-	V	
	V_{CC}	3.0	3.3	3.6	V	
Digital Input Voltage	V_{IH}	$0.8V_{DD1}$	-	V_{DD1}	V	
	V_{IL}	0	-	$0.2V_{DD1}$	V	

7-3) Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	I_{GG}	$V_{GG}=+27V$	TBD	TBD	mA	
Supply Current for Gate Driver (Low level)	I_{EE}	$V_{EE}=-10V$	TBD	TBD	mA	
Supply Current for Source Driver (Digital)	I_{DD1}	$V_{DD1}=+3.3V$	TBD	TBD	mA	
Supply Current for Source Driver (Analog)	I_{DD2}	$V_{DD2}=+9.5V$	TBD	TBD	mA	
Supply Current for Gate Driver (Digital)	I_{CC}	$V_{CC}=+3.3V$	TBD	TBD	mA	
LCD Panel Power Consumption			TBD	TBD	W	

8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

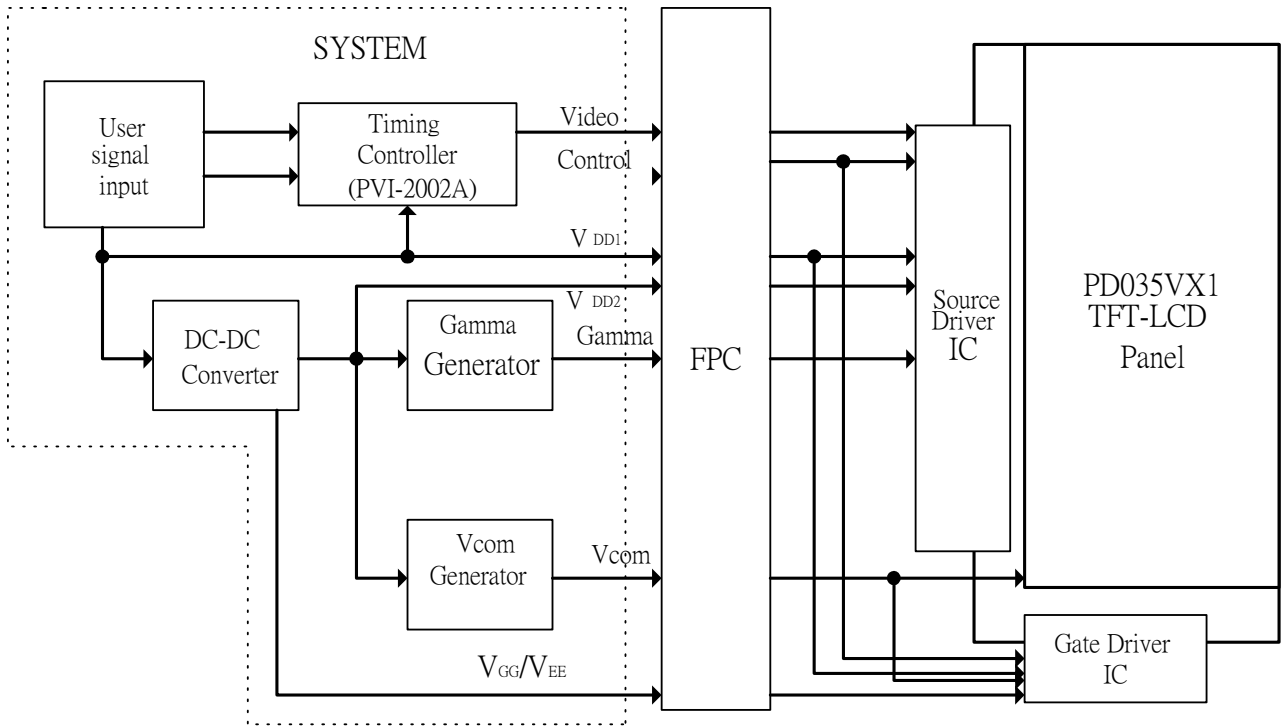


9. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

10. Block Diagram

10-1) TFT-module Block Diagram



If you use PD035VX1, you must apply PVI-2002A(Timing controller) which Will generate signal to support PD035VX1.

11. Interface Timing

11.1) Timing Parameters

AC Electrical Characteristics ($V_{CC}=V_{DD1}=3.3V$, $V_{DD2}=9.5V$, $GND=V_{SS1}=V_{SS2}=0V$, $T_a=25^{\circ}C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	Fclk	-	25	40	MHz
CLK Pulse Width	T _{CPH}	25	-	-	ns
Data Set-up Time	T _{su}	4	-	-	ns
Data Hold Time	T _{hd}	2	-	-	ns
Propagation Delay of DIO2/1	T _{phl}	6	10	15	ns
Time That The Last Data to LD	T _{ld}	1	-	-	T _{CPH}
Pulse width of LD	T _{wld}	2	-	-	T _{CPH}
Time That LD to DIO1/2	T _{lds}	5	-	-	T _{CPH}
POL Set-up Time	T _{psu}	6	-	-	ns
POL Hold Time	T _{phd}	6	-	-	ns
OE Pulse Width	T _{OEV}	1	-	-	μs
CKV Pulse Width	T _{CKV}	500	-	-	ns
STV Set-up Time	T _{SUV}	400	-	-	ns
STV Hold Time	T _{HDV}	400	-	-	ns
Horizontal Display Period	T _{HDP}	-	640	-	T _{CPH}
Horizontal Period Timing Range	T _{HP}	-	800	-	T _{CPH}
Horizontal Lines Per Field	T _V	520	525	640	T _{HP}
Vertical Display Timing Range	T _{DV}	-	480	-	T _{HP}

11.2) Timing Diagram

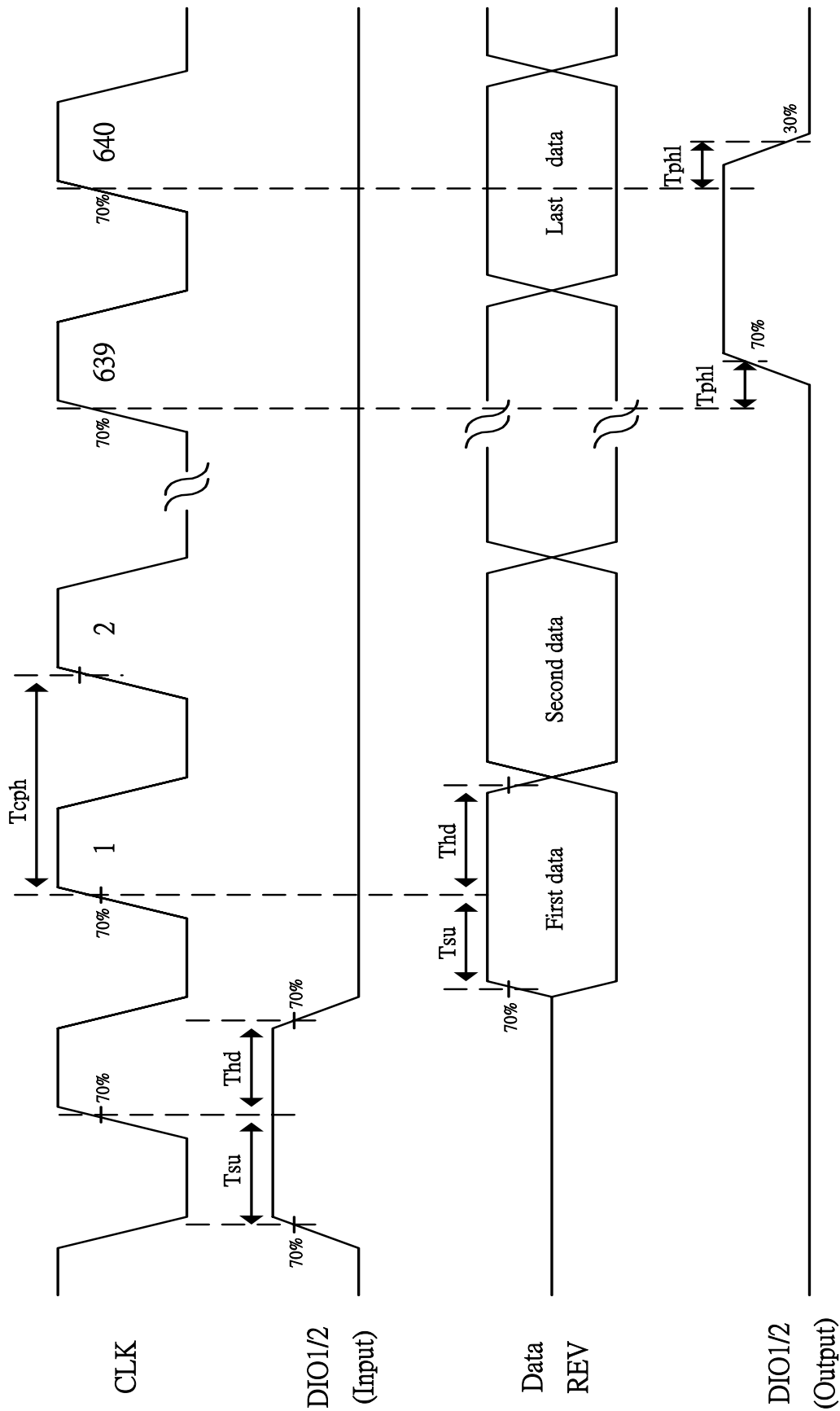


Fig. 11-1 Horizontal timing(1)

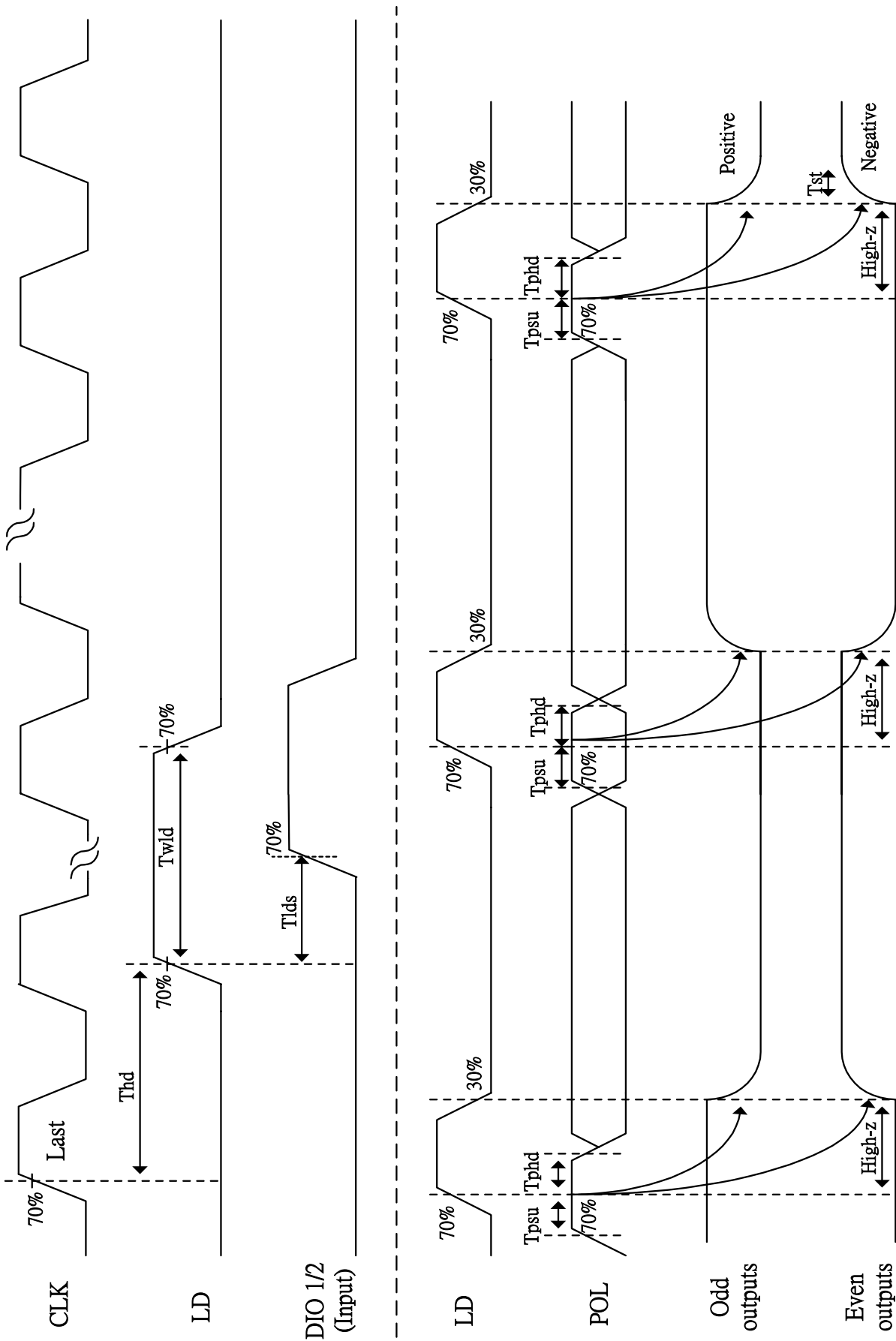


Fig. 11-2 Horizontal timing(2)

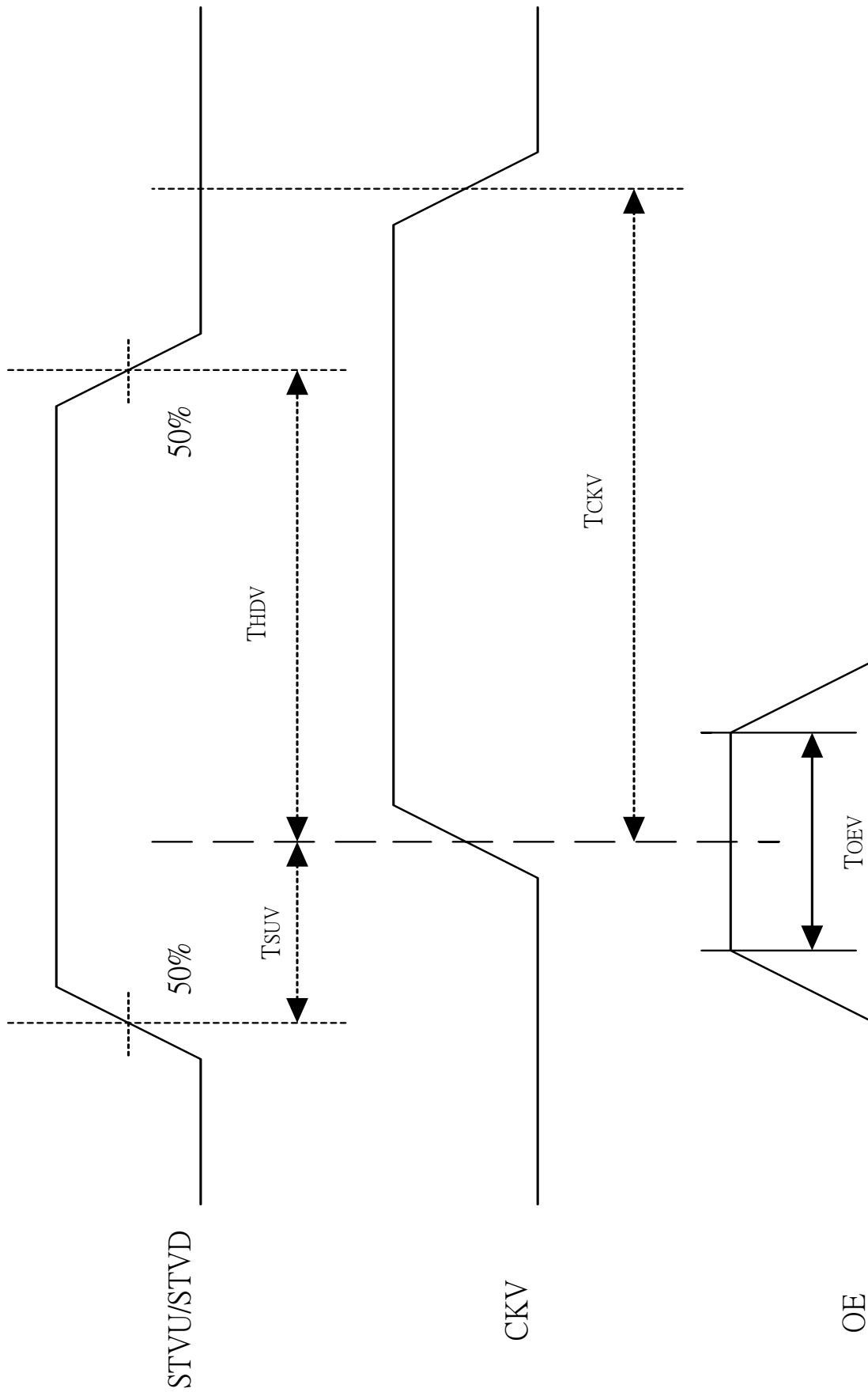


Fig. 11-3 Vertical shift clock timing

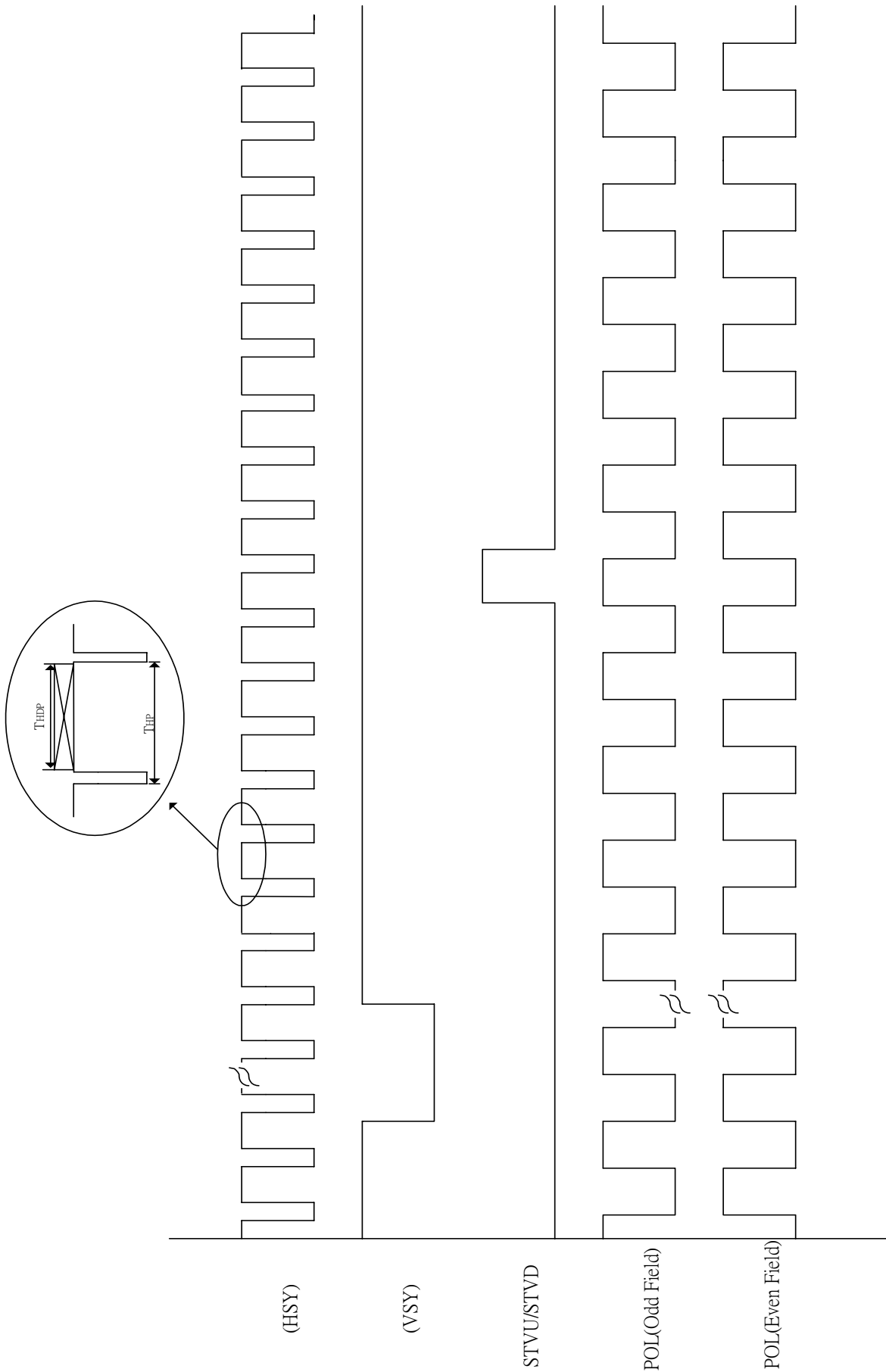
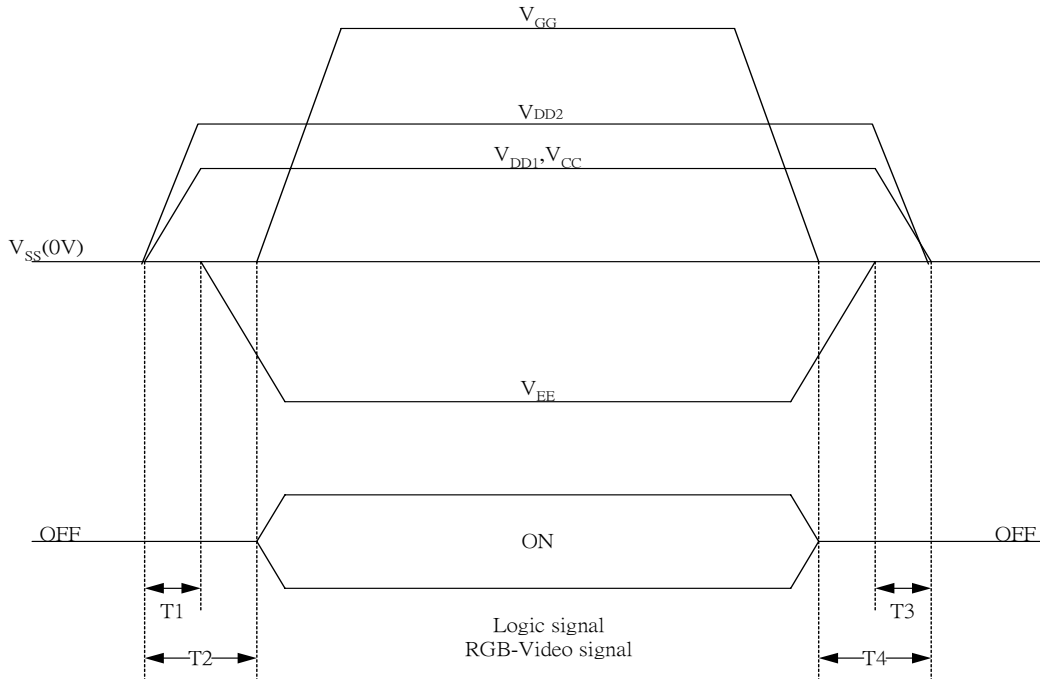


Fig. 11-4 Vertical timing

12. Power On Sequence



1. $1.10\text{ms} \leq T1 < T2$

2. $0\text{ms} < T3 \leq T4 \leq 10\text{ms}$

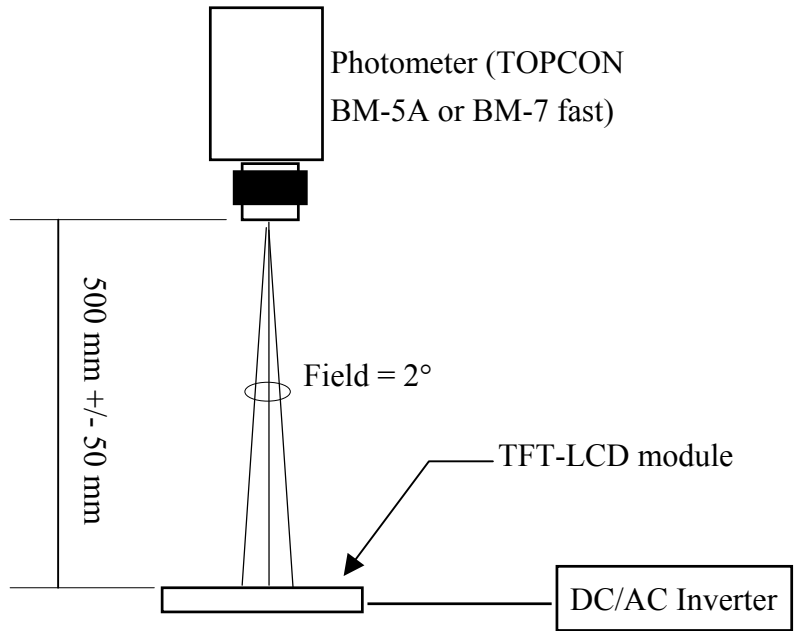
13. Optical Characteristics

13-1) Specification:

Ta=25°C

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR > 100	±TBD	±TBD		deg	Note 13-2
	Vertical	θ 12(to 12 o'clock)		TBD	TBD	-	deg	
		θ 11(to 6 o'clock)		TBD	TBD	-	deg	
Contrast Ratio		CR		TBD	TBD	-	-	Note 13-4
Response time	Rise	Tr	$\theta = 0^\circ$	-	15	30	ms	Note 13-3
	Fall	Tf		-	25	50	ms	
White Chromaticity		x		0.28	0.310	0.34	-	Note 13-1
		y		0.30	0.330	0.36	-	
Transmission Ratio		T		TBD	TBD		%	

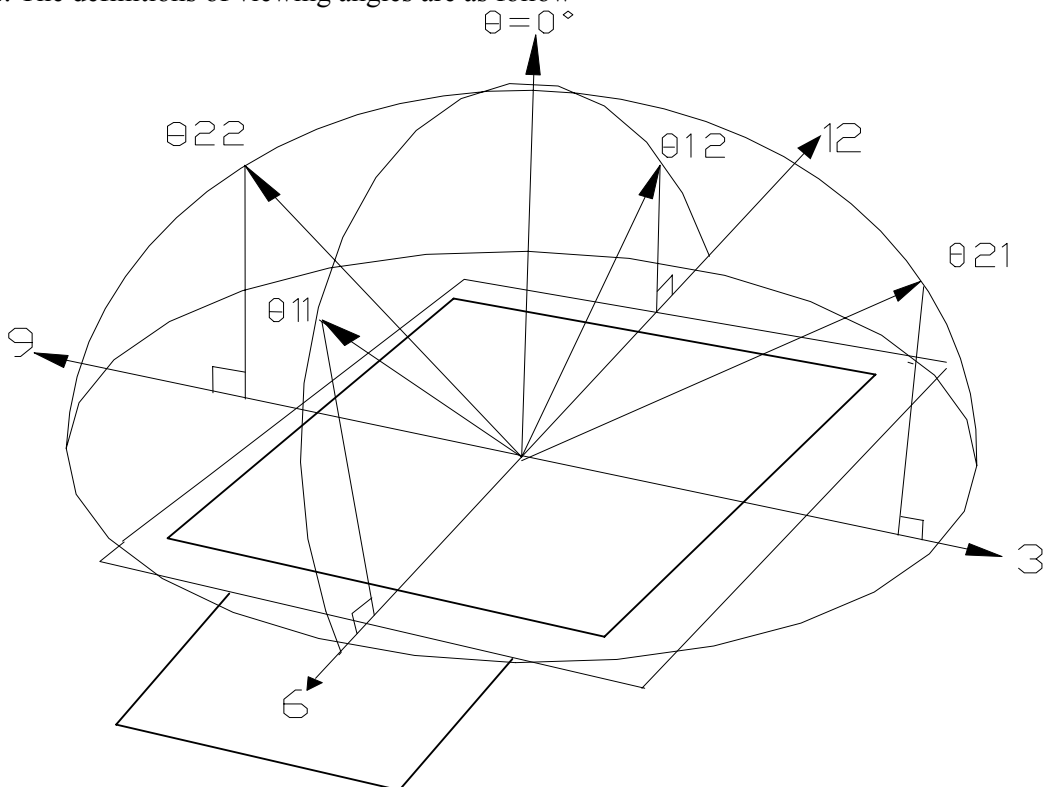
All the optical measurement shall be executed 1 minute after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



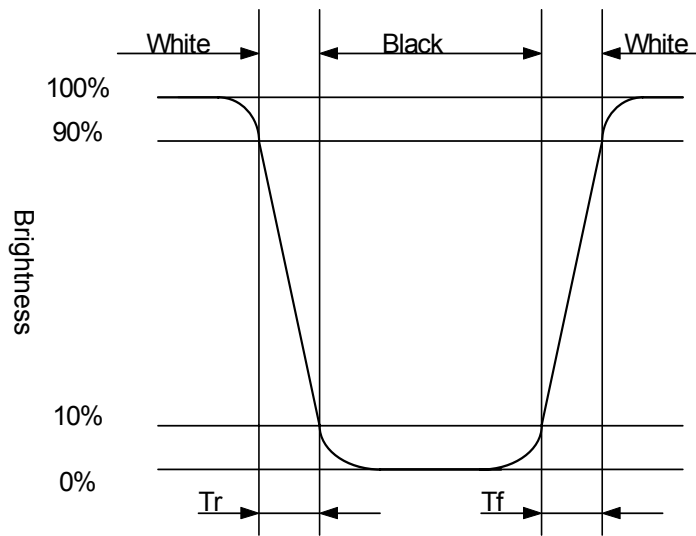
Optical characteristics measuring configuration

- Note 13-1: 1.Topcon BM-5A or BM-7 fast luminance meter 1° field of view is used in the testing (after 1 minute operation).
 2.LED current : 20 mA
 3.Backlight Module : TBD.

Note 13-2: The definitions of viewing angles are as follow



Note 13-3: Definition of Response Time T_r and T_f :



Note 13-4: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

14. Handling Cautions

14-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

14-2) Precautions in mounting

- a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.

15. Reliability Test

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +80°C, 240 hrs	
2	Low Temperature Storage Test	Ta = -10°C, 240 hrs	
3	High Temperature Operation Test	Ta = +80°C, 240 hrs	
4	Low Temperature Operation Test	Ta = 0°C, 240 hrs	
5	High Temperature & High Humidity Operation Test	Ta = +70°C, 80%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-10°C → +80°C, 200 Cycles 30min 30min	
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal	

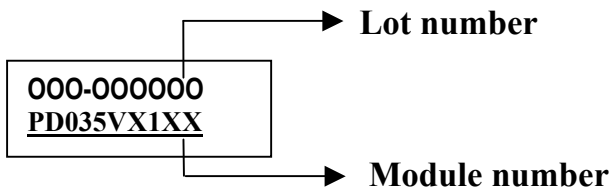
Ta: ambient temperature

[Judgement Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

16. Indication of Lot Number Label

Indicated contents of the label



Contents of lot number : 1st~3rd—The OEM product

5th—Production year : 1999⇒9, 2000⇒A, 2001⇒B.....

6th—Production month : 1, 2, 3,...9, A, B, C

7th~8th—Production size : 3.5" ⇒35

9th~10th— Serial numbers : 01~99

17. Packing Diagram

TBD

Revision History

Rev.	Issued Date	Revised	Contents
0.1	Aug. 03 , 2004	New	