

# MX82C171

## FEATURES

- Pixel rates up to 35 MHz
- 256 colors
- Single monolithic, high performance CMOS design
- Up to 8 bits per pixel
- Pixel word mask
- RGB analog output, 6 bit DAC per gun, composite blank
- Low DAC glitch energy
- Video signal output into 75 ohms or doubly terminated 75 ohm cable
- TTL compatible inputs
- Microprocessor compatible interface
- Single +5V ±10% power supply
- Low power dissipation, 750 mW max. at maximum pixel rate
- Standard 600 mil 28 pin DIP package
- The contents of the look-up table and all microprocessor interface registers can be read.

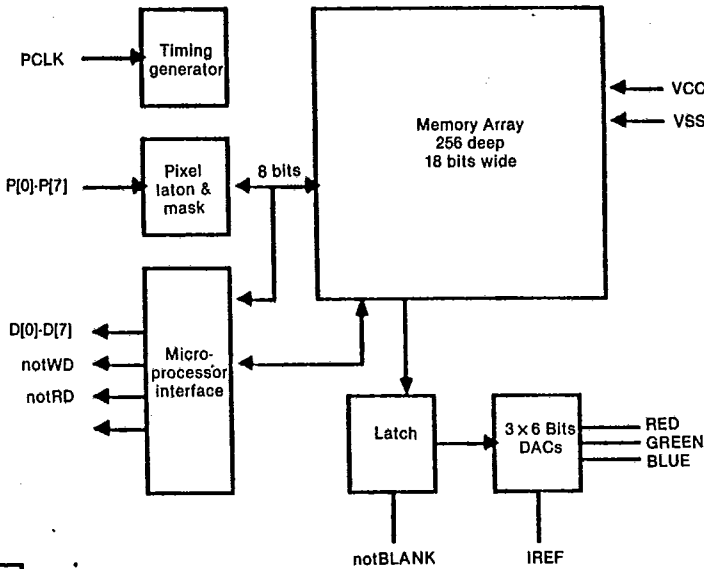
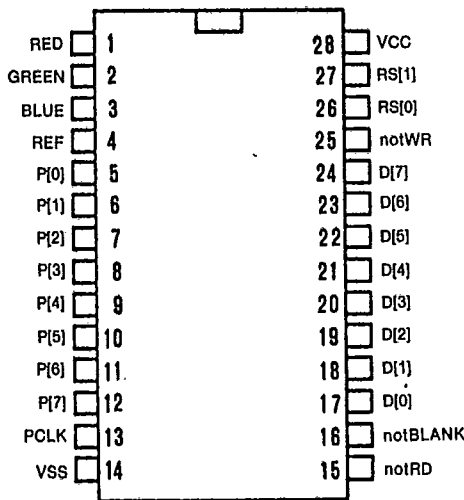
## DESCRIPTION

THE MX82C171 video DAC is an integration of three 6 bit digital to analog converters and a color look up table. The DAC section can handle loads of 37.5 or 75 ohms. The microprocessor interface is bidirectional for this 28 pin integrated circuit.

The MX82C171 can display 256 colors from a palette of 256K. The part replaces TTL & ECL components, thereby reducing costs and board space. Full CMOS design also reduces power consumption.

The pixel work mask changes colors displayed in single write cycles rather than by changing the entire palette.

## PIN CONFIGURATION



### PIN NAMES

|                  |                       |
|------------------|-----------------------|
| P[0]-P[7]        | Pixel address inputs  |
| D[0]-D[7]        | Program data bus      |
| RS[0]-RS[1]      | Register select       |
| RED, GREEN, BLUE | Analog video outputs  |
| PCLK             | Pixel clock           |
| notWR            | Write enable          |
| notRD            | Read enable           |
| notBLANK         | Video blanking input  |
| IREF             | Reference current     |
| VCC              | + 5 volt supply input |
| VSS              | Ground                |



**APPLICATION INFORMATION**

**Analog output - Power supply distribution**

To ensure the proper operation of the MX 82C171 it is necessary to adopt a high frequency board layout and power supply distribution technique.

The impedance in the decoupling path between the power supply pins (Vcc pin 28 and Vss pin 14) should be kept to a minimum. It is recommended that the decoupling capacitance between Vcc and Vss should be a 0.1μF high frequency capacitor in parallel with a larger tantalum capacitor with a value between 22μF and 47μF. An inductance may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the MX 82C171.

**Analog output - Line driving**

The DACs in the MX82C171 are made from switched current sources. Each current source is based on a current mirror such that the current source will provide one thirtieth of the reference current IREF when it is active.

Each of the three DACs contains 63 current sources. The binary data input to the DAC controls 63 sources.

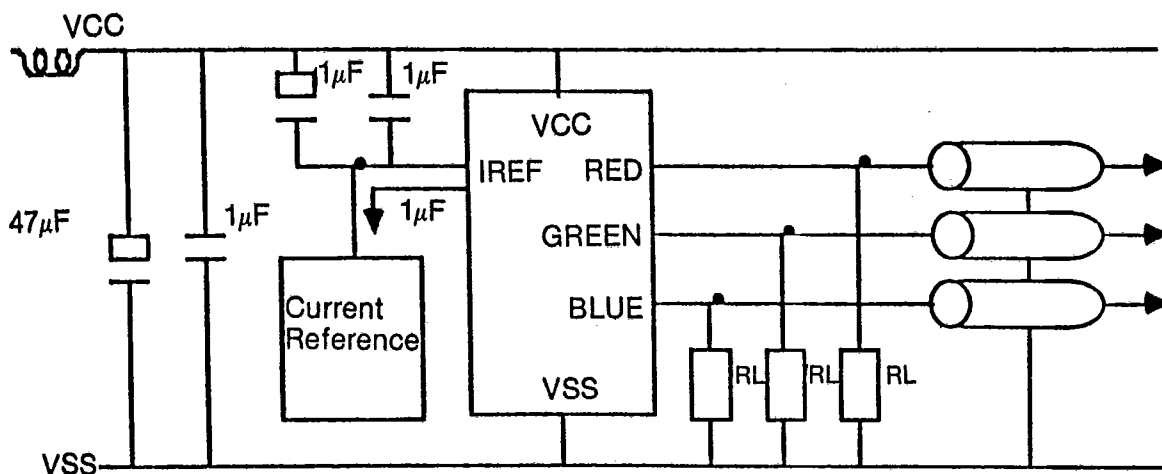
The output current from the DACs and the output voltage is determined by the reference current IREF. This reference current develops a voltage reference within the MX82C171 relative to Vcc. IREF should be decoupled to the Vcc input to prevent a noise differential between the IREF input and Vcc and hence prevent noise on the analog outputs of the MX82C171.

**Signal termination**

The trace lines between the outputs of the TTL devices driving the MX 82C171 and the inputs of the MX 82C171 behave like low impedance transmission lines driven from a low impedance source and terminated by a high impedance load. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going signals, line termination is recommended. The termination may be either series or parallel.

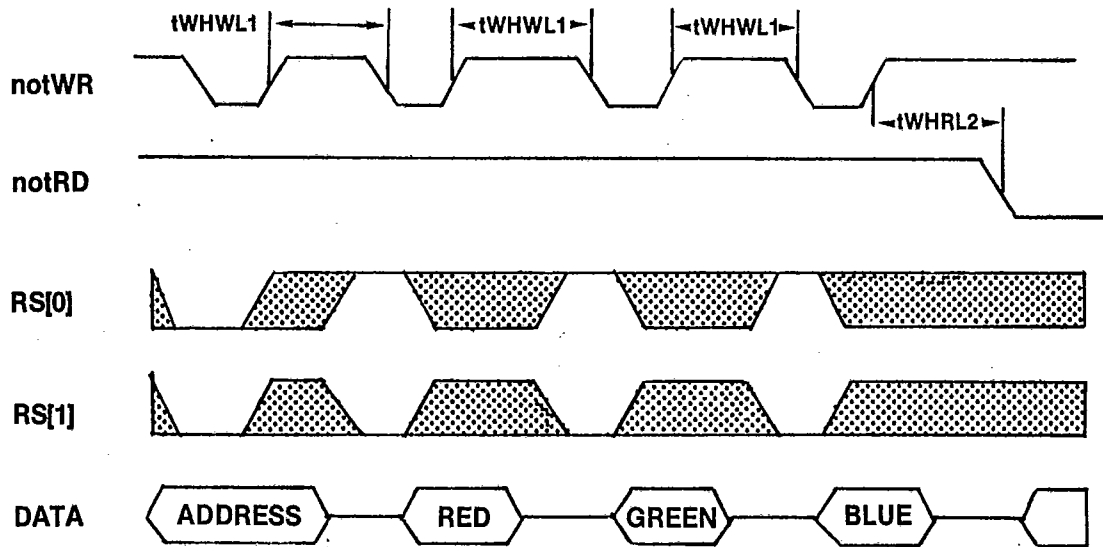
The recommended technique is to use series termination. The series termination technique has the advantages of drawing no DC current and using fewer components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the MX82C171.

Some experimentation will have to be done to find proper value to use for the series termination to minimize reflections, but generally a value around 100 ohms will be required. Because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of the resistance should therefore be selected empirically.

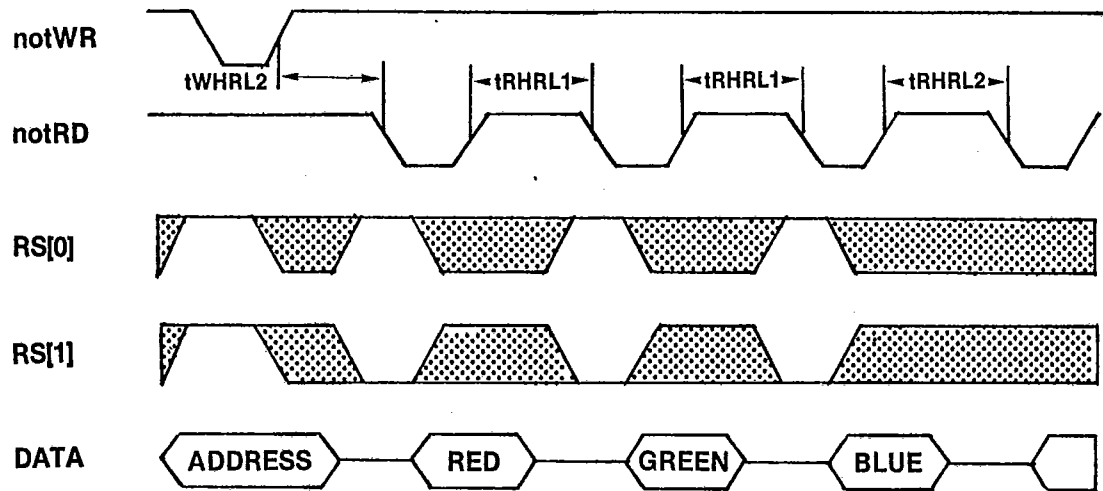




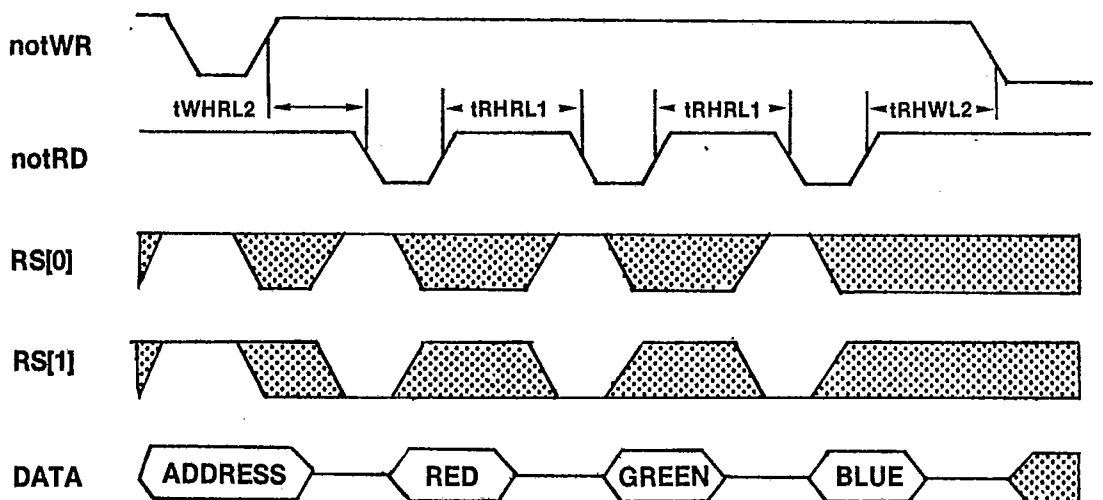
Microprocessor Interface: Color value write followed by any read.



Microprocessor Interface: Color value read followed by any read.

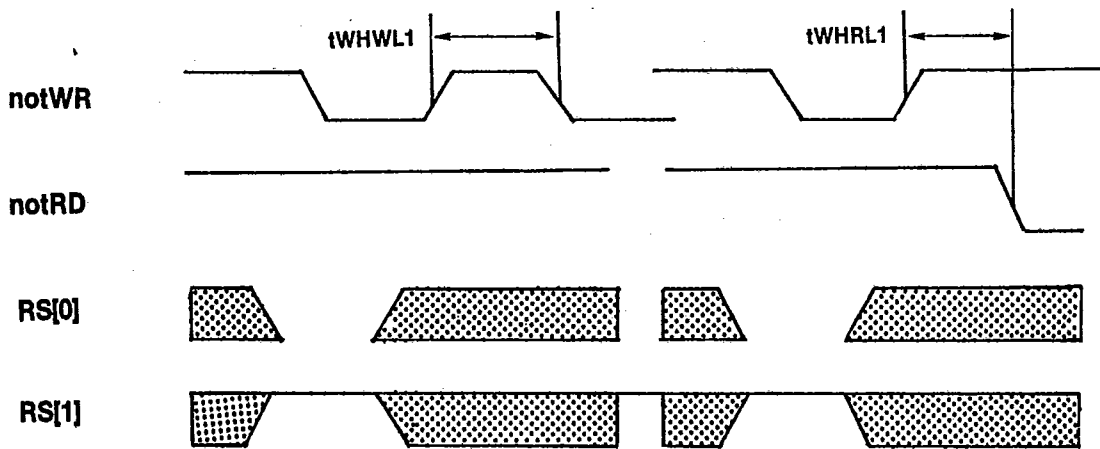


Microprocessor Interface: Color value read followed by any write.

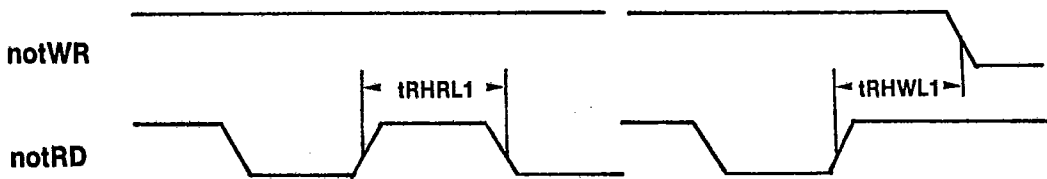




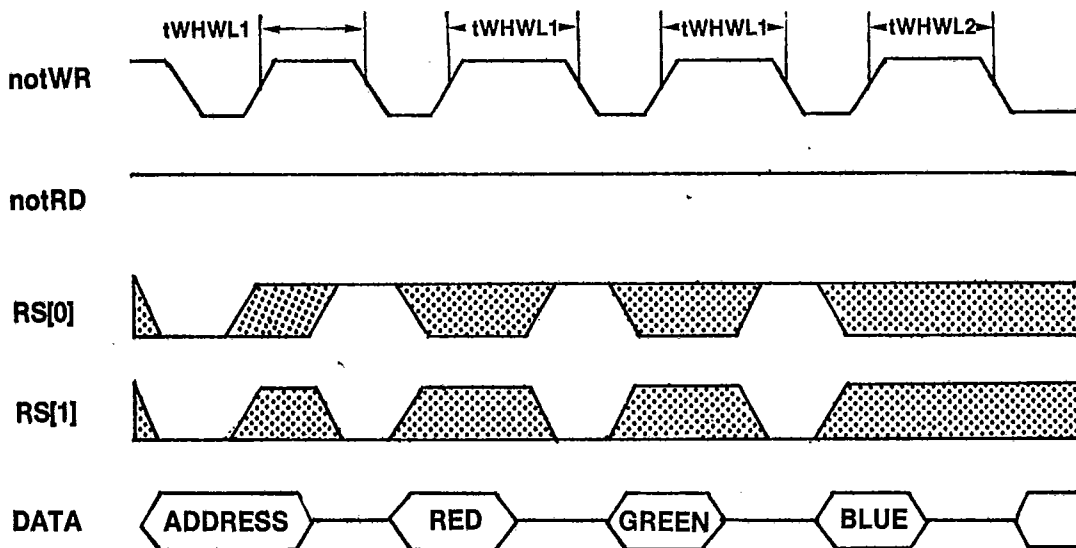
Microprocessor Interface: Write to Pixel Mask register followed by any access



Microprocessor Interface: Read from (a) Pixel Mask register  
 (b) Pixel Address register (Read Mode)  
 (c) Pixel Address register (Write Mode) followed by any access.

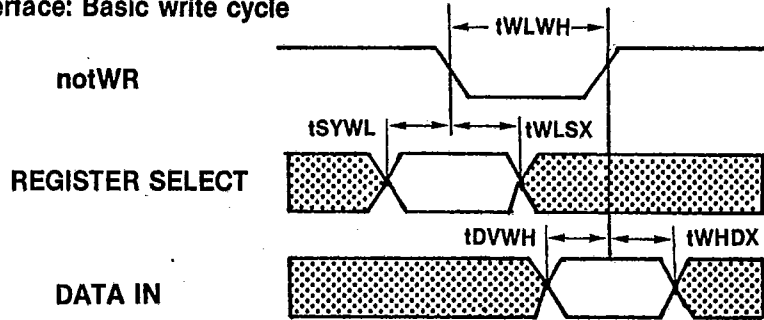


Microprocessor Interface: Color value write followed by any write.

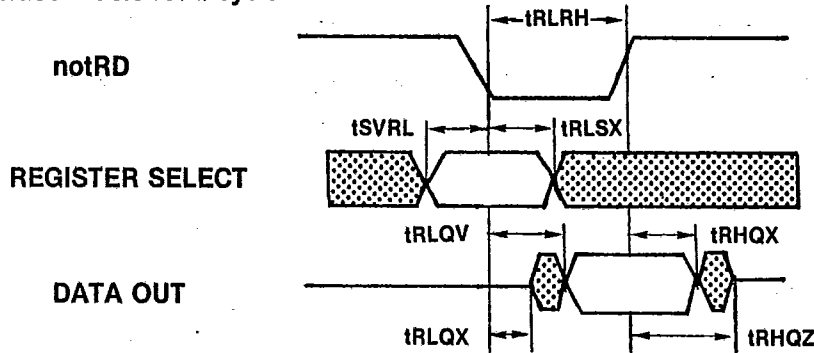




Microprocessor Interface: Basic write cycle



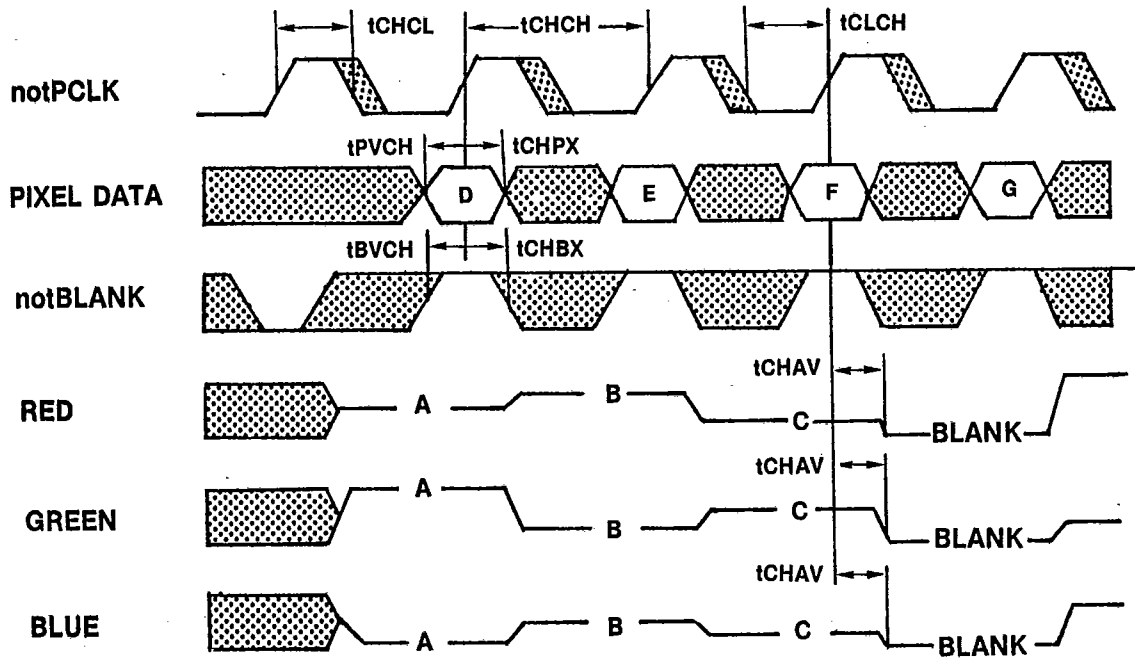
Microprocessor Interface: Basic read cycle



|        |                              | MX 82C171-35 |     |       |        |
|--------|------------------------------|--------------|-----|-------|--------|
| Symbol | Parameter                    | Min          | Max | Units | Notes  |
| tWLWH  | notWR pulse width low        | 50           |     | ns    |        |
| tRLRH  | notRD pulse width low        | 50           |     | ns    |        |
| tSVWL  | Register select setup time   | 15           |     | ns    |        |
| tSVRL  | Register select setup time   | 15           |     | ns    |        |
| tWLSX  | Register select hold time    | 15           |     | ns    |        |
| tRLSX  | Register select hold time    | 15           |     | ns    |        |
| tDVWH  | Write data setup time        | 15           |     | ns    |        |
| tWHDX  | Write data hold time         | 15           |     | ns    |        |
| tRLQX  | Output turn-on delay         | 5            |     | ns    |        |
| tRLQV  | Read enable access time      |              | 40  | ns    |        |
| tRHQX  | Output hold time             | 5            |     | ns    |        |
| tRHQZ  | Output turn-off delay        |              | 20  | ns    |        |
| tWHWL1 | Successive write interval    | 3*tCHCH      |     |       |        |
| tWHRL1 | Write followed by read       | 3*tCHCH      |     |       |        |
| tRHRL1 | Successive read interval     | 3*tCHCH      |     |       |        |
| tRHWL1 | Read followed by write       | 3*tCHCH      |     |       |        |
| tWHWL2 | Write after color write      | 3*tCHCH      |     |       | Note 1 |
| tWHRL2 | Read after color write       | 3*tCHCH      |     |       | Note 1 |
| tRHRL2 | Read after color read        | 6*tCHCH      |     |       | Note 1 |
| tRHWL2 | Write after color read       | 6*tCHCH      |     |       | Note 1 |
|        | Write enable transition time |              | 50  | ns    |        |
|        | Read enable transition time  |              | 50  | ns    |        |

Notes:

1. This parameter allows for synchronization with the pixel stream when a new color value is being written to the look-up table or read from it, therefore this parameter is specified in terms of the pixel clock period tCHCH.

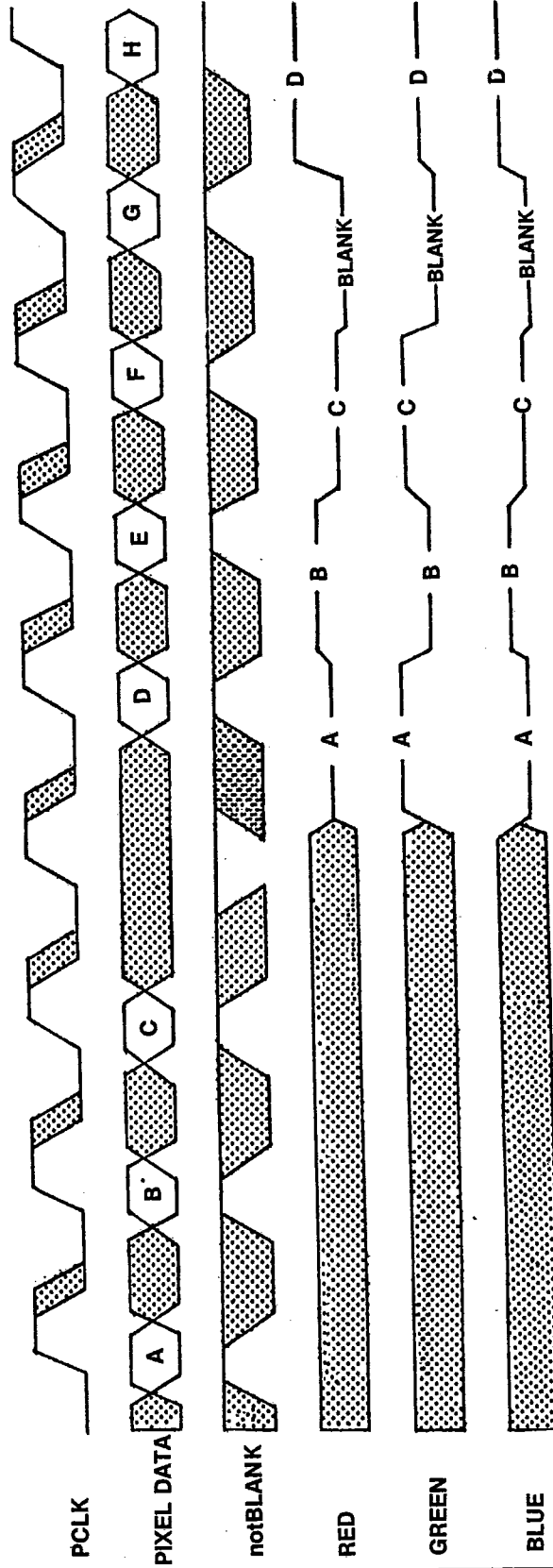


|        |                             | MX 82C171-35 |       |       |                  |
|--------|-----------------------------|--------------|-------|-------|------------------|
| Symbol | Parameter                   | Min          | Max   | Units | Notes            |
| tCHCH  | PCLK period                 | 25           | 10000 | ns    | Note 1           |
| ΔtCHCH | PCLK jitter                 |              | ±2.5  | %     |                  |
| tCLCH  | PCLK width low              | 9            | 10000 | ns    | Note 2<br>Note 3 |
| tCHCL  | PCLK width high             | 9            | 10000 | ns    |                  |
| tPVCH  | Pixel word setup time       | 4            |       | ns    |                  |
| tCHPX  | Pixel word hold time        | 4            |       | ns    |                  |
| tBVCH  | notBLANK setup time         | 4            | 45    | ns    |                  |
| tCHBX  | notBLANK hold time          | 4            | 1     | ns    |                  |
| tCHAV  | PCLK to valid DAC output    | 15           | 50    | ns    |                  |
| ΔtCHAV | Differential output delay   |              |       | ns    |                  |
|        | Pixel clock transition time |              |       | ns    |                  |

- Notes:
1. This parameter allowed variation in the Pixel Clock frequency does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.
  2. A valid analog output is defined as when the changing analog signal is half way between its successive values.
  3. Between different analog outputs on the same device.
- \*\*NOTE\*\*** The values given here are preliminary and are subject to change.



Video Timing: Normal operation + blanking





## ABSOLUTE MAXIMUM RATINGS

Voltage on VCC 7.0V  
 Voltage on other pin Vss -1.5V to Vcc + 0.5V  
 Temperature under bias -40°C to 85°C  
 Storage temperature (ambient) -65°C to 150°C  
 Power dissipation 1 W  
 Reference current -15 mA  
 Analog output current (per output) 45 mA  
 DC digital output current 25 mA

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC OPERATING CONDITION (a)

| Symbol | Parameter                     | Min  | Typ | Max       | Units |
|--------|-------------------------------|------|-----|-----------|-------|
| Vcc    | Positive supply voltage       | 4.5  | 5.0 | 5.5       | Volts |
| Vss    | Ground                        |      | 0   |           | Volts |
| VIH    | Input logic "1" voltage       | 2.0  |     | Vcc + 0.5 | Volts |
| VIL    | Input logic "0" voltage       | -1.0 |     | 0.8       | Volts |
| TA     | Ambient operating temperature | 0    |     | 70        | °C    |

## DC ELECTRICAL CHARACTERISTICS (a,b) (0°C ≤ TA ≤ 70°C)(Vcc = 5.0V ± 10%)

| Symbol   | Parameter                                | Min  | Max | Units | Notes       |
|----------|--|------|-----|-------|-------------|
| ICC      | Average power supply current             |      | 150 | mA    | c           |
| IREF     | Reference current                        | -1.5 | -10 | mA    | d           |
| VOA(max) | Maximum analog output voltage            | 1.5  |     | V     | 10A ≤ 10 mA |
| IOA(max) | Maximum analog output current            | 21   |     | mA    | VOA ≤ 0.7V  |
|          | Full scale accuracy                      | ±5   |     | %     |             |
|          | Differential accuracy                    | ±1   |     | %     | e           |
|          | Linearity                                | ±0.5 |     | LSB   | F           |
| IIN      | Digital input current (any input)        |      | ±10 | μA    | g,n         |
| IOZ      | Off state digital output leakage current |      | ±50 | μA    | g,o         |
| VOH      | Output logic "1" voltage                 | 2.4  |     | V     | 10-5 mA     |
| VOL      | Output logic "0" voltage                 |      | 0.4 | V     | 10-5 mA     |

## AC ELECTRICAL CHARACTERISTICS (b) (0°C ≤ TA ≤ 70°C)(Vcc = 5.0V ± 10%)

| Symbol | Parameter                | Min | Max | Units | Notes |
|--------|--------------------------|-----|-----|-------|-------|
|        | Rise time (10% to 90%)   |     | 8   | ns    | h     |
|        | Full scale settling time |     | 28  | ns    | h,i   |
|        | Glitch energy            |     | 200 | pVsec | j     |

## CAPACITANCE(j,k)

| Symbol | Parameter                  | Max | Units | Notes |
|--------|----------------------------|-----|-------|-------|
| CI     | Digital input capacitance  | 7   | pF    | n     |
| CO     | Digital output capacitance | 7   | pF    | l,o   |
| COA    | Analog output capacitance  | 10  | pF    | m     |





## AC TEST CONDITIONS

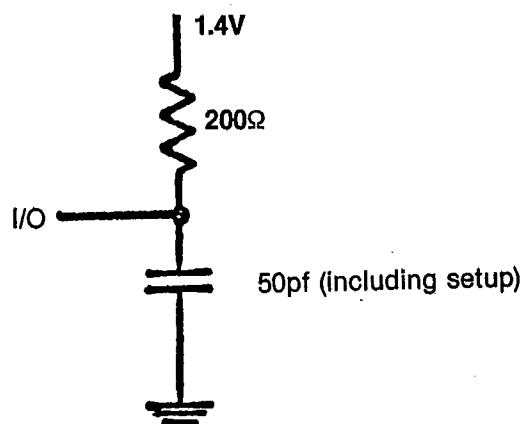
Input pulse levels  $V_{ss}$  to 3V  
 Input rise and fall times 2.5m  
 Digital input timing reference level 1.5V  
 Digital output timing reference level 0.8V and 2.4V  
 Digital output load See Figure 1

### Notes:

- a - All voltages in this data sheet are with respect to  $V_{ss}$  unless specified otherwise
- b - The Pixel Clock frequency must be stable for a period of at least 20  $\mu$ s after power-up (or after a change in Pixel Clock frequency) before proper device operation is guaranteed.
- c - Pixel Clock frequency = 35 MHz. 10A = 10A(max).
- d - Voltage at IREF input (pin 4)  $V_{cc}$  to  $V_{cc} - 3V$ .
- e - Between different analogue outputs on the same device.
- f - Monotonicity guaranteed.
- g -  $V_{cc} = \max, V_{ss} \leq V_{in} \leq V_{cc}$ .
- h - Load =  $75\Omega + 30$  pF.
- i - Between 1% and 99% of full scale voltage.
- j - This parameter is sampled, not 100% tested.
- k - Capacitance measured with a Hewlett Parkard meter.
- l -  $\text{notRD} \geq V_{IH}(\text{min})$  to disable D[0]-D[7].
- m -  $\text{notBLANK} \leq V_{IL}(\text{max})$  to disable RED, GREEN and BLUE.
- n - On pin numbers 5 to 16 and 25 to 27.
- o - On pin numbers 17 to 24.

**\*\*NOTE\*\*** The values given here are preliminary and are subject to change.

Figure 1. Output Load





**DEVICE OPERATION**

**Video path**

The Pixel Address and notBLANK inputs are sampled on the rising edge of Pixel Clock and appear at the analog outputs after three further rising edges of Pixel Clock.

**Analog Outputs**

The outputs of the DACs are intended to product 0.7 volt peak white amplitude when driving a 75 ohms load with 4.44mA IREF supplied, or a doubly terminated 75 ohm cable with 8.88 mA IREF supplied.

The notBLANK input to the MX 82C171 acts on all three of the analog outputs. When the notBLANK input is low a binary zero is applied to the inputs of the DACs.

The expressions for peak white voltage/output loading combinations given below:-

$$V_{\text{peak white}} = \frac{\text{IREF} \times 63 \times R_{\text{load}}}{30}$$

$$V_{\text{black level}} = 0$$

**Microprocessor interface**

There are three internal registers in the MX82C171. Each register can both be written to and read from. The registers are:-

| RS1 | RS0 | REGISTER                   | NAME |
|-----|-----|----------------------------|------|
| 0   | 0   | Pixel Address (Write Mode) |      |
| 1   | 1   | Pixel Address (Read Mode)  |      |
| 0   | 1   | Color Value                |      |
| 1   | 0   | Pixel Mask                 |      |

The Value in the Pixel Address register specifies a location in the look-up table. The Color Value register allows data to be written to or read from the look-up table at the location specified by the Pixel Address register. The Pixel Mask register is an 8 bit register. The value in the mask register is bitwise ANDed with the incoming pixel address to give a masked pixel address.

The microprocessor interface is asynchronous with the video path, the timing of operations on the interface registers being controlled by the

Write Enable signal (not WR) and the Read Enable signal (not RD). After certain accesses to the microprocessor interface data has to be written to or from the look-up table. To allow these operations to be synchronised to the pixel stream minimum inactive periods (not notWR and notRD high) are specified between accesses to the microprocessor interface. Each time a color value is written to (or read from) the look-up table the write (or read) cycle will replace the colour value red cycle for one pixel.

To access a color definition in the look-up table first both the mode of access (read or write) and the pixel address must be specified, then an 18 bit data word must be read from or written to the location specified.

The mode of access (read or write) is determined by writing a value into the Pixel Address register with RS[0]=RS[1]=1 to enter Read Mode or RS[0]=RS[1]=0 to enter Write Mode.

Once the mode and pixel address have been set one or more locations in the look-up table can be accessed. The first access will occur at the location specified by the value written to the Pixel Address register then, (as the Pixel Address register increments after each complete color value write or color value read sequence) further accesses can occur to a succession of locations.

A color value write sequence can occur when the MX 82C171 is in write mode. A color value write sequence is three successive byte writes to the Color Value register. The least significant 6 bits are taken from each byte written and concatenated into an 18-bit word in the Color Value register. The first byte written will define the red intensity, the second the green and the last the blue. When the three values have been written to the register its contents are written to the look-up table and the Pixel Address register is then incremented.

A color value read sequence can occur when MX 82C171 is in read mode. A color value read sequence

is three successive byte reads from the Color Value register. The least significant 6 bits of each byte read are taken from the 18 bit word in the Color Value register. The most significant two bits of each byte will be set to zero. The first byte read will contain the data for the red intensity, the second the green and the last the blue. When the three values have been read from the register the Pixel Address register is incremented and a new color value is read from the look-up table into the Color Value register.

The pixel address supplied to the Pixel Address inputs is bitwise ANDed with the Pixel Mask register before it is used to access the look-up table. This pixel masking process can be used to alter the displayed colors without altering the video memory or the lookup table contents. By partitioning the color definitions by one or more bits in the pixel address rapid animation and flashing objects can be produced.

If the Pixel Address register is written to during either a color value read or a color value write sequence the Color Value register is initialised, aborting any unfinished read or write sequence. The effects of reading from the color value register during a color value write sequence or writing to the register during a read sequence are not defined and may change the look-up table contents.

Accesses to the Pixel Mask register and read from the Pixel Address register can occur without reference to the state of colour value read or write sequences.



**DEVICE DESCRIPTION**

The MX 82C171 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store of 256 x 18 bit words, three 6 bit high speed DACs, 6 micro-processor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address Input is used as a read address for the store and results in an 18 bit data word. This data is partitioned as three fields of 6 bits, with each fields being applied to the

inputs of a 6 bit DAC.

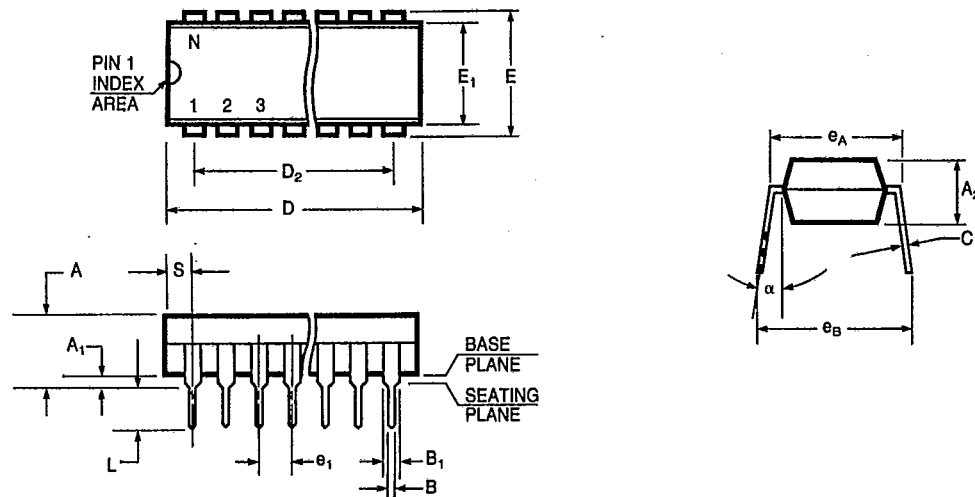
Pixel rates of upto 35 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blanking signal can be input to the MX 82C171; this signal acts on all three of the analog outputs. The notBLANK signal is delayed internally by pipelining so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be modified and examined via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows operations on the interface to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. The permits rapid changes of the effective contents of the Color Look-Up Table to facilitate such operations as

| Internal Registers |       |             | Register Name                       | Description<br>(All registers can be written to and read from)  |
|--------------------|-------|-------------|-------------------------------------|---|
| RS[1]              | RS[0] | SIZE (bits) |                                     |   |
| 0                  | 0     | 8           | Pixel Address Register (Write Mode) | Writing to the Pixel Address register In Write Mode sets the start address for one or more color value write sequences. Writing to the Pixel Address register in Read Mode set the start address for one or more colour value read sequences. Reading the Pixel Address register will read the current pixel address and will leave the device in its existing mode (Read Mode or Write Mode).  |
| 1                  | 1     | 8           | Pixel Address Register (Read Mode)  |   |
| 0                  | 1     | 18          | Color Value                         | The Color Value register is 18 bits wide. In Write Mode it is used to assemble a new color value before it is written to the loop-up table. In Read Mode it holds a color value read from the look-up table. The Color Value register is loaded by a sequence of three accesses. The first access is to the red DAC data, the second to the green DAC data and the third to the blue DAC data. In write sequences the least significant 6 bits of each byte are written to the Color Value register where they are concatenated to form an 18 bit color word. In read sequences the least significant 6 bits of each byte read come from the Color Value register and contain the data for one color in the 18 bit color word; the most significant two bits of the byte are set to zero. |
| 1                  | 0     | 8           | Pixel Mask                          | The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel address inputs (P[0]-P[7]). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Pixel Address used when the look-up table is being accesses via the microprocessor interface.  |



## PLASTIC DUAL-IN-LINE PACKAGES (PDIP)

16, 18, 20, 24, 28 LEAD 300 MIL WIDE AND 24, 28, 32, 40 LEAD 600 MIL WIDE

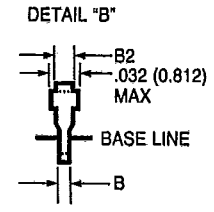
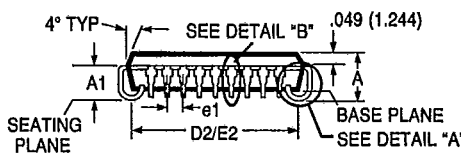
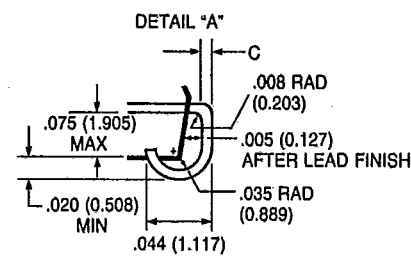
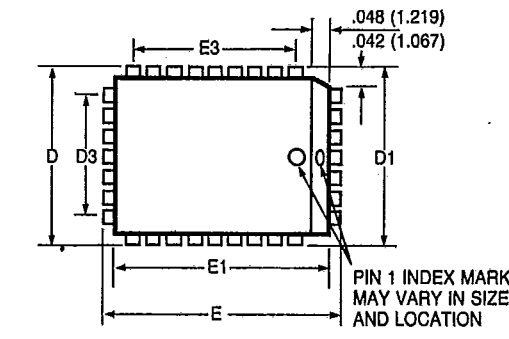
| LEADS WIDTH       | 24<br>.300       |                  | 24<br>.500       |                  | 28<br>.300       |                  | 28<br>.600       |                  | 32<br>.600       |                  | 40<br>.600       |                  |
|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| SYMBOL            | MIN              | MAX              | MIN              | MAX              | MIN              | MAX              | MIN              | MAX              | MIN              | MAX              | MIN              | MAX              |
| A                 | .150<br>(3.81)   | .200<br>(5.08)   | .150<br>(3.81)   | .200<br>(5.08)   | .150<br>(3.81)   | .200<br>(5.08)   | .150<br>(3.81)   | .200<br>(5.08)   | .150<br>(3.81)   | .200<br>(5.08)   | .150<br>(3.81)   | .200<br>(5.08)   |
| A1                | .015<br>(.381)   | .070<br>(1.78)   | .015<br>(.381)   | .070<br>(1.78)   | .015<br>(.381)   | .070<br>(1.78)   | .015<br>(.381)   | .070<br>(1.78)   | .015<br>(.381)   | .070<br>(1.78)   | .015<br>(.381)   | .070<br>(1.78)   |
| A2                | .125<br>(3.18)   | .155<br>(3.94)   | .135<br>(3.43)   | .165<br>(4.19)   | .125<br>(3.18)   | .155<br>(3.94)   | .135<br>(3.43)   | .165<br>(4.19)   | .135<br>(3.43)   | .165<br>(4.19)   | .135<br>(3.43)   | .165<br>(4.19)   |
| B                 | .015<br>(.381)   | .023<br>(.584)   | .015<br>(.381)   | .023<br>(.584)   | .015<br>(.381)   | .023<br>(.584)   | .015<br>(.381)   | .023<br>(.584)   | .015<br>(.381)   | .023<br>(.584)   | .015<br>(.381)   | .023<br>(.584)   |
| B1                | .060<br>(1.52)   | TYP              | .060<br>(1.52)   | TYP              | .060<br>(1.52)   | TYP              | .060<br>(1.52)   | TYP              | .050<br>(1.27)   | TYP              | .060<br>(1.52)   | TYP              |
| C                 | .008<br>(.203)   | .015<br>(.381)   | .008<br>(.203)   | .015<br>(.381)   | .008<br>(.203)   | .015<br>(.381)   | .008<br>(.203)   | .015<br>(.381)   | .008<br>(.203)   | .015<br>(.381)   | .008<br>(.203)   | .015<br>(.381)   |
| D                 | 1.230<br>(31.24) | 1.270<br>(32.26) | 1.230<br>(31.24) | 1.280<br>(32.51) | 1.345<br>(34.16) | 1.355<br>(34.42) | 1.390<br>(35.31) | 1.470<br>(37.34) | 1.640<br>(41.66) | 1.660<br>(42.16) | 2.030<br>(51.56) | 2.080<br>(52.83) |
| D2                | 1.100<br>(27.94) | TYP              | 1.100<br>(27.94) | TYP              | 1.300<br>(33.02) | TYP              | 1.300<br>(33.02) | TYP              | 1.400<br>(35.56) | TYP              | 1.900<br>(48.26) | TYP              |
| E                 | .300<br>(7.62)   | .320<br>(8.13)   | .600<br>(15.24)  | .620<br>(15.75)  | .300<br>(7.62)   | .325<br>(8.26)   | .600<br>(15.24)  | .620<br>(15.75)  | .600<br>(15.24)  | .620<br>(15.75)  | .600<br>(15.24)  | .620<br>(15.75)  |
| E1 (4)            | .240<br>(6.10)   | .280<br>(7.11)   | .520<br>(13.21)  | .560<br>(14.22)  | .270<br>(6.86)   | .290<br>(7.37)   | .520<br>(13.21)  | .560<br>(14.22)  | .520<br>(13.21)  | .560<br>(14.22)  | .520<br>(13.21)  | .560<br>(14.22)  |
| e1 (3)            | .100<br>(2.54)   | TYP              | .100<br>(2.54)   | TYP              | .100<br>(2.54)   | TYP              | .100<br>(2.54)   | TYP              | .100<br>(2.54)   | TYP              | .100<br>(2.54)   | TYP              |
| eA(3)             | .300<br>(7.62)   | TYP              | .600<br>(15.24)  | TYP              | .300<br>(7.62)   | TYP              | .600<br>(15.24)  | TYP              | .600<br>(15.24)  | TYP              | .600<br>(15.24)  | TYP              |
| eB (3)            | .350<br>(8.89)   | TYP              | .650<br>(16.51)  | TYP              | .350<br>(8.89)   | TYP              | .650<br>(16.51)  | TYP              | .650<br>(16.51)  | TYP              | .650<br>(16.51)  | TYP              |
| L                 | .120<br>(3.05)   | .140<br>(3.56)   | .120<br>(3.05)   | .140<br>(3.56)   | .120<br>(3.05)   | .140<br>(3.56)   | .120<br>(3.05)   | .140<br>(3.56)   | .120<br>(3.05)   | .140<br>(3.56)   | .120<br>(3.05)   | .140<br>(3.56)   |
| N                 | 24               |                  | 24               |                  | 28               |                  | 28               |                  | 32               |                  | 40               |                  |
| S                 | .040<br>(1.02)   | .085<br>(2.16)   | .040<br>(1.02)   | .085<br>(2.16)   | .020<br>(.508)   | .030<br>(.762)   | .040<br>(1.02)   | .085<br>(2.16)   | .040<br>(1.02)   | .085<br>(2.16)   | .040<br>(1.02)   | .090<br>(2.29)   |
| α (5)             | 0                | 15               | 0                | 15               | 0                | 15               | 0                | 15               | 0                | 15               | 0                | 15               |
| Theta JA Cu: (6)  |                  |                  | 55               |                  | 50               |                  | 55               |                  | 45               |                  | 45               |                  |
| °C/Watt AL42: (6) |                  |                  | 110              |                  | 105              |                  | 110              |                  | 105              |                  | 105              |                  |

**NOTES:**

1. Refer to applicable symbol glossary.
2. All dimensions are in inches (mm).
3. e1, eA and eB apply for installing on a PC board.
4. D and E1 do not include mold flash.
5. α In degrees applies to spread of leads.



6. The Thermal Resistance, Theta JA, in °C/Watt, quoted above is for a 10,000 sq. mil die in still air and shown for both copper and alloy-42 frames. Values are approximate.
7. Lead frame material: alloy 42 or copper.
8. Lead finish: Matte tin or Sn/Pb solder.
9. Note: Call Manufacturer for dimensional information on 16, 18, 20, 48 and 64 lead packages.



## PLASTIC LEADED CHIP CARRIERS (PLCC) 24, 32, 44, 68, AND 84 LEAD

LEADS 28 32 44 68 84

| SYMBOL                    | 28              |                 | 32              |                 | 44              |                 | 68              |                 | 84               |                  |
|---------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|
|                           | MIN             | MAX             | MIN             | MAX             | MIN             | MAX             | MIN             | MAX             | MIN              | MAX              |
| A                         | .165<br>(4.19)  | .180<br>(4.57)  | .100<br>(2.54)  | .140<br>(3.56)  | .165<br>(4.19)  | .180<br>(4.57)  | .165<br>(4.19)  | .200<br>(5.08)  | .165<br>(4.19)   | .200<br>(5.08)   |
| A1                        | .090<br>(2.29)  | .120<br>(3.05)  | .060<br>(1.52)  | .095<br>(2.41)  | .090<br>(2.29)  | .120<br>(3.05)  | .090<br>(2.29)  | .130<br>(3.30)  | .090<br>(2.29)   | .130<br>(3.30)   |
| B                         | .013<br>(.330)  | .021<br>(.533)  | .013<br>(.330)  | .021<br>(.533)  | .013<br>(.330)  | .021<br>(.533)  | .013<br>(.330)  | .021<br>(.533)  | .013<br>(.330)   | .021<br>(.533)   |
| B2                        | .026<br>(.660)  | .032<br>(.813)  | .026<br>(.660)  | .032<br>(.813)  | .026<br>(.660)  | .032<br>(.813)  | .026<br>(.660)  | .032<br>(.813)  | .026<br>(.660)   | .032<br>(.813)   |
| C                         | .008<br>(.203)  | .010<br>(.254)  | .008<br>(.203)  | .010<br>(.254)  | .008<br>(.203)  | .010<br>(.254)  | .008<br>(.203)  | .010<br>(.254)  | .008<br>(.203)   | .010<br>(.254)   |
| D                         | .485<br>(12.32) | .495<br>(12.57) | .485<br>(12.32) | .495<br>(12.57) | .685<br>(17.40) | .695<br>(17.65) | .985<br>(25.02) | .995<br>(25.27) | 1.185<br>(30.10) | 1.195<br>(30.35) |
| D1                        | .450<br>(11.43) | .456<br>(11.58) | .447<br>(11.35) | .453<br>(11.51) | .650<br>(16.51) | .656<br>(16.66) | .950<br>(24.13) | .958<br>(24.33) | 1.150<br>(29.21) | 1.158<br>(29.41) |
| D2                        | .390<br>(9.91)  | .430<br>(10.92) | .390<br>(9.91)  | .430<br>(10.92) | .590<br>(14.99) | .630<br>(16.00) | .890<br>(22.61) | .930<br>(23.62) | 1.090<br>(27.69) | 1.130<br>(28.70) |
| D3                        | .300<br>(7.62)  | REF             | .300<br>(7.62)  | REF             | .500<br>(12.70) | REF             | .800<br>(20.32) | REF             | 1.000<br>(25.40) | REF              |
| E                         | .485<br>(12.32) | .495<br>(12.57) | .585<br>(14.86) | .595<br>(15.11) | .685<br>(17.40) | .695<br>(17.65) | .985<br>(25.02) | .995<br>(25.27) | 1.185<br>(30.10) | 1.195<br>(30.35) |
| E1                        | .450<br>(11.43) | .456<br>(11.58) | .547<br>(13.89) | .553<br>(14.05) | .650<br>(16.51) | .656<br>(16.66) | .950<br>(24.13) | .958<br>(24.33) | 1.150<br>(29.21) | 1.158<br>(29.41) |
| E2                        | .390<br>(9.91)  | .430<br>(10.92) | .490<br>(12.45) | .530<br>(13.46) | .590<br>(14.99) | .630<br>(16.00) | .890<br>(22.61) | .930<br>(23.62) | 1.090<br>(27.69) | 1.130<br>(28.70) |
| E3                        | .300<br>(7.62)  | REF             | .400<br>(10.16) | REF             | .500<br>(12.70) | REF             | .800<br>(20.32) | REF             | 1.000<br>(25.40) | REF              |
| e1                        | .050<br>(1.27)  | TYP             | .050<br>(1.27)  | TYP             | .050<br>(1.27)  | TYP             | .050<br>(1.27)  | TYP             | .050<br>(1.27)   | TYP              |
| N                         | 28              |                 | 32              |                 | 44              |                 | 68              |                 | 84               |                  |
| ND                        | 7               |                 | 7               |                 | 11              |                 | 17              |                 | 21               |                  |
| NE                        | 7               |                 | 9               |                 | 11              |                 | 17              |                 | 21               |                  |
| Theta JA (5)<br>(°C/Watt) | 45              |                 | 45              |                 | 45              |                 | 45              |                 | 45               |                  |

- NOTES:**  
 1. Refer to applicable symbol glossary.  
 2. All dimensions are in inches (mm).  
 3. Controlling dimension Inch.  
 4. D1 and E1 do not include mold flash.



5. The Thermal Resistance, Theta JA, in °C/Watt, quoted above is for a 10,000 sq. mil die in still air with copper frame. Values are approximate.  
 6. Lead frame material: copper.  
 7. Lead finish: Matte tin or Sn/Pb solder dip.  
 8. Note: Call Manufacturer for dimensional information on 20, 52 and 84 lead packages.