PM7346

S/UNI-QJET

SATURN USER NETWORK INTERFACE (QJET)

ERRATA

ISSUE1 JUNE 1999

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	June 1999	This document contains errata information corresponding to the issue 5 datasheet.

CONTENTS

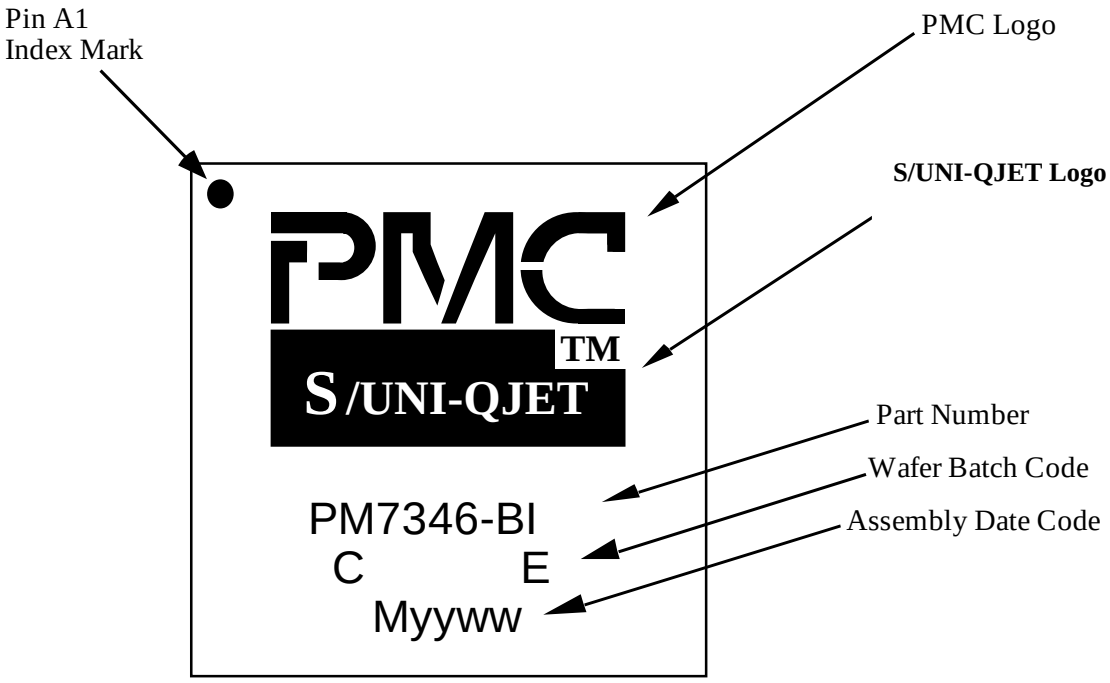
1 ISSUE 1 ERRATA

This issue 1 contains errata applied to the PMC-960835 S/UNI-QJET Issue 5 datasheet. The issue 5 datasheet and issue 1 errata supersede all prior editions and versions.

1.1 Device Identification

The information contains in this document applies to the PM7346 S/UNI-QJET revision E. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM7346 S/UNI-QJET revision E is packaged in a 256 pin Super BGA package.

Figure 1: PM7346 S/UNI-QJET Branding Format



TOP VIEW
SCALE : 2:1
(APPROX.)

2 SOFTWARE RESET REQUIRED AFTER POWER UP

After hardware reset the S/UNI-QJET needs a software reset to reduce power consumption. This problem has no implications to the functionality of the part except for excessive power consumption and resulting excess heat dissipation.

Software initialization sequence:

A modification to the software initialization sequence used will guarantee that the S/UNI QJET operates with normal power consumption.

The sequence below will set the all the RAM in the QJET to a low power state.

1. Reset the S/UNI QJET.

2. Set IOTST (bit 2) in the Master Test Register (datasheet pg. 291) to '1' (by writing 00000100 to register 400H).

3. Put the QJET Receive Cell Processor (RXCP) into test mode by writing:
   00000101 to test register 461H
   00000101 to test register 561H
   00000101 to test register 661H
   00000101 to test register 761H

4. Set QJET Receive Cell Processor block built in self-test (BIST) controls signals by writing:
   01000000 to test register 462H
   01000000 to test register 562H
   01000000 to test register 662H
   01000000 to test register 762H

   10101010 to test register 463H
   10101010 to test register 563H
   10101010 to test register 663H
   10101010 to test register 763H

5. Put the QJET Transmit Cell Processor (TXCP) into test mode by writing:
   00000011 to test register 481H
   00000011 to test register 581H
   00000011 to test register 681H
   00000011 to test register 781H

6. Set QJET Transmit Cell Processor block built in self-test (BIST) controls signals by writing:
   10000000 to test register 480H
   10000000 to test register 580H
   10000000 to test register 680H

10000000 to test register 780H

10101010 to test register 482H
10101010 to test register 582H
10101010 to test register 682H
10101010 to test register 782H

7. Toggle REF8KI (pin T3, datasheet page 29) signal several times (this provides the clock to the RAM). REF8KI is the test clock used by the TXCP and RXCP blocks when in test mode.

8. Set IOTST (bit 2) in the Master Test register (datasheet pg. 291) to '0' (by writing 00000000 to register 400H).

This sequence will correct the excess power consumption of the internal RAM.

Performance without software sequence:

Failure to run this sequence will result in excess power consumption and a degraded long term reliability. Therefore, it is critical that the above software fix be implemented.

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
(604) 415-4533
Web Site: http://www.pmc-sierra.com

PMC-990537 (R1) ref PMC 960835 (R5) Issue date: June 1999