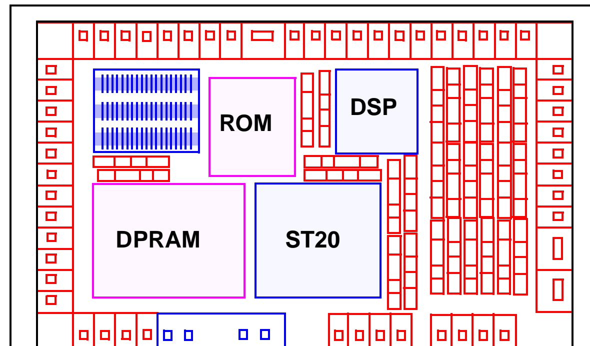
CB55000 Series

HCMOS7 Standard Cells

FEATURE

- 0.25 micron drawn (0.20 micron effective channel length process), six layers of metal connected by fully stackable vias and contacts, Shallow Trench Isolation, low resistance, salicided active areas and gates. Deep UV lithography.
- 2.5 V optimized transistor with 3.3 V I/O and supply interface capability.
- Average gate density: 30 K/mm2, plus low power consumption of 70 nanoWatt/Gate/MHz/ Stdload.
- Two input NAND delay of 90 pS (typical) with fanout=2.
- Library available in commercial, industrial and military temperature range with supply ranging from 2.70 V down to 1.8 V for the core according to EIA/JESD 8-5 specification. Additional low voltage range down to 1.5 V for very low voltage/low power applications supported
- Broad I/O functionality including:
  – Low Voltage CMOS.
  – Low Voltage TTL, PECL, HSTL, SSTL, LVDS, PCI.
- AGP 2X and 4X, USB to support 2.5 V and 3.3 V I/O interface according to EIA/JESD 8A specification.
- Drive capability up to 8 mA per buffer with slew rate control, current spike suppression impedance matching, and process compensation capability to reduce delay variation.
- Designs easily portable from previous generations of CB45000 through cell mapping with an average factor 2 density increase, 1.7 speed increase and 2.5 power reduction at respective nominal voltages.
- Generators to support Single Port, Dual port and multiple Port RAM, and ROMs with BIST options.
- Extensive embedded function library including ST DSP and micro-cores, third-party IPs, Synopsys and Mentor Inventra synthetic libraries ideally suited for complete System On Chip fast integration .
- 80 µm pitch linear and 50 µm staggered pad libraries.
- Fully independent power and ground configuration for core and I/Os supported.
- I/O ring capability up to 1500 pads.
- Latch-up trigger current > +/- 500 mA. ESD protection above 4 kV in H.B.M.
- Oscillators and PLLs for wide frequency spectrum.
- Broad range of more than 600 SSI cells.
- Design for test features including IEEE 1149.1 JTAG Boundary Scan architecture.
- Synopsys, Cadence and Mentor based design systems with interface from multiple workstations.
- Broad range of packaging solutions, including BGA, LBGA, TQFP, PQFP, PLCC up to 1000 pins with enhanced power dissipation options.
- 1.25 GigaHertzGigabit DLL technique.

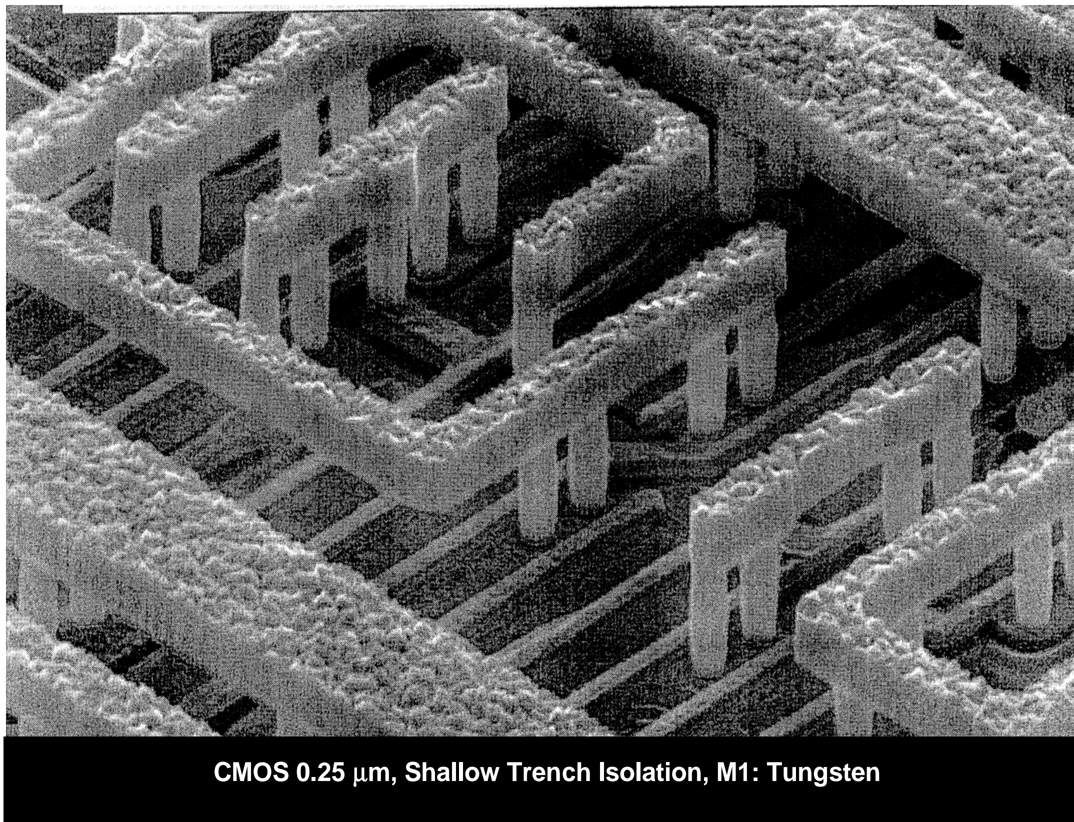


CB55000 Super Integration

Cost Effective Product
- Architecture partitioning
- Trouble-free integration
- Application-specific

Your Product is Unique
- User specified cell integration
- Design confidentiality
- IP fully re-usable

Figure 1. Metal 1 perspective view



CMOS 0.25 µm, Shallow Trench Isolation, M1: Tungsten

1 GENERAL DESCRIPTION

The CB55000 standard cell series uses a high performance, low-voltage, 0.25 µm drawn (0.20 µm effective), six metal levels CMOS process HCMOS7 to a 90 pico-second internal delay while offering very low power dissipation and high noise immunity.

With an average routed gate density of 30,000 gates/mm^2, the CB55000 family allows the integration of up to 15 million equivalent gates and is ideal for high-complexity or high-performance devices for computer, telecommunication and consumer products.

With a typical gate delay of 70 ps (for a 2-input NAND gate at fan-out 1), the library meets the most demanding speed requirements in telecommunication and computer application designs today.

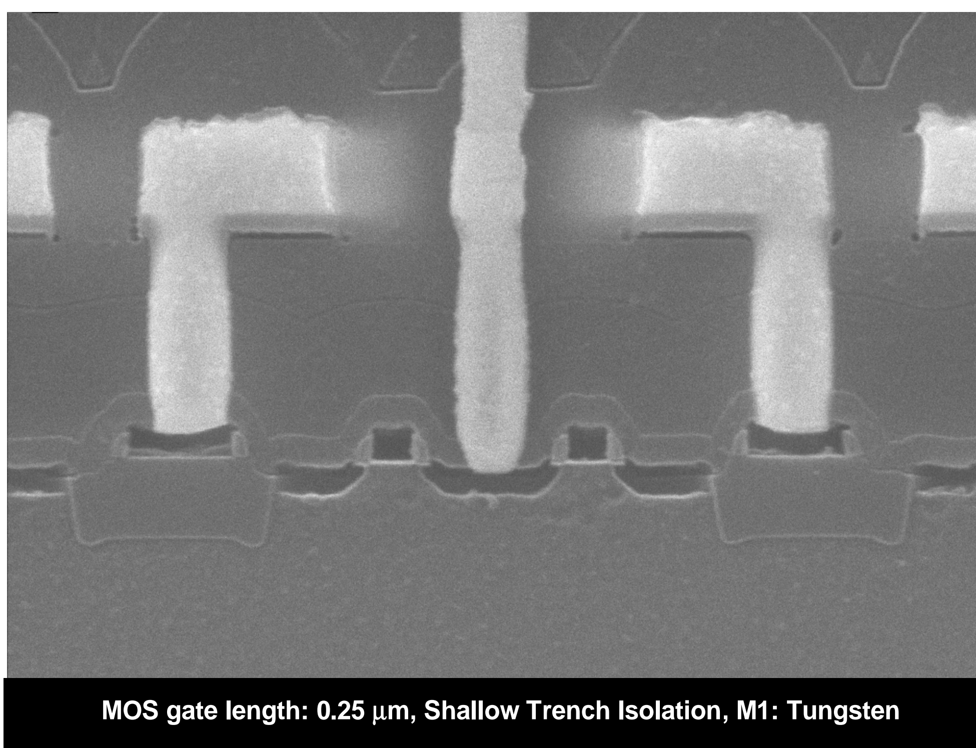
Optimized for 2.5 V operation, the library features a power consumption of less than 70 nW/Gate/MHz (fan-out=1) and 30 nW/Gate/MHz (fan-out=1) at 1.8 V.

The I/O buffers can be fully configured for both 2.5 V and 3.3 V interface options, with several high speed buffer types available. These include: low voltage differential (LVDS) I/Os, PCI/AGP, PECLs, and HSTL.

The pad pitch down to 50 µm, in a staggered arrangement, meets the requirements of high pin-count devices which tend to become pad-limited at such library densities. For very high pin-count ICs, advanced packaging solutions such as Chip Scale Packaging in fine pitch BGA are available.

New packaging solutions using a flip-chip approach are currently being developed.

Figure 2. HCMOS7 Front end cross section



MOS gate length: 0.25 µm, Shallow Trench Isolation, M1: Tungsten

2 TECHNOLOGY OVERVIEW

The advanced HCMOS7 transistor architecture: at 0.25 µm drawn length and 0.20 µm effective length, very thin gate oxide: 5 nanometers, optimized threshold voltages and salicided source, drain, and gate leads to intrinsically high performances in both N channel and P channel driving currents.

The major scaling factor is obtained through deep UV lithography at most masking levels, making sub-micron pitch a reality.

Further integration in the process front-end comes from the use of the Shallow Trench Isolation process between active regions, both improving density and planarity of transistors. In order to allow full utilization of such transistor density, up to 6 levels of metal are made available for routing.

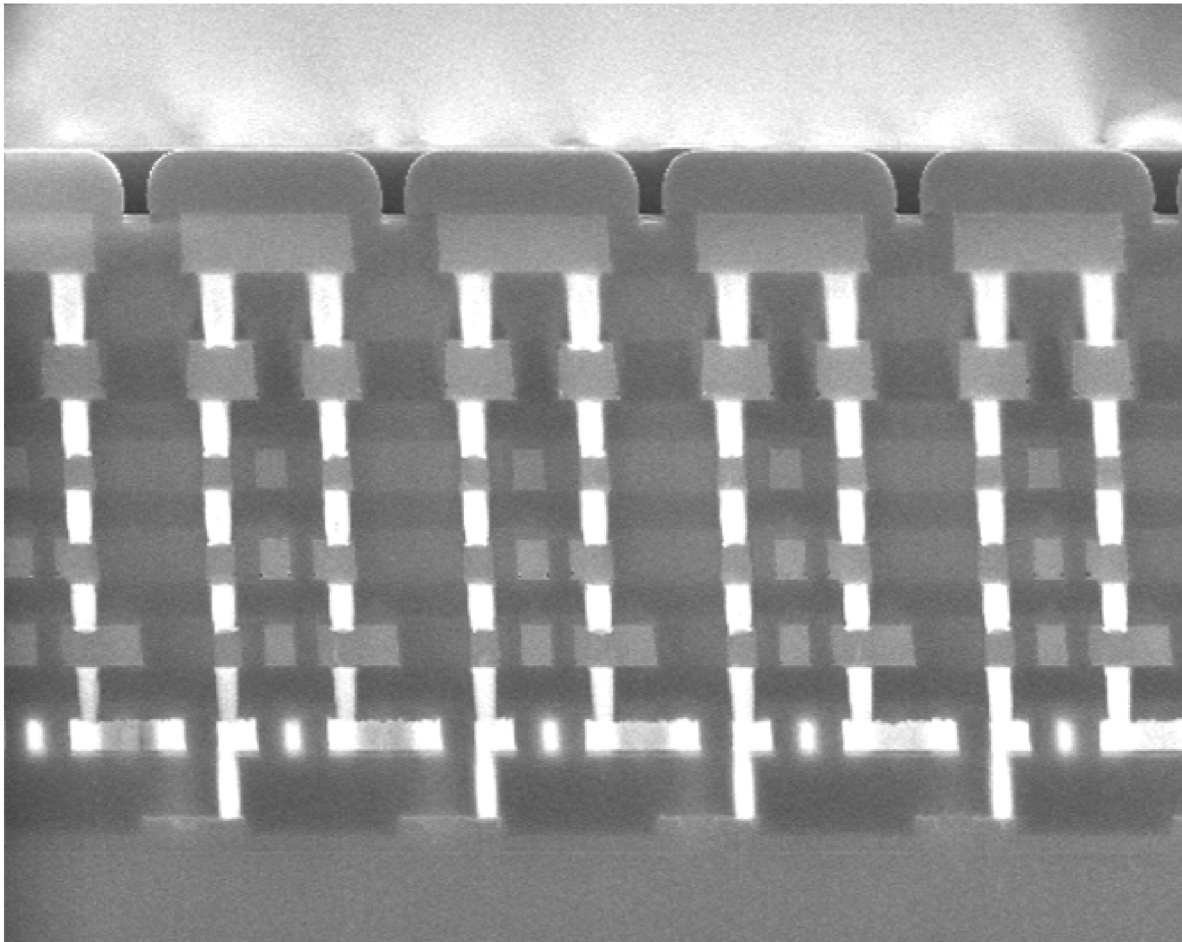
The first metal level is Tungsten for local interconnection, while the other five metal levels are of low resistivity aluminum for long range interconnection and power distribution.

The thick inter-level dielectric is completely planarized by Chemical Mechanical Polishing, which provides defect-free isolation between stripes within the same as well as between different levels.

Usage of Tungsten plugs at contacts and vias allows extremely dense and reliable interconnection between metal layers. These vias and contacts are fully stackable, providing a direct vertical electrical connection from the active level up to the sixth metal level. This efficient interconnect scheme makes routing fast and easy, as well as having a very positive impact on high gate count, random-logic blocks density and routability.

The combination of both high drive and dense transistors, easily interconnected with up to six fine-pitch metal levels and isolated by thick dielectric leads to an optimum gate density, with low parasitic resistance and capacitance. This results in very short interconnected gate delay and minimized power consumption.

Figure 3. HCMOS7 Back end Cross Section



3 LIBRARY

The CB55000 library is organized into three categories:

– SSI cell library
– I/O cell library
– Macrofunctions

3.1 SSI Cell Library Overview

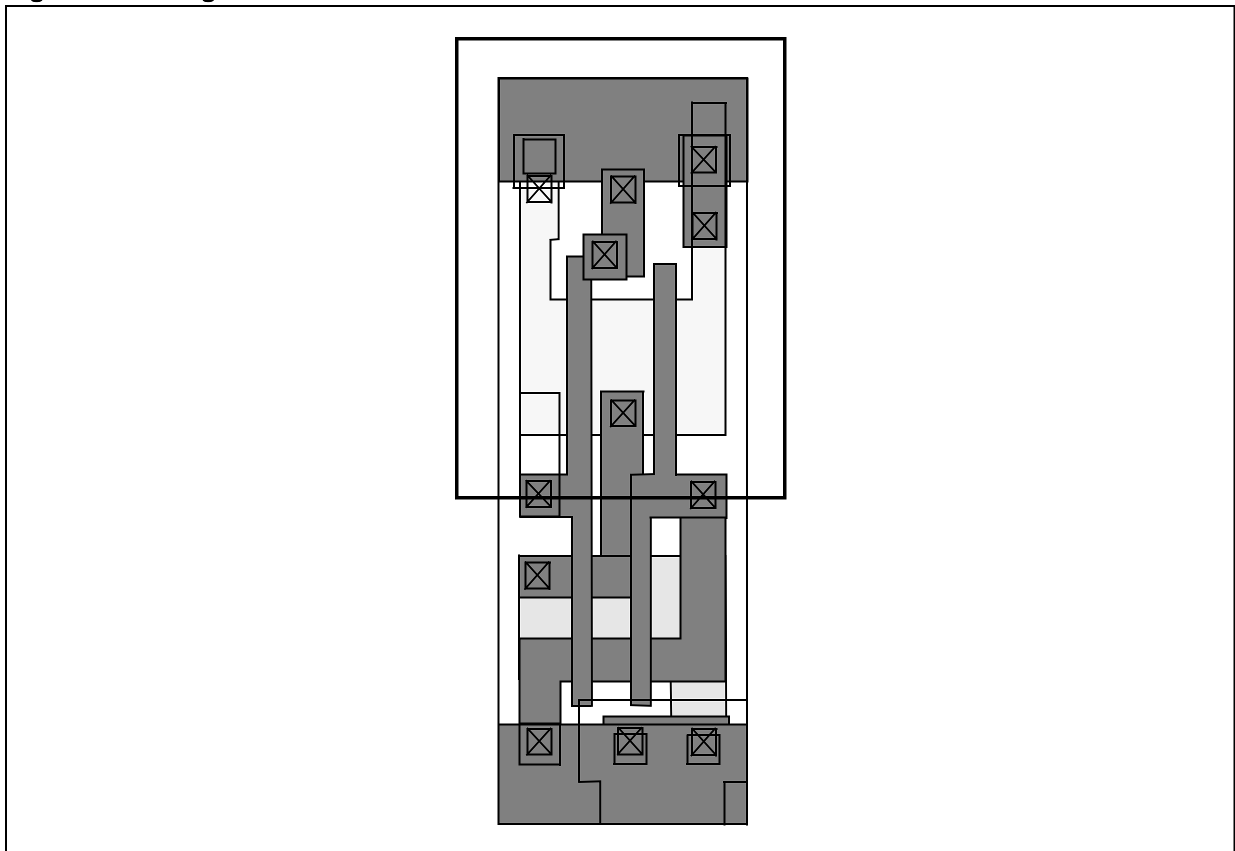
The design of the CB55000 family has been optimized to allow extremely high density, high speed and low power designs. For these reasons, a wide range of cells with different ranges of driving capabilities are available in the library.

The library cells have been optimized in terms of functional and electrical parameters, in order to have:

– Good balancing
– Maximum speed
– Optimum threshold voltage
– Symmetric V_{dd}/V_{ss} noise margins
– Minimum power-speed value

The geometrical aspect of the cells was configured to allow an extremely dense design, fully exploiting the features of the Place and Route tool in terms of horizontal and vertical routing grids. For Place and Route, up to six layers of metal are utilized; the first metal layer is dedicated to intracell wiring, the second layer to power distribution and routing, the third and forth layers to routing, and the fifth and sixth to power distribution, clock bussing and routing.

Figure 4. ND2 figure from CB55000



3.2 Core Logic

The propagation delays shown in CB55000 data book are given for nominal processing, 2.5 V, 25°C temperature. However, there are additional factors that affect the delay characteristics of the cells. These include: loading due to fanout and interconnect routing, supply voltage, junction temperature of the device, processing tolerance and input signal transition time.

Prior to physical layout, the design system can estimate the delays associated with any critical path. The impact of the placement and routing can be accurately RC back-annotated from the layout for final simulations of critical timing. The median effects on the cells delay of junction temperature (Kt coefficient) and supply voltage (Kv coefficient) are summarized in the following tables at a fixed cell input slope. A third factor is related to process variations and has a minimum median of 0.84 for best case process and a maximum median of 1.18 for worst case process.

Table 1. Junction temperature multipliers

Temperature (°C)	Kt
-55	.84
-40	.87
25	1.00
70	1.09
85	1.12
105	1.16
125	1.20

Table 2. Voltage multipliers

V_{dd} (V)	Kv
1.80	1.33
2.00	1.21
2.25	1.09
2.50	1.00
2.75	0.94

3.3 I/O Buffer Libraries

Two basic buffer libraries are offered with CB55000, one 80 µm pad in line pitch library and one 50 µm staggered pad library to support pad limited designs.

Apart from standard ESD and latch-up protections present in each I/O, a proprietary clamp within each power supply provides proper paths to all types of ESD discharges, efficiently protecting the I/Os. As a result, the buffers withstand more than 4 kV ESD according to Mil 883C Human Body Model specification.

In order to limit switching noise and keep a fixed buffer delay, independent of process, supply voltage and temperature, compensated active slew rate buffers can be selected, providing a fixed and stable dI/dt at 8,16 or 32 mA/ns.

In order to interface with 3.3 V application (from 2.7 up to 3.6 V), a wide range of 3.3 V capable input/output buffers (mixable with standard 2.5V ones) can be chosen. In this case the 3.3 V rail in the chip periphery must be powered through a 3.3 V external supply.

True 5 volt tolerant input buffer is also available with process option.

3.4 I/O Test Interface

The I/O cells have a dedicated test interface to facilitate parametric and Iddq testing of devices. This test interface connects standard core signals or dedicated test signals to the I/O cells allowing all output buffers to be driven high, low or put into tri-state regardless of the state of the internal logic.

This greatly simplifies parametric testing of the device and also assisting customers who wish to use this feature during board testing. Note that all output buffers can be tri-stated by this function including buffers that normally do not tri-state.

This test function also turns off all pull down resistors, shuts down all differential receivers and converts them into standard CMOS receivers. This allows Iddq test methodologies to be employed in a very efficient way, avoiding unneeded circuit overhead.

3.5 Macrocells

The CB55000 series has internal macrocells that are robust in variety and performance. The cell selection has been driven by the need of Synthesis and HDL-based design techniques. This offering is rich in buffers, complex combination cells and multi-power drive cells, which allow the Synthesis tool to create a netlist compatible with the requirements of Place and Route tools.

Macrofunctions are a series of soft-macros facilitating quick capture of large functional blocks and are available for such functions as counters, shift registers and adders. Macrofunctions are implemented at layout by utilizing macrocells and interconnecting to create the logic function.

3.5.1 Module generators

A series of module generators using compiled cell generation techniques are available to support a range of megacells. These modules enable the designer to choose individual parameters in order to create a compiled cell, which meets the specific application requirements. These include ROM, single and dual port RAM, multi-port RAM and FIFO.

For most of the above memories, two different generators are provided, one optimized for speed and one optimized for power. All memories have a complete standby mode where current consumption is limited to process leakage.

Table 3. List of module generators

Generator	Description	Bit (Min.)	Kbit (Max)	Word width (Max.)
Romd	High speed Sync. Diffusion ROM	128	2000	64
Rom3	Low power Sync. Diffusion ROM	128	256	32
SPS2	High speed Sync. Single port RAM	64	512	64
SPS3	Low power Sync. Single Port RAM	16	32	32
SPS4	Small cuts Sync. Low power Single Port Ram	2	16	128
SPS5	Low power Sync. Single Port RAM	1000	512	64
SPS6	High density Low power & voltage High density Sync. Single Port Ram	2000	2000 byte write supported	32

Table 3. List of module generators (continued)

Generator	Description	Bit (Min.)	Kbit (Max)	Word width (Max.)
SPS2HD	High speed & density High density Sync. Single port RAM	64	512	64
DPR2 DPR3	High speed Sync. Dual port RAM Low power Sync. Dual port RAM	64 16	256 32	64 32
DP7E	Asynchronous Reg. file Dual port RAM 1W + 1R	2	16	128
MP7A	Multiport RAM High density Sync. 2W + 2R or 2W + 4R	2	32	128
FIFO	High speed	8	4	32

Embedded Non Volatile Memories (OTP, Flash, ...) with specific process options are also under development.

3.5.2 MicroLibrary & I.P.s

MicroLibrary includes an extensive portfolio of microcores and application specific I.P.s; provided through both internal developments and partners licensing agreements.

A short list of this portfolio consists of:

- General purpose macro functions.
  - Microcores (8,16,32 bits) like:8051,ST10,ST20,SH4,ARM7TDMI,
  - DSP:D950,ST100,
  - PLL, Frequency synthesizer, Comparators,
  - DAC,ADC (8,10,16 bits).
- Application specific I.P.s for:
  - Data communications (10/100 ETH MAC & PHY, Gigabit,..),
  - Telecommunication (622MHz phase aligner, clock recovery),
  - Computer and peripherals (PCI,USB,SSCI,RAMDAC,IEEE1394,FiberChannel),
  - Audio (CODEC,..).

4 DESIGN FOR TESTABILITY

The test time and cost for ASIC testing increases exponentially as the complexity and size of the ASIC grows. Using a *design-for-testability* methodology allows large, more complex ASICs to be efficiently and economically tested.

At system level, STMicroelectronics fully supports IEEE 1149.1; the I/O structure utilized in this family is completely compatible. Several types of core scan cells are provided in the CB55000 Series library. Examples include FDxS/FJKxS edge sensitive and LDxS level sensitive cells. Non-overlapping clock generator macros are also available.

Test coverage and reliability are further supported by IDDQ (quiescent current) testing; all blocks are designed to be “IDDQable” so that anomalous leakage due to metal bridging and dielectric defects can be screened using proper set of vectors extracted from the test patterns.

For parametric and Iddq testing, the I/O cells contain a dedicated test interface as described previously (see I/O Test Interface’ on page 7).

5 EVALUATION DEVICE

As per STMicroelectronics’ standard policy, all cells and macro-blocks are fully validated and characterized on silicon through dedicated test vehicules, before final release in the library. In addition, a 3 million-gates evaluation chip: CB55Q, has been designed and in order to demonstrate the performances and qualify the global CB55000 library, as well as verify the effectiveness of the design system.

CB55Q is packaged in a 256 Ball Grid Array (BGA) and permits accurate characterisation of most representative cells from the library including I/O buffers, single and mixed cell chains (IV, ND2, NR2...),Flip-flops and memory cuts from various generators.

Typical result on ring SSI chain in ring oscillator mode show a mean between Thl and Tlh of around 37 ps for an inverter with 1 standard load , and toggle frequency of above 1 GigaHertz for an FD2.

Figure 5. CB55Q Die View

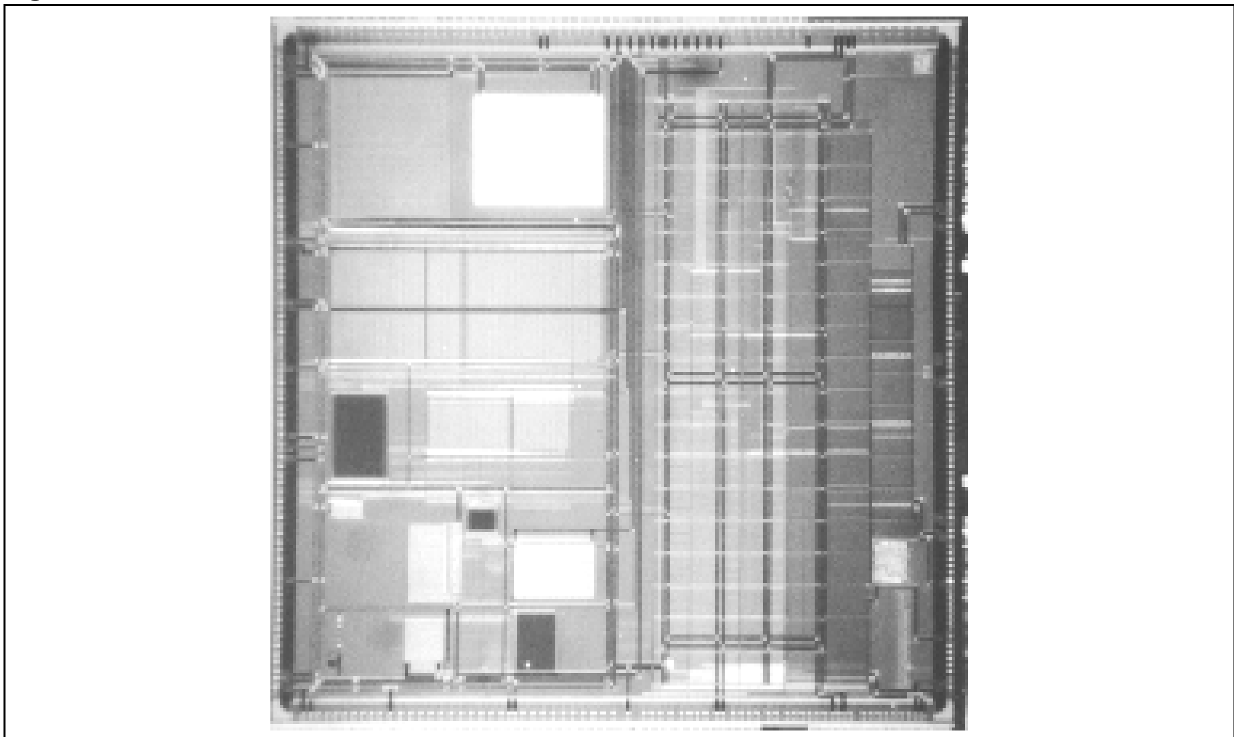
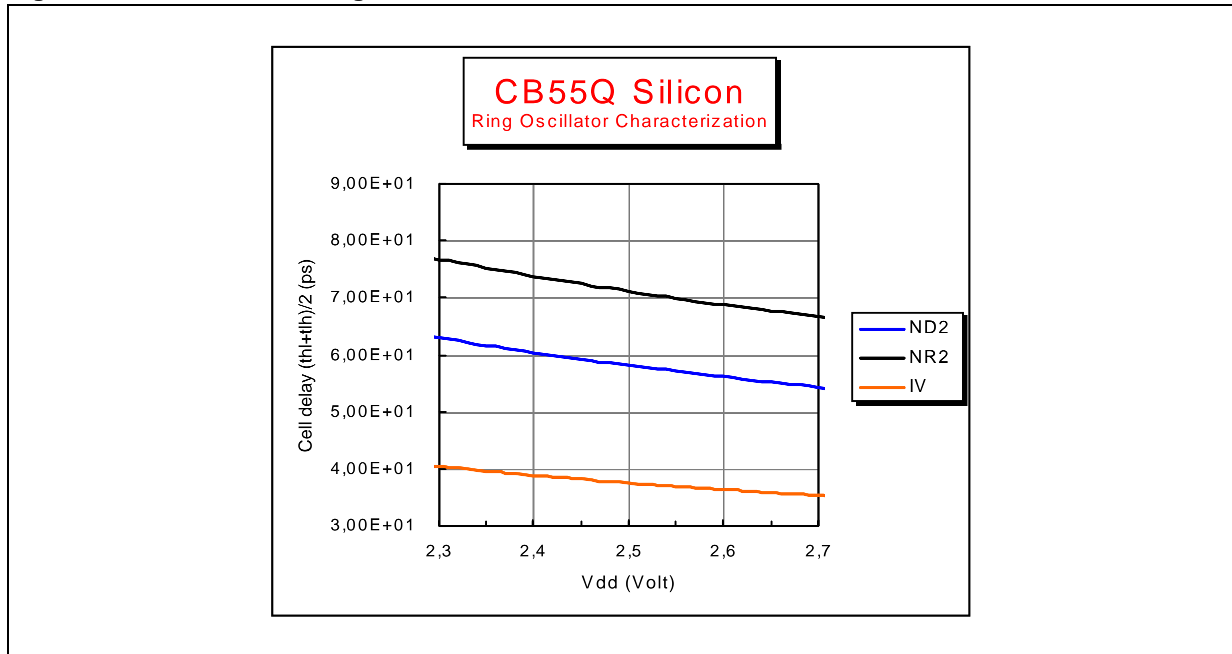


Figure 6. CB55Q Silicon ring oscillator characterization



6 PACKAGE AVAILABILITY

The CB55000 Series is designed so that it can be made compatible with all types of traditional (PLCCs, PQFPs) surface mount packages and also more advanced BGAs and Low Profile BGAs. The main packaging options include:

Plastic Leaded Chip Carriers (PLCC) up to 84 pins, Metric Quad Flat Pack (xQFP) thin and standard, up to 208 pins including high power dissipation versions with slug or spreader.

Ball Grid Array package family:

Plastic BGA, 1.27mm ball pitch	from 208 to 456 pins
High performance BGA, 1.27mm ball pitch	from 168 to 640 pins
Flip-Chip BGA, 1.27 or 1mm ball pitch	from 352 to1000 pins
Low profile BGA, 1mm ball pitch	from 144 to 256 pins
Low profile Fine pitch BGA. 8mm ball pitch	from 36 to 180 pins
Ultra Fine pitch BGA .5mm ball pitch	from 40 to 304 pins

The diversity in pin count and package style gives the designer the opportunity to find the best compromise for system size, cost and performances requirements.

Table 4. Package / pin availability

Pin Count	PLCC	TQFP 7x7	TQFP 10x10	TQFP 14x14	TQFP 20x20	TQFP 24x24	PQFP 10x10	PQFP 14x14	PQFP 14x20	PQFP 28x28	PQFP 28x28 with slug	PQFP 28x28 with spreader
20	❍											
28	❍											
44	❍		❍				❍					
48		❍										
64			❍					❍	❍			
68	❍											
80				❍					❍			
84	❍											
100				❍					❍			
120										❍	❍	❍
128										❍	❍	❍
144					❍					❍	❍	❍
160										❍	❍	❍
176						❍						
208										❍	❍	❍

7 DESIGN METHODOLOGY

STMicrolectronics (STM) ASIC design flow is intended for high performance, high complexity submicron ASIC designs. 3rd parties tools from leading EDA vendors such as Synopsys, Cadence, Mentor Graphics and STM proprietary systems are integrated into a framework free design environment that efficiently supports all design phases.

A hierarchical design methodology with a FastLoop, between floorplanning timing-driven placement and synthesis/static timing analysis, guarantees a fast timing prediction and closure after routing.

Other features such as hierarchical Clock tree synthesis, advanced test methodology, formal verification, 3D parasitic extraction, Crosstalk analysis, IP-reuse, qualifies the STM ASIC design flow as one of the industry's leading solutions for today's and tomorrow's complex designs.

8 ELECTRICAL SPECIFICATIONS

Table 5. Absolute Maximum Ratings (refer to Notes 1 and 2)

Symbol	Parameters	Value	Unit
V_{dd}	2.5 V Power Supply Voltage	-0.5 to 3.3	V
	2.5 V Input or Output Voltage	-0.5 to (V_{dd} + 0.5)	V
V_{dd}	3.3 V Power Supply Voltage	-0.5 to 4	V
	3.3 V Input or Output Voltage	-0.5 to (V_{dd3} + 0.5)	V

Notes: 1. Referenced to Vss. Stresses above those listed under "absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.
2. A dedicated 3.3 V power supply is needed for 3.3 V inputs and outputs.

Table 6. Recommended DC Operating Conditions

Main Supply Normal Range Operating Voltage V_{dd} (refer to note 1)	2.5 V +/- 10% (2.25 V to 2.75 V)
Additional Ring Supply Voltage (refer to notes 1 and 2)	3.3 V + 0.3V/-0.6 V (2.7 V to 3.6 V)
Main Supply Extended Range Operating Voltage (refer to notes 1 and 3)	2.5 V +/- 10% -28% (1.8 V to 2.75 V)
Operating Ambient Temperature Commercial (refer to note 4) Industrial (refer to note 4) Military (refer to note 5)	 0 to 70 degrees Centigrade -40 to +85 degrees Centigrade -55 to +125 degrees Centigrade

Notes: 1. Commercial, Industrial, and Military Conditions.
2. Mandatory for 3.3 V buffers only.
3. 3 V buffer specifications are not applicable for main supply below 2.25 V.
4. All circuits will operate to full specifications with a junction temperature of -40 to +125 degrees centigrade. These junction temperatures are compatible with the Commercial and Industrial Temperature Ranges.
5. All circuits will be functional from -55 to +150 degrees centigrade junction temperature (military Ambient Temperature Range) but will not necessary operate to published specifications. Only circuits specified as operational to extended temperature range may be used when operating to Military temperature conditions.

Table 7. General Interface DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Type	Max	Unit
I_{il}	Low level input current without pull-up device	$V_i = 0$ V			1[1]	µA
I_{ih}	High level input current without pull-down device	$V_i = V_{dd}$			1[1]	µA
I_{ox}	Tri-state output leakage without pull up/ down device	$V_o = 0$ V or V_{dd}			1[1]	µA
C_{in}	Input capacitance					
C_{out}	Output capacitance					
C_{io}	I/O capacitance					
$I_{latchup}$	I/O latch-up current	V < 0 V; V > V_{dd}[2]	500[3]			mA
V_{exd}	Electrostatic protection[4]	Leakage < 1 µA	4000			V

1) The leakage currents are generally very small (<1 an). The value given here, 1 µA, is the maximum that can occur after an electrostatic stress on the pin.
2) V > V_{dd3} for 3.3 V buffers.
3) V > V_{dd3} for 3.3 V buffers.
4) Human body model.

Table 8. Pull-Up and Pull-Down Characteristics

Symbol	Parameter	Conditions	Min.	Type	Max	Unit
I_{pu}	Pull-up current	$V_i = 0$ V		-50		µA
I_{pd}	Pull-down current	$V_i = V_{dd}$[1]		50		µA
R_{pu}	Equivalent pull-up resistance	$V_i = 0$ V		50		kΩ
R_{pu}	Equivalent pull-down resistance	$V_i = V_{dd}$[1]		50		kΩ

1) $V_i = V_{dd3}$ for 3.3 V buffer

8.1 2.5 V Buffer Specifications

The buffers are called “CMOS” buffers. The nominal supply voltage is 2.25 V < V_{dd} < 2.75 V. However, the specifications shown in are still valid for lower voltages.

Table 9. Low Voltage CMOS DC Input Specifications

Symbol	Parameter	Conditions	Min.	Type	Max	Unit
V_{il}	Low level threshold (input falling)	No Schmitt		0.5*V_{dd}		V
V_{ih}	High level threshold (input rising)	No Schmitt		0.5*V_{dd}		V
V_{il}	Low level input voltage	Schmitt input			0.26*V_{dd}	V
V_{ih}	High level input voltage	Schmitt input	0.7*V_{dd}			V
V_{hyst}	Schmitt trigger hysteresis	Schmitt input	0.23*V_{dd}			V
V_{ol}	Low level output voltage[1]	I_{ol} = X mA[2]			0.15*V_{dd}	V
V_{oh}	High level output voltage[(1)]	I_{oh} = -X mA[2]	0.85*V_{dd}			V

1) Takes into account 0.075*V_{dd} voltage drop in both supply lines.
2) “X” is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

2.5 V output buffers will be offered with passive slew rate control and process-compensated slew rate control. In both cases, the typical output current is that shown in Table 10.

Table 10. Slew Rate Versus Drive

Drive (mA):	**2**	**4**	**8**
Slew Rate (mA/ns Typical)	8	16	32
Active Slew Rate (mA/ns Typical)	8	16	32
Typical peak current (mA)	25	50	100

8.2 3.3 V Buffer Specifications

The 3.3 V buffers comply with the JEDEC standard 8-A (June, 1994). They are also compatible with the 74VCX DC specifications for 2.7 V to 3.6 V operation. These buffers are called “TTL”, however they also comply with Low Voltage CMOS levels. For all buffers, V_{dd}(min) = 2.25 V and V_{dd}(max) = 2.75 V (core supply).

Table 11. LVTTL and LVCMOS DC Input Specifications (2.7 V < V_{dd3} < 3.6 V)

Symbol	Parameter	Conditions	Min.	Type	Max	Unit
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2.0			V
V_{ilhyst}	Low level threshold (input falling)		0.8		1.35	V
V_{ihhyst}	High level threshold (input rising)		1.3		2.0	V
V_{hyst}	Schmitt trigger hysteresis		0.3		0.8	V

Table 12. LVTTL DC Output Specifications (3.0 V < V_{dd3} < 3.6 V)

Symbol	Parameter	Conditions	Min.	Type	Max	Unit
V_{ol}	Low level input voltage[1,2]	I_{ol} = X mA[3]			0.4	V
V_{oh}	High level input voltage[1,2]	I_{oh} = -X mA[3]	2.4			V

1) The output buffers are functional at V_{dd3} = 2.7 V, but the above specifications are not guaranteed at this voltage.
2) Takes into account a 200 mV voltage drop in both supply lines.
3) “X” is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

Table 13. LVCMOS DC Output Specifications (2.7 V < V_{dd3} < 3.6 V)

Symbol	Parameter	Conditions	Min.	Type	Max	Unit
V_{ol}	Low level input voltage	I_{ol} = 100 µA			0.2	V
V_{oh}	High level input voltage	I_{oh} = -100 µA	V_{dd3} - 0.2			V

Table 14. Slew Rate Versus Drive

Drive (mA):	**2**	**4**	**8**
Slew Rate (mA/ns Typical)	8	16	32
Typical peak current (mA)	25	50	100

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