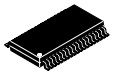
TEXAS INSTRUMENTS



SLUS502 – SEPTEMBER 2001

SBS COMPLIANT GAS GAUGE IC FOR USE WITH THE bq29311

FEATURES

- **Provides Accurate Measurement of Available Charge in Li-Ion and Li-Polymer Batteries**
- **Supports the Smart Battery Specification (SBS) V1.1**
- **Works With the TI bq29311 Protection IC to Provide Complete Pack Electronics for 10.8-V or 14.4-V Battery Packs with Few External Components**
- **Based on a Powerful Low-Power RISC CPU Core With High-Performance Peripherals**
- **Integrated FLASH Memory Eliminates the Need for External Configuration EEPROM**
- **Measures Charge Flow Using a High Resolution 15–Bit Integrating Converter**
  - **Better Than 3-nVh of Resolution**
  - **Self-Calibrating**
  - **Offset Error Less Than 1-μV**
- **Uses 15-Bit Delta Sigma Converter for Accurate Voltage, Temperature, and Current Measurements**
- **Programmable Cell Modeling for Maximum Battery Fuel Gauge Accuracy**
- **Drives 4- or 5-Segment LED Display for Remaining Capacity Indication**
- **38–pin TSSOP (DBT)**

DESCRIPTION

The bq2081 SBS Compliant gas gauge IC for battery pack or in-system installation maintains an accurate record of available charge in Li-Ion or Li-Polymer batteries. The bq2081 monitors capacity and other critical parameters of the battery pack and reports the information to the system host controller over a serial communication bus. It is designed to work with the bq29311 protection IC to maximize functionality and safety and minimize component count and cost in smart battery circuits.

The bq2081 uses an integrating converter with continuous sampling for the measurement of battery charge and discharge currents. Optimized for coloumb counting in portable applications, the self-calibrating integrating converter has a resolution better than 3-nVh and an offset measurement error of less than 1-μV (typical). For voltage, temperature, and current reporting, the bq2081 uses a 15-bit A-to-D converter. In conjunction with the bq29311, the onboard ADC also monitors individual cell voltages in a battery pack and allows the bq2081 to generate the control signals necessary to implement the required safety protection for Li-Ion and Li-Polymer battery chemistries.

The bq2081 supports the smart battery data (SBData) commands and charge control functions. It communicates data using the System Management Bus (SMBus) 2-wire protocol or the 1-wire HDQ16 protocol. The data available includes the battery's remaining capacity, temperature, voltage, current, and remaining run-time predictions. The bq2081 provides LED drivers and a push button input to depict remaining battery capacity from full to empty in 20% or 25% increments with a 4 or 5 segment display.

The bq2081 contains 512 bytes of internal FLASH EPROM, whith store configuration information. The information includes nominal capacity and voltage, self–discharge rate, rate compensation factors, and other programmable cell–modeling factors used to accurately adjust remaining capacity for use–conditions based on time, rate, and temperature. The bq2081 also automatically calibrates or learns the true battery capacity in the course of a discharge cycle from programmable near full to near empty levels.

The bq29311 protection IC provides power to the bq2081 from a 3 or 4 series Li-Ion cell stack, eliminating the need for an external regulator circuit.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL No.	I/O	DESCRIPTION
CLKOUT	35	I	32.768-kHz output to the bq29311
$\overline{\text{DISP}}$	25	I	Display control for the LED drivers LED1 through LED5
FILT	32	I	Serial memory clock for data transfer between the bq2063 and the external nonvolatile configuration memory
HDQ16	14	I/O	Serial communication open-drain bidirectional communications port
INT	17	I	Safety interrupt from the bq2081
LED1	20	O	LED display segments that each may drive an external LED
LED2	21	O	
LED3	22	O	
LED4	23	O	
LED5	24	O	
MRST	26	I	Master reset input that forces the device into reset when held high
N/C	4, 5, 7, 12, 13, 18, 36, 37	–	No connection
OC	3	I	Analog input for auto ADC offset compensation.
RBI	9	I	Register backup that provides backup potential to the bq2081 registers during periods of low operating voltage. RBI accepts a storage capacitor or a battery input.
SCLK	6	O	Communication clock to the bq29311
SDATA	10	I/O	Data transfer to and from bq29311
SMBC	15	I/O	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq2081
SMBD	16	I/O	SMBus data open-drain bidirectional pin used to transfer address and data to and from the bq2081
SR1	28	I	Connections for a small-value sense resistor to monitor the battery charge- and discharge-current flow
SR2	27	I	
TS	2	I	Thermistor voltage input connection to monitor temperature
VDDA	31	I	Positive supply for analog circuitry
VDDD	8	I	Positive supply for digital circuitry and I/O pins
VIN	1	I	Single cell voltage input from the bq29311
VSSA	30	I	Negative supply for analog circuitry
VSSD	11, 19, 38	I	Negative supply for digital circuitry
VSSP	29	I	Negative supply for output circuitry
XCK1	34	I	32.768kHz crystal oscillator input pin
XCK2	33	O	32.768kHz crystal oscillator output pin

AVAILABLE OPTIONS

PART NUMBER	PACKAGE (38-PIN TSSOP)
bq20811DBT	Standard device

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} relative to V_{SS} (see Note 1) . . . . . –0.3 V to 6 V
Open-drain I/O pins, $V_{(IOD)}$ relative to V_{SS} (see Note 1) . . . . . –0.3 V to 6 V
Input voltage range to all other pins, V_I relative to V_{SS} (see Note 1) . . . . . –0.3 V to V_{DD} + 0.3V
Operating free-air temperature range, T_A . . . . . –20°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: 1: V_{SS} refers to the common node of $V_{(SSA)}$, $V_{(SSD)}$, and V_{SS}.

electrical characteristics for V_{DD} = 3.0 V to 3.6 V, T_A = –20°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
I_{DD}	Operating current			200		µA
$I_{(SLP)}$	Low-power storage mode current			1		µA
$VI_{(OLS)}$	Output voltage low: (LED1–LED5)	$I_{(OLS)}$ = 10 mA			0.4	V
$V_{(IL)}$	Input voltage low $\overline{DISP}$		–0.3		0.8	V
V_{IH}	Input voltage high $\overline{DISP}$		2		V_{CC} + 0.3	V
V_{OL}	Output voltage low SMBC, SMBD, HDQ16, SDATA, SCLK	I_{OL} = 0.5 mA			0.4	V
$V_{(ILS)}$	Input voltage low SMBC, SMBD, HDQ16, SDATA, SCLK		–0.3		0.8	V
$V_{(IHS)}$	Input voltage high SMBC, SMBD, HDQ16, SDATA, SCLK		1.7		6	V
$V_{(AI)}$	Input voltage range VIN, TS, OC		V_{SS} – 0.3		1.0	V
$I_{(RB)}$	RBI data-retention input current	$V_{(RBI)}$ > 3 V, V_{CC} < 2.5 V		10	50	nA
$V_{(RBI)}$	RBI data-retention voltage		1.3			V
$Z_{(AI1)}$	Input impedance SR1, SR2	0 V–1.0 V	10			MΩ
$Z_{(AI2)}$	Input impedance VIN, TS, OC	0 V–1.0 V	8			MΩ

integrating ADC characteristics, V_{DD} = 3.0 V to 3.6 V, T_A= –20°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SR)}$	Input voltage range, $V_{(SR2)}$ and $V_{(SR1)}$	$V_{SR} = V_{(SR2)} - V_{(SR1)}$	–0.3		1.0	V
$V_{(SROS)}$	Input offset			1		µV
INL	Integral nonlinearity error			0.003%	0.009%	

PRODUCT PREVIEW

SMBus timing specifications, T_A = –20°C to 70°C, 3.0 V < V_{DD} < 3.6 V (unless other noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
F_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
T_{BUF}	Bus free time between start and stop		4.7			µs
$T_{HD:STA}$	Hold time after (repeated) start		4.0			µs
$T_{SU:STA}$	Repeated start setup time		4.7			µs
$T_{SU:STO}$	Stop setup time		4.0			µs
$T_{HD:DAT}$	Data hold time	Receive mode	0			µs
		Transmit mode	300			
$T_{SU:DAT}$	Data setup time		250			µs
$T_{TIMEOUT}$	Error signal/detect	See Note 1	25		35	ms
T_{LOW}	Clock low period		4.7			µs
T_{HIGH}	Clock high period	See Note 2	4.0		50	µs
$T_{LOW:SEXT}$	Cumulative clock low slave extend time	See Note 3			25	ms
$T_{LOW:MEXT}$	Cumulative clock low master extend time	See Note 4			10	ms
T_F	Clock/data fall time	See Note 5			300	ns
T_R	Clock/data rise time	See Note 6			1000	ns

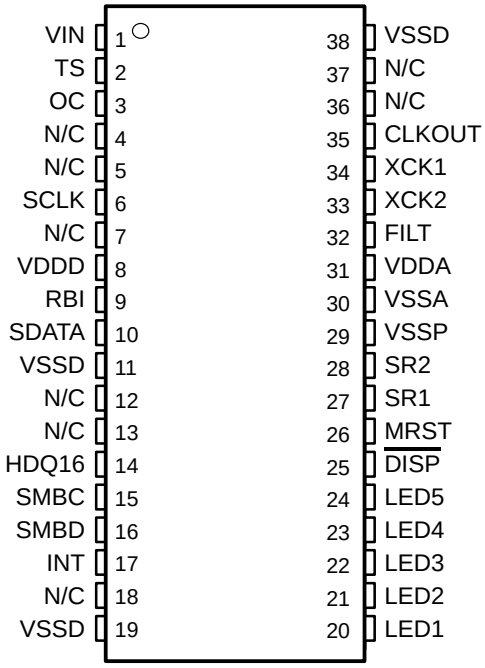
NOTES: 1. The bq2081 times out when any clock low exceeds $T_{TIMEOUT}$
2. T_{HIGH} Max. is minimum bus idle time. SMBC = SMBD = 1 for t > 50 µs causes reset of any transaction involving bq2081 that is in progress.
3. $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
4. $T_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
5. Rise time T_R = (V_{ILMAX} – 0.15 V) to (V_{IHMIN} + 0.15 V).
6. Fall time T_F = 0.9 V_{DD} to (V_{ILMAX} – 0.15 V).

HDQ timing characteristics, T_A = –20°C to 70°C, 3.0 V < V_{DD} < 3.6 V (unless otherwise noted)

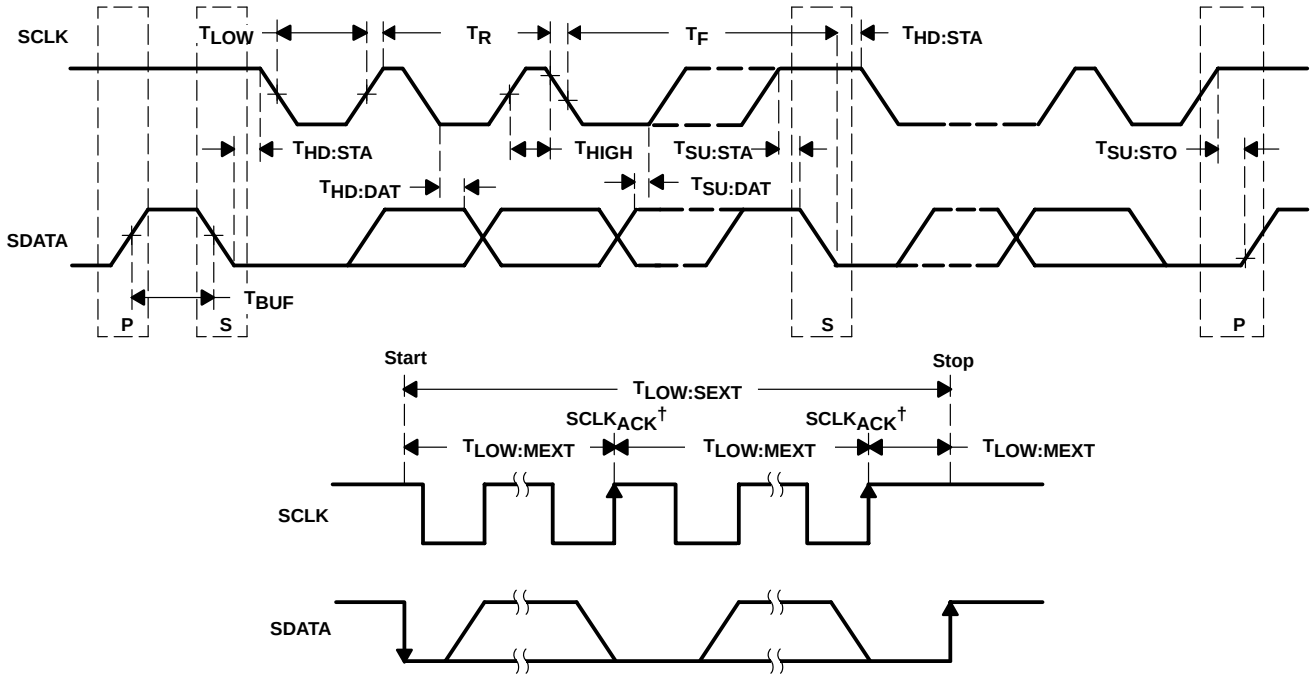
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(CYCH)}$	Cycle time, host to bq2081 (write)		190			µs
$t_{c(CYCB)}$	Cycle time, bq2081 to host (read)		190	205	250	µs
$t_{h(STRH)}$	Start hold time, host to bq2081 (write)		5			ns
$t_{h(STRB)}$	Start hold time, host to bq2081 (read)		32			µs
$t_{su(DSU)}$	Data setup time				50	µs
$t_{su(DSUB)}$	Data setup time				50	µs
$t_{h(DH)}$	Data hold time		100			µs
$t_{(DV)}$	Data valid time		80			µs
$t_{su(SSU)}$	Stop setup time				145	µs
$t_{su(SSUB)}$	Stop setup time				145	µs
$t_{(RSPS)}$	Response time, bq2081 to host		190		320	µs
$t_{(B)}$	Break time		190			µs
$t_{(BR)}$	Break recovery time		40			µs

Figures 6–9 are timing diagrams for the bq2081 .

TSSOP PACKAGE
(TOP VIEW)



SMBus timing diagrams



† $SCLK_{ACK}$ is the acknowledge–related clock pulse generated by the master.

Figure 1. SMBus Timing Diagram

PRODUCT PREVIEW

HDQ timing diagrams

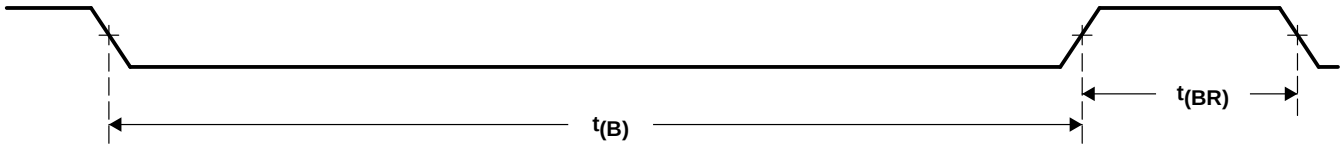


Figure 2. HDQ Break Timing

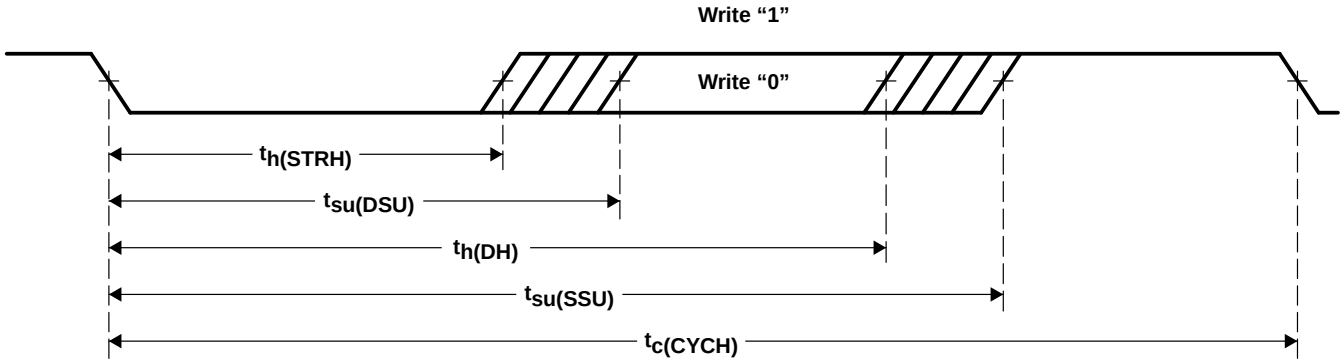


Figure 3. HDQ Host to bq2081

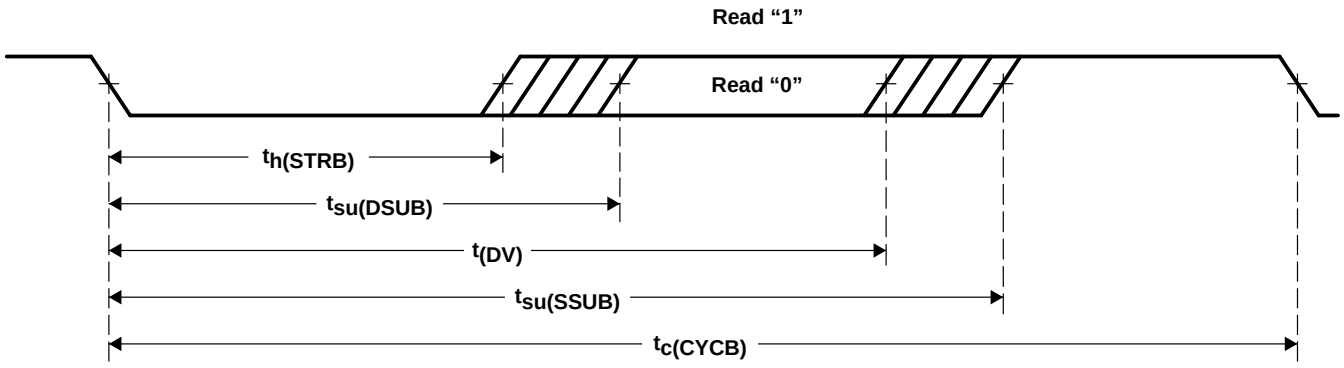
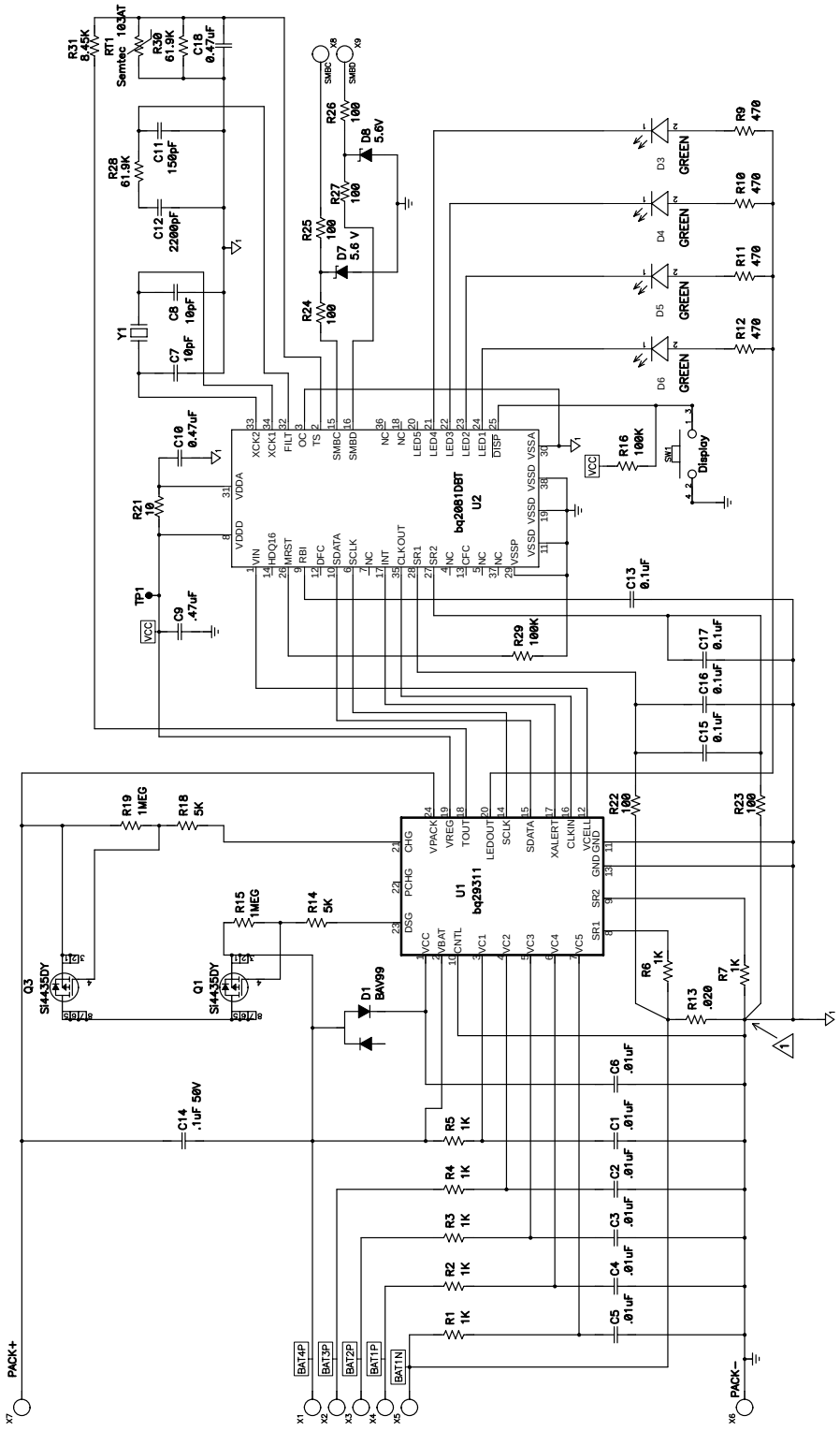


Figure 4. HDQ bq2081 to Host

APPLICATION INFORMATION

typical application



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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265