

**Preliminary Technical Data**
**AD8677**
**FEATURES**

- Low Offset Voltage: 75  $\mu$ V Max
- Input Offset Drift: 1.2  $\mu$ V/ $^{\circ}$ C Max
- Low Noise: 0.6 $\mu$ Vp-p max
- High Gain, CMRR and PSRR: 110 dB min
- Low Supply Current: 1.2 mA
- Wide Supply Voltage Range:  $\pm$ 5V to  $\pm$ 15V Operation

**APPLICATIONS**

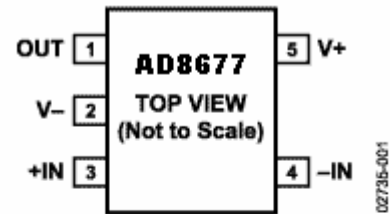
- Medical & Industrial Instrumentation
- Sensors & Controls
  - Thermocouple
  - RTDs
  - Strain Bridges
  - Shunt Current Measurements
- Precision Filters

**GENERAL DESCRIPTION**

The AD8677 is the next generation of precision, ultra-low offset amplifiers. It builds on the high performance of the OP07 and integrates lower power (1.2 mA typ), low input bias current ( $\pm$ 2 nA max) and higher CMRR/PSRR (130dB) in the small TSOT23 package. Operation is fully specified from  $\pm$ 5 V to  $\pm$ 15 V supply.

The AD8677 provides higher accuracy than industry standard OP07-type amplifiers due to Analog Devices' iPolar™ process that supports enhanced performance in a smaller footprint. These performance enhancements include wider output swing, lower power and higher CMRR and PSRR. The AD8677 maintains stability of offsets and gain virtually regardless of variations in time or temperature. Excellent linearity and gain accuracy can be maintained at high closed-loop gains.

The AD8677 is fully specified over the extended industrial ( $-40^{\circ}$  to  $+125^{\circ}$ C) temperature range. The AD8677 amplifier is available in the tiny 5-lead TSOT-23 and the popular 8-pin narrow SOIC lead-free packages.


**5-Lead TSOT (UJ-5)**

**NC = NO CONNECT**
**8-Lead SOIC (R-8)**

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## ELECTRICAL SPECIFICATIONS

( $V_S = \pm 5.0V$ ,  $T_A = +25^\circ C$  unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$			30	75	$\mu V$
Input Bias Current	$I_B$			$\pm 0.5$	$\pm 2$	nA
		$-40^\circ C \leq T_A \leq +125^\circ C$			$\pm 5$	nA
Input Offset Current	$I_{OS}$			0.5	3.8	nA
		$-40^\circ C \leq T_A \leq +125^\circ C$			TBD	nA
Input Voltage Range			-3.5		3.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 3V$	110	130		dB
		$-40^\circ C \leq T_A \leq +125^\circ C$	TBD	TBD		dB
Open Loop Gain (Note 1)	$A_{VO}$	$R_L = 2 k\Omega$ to Ground, $V_O = \pm 3V$	114	TBD		dB
		$-40^\circ C \leq T_A \leq +125^\circ C$	TBD	TBD		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ C \leq T_A \leq +125^\circ C$		0.5	1.2	$\mu V/^\circ C$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OUT}$	$R_L = 10k\Omega$ to Ground	$\pm 3.9$	$\pm 4$		V
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		V
		$R_L = 2k\Omega$ to Ground	$\pm 3.4$	$\pm 3.5$		V
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		V
Short Circuit Limit	$I_{SC}$			30		mA
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		mA
Output Current	$I_O$	$V_O = 3.5V$		10		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.0V$ to $\pm 18.0V$	110	TBD		dB
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0V$		1.2	1.4	mA
		$-40^\circ C \leq T_A \leq +125^\circ C$			TBD	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10k\Omega$		0.2		V/ $\mu s$
Overload Recovery Time				TBD		ms
Gain Bandwidth Product	GBP			0.6		MHz
Phase Margin				80		degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n\ p-p}$	0.1 to 10 Hz		0.35	0.6	$\mu V_{p-p}$
Voltage Noise Density	$e_n$	$f = 1\ kHz$		11	TBD	nV/ $\sqrt{Hz}$
Current Noise Density	$i_n$	$f = 10\ Hz$		0.17		pA/ $\sqrt{Hz}$

## ELECTRICAL SPECIFICATIONS ( $V_S = \pm 15V$ , $T_A = +25^\circ C$ unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$			30	75	$\mu V$
Input Bias Current	$I_B$			$\pm 0.5$	$\pm 2.0$	nA
Input Offset Current	$I_{OS}$	$-40^\circ C \leq T_A \leq +125^\circ C$			$\pm 5$	nA
		$-40^\circ C \leq T_A \leq +125^\circ C$		0.5	3.8	nA
Input Voltage Range			-13.5		+13.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	130		dB
		$-40^\circ C \leq T_A \leq +125^\circ C$	TBD	TBD		dB
Open Loop Gain	$A_{VO}$	$R_L = 2k\Omega$ to Ground, $V_O = \pm 11V$	114	TBD		dB
		$-40^\circ C \leq T_A \leq +125^\circ C$	TBD			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ C \leq T_A \leq +125^\circ C$		0.5	1.2	$\mu V/^\circ C$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage Swing	$V_{OUT}$	$R_L = 10k\Omega$ to Ground	$\pm 13.9$	$\pm 14$		V
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		V
		$R_L = 2k\Omega$ to Ground	$\pm 13.4$	$\pm 13.5$		V
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		V
Short Circuit Limit	$I_{SC}$			30		mA
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		mA
Output Current	$I_O$	$V_O = 13.5V$		10		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.0V$ to $\pm 18.0V$	110	TBD		dB
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0V$		1.2	1.4	mA
		$-40^\circ C \leq T_A \leq +125^\circ C$		TBD	TBD	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10k\Omega$		0.2		V/ $\mu s$
Overload Recovery Time				TBD		ms
Gain Bandwidth Product	GBP			0.6		MHz
Phase Margin				80		degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n p-p}$	0.1 to 10 Hz		0.35	0.6	$\mu V_{p-p}$
Voltage Noise	$e_{n p-p}$	0.1 to 1.0 Hz		0.6		$\mu V_{p-p}$
Voltage Noise Density	$e_n$	$f = 1 kHz$		11		nV/ $\sqrt{Hz}$
Current Noise Density	$i_n$	$f = 10 Hz$		0.17		pA/ $\sqrt{Hz}$

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	$\pm 18V/+36V$
Input Voltage .....	$\pm V_{\text{supply}}$
Differential Input Voltage .....	$\pm 30V$
Output Short-Circuit Duration to Gnd .....	Indefinite
Storage Temperature Range	
UJ, R Package.....	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	
AD8677 .....	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Junction Temperature Range	
UJ, R Package.....	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 10 sec) .....	$+300^{\circ}\text{C}$

Package Type	$\theta_{JA}^1$	$\theta_{JC}$	Units
5-Pin TSOT23 (UJ-5)	207	61	$^{\circ}\text{C}/\text{W}$
8-Pin SOIC (R-8)	158	43	$^{\circ}\text{C}/\text{W}$

## NOTES

<sup>1</sup>  $\theta_{JA}$  is specified for the worst case conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for P-DIP packages;  $\theta_{JA}$  is specified for device soldered in circuit board for SOIC and TSSOP packages.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8677AUJZ	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	5-Lead TSOT-23	UJ-5
AD8677ARZ	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8-Lead SOIC	R-8