



LC74772V

Camcorder On-Screen Display LSI

Overview

The LC74772V is a CMOS LSI that implements on-screen display for camcorders. It displays characters and patterns in a camcorder viewfinder under microprocessor control. The LC74772V displays a 12 × 18 dot font with 256 characters.

Features

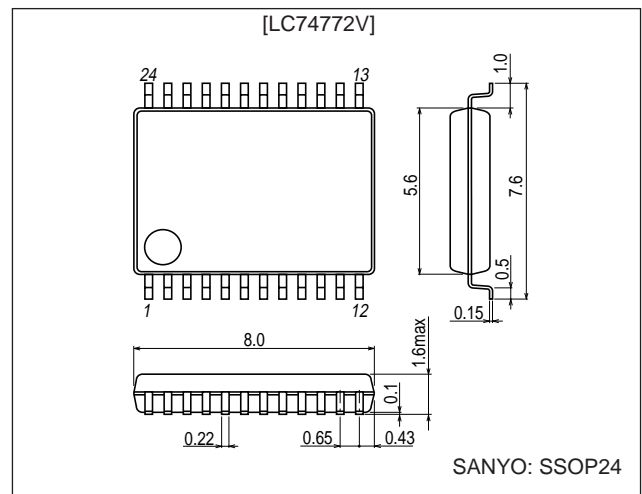
- Screen format: 12 lines × 24 characters (up to 288 characters)
- Number of characters displayed: Up to 288 characters
- Character format: 12 (horizontal) × 18 (vertical) dots
- Number of characters in font: 256 characters
- Character sizes: Normal and double, specified in line units
- Display start position
 - Horizontal: 64 positions
 - Vertical: 64 positions
- Character reverse video function: Individual characters can be displayed in reverse video.
- Types of blinking: Two types with periods of 1.0 and 0.5 seconds, specifiable on a per character basis. (Blinking has a 60% display on duty.)
(Four divisors: 1/25, 1/30, 1/50, 1/60)

- Outputs: R, G, B plus 2 output systems
Or: 4 output systems (character data and blanking data: 4 outputs each)
- External control input: 8-bit serial data input format.

Package Dimensions

unit: mm

3175A-SSOP24



Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|-----------|--|----------------------------------|------|
| Supply voltage | V_{DD} | V_{DD} | $V_{SS} - 0.3$ to $V_{SS} + 7.0$ | V |
| Input voltage | V_{IN} | All input pins | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Output voltage | V_{OUT} | CK _{OUT} , CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Allowable power dissipation | Pd max | Ta = 25°C | 300 | mW |
| Operating temperature | Topr | | -30 to +70 | °C |
| Storage temperature | Tstg | | -40 to +125 | °C |

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC74772V

Allowable Operating Ranges at Ta = -30 to +70°C

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--------------------------|------------------|--|-----------------------|-----|-----------------------|------|
| | | | min | typ | max | |
| Supply voltage | V _{DD} | V _{DD} | 2.7 | 5.0 | 5.5 | V |
| Input high-level voltage | V _{IH} | CTRL1, TEST _{IN} , $\overline{\text{CS}}$, SCLK, SIN, OUT _{MOD} , $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{RST}}$ | 0.8 V _{DD} | | V _{DD} + 0.3 | V |
| Input low-level voltage | V _{IL} | CTRL1, TEST _{IN} , $\overline{\text{CS}}$, SCLK, SIN, OUT _{MOD} , $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{RST}}$ | V _{SS} - 0.3 | | 0.2 V _{DD} | V |
| Oscillator frequency | F _{OSC} | OSC _{IN} , OSC _{OUT} (LC oscillator) | 6 | (8) | 10 | MHz |

Electrical Characteristics at Ta = -30 to +70°C, unless otherwise specified V_{DD} = 5 V

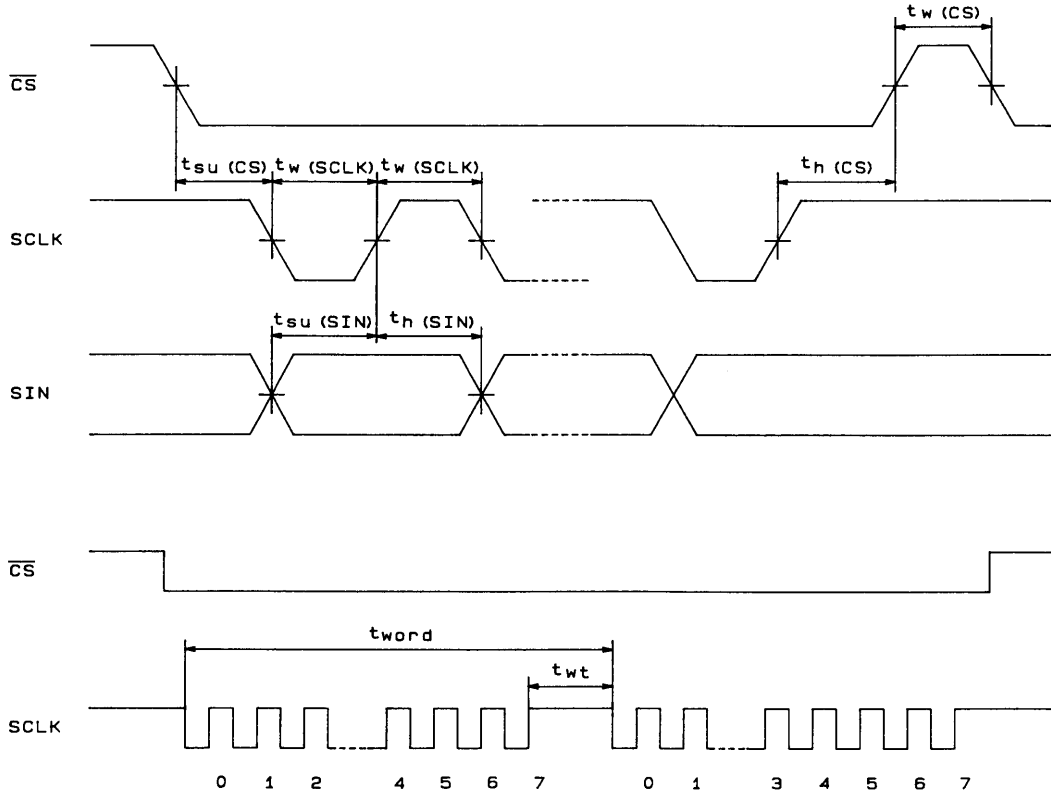
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|-----------------|--|---------------------|-----|---------------------|------|
| | | | min | typ | max | |
| Output high-level voltage | V _{OH} | CK _{OUT} , CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK: V _{DD} = 5.5 to 4.5 V (V _{DD} = 4.4 to 2.7 V), I _{OH} = -1.0 mA (-0.5 mA) | 0.9 V _{DD} | | | V |
| Output low-level voltage | V _{OL} | CK _{OUT} , CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK: V _{DD} = 5.5 to 4.5 V (V _{DD} = 4.4 to 2.7 V), I _{OL} = 1.0 mA (0.5 mA) | | | 0.1 V _{DD} | V |
| Input current | I _{IH} | CTRL1, TEST _{IN} , $\overline{\text{CS}}$, SCLK, SIN, OUT _{MOD} , $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$: V _{IN} = V _{DD} | | | 1 | μA |
| | I _{IL} | CTRL1, TEST _{IN} , $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$: V _{IN} = V _{SS} | -1 | | | μA |
| Operating current drain | I _{DD} | V _{DD} pin; all outputs open, LC oscillator: 8 MHz | | | 10 | mA |

Timing Characteristics at Ta = -30 to +70°C, V_{DD} = 5 ± 0.5 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|----------------------|---|---------|-----|-----|------|
| | | | min | typ | max | |
| Minimum input pulse width | t _{W(SCLK)} | SCLK | 200 | | | ns |
| | t _{W(CS)} | $\overline{\text{CS}}$ (the period that $\overline{\text{CS}}$ is high) | 1 | | | μs |
| Data setup time | t _{SU(CS)} | $\overline{\text{CS}}$ | 200 | | | ns |
| | t _{SU(SIN)} | SIN | 200 | | | ns |
| Data hold time | t _{H(CS)} | $\overline{\text{CS}}$ | 2 | | | μs |
| | t _{H(SIN)} | SIN | 200 | | | ns |
| One-word write time | t _{word} | The time to write 8 bits of data | 4.2 | | | μs |
| | t _{wt} | The RAM data write time | 1 | | | μs |

LC74772V

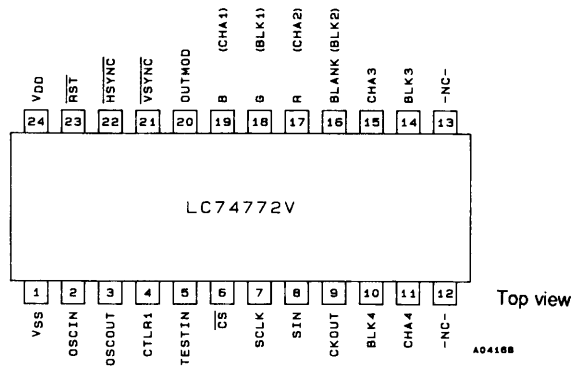
Serial Data Input Timing



A04169

Pin Assignment

The signal names in parentheses indicate the output pin functions when 4-system output mode is used.



A04168

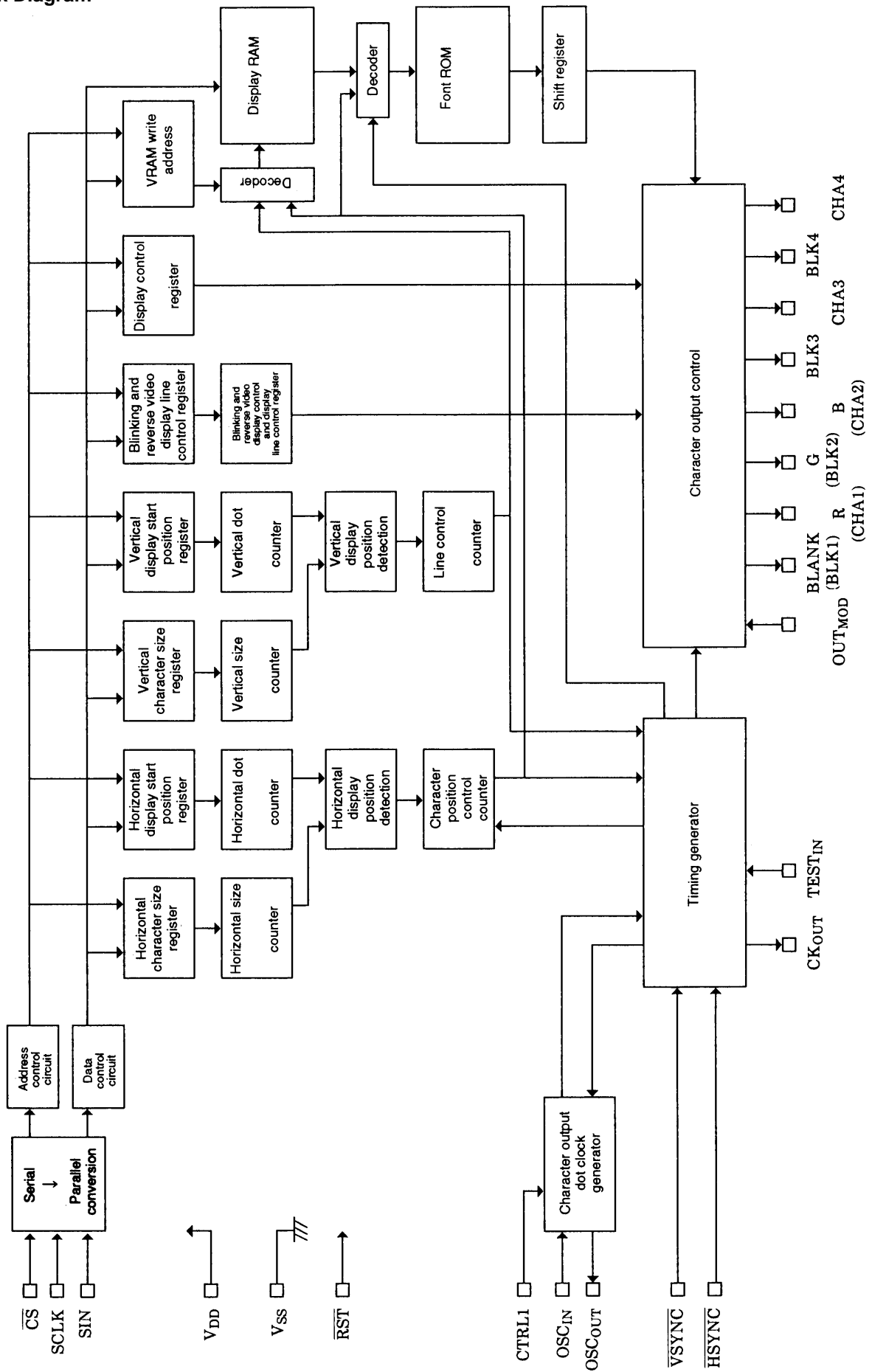
LC74772V

Pin Functions

| PinNo. | Symbol | Function | Description |
|--------|---------------------------|-------------------------------------|--|
| 1 | V _{SS} | Ground | Ground connection |
| 2 | OSC _{IN} | LC oscillator | Connections for the coil and capacitor that form the oscillator that generates the character output horizontal dot clock. |
| 3 | OSC _{OUT} | | |
| 4 | CTRL1 | Clock input control | Control input that switches between LC oscillator mode and clock input mode Low: LC oscillator mode, high: clock input mode |
| 5 | TEST _{IN} | Test control input | Test mode control input (The IC operates in test mode when this input is high.) |
| 6 | $\overline{\text{CS}}$ | Enable input | Serial data input enable input Low: active (This input has hysteresis characteristics.) |
| 7 | SCLK | Clock input | Serial data input clock input (This input has hysteresis characteristics.) |
| 8 | SIN | Data input | Serial data input (This input has hysteresis characteristics.) |
| 9 | CK _{OUT} | Clock output | LC oscillator clock monitor output This signal is output when $\overline{\text{RST}}$ is low. |
| 10 | BLK4 | Blanking signal output | Blanking signal output (system 2) Functions as the system 4 blanking data signal output in 4-system mode. |
| 11 | CHA4 | Character data output | Character data signal output (system 2) Functions as the system 4 character data signal output in 4-system mode. |
| 12 | NC | Unused | Must be left open or tied to ground in normal operation. |
| 13 | NC | Unused | Must be left open or tied to ground in normal operation. |
| 14 | BLK3 | Blanking signal output | Blanking signal output (system 1) Functions as the system 3 blanking data signal output in 4-system mode. |
| 15 | CHA3 | Character data output | Character data signal output (system 1) Functions as the system 3 character data signal output in 4-system mode. |
| 16 | BLANK | Blanking signal output | Blanking signal output (blanking signal for RGB output) Functions as the system 2 blanking data signal output in 4-system mode. |
| 17 | R | Character data output | Character data (R) signal output Functions as the system 2 character data signal output in 4-system mode. |
| 18 | G | Character data output | Character data (G) signal output Functions as the system 1 blanking data signal output in 4-system mode. |
| 19 | B | Character data output | Character data (B) signal output Functions as the system 1 character data signal output in 4-system mode. |
| 20 | OUT _{MOD} | Output control input | Control input that switches between RGB output and 4-system output Low: RGB output, high 4-system output |
| 21 | $\overline{\text{VSYNC}}$ | Vertical synchronizing signal input | Vertical synchronizing signal input (This input has hysteresis characteristics.) |
| 22 | $\overline{\text{HSYNC}}$ | Horizontal synchronizing | Horizontal synchronizing signal input (This input has hysteresis characteristics.) signal input |
| 23 | $\overline{\text{RST}}$ | Reset input | System reset signal input (This input has hysteresis characteristics.) |
| 24 | V _{DD} | Power supply | Power supply connection (+5 V) |

Note: 1. Built-in pull-up resistors can be specified for inclusion in the $\overline{\text{CS}}$ (pin 6), SCLK (pin 7), SIN (pin 8), and $\overline{\text{RST}}$ (pin 23) pins as mask options.
2. In clock input mode (when CTRL1 is high), the function that holds the OSC_{IN} (pin 2) pin high during an oscillator reset is stopped.

Block Diagram



Display Control Commands

The display control commands have an 8-bit serial input format. Data is input LSB first.

Display Control Command Table

| Command | First byte | | | | | | | | Second byte | | | | | | | |
|---|--------------|----|----|-----|--------------|--------------|-------------|-------------|-------------|------------|------------|------------|------------|------------|------------|------------|
| | Command code | | | | Data | | | | Data | | | | | | | |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| COMMAND 0 System setup 1 | 0 | 0 | 0 | 0 | RST SYS | RAM CLR | OSC STP | TST MOD | — | — | — | — | — | — | — | — |
| COMMAND 1 System setup 2 | 0 | 0 | 0 | 1 | CSYN MOD | CLK POLT | CLK MOD1 | CLK MOD0 | — | — | — | — | — | — | — | — |
| COMMAND 2 Input control setup | 0 | 0 | 1 | 0 | VSYN POLT | HSYN POLT | DATA FMT | ART FMT | — | — | — | — | — | — | — | — |
| COMMAND 3 General-purpose port control | 0 | 0 | 1 | 1 | PORT SET | OUT P11 | OUT P10 | OUT P9 | — | — | — | — | — | — | — | — |
| COMMAND 4 Display operation control: reverse video and blinking | 0 | 1 | 0 | 0 | RVS ON | BLK ON | BLK 1 | BLK 0 | — | — | — | — | — | — | — | — |
| COMMAND 5 Display control: on/off settings for each output | 0 | 1 | 0 | 1 | DSP 4 | DSP 3 | DSP 2 | DSP 1 | — | — | — | — | — | — | — | — |
| COMMAND 6 Output control: systems 3 and 4 | 0 | 1 | 1 | 0 | DSPF SL34 | DSP RSG | DSP GSG | DSP BSG | — | — | — | — | — | — | — | — |
| COMMAND 8 Display control: border | 1 | 0 | 0 | 0 | 0 | BKC R | BKC G | BKC B | BKO4 F1 | BKO4 F0 | BKO3 F1 | BKO3 F0 | BKO2 F1 | BKO2 F0 | BKO1 F1 | BKO1 F0 |
| COMMAND 9 Display start position | 1 | 0 | 0 | 1 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 |
| COMMAND 10 Display line control | 1 | 0 | 1 | 0 | LN SZ | LN OT4 | LN OT3 | LN SEL | 0 | 0 | LIN 126 | LIN 115 | LIN 104 | LIN 93 | LIN 82 | LIN 71 |
| COMMAND 11 RAM write address | 1 | 0 | 1 | 1 | VADR 3 | VADR 2 | VADR 1 | VADR 0 | 0 | 0 | 0 | HADR 4 | HADR 3 | HADR 2 | HADR 1 | HADR 0 |
| COMMAND 14 Display RAM setup data | 1 | 1 | 1 | BLK | RV | R | G | B | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |

①

②

① Command code: (These 4 bits in the first byte identify the command.)

Command 14 is recognized by the upper 3 bits.

② Command data: (These bits specify the data for each command.)

- For commands 0 through 7, 8 bits of data are read in.
- For commands 8 through 14, 16 bits of data are read in.
- If the command 2 data-1 bit (DATAFMT) was set to 1, after the first byte of a command 14 is read in, the system goes to continuous transfer mode for reading in a series of following bytes.

Note: 1. If the \overline{CS} pin is set high, the command state is set to the command 0 (system control setup) state.

2. If a system reset is executed from the RST pin or by a command reset, the command register is set to 0.

① COMMAND 0 (System control setup 1)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|---|---|
| | | State | Function | |
| 7 | — | 0 | Command 0 identification code | |
| 6 | — | 0 | | |
| 5 | — | 0 | | |
| 4 | — | 0 | | |
| 3 | RST SYS | 0 | Normal operation | If \overline{CS} is low, the reset is executed, but if \overline{CS} is high this command will be excluded. |
| | | 1 | System reset | |
| 2 | RAM CLR | 0 | Normal operation | The VRAM clear operation is not executed when the oscillator is stopped. |
| | | 1 | Normal operation VRAM clear (All data is set to FE (hexadecimal)) | |
| 1 | OSC STP | 0 | The LC oscillator operating state is maintained. | Valid when the display is off. VRAM write is not possible when the oscillator is stopped. |
| | | 1 | The LC oscillator is stopped. | |
| 0 | TST MOD | 0 | Normal operation | Illegal setting. This bit must always be set to 0. |
| | | 1 | Test mode | |

Note: This register is set to 0 on a reset (either by the \overline{RST} pin or by a command reset).

Notes on command settings

- RSTSYS:** A command reset is executed immediately after the data is read.
The reset is cleared by returning the \overline{CS} pin to high to reset this register. The reset is also cleared if this command is executed consecutively or if this register is set to 0.
- RAMCLR:** The RAM can only be erased when display is off. This operation is not executed during display. This operation cannot be executed if the LC oscillator is stopped. Only use this command when the LC oscillator is operating.

 - This command bit is automatically cleared when the RAM erase operation completes.
 - Once the RAM erase command has been read in, the following time is required to complete the operation.
— $T_{clear} = 5 [\mu s] + 4/f_{OSC} (LC\text{-oscillator}) \times 288$
- OSCSTP:** The LC oscillator stop command stops the LC oscillator connected to pins 2 and 3 (OSC_{IN} and OSC_{OUT}). The oscillator stop command is only executed when display is off. It is not executed if display is in progress.

 - In external clock input mode, this command stops the acquisition of that clock signal.
- TSTMOD:** The test mode command is executed if the $TEST_{IN}$ pin (pin 5) is high. This command should not be used by applications in normal operation.

LC74772V

② COMMAND 1 (System control setup 2)

First byte

| DA0 to DA7 | Register name | Register content | | | Note | | | | | | | | | | | | | | | |
|------------|---------------|---------------------|--|-----------|--|------|-----------|---|---|--------------------|---|---|---------------------|---|---|--------------------|---|---|-------------------|---|
| | | State | Function | | | | | | | | | | | | | | | | | |
| 7 | — | 0 | Command 1 identification code | | | | | | | | | | | | | | | | | |
| 6 | — | 0 | | | | | | | | | | | | | | | | | | |
| 5 | — | 0 | | | | | | | | | | | | | | | | | | |
| 4 | — | 1 | | | | | | | | | | | | | | | | | | |
| 3 | CSYN MOD | 0 | HSYNC (pin 22) functions as the horizontal synchronizing signal input | | The VSYNC pin (pin 21) must be tied to ground or V _{DD} in composite synchronizing signal input mode. | | | | | | | | | | | | | | | |
| | | 1 | HSYNC (pin 22) functions as the composite synchronizing signal input | | | | | | | | | | | | | | | | | |
| 2 | CLK POLT | 0 | The system clock has a positive polarity. | | This sets the clock polarity for system operation when pin 2 is used as a clock input. | | | | | | | | | | | | | | | |
| | | 1 | The system clock has a negative polarity. | | | | | | | | | | | | | | | | | |
| 1 | CLK MOD1 | 0 | <table border="1" style="width: 100%;"> <thead> <tr> <th>MOD1</th> <th>MOD0</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LC oscillator mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>Clock input (1 dot)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Clock input (NTSC)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Clock input (PAL)</td> </tr> </tbody> </table> | | MOD1 | MOD0 | Operation | 0 | 0 | LC oscillator mode | 0 | 1 | Clock input (1 dot) | 1 | 0 | Clock input (NTSC) | 1 | 1 | Clock input (PAL) | Valid when the CTRL1 pin (pin 4) is high. The input clock frequency in clock input mode is either 4fsc or the dot clock frequency. |
| | | MOD1 | MOD0 | Operation | | | | | | | | | | | | | | | | |
| 0 | 0 | LC oscillator mode | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Clock input (1 dot) | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Clock input (NTSC) | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Clock input (PAL) | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | |
| 0 | CLK MOD0 | 0 | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | |

③ COMMAND 2 (Input control)

First byte

| DA0 to DA7 | Register name | Register content | | | Note |
|------------|---------------|------------------|--|--|--|
| | | State | Function | | |
| 7 | — | 0 | Command 2 identification code | | |
| 6 | — | 0 | | | |
| 5 | — | 1 | | | |
| 4 | — | 0 | | | |
| 3 | VSYN POLT | 0 | The vertical synchronizing signal input polarity is low active. | | Sets the pin 21 (VSYNC) signal input polarity. |
| | | 1 | The vertical synchronizing signal input polarity is high active. | | |
| 2 | HSYN POLT | 0 | The horizontal synchronizing signal input polarity is low active. | | Sets the pin 22 (HSYNC) signal input polarity. |
| | | 1 | The horizontal synchronizing signal input polarity is high active. | | |
| 1 | DATA FMT | 0 | Data is transferred in 16-bit units. | | Sets the COMMAND 14 data transfer format. |
| | | 1 | Continuous transfers with the upper 8 bits input first and then the lower 8 bits | | |
| 0 | ATR FMT | 0 | RV specifies the reverse video display function. | | COMMAND-14 Data 11: Valid in RV RGB output mode. |
| | | 1 | RV specifies system 3 output control. | | |

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

LC74772V

④ COMMAND 3 (General-purpose port control)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|--|--|
| | | State | Function | |
| 7 | — | 0 | Command 3 identification code | |
| 6 | — | 0 | | |
| 5 | — | 1 | | |
| 4 | — | 1 | | |
| 3 | PORT SET | 0 | System 4 functions as a normal character and border outputs. | Controls the pin 10 (BLK4) and pin 11 (CHA4) outputs. |
| | | 1 | System 4 functions as general-purpose ports. | |
| 2 | OUT P11 | 0 | The pin 11 output is set to low. | Sets the output when PORTSET is set to 1. |
| | | 1 | The pin 11 output is set to high. | |
| 1 | OUT P10 | 0 | The pin 10 output is set to low. | Sets the output when PORTSET is set to 1. |
| | | 1 | The pin 10 output is set to high. | |
| 0 | OUT P9 | 0 | The pin 9 output is set to low. | Sets the output for pin 9 during normal operation (other than during a reset). |
| | | 1 | The pin 9 output is set to high. | |

⑤ COMMAND 4 (Display control: reverse video and blinking)

First byte

| DA0 to DA7 | Register name | Register content | | | Note | | | | | | | | | | | | | | | |
|------------|---------------|----------------------|---|--|------|-----------|-----------|---|---|---------------------|---|---|----------------------|---|---|---------------------|---|---|----------------------|--|
| | | State | Function | | | | | | | | | | | | | | | | | |
| 7 | — | 0 | Command 4 identification code | | | | | | | | | | | | | | | | | |
| 6 | — | 1 | | | | | | | | | | | | | | | | | | |
| 5 | — | 0 | | | | | | | | | | | | | | | | | | |
| 4 | — | 0 | | | | | | | | | | | | | | | | | | |
| 3 | RVS ON | 0 | — | | | | | | | | | | | | | | | | | |
| | | 1 | Characters for which the attribute is specified are displayed in reverse video. | | | | | | | | | | | | | | | | | |
| 2 | BLK ON | 0 | — | | | | | | | | | | | | | | | | | |
| | | 1 | Characters for which the attribute is specified are displayed blinking. | | | | | | | | | | | | | | | | | |
| 1 | BLK1 | 0 | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>BLK1</th> <th>BLK0</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>V × 25 (PAL: 0.5 s)</td> </tr> <tr> <td>0</td> <td>1</td> <td>V × 30 (NTSC: 0.5 s)</td> </tr> <tr> <td>1</td> <td>0</td> <td>V × 50 (PAL: 1.0 s)</td> </tr> <tr> <td>1</td> <td>1</td> <td>V × 60 (NTSC: 1.0 s)</td> </tr> </tbody> </table> | | BLK1 | BLK0 | Operation | 0 | 0 | V × 25 (PAL: 0.5 s) | 0 | 1 | V × 30 (NTSC: 0.5 s) | 1 | 0 | V × 50 (PAL: 1.0 s) | 1 | 1 | V × 60 (NTSC: 1.0 s) | The blinking period setting The duty is 60% for all types. Character display on: 60% Character display off: 40% V: Vertical period |
| | | BLK1 | | | BLK0 | Operation | | | | | | | | | | | | | | |
| 0 | 0 | V × 25 (PAL: 0.5 s) | | | | | | | | | | | | | | | | | | |
| 0 | 1 | V × 30 (NTSC: 0.5 s) | | | | | | | | | | | | | | | | | | |
| 1 | 0 | V × 50 (PAL: 1.0 s) | | | | | | | | | | | | | | | | | | |
| 1 | 1 | V × 60 (NTSC: 1.0 s) | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | |
| 0 | BLK0 | 0 | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | |

Note: This register is set to 0 on a reset (either by the \overline{RST} pin or by a command reset).

LC74772V

⑥ COMMAND 5 (Display control: on/off settings for each output system)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|-------------------------------|---|
| | | State | Function | |
| 7 | — | 0 | Command 5 identification code | |
| 6 | — | 1 | | |
| 5 | — | 0 | | |
| 4 | — | 1 | | |
| 3 | DSP4 | 0 | System 4 output off | Pin 10 (BLK4) and pin 11 (CHA4) output control |
| | | 1 | System 4 output on | |
| 2 | DSP3 | 0 | System 3 output off | Pin 14 (BLK3) and pin 15 (CHA3) output control |
| | | 1 | System 3 output on | |
| 1 | DSP2 | 0 | System 2 output off | Pin 16 (BLK2) and pin 17 (CHA2) output control Invalid in RGB output mode. |
| | | 1 | System 2 output on | |
| 0 | DSP1 | 0 | System 1 (RGB) output off | Pin 18 (BLK1) and pin 19 (CHA1) output control Functions as the RGB output control in RGB output mode. |
| | | 1 | System 1 (RGB) output on | |

⑦ COMMAND 6 (Output control: systems 3 and 4 output control settings)

First byte

| DA0 to DA7 | Register name | Register content | | | | Note | |
|------------|---------------|------------------|---|--------|--------|---|--|
| | | State | Function | | | | |
| 7 | — | 0 | Command 6 identification code | | | | |
| 6 | — | 1 | | | | | |
| 5 | — | 1 | | | | | |
| 4 | — | 0 | | | | | |
| 3 | DSPF SL34 | 0 | Sets the system 3 output conditions according to the command described below. | | | Only system 4 is valid in 4-system output mode. System 4 cannot be set when the general-purpose output port usage is specified. | |
| | | 1 | Sets the system 4 output conditions according to the command described below. | | | | |
| 2 | DSP RSG | 0 | DSPRSG | DSPGSG | DSPBSG | Output selection | Note: The following registers are set to 1 during a reset. DSPRSG DSPGSG DSPBSG As a result, the "All of R, G, B are output" state is selected during a reset. |
| | | 1 | 0 | 0 | 0 | Signals other than R, G, B are output. | |
| 1 | DSP GSG | 0 | 0 | 0 | 1 | B is output. | |
| | | 1 | 0 | 1 | 0 | G is output. | |
| 0 | DSP BSG | 0 | 1 | 0 | 0 | R is output. | |
| | | 1 | 1 | 0 | 1 | R and B are output. | |
| | | 0 | 1 | 1 | 0 | R and G are output. | |
| | | 1 | 1 | 1 | 1 | All of R, G, B are output. | |

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

LC74772V

⑧ COMMAND 8 (Output control: background color setting: RGB output mode)

First byte

| DA0 to DA7 | Register name | Register content | | | | Note | |
|------------|---------------|------------------|-------------------------------|------|------|---------|------------------|
| | | State | Function | | | | |
| 7 | — | 1 | Command 8 identification code | | | | |
| 6 | — | 0 | | | | | |
| 5 | — | 0 | | | | | |
| 4 | — | 0 | | | | | |
| 3 | | 0 | — | | | | |
| 2 | BKCR | 0 | BKCR | BKCG | BKCB | | Background color |
| | | 1 | 0 | 0 | 0 | | Black |
| 1 | BKCG | 0 | 0 | 0 | 1 | Blue | |
| | | | 0 | 1 | 0 | Green | |
| | | 1 | 0 | 1 | 1 | Cyan | |
| | | | 1 | 0 | 0 | Red | |
| 0 | BKCB | 0 | 1 | 0 | 1 | Magenta | |
| | | | 1 | 1 | 0 | Yellow | |
| | | 1 | 1 | 1 | 1 | White | |

Background color setting in RGB output mode
This command is invalid in 4-system output mode.
• Invalid when pin 20 (OUT_{MOD}) is high.
• Valid when pin 20 (OUT_{MOD}) is low.

Second byte

| DA0 to DA7 | Register name | Register content | | | | Note |
|------------|---------------|------------------|----------|--------|--|--|
| | | State | Function | | | |
| 7 | BKO4 F1 | 0 | BKO4F1 | BKO4F0 | Operation function | The system 4 output border setting |
| | | 1 | 0 | 0 | No background or border | |
| 6 | BKO4 F0 | 0 | 0 | 1 | Font size (black characters) | |
| | | | 1 | 0 | Border | |
| | | 1 | 1 | 0 | Border | |
| | | | 1 | 1 | Areas other than the font (all filled) | |
| 5 | BKO3 F1 | 0 | BKO3F1 | BKO3F0 | Operation function | The system 3 output border setting |
| | | 1 | 0 | 0 | No background or border | |
| 4 | BKO3 F0 | 0 | 0 | 1 | Font size (black characters) | |
| | | | 1 | 0 | Border | |
| | | 1 | 1 | 0 | Border | |
| | | | 1 | 1 | Areas other than the font (all filled) | |
| 3 | BKO2 F1 | 0 | BKO2F1 | BKO2F0 | Operation function | The system 2 output border setting This command is invalid in RGB output mode. • Invalid when pin 20 (OUT _{MOD}) is low. • Valid when pin 20 (OUT _{MOD}) is high. |
| | | 1 | 0 | 0 | No background or border | |
| 2 | BKO2 F0 | 0 | 0 | 1 | Font size (black characters) | |
| | | | 1 | 0 | Border | |
| | | 1 | 1 | 0 | Border | |
| | | | 1 | 1 | Areas other than the font (all filled) | |
| 1 | BKO1 F1 | 0 | BKO1F1 | BKO1F0 | Operation function | The system 1 or RGB output border setting |
| | | 1 | 0 | 0 | No background or border | |
| 0 | BKO1 F0 | 0 | 0 | 1 | Font size | |
| | | | 1 | 0 | Border | |
| | | 1 | 1 | 0 | Border | |
| | | | 1 | 1 | Areas other than the font (all filled) | |

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

LC74772V

⑨ COMMAND 9 (Display start position setting)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|---|------|
| | | State | Function | |
| 7 | — | 1 | Command 9 identification code | |
| 6 | — | 0 | | |
| 5 | — | 0 | | |
| 4 | — | 1 | | |
| 3 | VP5 | 0 | If VS is the vertical display start position then: $VS = H \times \left(\sum_{n=0}^5 2^n VP_n \right) + 16H$ Where H is horizontal period pulse period. | |
| | | 1 | | |
| 2 | VP4 | 0 | | |
| | | 1 | | |
| 1 | VP3 | 0 | | |
| | | 1 | | |
| 0 | VP2 | 0 | | |
| | | 1 | | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|--|------|
| | | State | Function | |
| 7 | VP1 | 0 | If VS is the horizontal display start position then: $HS = T_c \times \left(\sum_{n=0}^5 2^n HP_n \right) + 12T_c$ Where T_c is a single period of the LC oscillator connected to pins 2 and 3 (OSC_{IN} and OSC_{OUT}), or: T_c is the period of the input clock (4fsc input) if CTRL1 (pin 4) is high. NTSC mode: 7.159 MHz = 4fsc × 1/2 PAL mode: 7.094 MHz = 4fsc × 2/5 | |
| | | 1 | | |
| 6 | VP0 | 0 | | |
| | | 1 | | |
| 5 | HP5 | 0 | | |
| | | 1 | | |
| 4 | HP4 | 0 | | |
| | | 1 | | |
| 3 | HP3 | 0 | | |
| | | 1 | | |
| 2 | HP2 | 0 | | |
| | | 1 | | |
| 1 | HP1 | 0 | | |
| | | 1 | | |
| 0 | HP0 | 0 | | |
| | | 1 | | |

Note: This register is set to 0 on a reset (either by the \overline{RST} pin or by a command reset).

LC74772V

⑩ COMMAND 10 (Display line control)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|--|---|
| | | State | Function | |
| 7 | — | 1 | Command 10 identification code | |
| 6 | — | 0 | | |
| 5 | — | 1 | | |
| 4 | — | 0 | | |
| 3 | LNF SZ | 0 | — | |
| | | 1 | Sets the character size. | |
| 2 | LNF OT4 | 0 | — | Invalid in general-purpose port mode. |
| | | 1 | Sets the system 4 display line. | |
| 1 | LNF OT3 | 0 | — | Invalid in system 4 output setup mode. |
| | | 1 | Sets the system 3 display line. | |
| 0 | LNF SEL | 0 | The line specified by the next 6 bits is one of lines 1 to 6. | Controls the line switching specified by the six bits in the second byte. |
| | | 1 | The line specified by the next 6 bits is one of lines 7 to 12. | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|---------------------------------|--|
| | | State | Function | |
| 7 | — | 0 | — | The character size or display line setting 0: Character size specification = normal Display line specification = off 1: Character size specification = double size Display line specification = on |
| 6 | — | 0 | — | |
| 5 | LIN 126 | 0 | Clears the line 6 (12) setting. | |
| | | 1 | Sets line 6 (12). | |
| 4 | LIN 115 | 0 | Clears the line 5 (11) setting. | |
| | | 1 | Sets line 5 (11). | |
| 3 | LIN 104 | 0 | Clears the line 4 (10) setting. | |
| | | 1 | Sets line 4 (10). | |
| 2 | LIN 93 | 0 | Clears the line 3 (9) setting. | |
| | | 1 | Sets line 3 (9). | |
| 1 | LIN 82 | 0 | Clears the line 2 (8) setting. | |
| | | 1 | Sets line 2 (8). | |
| 0 | LIN 71 | 0 | Clears the line 1 (7) setting. | |
| | | 1 | Sets line 1 (7). | |

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

LC74772V

⑪ COMMAND 11 (Display RAM write address setting)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|---|------|
| | | State | Function | |
| 7 | — | 1 | Command 11 identification code | |
| 6 | — | 0 | | |
| 5 | — | 1 | | |
| 4 | — | 1 | | |
| 3 | VADR 3 | 0 | The range of the display RAM vertical address (line address) setting is from 0 to B (hexadecimal) (12 lines). Values of C (hexadecimal) or larger are not allowed. | |
| | | 1 | | |
| 2 | VADR 2 | 0 | | |
| | | 1 | | |
| 1 | VADR 1 | 0 | | |
| | | 1 | | |
| 0 | VADR 0 | 0 | | |
| | | 1 | | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|--|------|
| | | State | Function | |
| 7 | — | 0 | — | |
| 6 | — | 0 | — | |
| 5 | — | 0 | — | |
| 4 | HADR 4 | 0 | The range of the display RAM horizontal address (character address) setting is from 00 to 17 (hexadecimal) (24 characters). Values of 18 (hexadecimal) or larger are not allowed. | |
| | | 1 | | |
| 3 | HADR 3 | 0 | | |
| | | 1 | | |
| 2 | HADR 2 | 0 | | |
| | | 1 | | |
| 1 | HADR 1 | 0 | | |
| | | 1 | | |
| 0 | HADR 0 | 0 | | |
| | | 1 | | |

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

LC74772V

⑫ COMMAND 14 (Display RAM setup data)

First byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|--|------|
| | | State | Function | |
| 7 | — | 1 | Command 14 identification code | |
| 6 | — | 1 | | |
| 5 | — | 1 | | |
| 4 | BLK | 0 | — | |
| | | 1 | Blinking character specification | |
| 3 | RV | 0 | — | |
| | | 1 | Reverse video character specification | |
| 2 | R | 0 | — | |
| | | 1 | R output specification (system 3 output in 4-system output mode) | |
| 1 | G | 0 | — | |
| | | 1 | G output specification (system 2 output in 4-system output mode) | |
| 0 | B | 0 | — | |
| | | 1 | B output specification (system 1 output in 4-system output mode) | |

Second byte

| DA0 to DA7 | Register name | Register content | | Note |
|------------|---------------|------------------|---|------|
| | | State | Function | |
| 7 | C7 | 0 | Character code setting There are 256 characters (00 to FF hexadecimal). FE hexadecimal is handled as blank data. Nothing is displayed, whatever the other conditions are set to. FF hexadecimal functions as the transfer termination code for character-code-only continuous transfers. Continuous transfer mode is set up by setting the data 0 bit (DATAFMT) in COMMAND 2 to 1. | |
| | | 1 | | |
| 6 | C6 | 0 | | |
| | | 1 | | |
| 5 | C5 | 0 | | |
| | | 1 | | |
| 4 | C4 | 0 | | |
| | | 1 | | |
| 3 | C3 | 0 | | |
| | | 1 | | |
| 2 | C2 | 0 | | |
| | | 1 | | |
| 1 | C1 | 0 | | |
| | | 1 | | |
| 0 | C0 | 0 | | |
| | | 1 | | |

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

Display Screen Organization

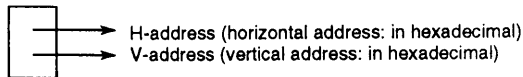
The display screen consists of 12 lines of 24 characters each.

Thus the maximum number of characters that can be displayed is 288 characters.

The display memory address consists of a line address (VADR0, VADR1, VADR2, and VADR3 representing values from 0 to B (hexadecimal)), and a column (character position) address (HADR0, HADR1, HADR2, HADR3, and HADR4 representing values from 0 to 17 (hexadecimal)).

Display Screen Organization (Display memory address)

| | | 24 characters | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| 12 rows | 1 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 2 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 3 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 4 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 5 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 6 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 7 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 8 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 9 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 10 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 11 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| | 12 | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |



- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of February, 1999. Specifications and information herein are subject to change without notice.