DATA SHEET

MOS FIELD EFFECT POWER TRANSISTOR
2SJ302, 302-Z

SWITCHING
P-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SJ302 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
  $R_{DS(on)} \leqq 0.1\ \Omega$ ($V_{GS} = -10$ V, $I_D = -8$ A)
  $R_{DS(on)} \leqq 0.24\ \Omega$ ($V_{GS} = -4$ V, $I_D = -6$ A)
- Low C_{iss} $C_{iss} = 1\ 200$ pF TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

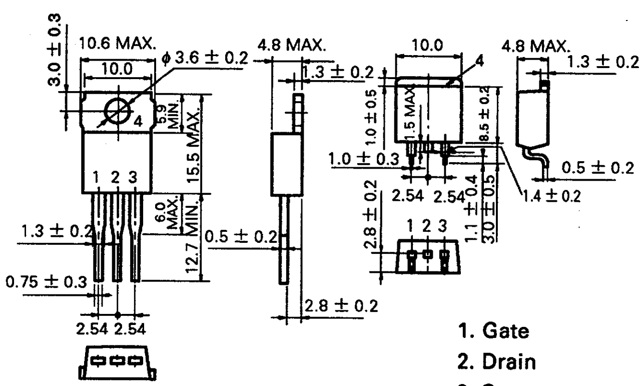
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	−60	V
Gate to Source Voltage	V_{GSS}	−20, +10	V
Drain Current (DC)	$I_{D(DC)}$	∓16	A
Drain Current (pulse)	$I_{D(pulse)}$*	∓64	A
Total Power Dissipation (T_c = 25 °C)	P_T	75	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

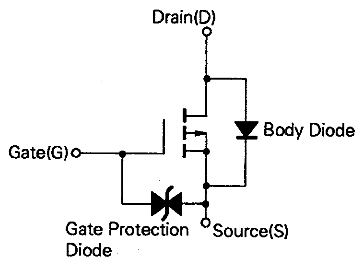
* PW ≦ 10 μs, Duty Cycle ≦ 1 %

PACKAGE DIMENSIONS

in millimeters



1. Gate
2. Drain
3. Source
4. Fin (Drain)

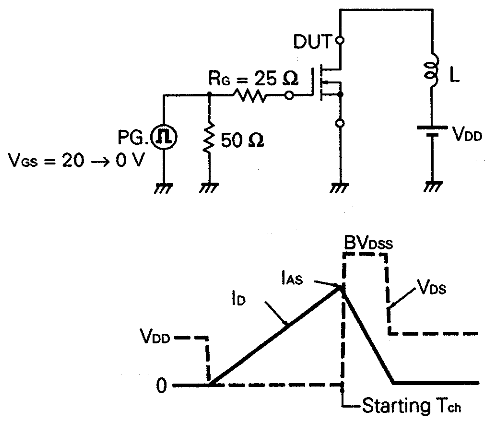


Document No. TC-2455
(O.D. No. TC-7944)
Date Published August 1993 M
Printed in Japan

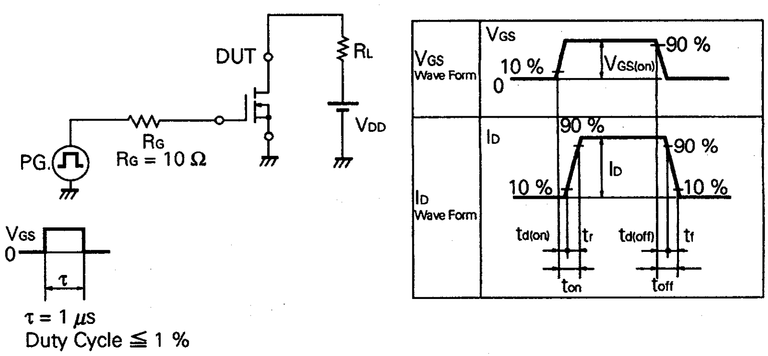
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		75	100	mΩ	V_{GS} = –10 V, I_D = –8 A
Drain to Source On-state Resistance	$R_{DS(on)}$		130	240	mΩ	V_{GS} = –4.0 V, I_D = –6 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	–1.0		–2.0	V	V_{DS} = –10 V, I_D = –1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	5.0			S	V_{DS} = –10 V, I_D = –8 A
Drain Leakage Current	I_{DSS}			–10	μA	V_{DS} = –60 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			∓10	μA	V_{GS} = ∓16 V, V_{DS} = 0
Input Capacitance	C_{iss}		1200		pF	V_{DS} = –10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		670		pF	
Reverse Transfer Capacitance	C_{rss}		290		pF	
Turn-On Delay Time	$t_{d(on)}$		30		ns	$V_{GS(on)}$ = –10 V V_{DD} = –30 V I_D = –8 A, R_G = 10 Ω R_L = 3.75 Ω
Rise Time	t_r		170		ns	
Turn-Off Delay Time	$t_{d(off)}$		150		ns	
Fall Time	t_f		130		ns	
Total Gate Charge	Q_G		42		nC	V_{GS} = –10 V I_D = –16 A V_{DD} = –48 V
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		17		nC	
Diode Forward Voltage	V_{SD}		1.0		V	I_F = –16 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		110		ns	I_F = –16 A, V_{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		220		nC	

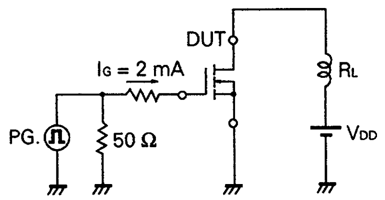
Test Circuit 1 : Avalanche Capability



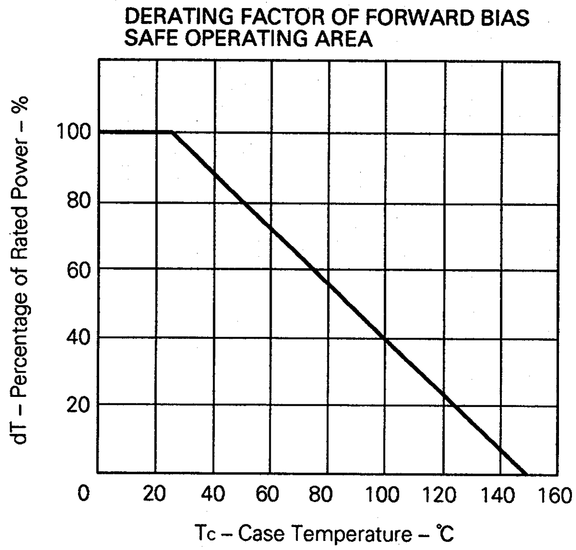
Test Circuit 2 : Switching Time

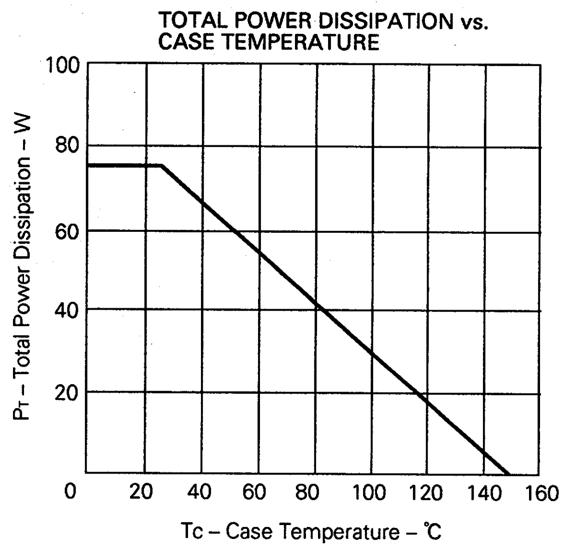


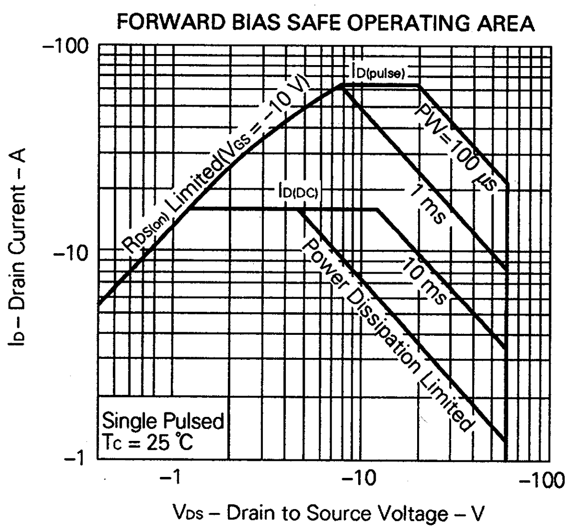
Test Circuit 3 : Gate Charge

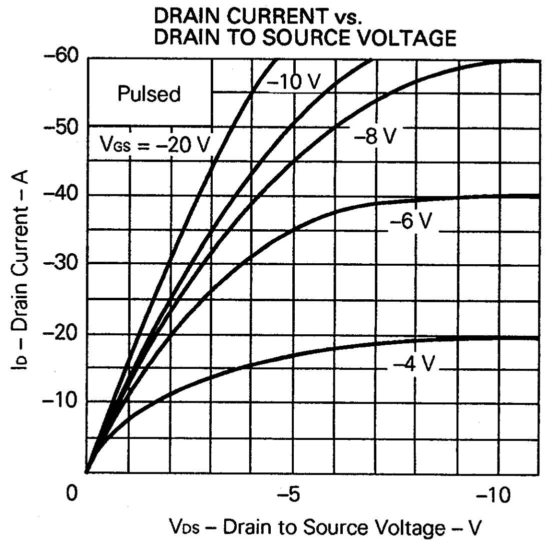


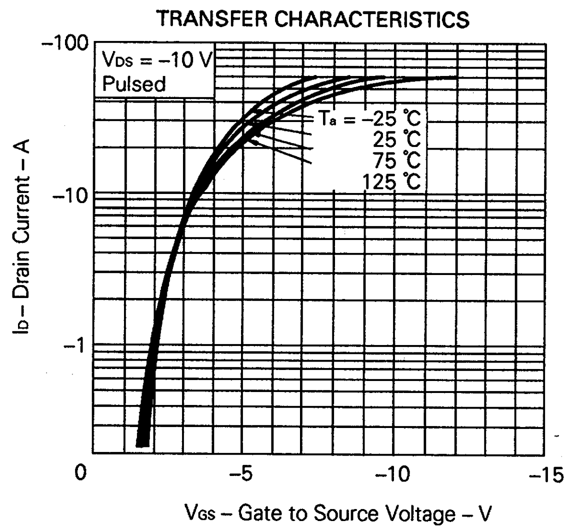
TYPICAL CHARACTERISTICS (T_a = 25 °C)



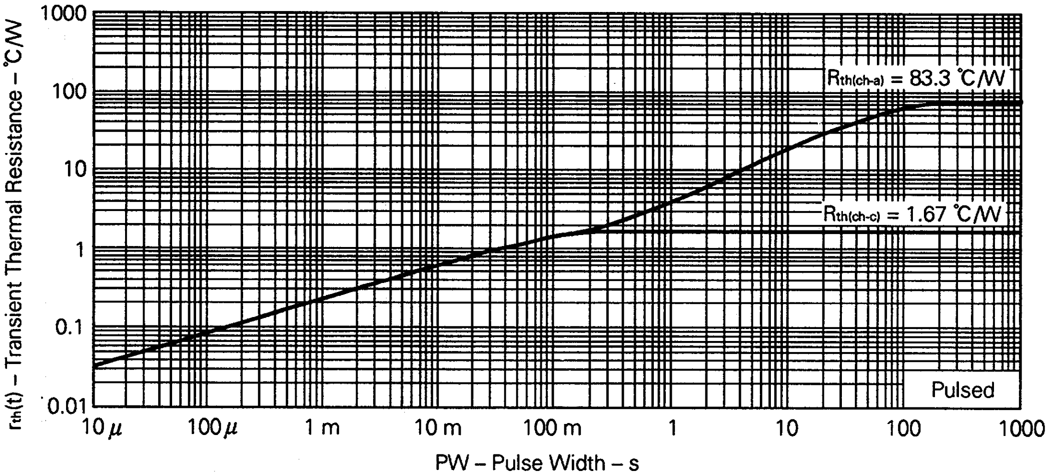




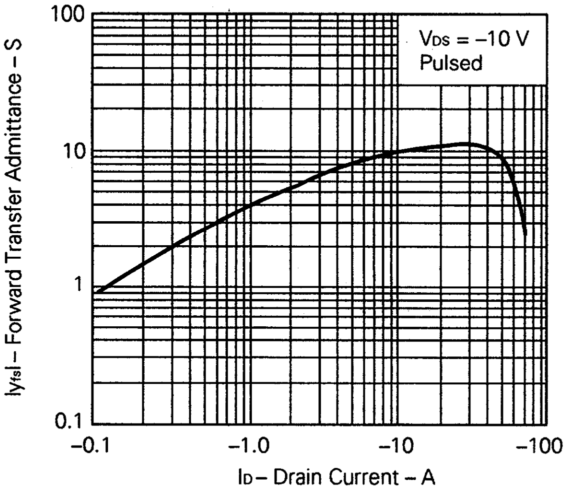




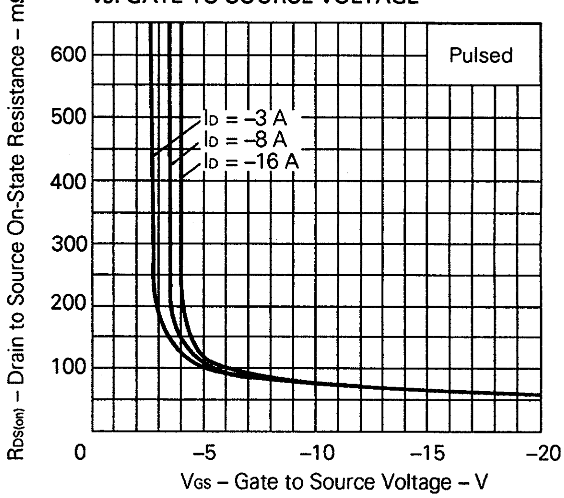
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



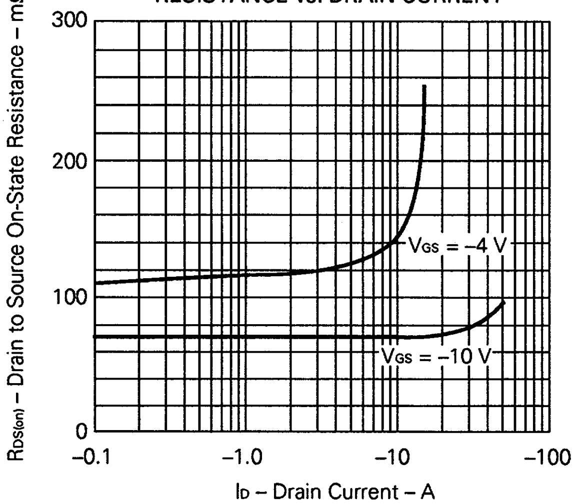
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



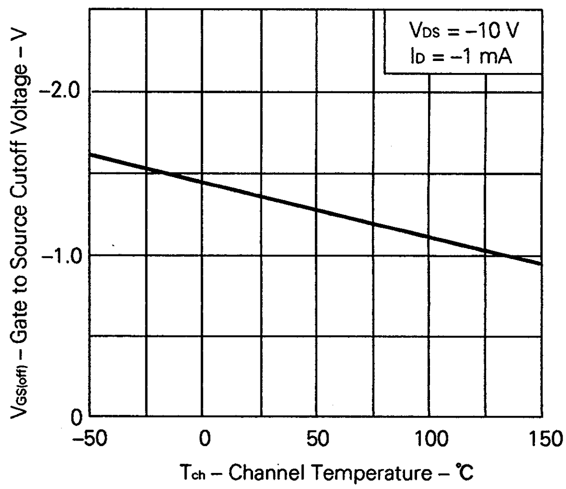
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



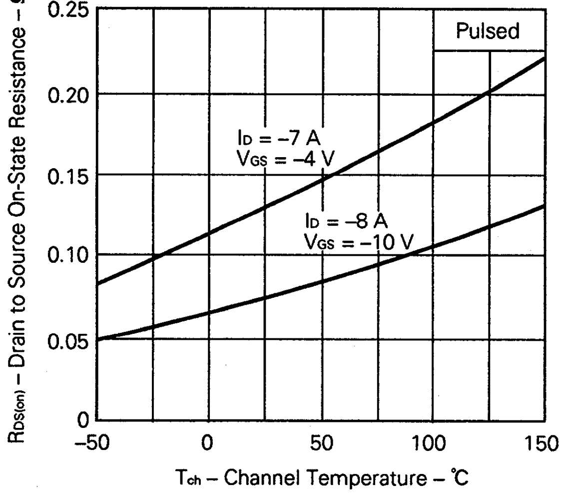
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



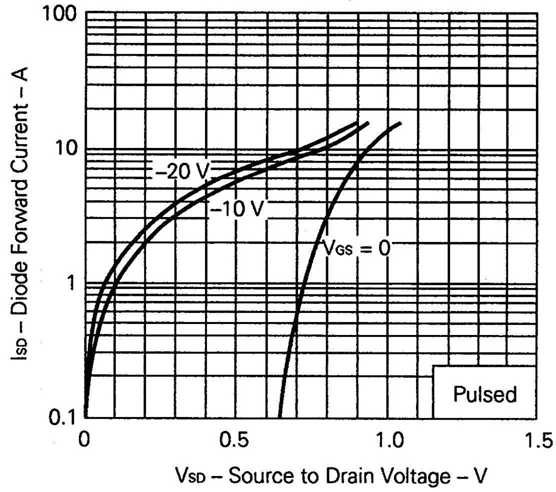
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



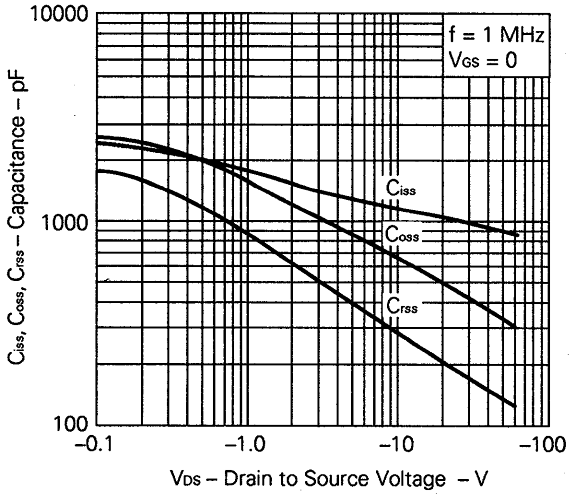
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



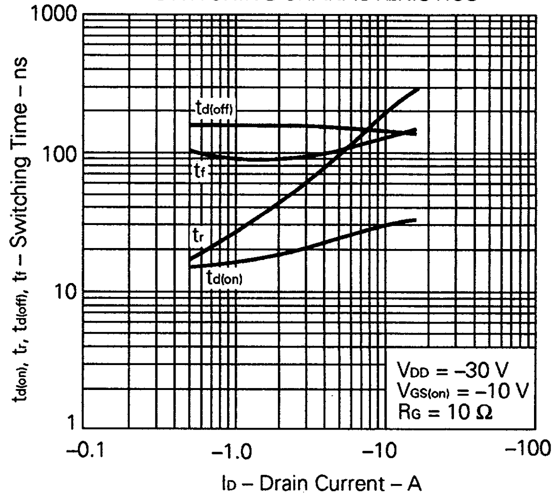
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



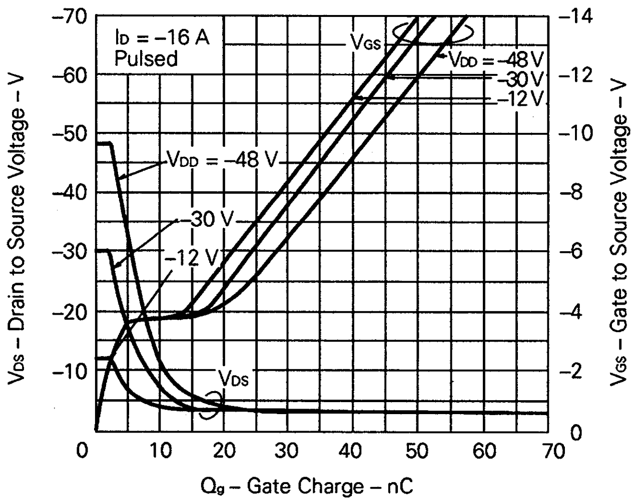
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



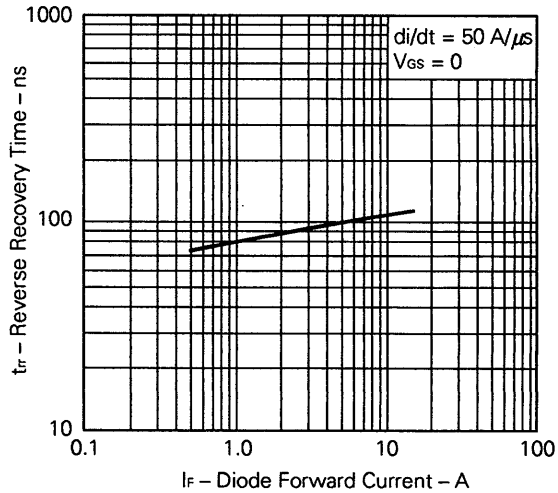
SWITCHING CHARACTERISTICS



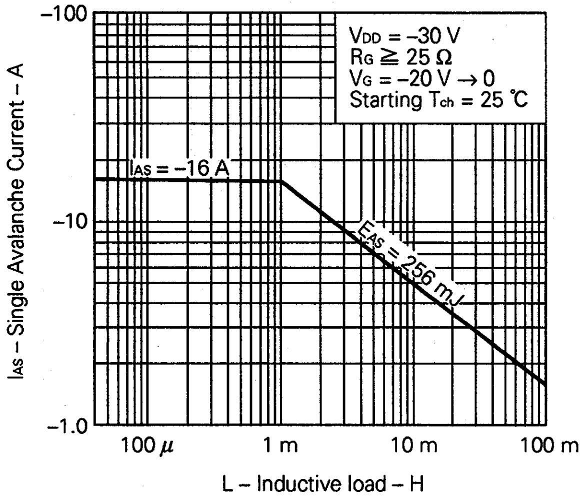
DYNAMIC INPUT CHARACTERISTICS



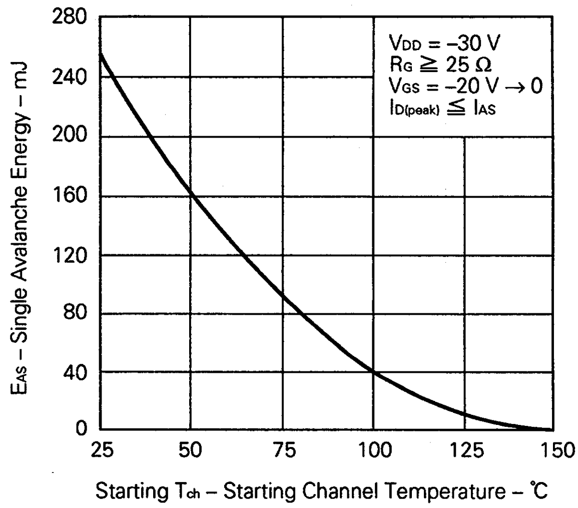
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

[MEMO]

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