PM7326

S/UNI™ - APEX

S/UNI-APEX

ATM/PACKET TRAFFIC MANAGER AND SWITCH

ERRATA

RELEASED

ISSUE 1: APRIL 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
Issue 1	April, 2000	Initial release of errata.

CONTENTS

This page left blank intentionally

1 INTRODUCTION

This document is complete list of all errata items associated with the PM7326 S/UNI-APEX, Revision A.

1.1 References

The information contained in this errata document applies to the following product documents:

PMC-981224, PM7326 S/UNI-APEX ATM/Packet Traffic Manager and Switch Data Sheet, Issue 6, May, 1999.

PMC-991454, PM7326 S/UNI-APEX Hardware Programming Guide, Issue 2, March, 2000.

PMC-991727, PM7326 S/UNI-APEX Driver Manual, Issue 1, December, 1999.

1.2 Organization

Each item in this document is grouped according to the type of errata and contains the following information:

- Descriptive title
- Document reference(s)
- Detailed description of item
- Additional relevant information

1.3 Additional Feedback

Please report any discrepancies not covered in this document to PMC-Sierra at:

PMC-Sierra, Inc.
105-8555 Baxter Place
Burnaby, BC, Canada V5A 4V7
Tel: (604) 415-6000
App Support: (604) 415-4533
Fax: (604) 415-6001
Product information: info@pmc-sierra.com
Applications information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

2 FUNCTIONAL DEFICIENCIES

This section describes known functional deficiencies of the S/UNI-APEX, as of the publication date of this document.

2.1 Service Arbitration Round-Robin Behavior

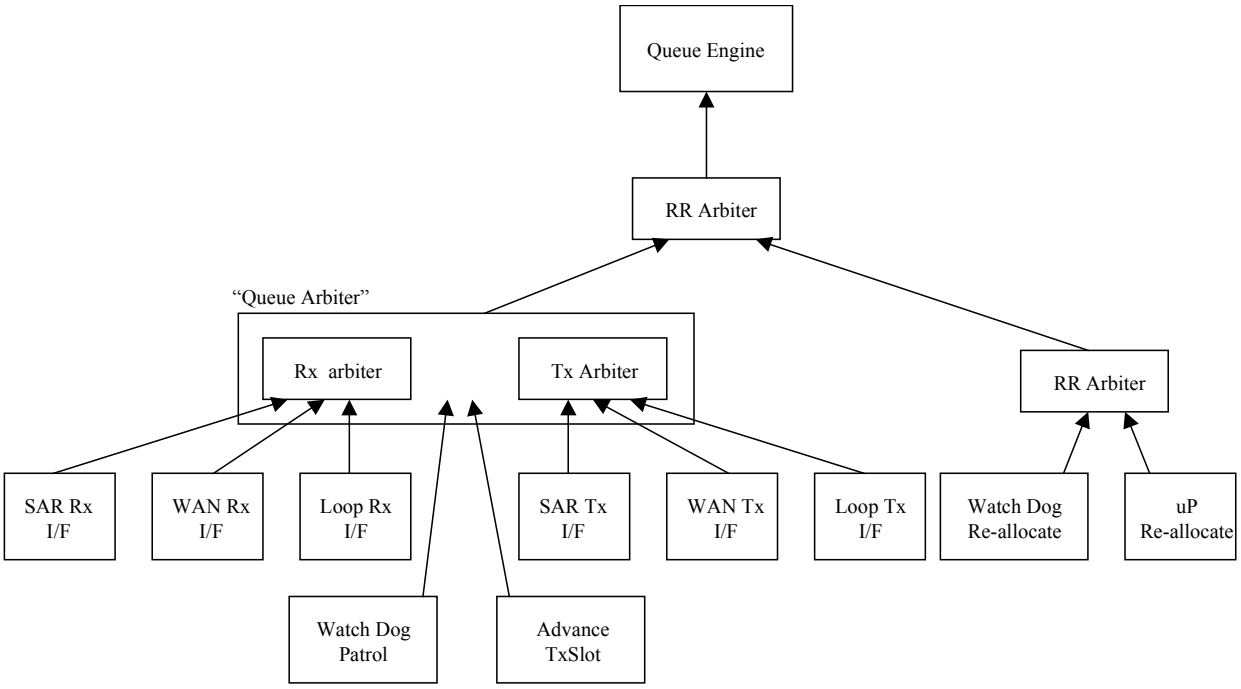
Document Reference

S/UNI-APEX ATM/Packet Manager and Switch Data Sheet, Sections 10.9.1 and 10.9.2.2

Description

Note that the behavior described below will only impact you if you are operating the S/UNI-APEX in frame continuous queuing mode.

In very limited circumstances, the service arbitration process may be inconsistent with the description shown in Section 10.9.1 of the data sheet. Referring to Figure 14 in the data sheet (reproduced below), in some cases the watch dog reallocation procedure may temporarily cause the Rx or Tx arbiters to repeatedly



service the same interface (SAR, loop or WAN) until reallocation is complete. This could cause potential starvation of one of the remaining interface services.

This is caused because the Rx and Tx arbiters continue to cycle even when the watch dog arbiter has “won” the next Queue Engine opportunity. This effectively blocks the next interface selected by the Rx or Tx arbiter from being serviced for that cycle. If multiple ICIs simultaneously time out, the watch dog could cause the same interface to be repeatedly blocked, which could starve the interface.

The effect of this behavior is dependent on the activity at the interfaces. A possible worst case scenario would occur if all of the following conditions were present:

- Two out of three interfaces (WAN, Loop or SAR) have 2 or more cells in the internal FIFOs waiting to be serviced
- Frame contiguous queuing of VCs is being used
- The VC timeout watch dog is enabled (QWwdActive=1)
- The watch dog patrol is executed and discovers re-assembly time out errors in VCs that have sequential ICIs

Resolution

The probability of a re-assembly time out for a sequence of VCs would be very low in normal operations. The most likely worst case scenario would be the simultaneous time out of all VCs associated with a given port due to a catastrophic fault on that port. If the VCs on any given port were mapped to non-sequential ICIs, the Rx and Tx interfaces would have an opportunity to successfully service requests between VC reallocations.

Typically there will be a device between the S/UNI Apex and the link layer that can perform an address resolution function (the S/UNI Atlas for example). This device could be also be used to map each VC on a port to non-contiguous ICIs.

One possible strategy would be to map VCs on even-numbered ports to even-numbered ICIs and VCs on odd-numbered ports to odd-numbered ICIs. This “striping” would ensure that the VCs associated with any port fault would not occupy contiguous ICIs and would therefore avoid the service arbitration behavior described above.

2.2 Any-PHY Bus, RSX Signal Timing Restriction

Document Reference

S/UNI-APEX ATM/Packet Manager and Switch Data Sheet:

- Section 9.1
- Section 9.3
- Register 0x10 - Hi Priority Interrupt Status
- Register 0x14 - High Priority Interrupt Mask

Description

Note that the behavior described below will only impact you if you are designing a custom Any-PHY slave device to interface to the S/UNI-APEX.

This behavior is only significant if the S/UNI-APEX is operating in Any-PHY master mode in the receive direction. The behavior is identical on the loop bus and the WAN bus. This behavior has no impact when the S/UNI-APEX is operating as a Utopia L2 master or Utopia L2 slave.

When functioning as an Any-PHY receive master the behavior of the RSX input signal (LRSX for the loop bus, WRSX for the WAN bus) is not precisely as documented in the data sheet. In Section 9.1 (9.3) the data sheet states, “LRSX (WRSX) is asserted by the selected PHY device during the first cycle of a data block transfer coinciding with the port address prepend.”

To be fully compliant with the Any-PHY specification the S/UNI-APEX should be able to accept the RSX signal being asserted at two or more clock periods after LRENB (WRENB) has been asserted. Indeed, the S/UNI-APEX will successfully accept a cell transfer if RSX is asserted 2 or more clock periods after RENB, however, unless RSX is asserted at exactly 2 clock periods after RENB the S/UNI-APEX will generated an erroneous “Runt cell error interrupt”, as defined in Register 0x10 - Hi Priority Interrupt Status.

Resolution

The behavior described below has no impact when the S/UNI-APEX is connected to PMC-Sierra Any-PHY devices such as the S/UNI-VORTEX and S/UNI-DUPLEX because these slave devices generate RSX exactly two clock periods after RENB.

Customers designing their own Any-PHY slave devices should ensure that their device responds to RENB by asserting RSX and initiating the cell transfer in exactly 2 clock periods. Typically, a 2 clock period response time is desirable

anyway since it provides the maximum bus throughput and is not difficult to achieve. Therefore this should have little or no impact on most designs.

If for some reason it is impossible to design your custom device to respond to RSX in 2 clock periods you can still operate the S/UNI-APEX with RSX occurring at 3 or more clock periods after the RENB. In this scenario, the receive cell transfers continue to function correctly, so simply mask out the runt cell interrupt using Register 0x14 and ignore the “runt cell” interrupt bit in Register 0x10.

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

PMC-1991770 (R1) ref PMC-981224 (R6), ref PMC-991454 (R2), ref PMC-991727 (P1) Issue date: April 2000