FAIRCHILD SEMICONDUCTOR®

January 2002

FM3580
5-Bit VID Controller with PC Security Element

General Description

The FM3580 is an standard 5-bit VID controller with an integrated a Security controller. FM3580 extends the typical VID feature to a PC motherboard by offering a security function which deters cloning of PC motherboards.

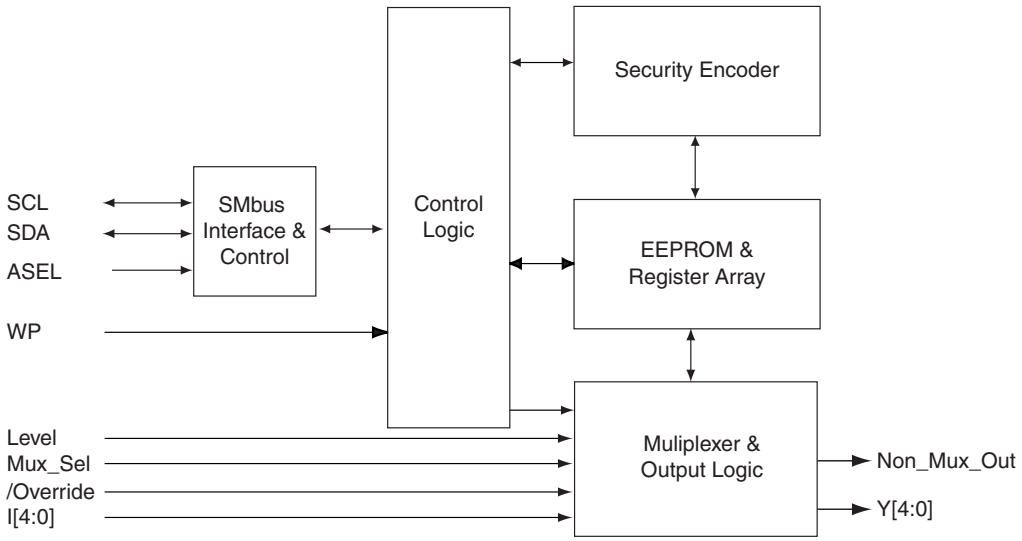
FM3580's Security block generates a new pseudo-random code each time one of its internal registers is read. The PC BIOS is programmed to poll pseudo-random code from the FM3580 at frequent intervals. If the appropriate code is not read, the system shuts down, or refuses to boot at power-up. The VID controller portion of FM3580 is identical to FM3560 and is pin compatible with FM3560.

FM3580 is designed using low power CMOS technology.

Features

- VID controller similar to FM3560
- Integrated "anti-clone" Security controller
- Configurable Output type
  - — TTL
  - — Open-Drain
- Pin compatible to FM3560
- SMBus interface to Security/VID controls
- Operating V_{CC} : 2.7V to 5.5V
- Operating Temp: 0°C to +70°C
- Package: 20-Pin TSSOP

Block Diagram

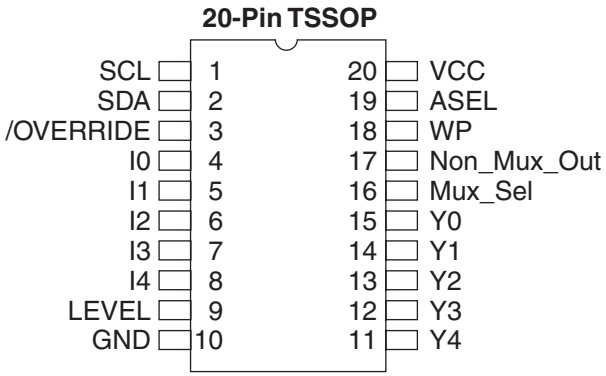


Ordering Code

Part Number	Package Number	Package Description
FM3580MT20	MT20	20-Pin TSSOP

Note: For other package options please consult Fairchild Sales/Marketing.

Pin Connection Diagram



Pin Description

Pin Name	Description
I[0:4]	Input data. These 5 signals have internal pullup (10KΩ to 40KΩ).
Y[0:4]	Multiplexed Output data signals.
SCL	Serial Clock Input for SMBus access. has an internal pullup (125KΩ).
SDA	Serial Data Input/Output for SMBus access. As an internal pullup (125KΩ).
/OVERRIDE	Active low input to select Y-port output data. See Table 1.
Level	Output level select input. When low, the Y[0:4] outputs are driven up to 2.5V and the Non_Mux_Out signal is driven up to V_{CC}; When high, the Y[0:4] outputs and the Non_Mux_Out signal operate as an Open-Drain type. This signal has an internal pullup resistor and can be left unconnected for Open-Drain type Y[0:4] outputs and Non_Mux_Out signal.
ASEL	Address select input. When set high, the device will respond to 1001-110 7-bit address and when set low, the device will respond to 0110-111 7-bit address.
WP	Write Protect input. When set high, prevents writes to internal registers.
Non_Mux_Out	Non-Multiplexed output.
Mux_Sel	Multiplexer select input to select Y-port output data. See Table 1.
V_{CC}	Power input to the device.
GND	Ground.

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.5V to V_{CC} + 0.5V
DC Input Voltage (V_I)	-0.5V to V_{CC} + 0.5V
Output Voltage (V_O)	
Outputs Tri-Stated	-0.5V to V_{CC} + 0.5V
Outputs Active	-0.5V to V_{CC} + 0.5V
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions

Power Supply	2.7V to 5.5V
Input Voltage	-0.3V to 3.8V
Output Voltage (V_O)	0V to V_{CC}
Output Current (I_{OL})	3mA
Free Air Operating Temperature (T_A)	-0°C to +70°C
Minimum Input Edge Rate (d_T/d_V)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10nS/V

Note 1: The "Absolute maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics (2.7V ≤ V_{CC} ≤ 5.5V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	High Level Input Voltage		2.7 – 5.5	2.1	V_{CC}	V
V_{IL}	Low Level Input Voltage		2.7 – 5.5		0.8	V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA I_{OL} = 2.5mA	2.7 – 5.5		0.2 0.4	V
V_{OH}	Output High Voltage	Fixed output mode LEVEL input = logical "0" 1 TTL load, 50pF cap	2.7 – 5.5	2.3	2.6	V
I_{IR}	Input Leakage Current	V_I = V_{CC}	5.5	-5	+5	µA
I_{CC}	Active Supply Current	V_I = V_{CC} or GND	2.7 – 5.5		5	mA

AC Characteristics (2.7V ≤ V_{CC} ≤ 5.5V) Y-Port Pull-up = 4.7kΩ

Symbol	Parameter	Condition	Min	Max	Units
T_{PHL_IY}	Propagation Delay from I-Port to Y-Port	Mux_Sel = H; /Override = Don't Care; I-Port is switching from H to L; Level = H		50	ns
T_{PLH_IY}	Propagation Delay from I-Port to Y-Port	Mux_Sel = H; /Override = Don't Care; I-Port is switching from L to H; Level = H		100	ns
T_{PHL_MY}	Propagation Delay from Mux_Sel to Y-Port	Mux_Sel is switching from H to L; /Override = L; I-Port = H; Level = H		50	ns
T_{PLH_MY}	Propagation Delay from Mux_Sel to Y-Port	Mux_Sel is switching from L to H; /Override = L; I-Port = H; Level = H		100	ns

SMBus AC Characteristics

Symbol	Parameter	T_A = 0°C to +70°C, C_L = 30pF, R_L = 500Ω		Units
		V_{CC} = 2.7 - 5.5V		
		Min	Max	
f_{SCL}	SCL Clock Frequency	10	90	kHz
T_1	Noise Supression Time Constant		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	4.8	µs
t_{BUF}	Time the Bus must be free before a new Transmission can start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	5.2	24000	µs
t_{HIGH}	Clock High Period	4.0	50	µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data in Hold Time	300		ns
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1000	ns
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
$t_{TIMEOUT}$	Detect Clock Low Timeout	20	35	ms

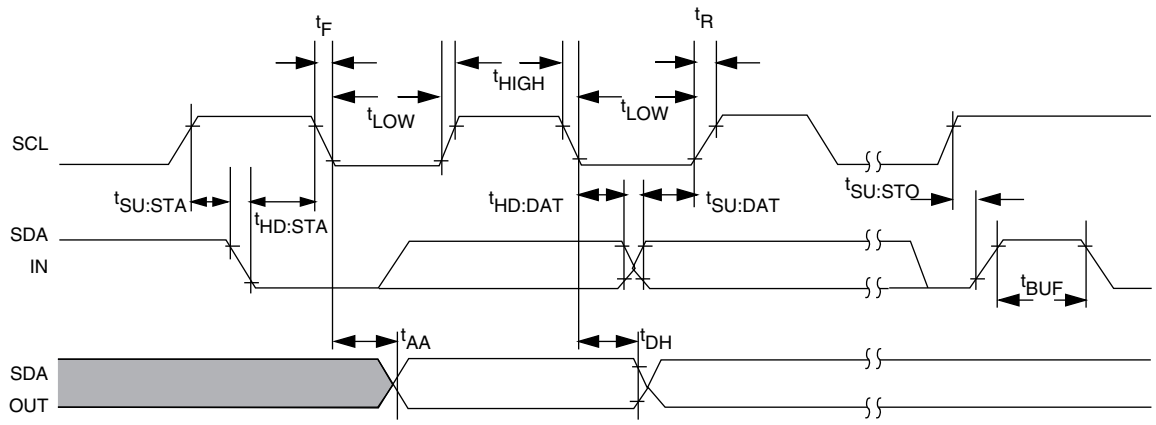
Capacitance (T_A = +25°C)

Symbol	Parameter	Conditions	Typical	Units
Cin	Input Capacitance	V_I = 0V or V_{CC}, V_{CC} = 5.5V	6	PF
$C_{I/O}$	Input/Output Capacitance	V_I = 0V or V_{CC}, V_{CC} = 5.5V	7	PF
C_{OUT}	Output Capacitance		7	PF

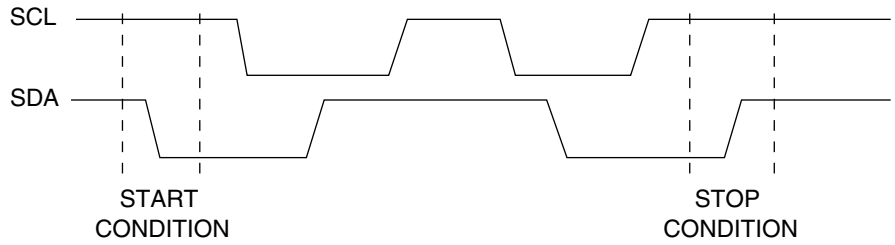
Non-Volatile Memory Characteristics

Parameter	Specification
Data Retention	10 years minimum
Number of writes	1,000,000 cycles

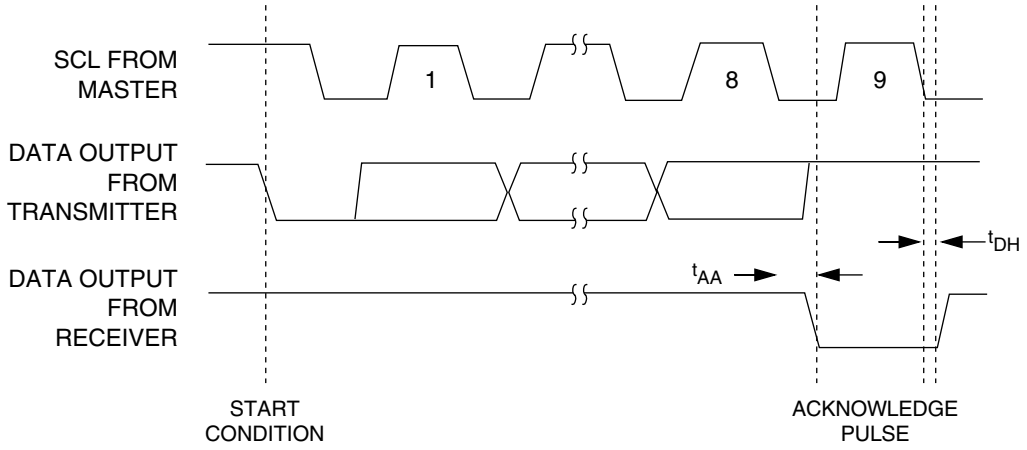
SMBus Timing



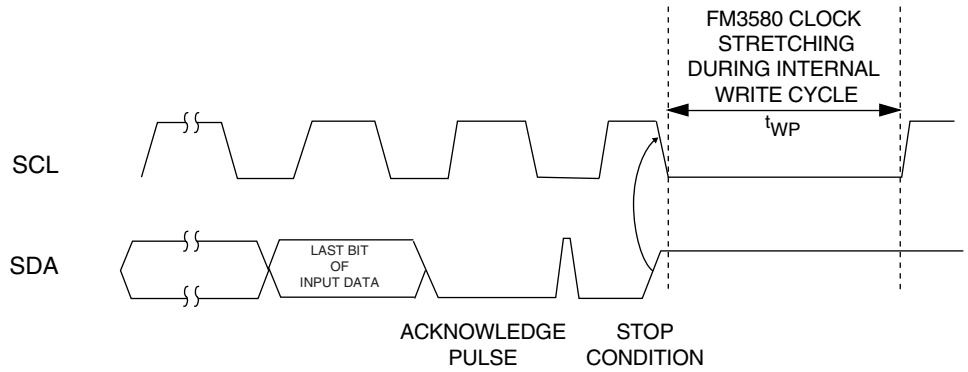
SMBus START/STOP Condition



SMBus ACK Pulse



Clock Stretching



Functional Description

Legacy VID Operation

During standard operation FM3580 (the device) will pass data from the I[0:4] inputs (I-Port) or data from an internal register SOPR-A or data from an internal register SOPR-B to the Y[0:4] outputs (Y-Port). Logic is implemented through a set of multiplexers. All the signals and the control involved in the VID operation are explained below.

Output Port (Y-Port): Y[0-4]

This Y-Port output forms the power management signals to determine the CPU power level and is typically connected to the motherboard DC-DC converter. As mentioned before this Y-Port is a multiplexed output of either the I-Port input or data from one of the two internal registers (SOPR-A ; SOPR-B). Choice of which one is selected is determined by Mux_Sel input signal and Bits[7:6] of SOPR-A/SOPR-B registers. Note that Bit7 and Bit 6 are defined to be common for both SOPR-A and SOPR-B registers. Rest of the bits (Bit5:0) are defined to be separate.

At power up the default path is from I-Port to Y-Port till a valid SMBus write command is issued to set Bits[7:6] at which point the Y-Port output is determined by the combined status of Mux_Sel input signal and the Bit[7:6] values. The multiplexer only updates when an SMBus stop condition is observed. The output type of the Y-Port can be configured for either an Open-drain type or TTL type using Level input. Y-Port is always active. Refer Multiplexer Block diagram. Table.1 summarizes above description.

Input Port (I-Port): I[0-4]

The I-port values are generated externally on the PC motherboard and may be either hardwired or driven by another device. Internal pull-up resistors are provided on the I-Port to accommodate this device being driven by an open-drain output driver.

Level Input

This input controls the output type of the Y-Port signals and Non_Mux_Out signal. If Level signal is connected to Ground, then the Y-Port outputs are actively driven to 2.5V and Non_Mux_Out signal is actively driven up to V_{CC}. If Level signal is connected to V_{CC} (or left unconnected), then the Y-Port signals and Non_Mux_Out signal operate as open-drain outputs. Level input has an internal pull-up resistor and hence can be left unconnected to recognize a logic high at its input.

Non_Mux_Out Output

This is an output signal and it reflects the Bit4 of either SOPR-A or SOPR-B register. Like the Y-Port, Bit[7:6] values determine the selection of either Bit 4 of SOPR-A or Bit4 of SOPR-B register. The Non_Mux_Out output is transparent when the Mux_sel signal is at logic 0 and will latch data on the rising edge of the Mux_sel signal.

Mux_Sel Input

This is an input signal and is used to select data for Y-Port outputs. If this signal is set to logic 1, I-Port data is driven on the Y-Port and when set to logic 0 (and /Override = 1), data from one of the two internal non-volatile registers (SOPR-A or SOPR-B) are driven on the Y0-4 outputs.

/Override Input

This is an input signal and when set to logic low (and Mux_Sel = 0), will cause all the Y-Port outputs and Non_Mux_Out output to be set to Logic Low.

VID Registers Description

FM3580 has 3 internal registers, viz. SOPR-A, SOPR-B and PIPR for VID function. These registers are made up of a combination of read-only, write-only and read-write bits.

Serial Output Port Register A (SOPR -A)

This is a 8-bit read-write register that contains 5-bit data for output Y-Port, 1-bit data for Non_Mux_Out Output and two multiplexer select bits. This register can be read and written through SMBus and is at address 0x00h. Refer SOPR-A/B diagram.

Serial Output Port Register B (SOPR -B)

This is a 8-bit read-write register that contains 5-bit data for output Y-Port, 1-bit data for Non_Mux_Out Output and two multiplexer select bits. This register can be read and written through SMBus and is at address 0x01h. Refer SOPR-A/B diagram.

Parallel Input Port Register (PIPR)

This is a 8-bit read-only register. Bits[7:5] are reserved and are set to read “0” always. Bits[4:0] contain latched I-Port value. I-port data is latched into this register on the first clock after a “START” condition is detected on the SMBus. This insures valid value be read from this register always. This register can only be read through SMBus and is at address 0x02h. Refer PIPR diagram.

SMBus Interface

FM3580 uses standard SMBus protocol to communicate with external interface (system). Various blocks and features of this device are accessible through the SMBus interface. This device supports both byte and block reads as defined in the SMBus specification. VID block is accessed through byte-write and block-read commands, while the Security block is accessed through block-read/write commands.

Device Addressing

FM3580 uses 7 bit SMBus addressing. If the ASEL input is ‘1,’ then the device will respond to 1001-110 address. If the ASEL input is ‘0,’ then the device will respond to 0110-111 address. The address byte is the first byte of data sent after a start condition. The device will not respond to the general call address 0000-000.

SOPR-A Register Write Operation (Byte)

Following is the SMBus command sequence to write SOPR-A register. Write operation starts with a valid “START” command, followed by device address byte with Read-Write bit set to “0.” On receiving a valid device address, FM3580 issues an “ACK” pulse. This is followed by register address byte (0x00h) to select the SOPR-A register. On receiving this register address byte, FM3580 issues an “ACK” pulse. This is followed by data byte to be written into the SOPR-A register. On receiving this data byte, FM3580 issues an “ACK” pulse. This is followed by a “STOP” command at which point write operation begins internally. Refer Write VID Registers diagram.

SOPR-B Register Write Operation (Byte)

Write sequence to SOPR-B register is same as the SOPR-A register write sequence described above except instead of 0x00h value for register address, 0x01h should be used. This will select SOPR-B register. Refer Write VID Registers diagram.

Functional Description (Continued)

SOPR-A/SOPR-B/PIPR Read Operation (Block)

Following is the SMBus command sequence to read from SOPR-A, SOPR-B and PIPR registers in single command sequence. Read operation starts with a valid "START" command, followed by device address byte with Read-Write bit set to "1". On receiving a valid device address, FM3580 issues an "ACK" pulse. The device now outputs a byte of data with a "byte count" value of 0x03h indicating 3 bytes of actual data are provided after this byte. Upon receiving this byte count information, the system issues an "ACK" pulse. The device now outputs a byte of data from SOPR-A register; upon receiving this data byte, the system issues an "ACK" pulse. The device continues to output a byte of data now from SOPR-B register; upon receiving this data byte, the system issues an "ACK" pulse. The device finally outputs a byte of data from PIPR register; upon receiving this data byte, the system stops the read operation by issuing a "NO ACK" pulse. Refer Read VID Registers diagram.

Security Block

The security block forms the core of the anti-cloning protection. The security block uses a 64-bit Seed data and a 16-bit Manufacturer ID (MID) to compute a 64-bit pseudo-random code. The Seed data is typically written into the FM3580 device by the BIOS during normal operation. The MID is assigned by Fairchild and is unique to each vendor and is permanently programmed into the FM3580 by Fairchild. Reading or Writing of the MID with respect to FM3580 is not possible.

Pseudo-random code generation

Every time the PC is cold booted, BIOS reads the 64-bit seed information it wrote during previous normal operation and the 64-bit pseudo-random code from the FM3580. Using the read 64-bit seed information and the 16-bit MID, the BIOS computes and generates the pseudo-random code. If both the "BIOS computed" code and the "FM35800 read" code match, then the BIOS allows the PC to boot. Otherwise, the BIOS alters the VID configuration so that the PC is powered down. For example, the SOPR-B register can be set with a VID value for NO CPU and then switching SOPR-B data to Y-Port. On a successful boot-up, the BIOS can write a new seed number into the FM3580 in order for the security code to be rolling.

Accessing Security Block

FM3580's internal security block can be accessed via the SMBus interface by using specific command bytes in the commands that are issued to the device. SMBus operations to security block are quite similar to VID block operations except the different command bytes (register address') are used. All SMBus accesses to the security block are of block-read/write type. Following are the supported commands.

Command Byte	Command Description
0xC0h	Write 64-bit Seed number
0xC1h	Read 64-bit Seed number
0xC3h	Read 64-bit Security code

Writing Seed Number

Writing the 64-bit Seed number is done as follows. Like all SMBus command, a valid START condition starts the cycle, followed by Device address byte with Read-Write bit set to "0". On receiving a valid device address FM3580 issues an "ACK" pulse. This is followed by Write Seed number command byte (0xC0h) for which FM3580 issues an "ACK" pulse. This is followed by Byte-count byte (0x08h) indicating 8 bytes of Seed data will be sent. FM3580 issues an "ACK" pulse for the Byte-count byte. After this the system issues 8 bytes of Seed data. For each byte thus received, FM3580 issues an "ACK" pulse. After receiving the last ACK pulse, the system issues a STOP condition at which point the write operation begins internally. Refer Write Seed Number diagram.

Reading Seed Number

Reading the 64-bit Seed number is done as follows. Like all SMBus command, a valid START condition starts the cycle, followed by Device address byte with Read-Write bit set to "0". On receiving a valid device address FM3580 issues an "ACK" pulse. This is followed by Read Seed number command byte (0xC1h) for which FM3580 issues an "ACK" pulse. **The system now re-issues a START condition, followed by Device address byte with Read-Write bit set to "1".** On receiving a valid device address FM3580 issues an "ACK" pulse. Now the FM3580 is ready to readout the Seed Data. FM3580 first provides Byte-count byte (0x08h) indicating 8 bytes of Seed data will be readout. On receiving the Byte-count byte, the system issues an "ACK" pulse. After this FM3580 issues 8 bytes of Seed data. For each byte thus received, the system issues an "ACK" pulse except for the 8th byte of Seed data for which the system issues a "No ACK" pulse and issues a STOP condition to terminate the read cycle. Refer Read Seed Number diagram.

Reading Security code

Reading the 64-bit Security code is performed the same way as reading the 64-bit Seed number but with the following difference: instead of issuing by Read Seed number command byte (0xC1h), Read Security code command byte (0xC3h) should be issued. Refer Read Security code diagram. **Of the 64-bit Security code, the first bit is always "1" and should be ignored. The next 63bits represent actual security code.**

SMBus timeout

FM3580 will timeout and reset itself during any cycle whenever it detects the LOW period of the SCL clock is more than 25ms. This is in compliance to SMBus specification. After the timeout, any new command to FM3580 should begin with a new START condition. See tTIMEOUT specification under AC characteristics table.

SMBus Clock Stretching

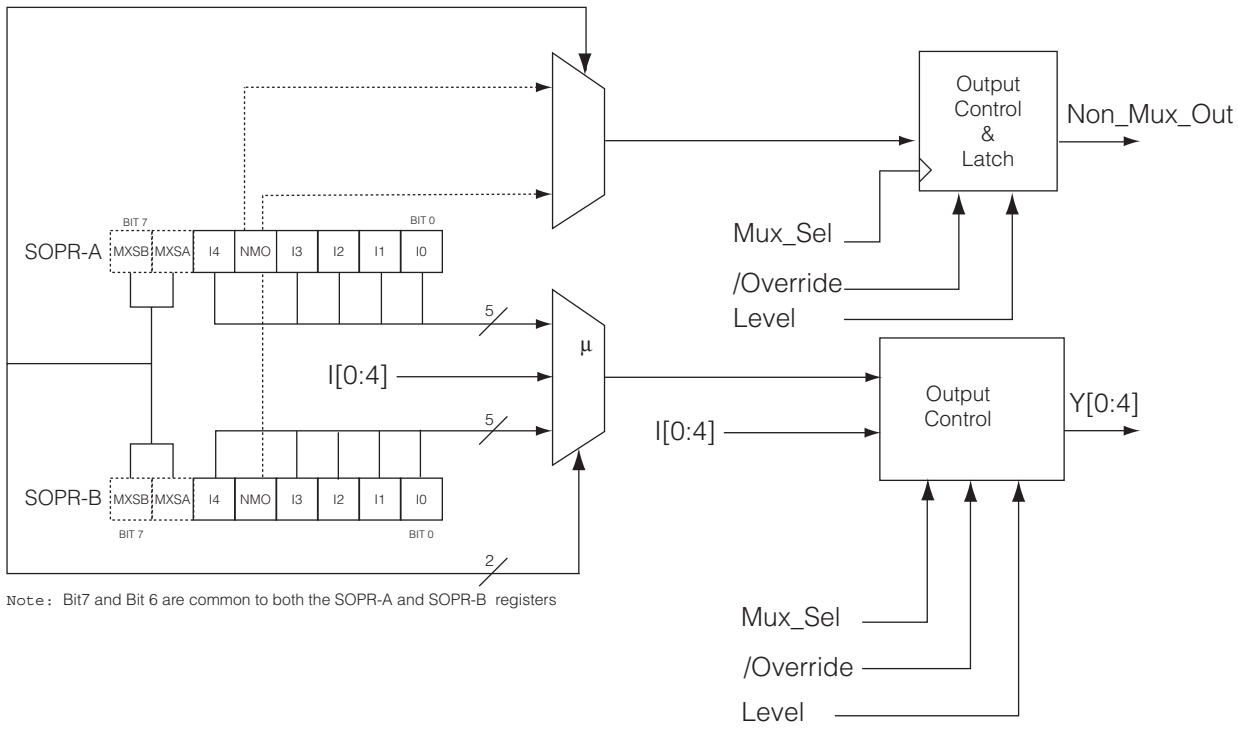
Whenever a write command is issued (VID and Seed Number writes), FM3580 will stretch the SCL clock LOW soon after the STOP condition is detected at the end of write command cycle. This clock stretching continues until the internal write is complete (duration of tWP). See "Clock Stretching Diagram".

SMBus Command compliance

Following table summarises FM3580 commands that are compliant to SMBus/IIC commands.

Commands	Compliant to
Write Seed number	SMBus (Block Write Command)
Read Seed number	SMBus (Block Read Command)
Read Security code	SMBus (Block Read Command)
Write VID Register	SMBus (Send Byte Command)
Read VID Registers	IIC Bus (Sequential Read Command)

Multiplexer Block Diagram



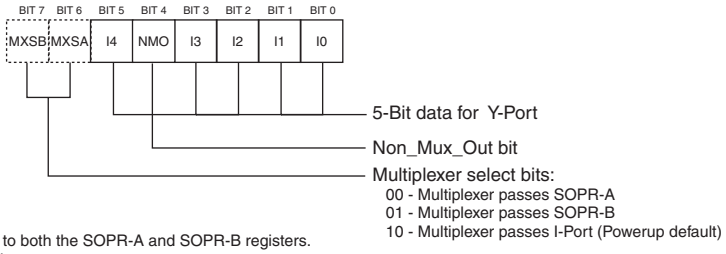
Note: Bit7 and Bit 6 are common to both the SOPR-A and SOPR-B registers

Table 1. Multiplexer Path Control

/Override Signal	Mux_Sel Signal	MXSB Bit	MXSA Bit	Y-Port Outputs Y[4:0]	Non_Mux_Out Signal
0	0	X	X	Logic “0”	Logic “0”
X	1	X	X	I-Port Inputs I[4:0]	Latched Non_Mux_Out (see Note)
1	0	0	0	Data from SOPR-A register	Data from SOPR-A register
		0	1	Data from SOPR-B register	Data from SOPR-B register
		1	0	I-Port Inputs I[4:0]	Latched Non_Mux_Out (see Note)
		1	1	Reserved (Do Not Use)	Reserved (Do Not Use)

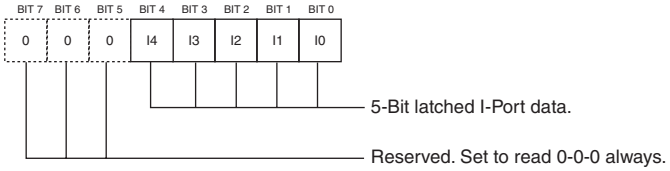
Note: Latched Non_Mux_Out is the data that was present at NMO multiplexer input during the rising edge of Mux_sel signal.

SOPR-A/B Register Diagram

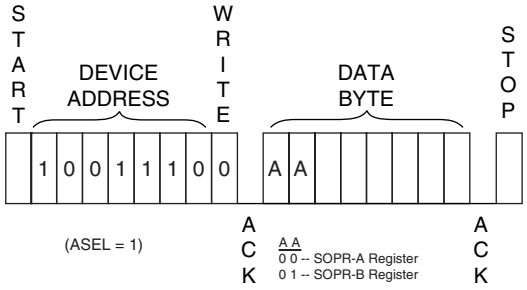


Note: -Bit 7 and Bit 6 are common to both the SOPR-A and SOPR-B registers.
-Bit 7 and Bit 6 are volatile bits.
-Bits [5:0] are non-volatile bits.

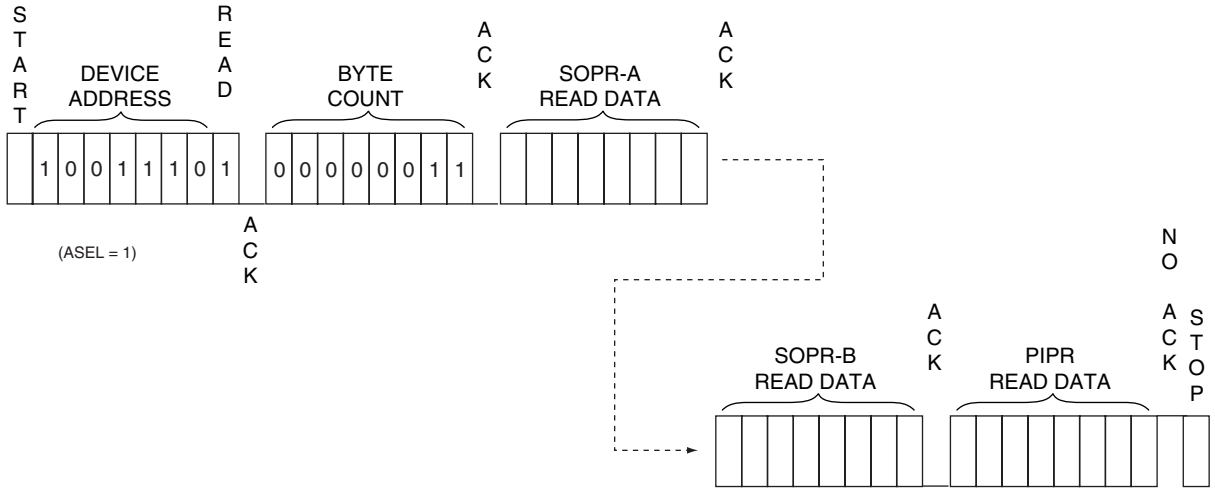
PIPR Register Diagram



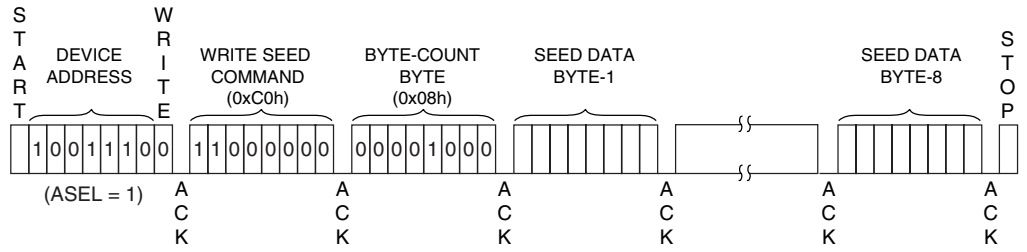
Write VID Registers Diagram



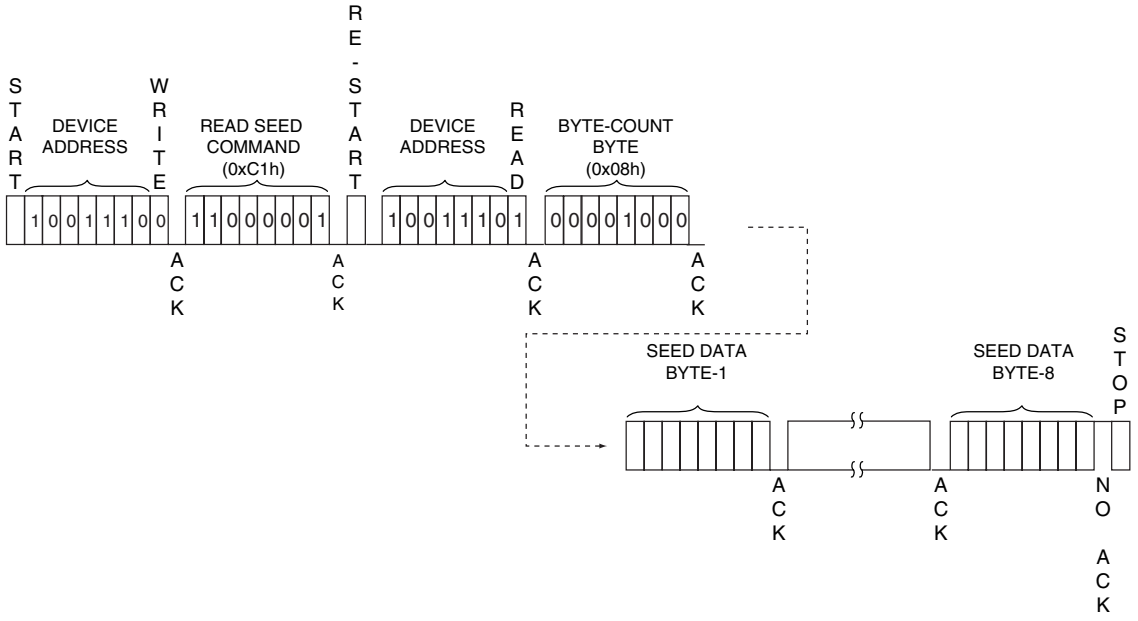
Read VID Registers Diagram



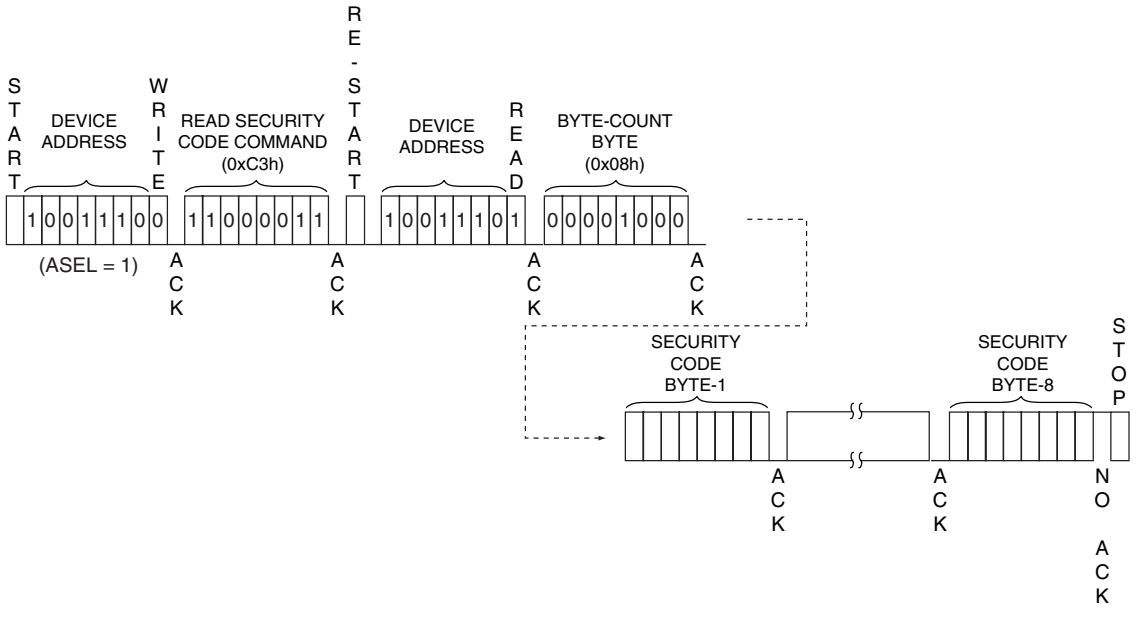
Write Seed Number Diagram



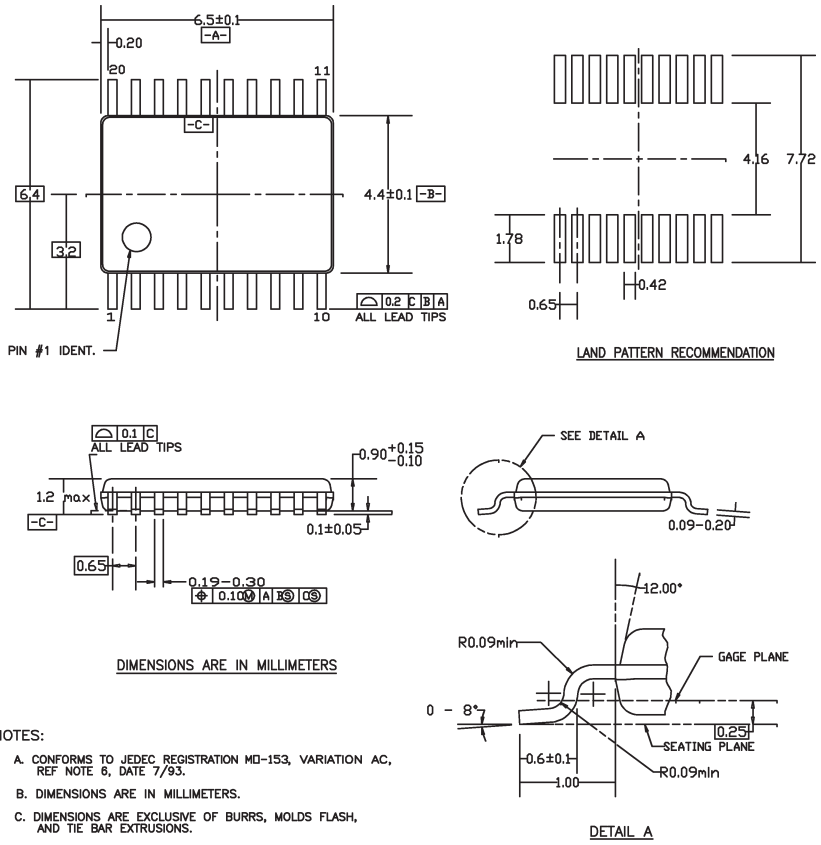
Read Seed Number Diagram



Read Security Code Diagram



Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

Package Number MTC20

Life Support Policy

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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