PM7390

S/UNI-MACH48

MULTI-SERVICE ACCESS DEVICE FOR CHANNELIZED INTERFACES

S/UNI-MACH48 ®

Data Sheet

Proprietary and Confidential

Production

Issue 4: December 2001

Legal Information

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PMC-1990823 (R4)

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Patents

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,640,398 and 5,835,602 and Canadian Patent No. 2,161,921.

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Revision History

Issue No.	Issue Date	Details of Change
4	December 2001	Created data sheet from issue 5 of the eng doc and information provided by Travis Karr. MONx_SYNCV bit polarity reversed as required. Upper and lower bounds on MAXPL specified Clarified CENTER, RSXPAUSE, TSx_REI, TSx_RMODE, FLUSH, SYNCV, SYNCI, LCDC, RDIPRIHI, RDIPRIMID, ICMPDLY, OCMPDLY, DLBEN, IPI, XOFF, INBANDADDR, BIT_ABRTE, DLCV, PTRCDIS, TSIN, POS_SEL, bit descriptions Fixed power/dc/ac specifications Added cross reference text to DT and BURST_SIZE descriptions Added glitch recovery section Fixed VDDI pin list Documented TCFP, RCFP, RXSDQ and TXSDQ counter behaviors. Clarified MINPL behavior for RCFP and RTDP Registers DS3+0x30 and DS3+0X40 were removed Update time for all PLCP counters changed to 95 DS3 clock cycles from 67 Indirect read/write behaviors clarified. IJ0J1 pin description modified to name IJ0J1[1] as the master , requiring it not to glitch, and the others to be aligned to it Clock activity monitor order fixed Updated actual behavior of TSOC Clarified SDQ configuration in section 14.13 All descriptions of IPAIS now mention that RHPP takes over when it is enabled. Revealed PERDIV[2:0] bits in RHPP Ind Reg 2, and RHPP Ind reg 7 Section 14.33 added Added R8TD Analog Control #3 register. Revealed DLL ERROR, ERRORE, and ERRORI bits. Fixed some erroneous designations of Read and Read/Write register bits. Removed statement in Operations section that stated SER_PRT_SEL switches on transport frame boundaries. Fixed up some typos.
3	November 2000	Created document from latest revision of eng. doc.
2	January 2000	Created document from latest revision of eng. doc.
1	May 1999	Document created as Preview version.

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1 Definitions

The following table defines the abbreviations for the S/UNI-MACH48.

ATM	Asynchronous Transfer Mode
CSU	Clock Synthesis Unit
DRU	Data Recovery Unit
D3 FRMR	DS3 Framer Block
DS3 PMON	DS3 Performance Monitor Block
DS3 TRAN	DS3 Transmitter Block
FEAC	Far-End Alarm and Control
FIFO	First-In-First-Out storage element
FCS	Frame Check Sequence
HCS	Header Check Sequence
HDLC	High-Level Data Link Control
LVDS	Low Voltage Differential Signaling
NNI	Network-to-Network Interface
PISO	Parallel to Serial Converter
POS	Packet Over SONET
PRBS	Pseudo-Random Bit Sequence
PRGM	SONET/SDH PRBS Generator/Monitor Block
PRGD	DS3 PRBS Generator/Detector Block
RBOC	DS3 Bit-Oriented Code Receiver Block
RCAS12	Receive 12 Channel Assigner Block
RCFP	Receive Cell and Frame Processor Block for STS-12c and STS-48c channels
RXPHY	Receive PHY Interface (UL3 or POS L3)
RXSDQ	Receive Scalable Data Queue FIFO
RDLC	Receive DS3 Data-Link Controller Block
RHPP	Receive High Order Path Processor
RTDP	Receive Time-sliced Datacom Processor Block for sub-STS-12c channels
SIPO	Serial to Parallel Converter
SIRP	SONET/SDH Inband Error Report Processor
STSI	Space and Timeslot Interchange
TCAS12	Transmit 12 Channel Assigner Block
TCFP	Transmit Cell and Frame Processor Block for STS-12c and STS-48c channels
TSI	Timeslot Interchange
TXPHY	Transmit PHY Interface (UL3 or POS L3)
TXSDQ	Transmit Scalable Data Queue FIFO
TDPR	Transmit DS3 Data-Link Controller Block
TTDP	Transmit Time-sliced Datacom Processor Block for sub-STS-12c channels
UNI	User-to-Network Interface
XBOC	DS3 Bit-Oriented Code Transmitter Block

2 Features

2.1 General

- Single chip ATM and packet processor capable of processing STS-48/STM-16 aggregate payload.
- Optionally interprets the incoming AU3/AU4 pointers to locate payload frame boundaries.
- Provides 48 ATM cell delineation blocks, 48 bit/byte HDLC processors, 48 DS3 mappers, 48 DS3 framers, and 48 PLCP framers.
- Programmable assignments for allocating STS-1 timeslots to arbitrary DS3, STS-1/STM-0, STS-3c/STM-1, STS-12c/STM-4, or STS-48c/STM-16 channels.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615(1619)/1662 of the PPP Working Group of the Internet Engineering Task Force (IETF).
- Supports a set of four duplex byte-serial 77.76 Mbyte/s STS-12c/STM-4-4c line side parallel TelecomBus interfaces which can also be grouped into a single 32-bit-wide STS-48c/STM-16c line side TelecomBus interface.
- Optionally supports two sets of four 777.6 Mbps LVDS serial TelecomBus links to transmit and receive working and protection 4xSTS-12/STM-4 or 1xSTS-48c/STM-16c line side data.
- Provides UTOPIA Level 3 32-bit wide System Interface (clocked up to 104 MHz) with parity support for ATM applications.
- Provides SATURN POS-PHY Level 3™ 32-bit System Interface (clocked up to 104 MHz) for Packet over SONET (POS), HDLC, or ATM applications.
- Provides per-channel PRBS insertion and detection.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8V CMOS device with 3.3V TTL compatible digital inputs and 3.3V CMOS/TTL compatible digital outputs.
- 560 pin Ultra BGA package.

2.2 Line Side Interface

- Provides 77.76 MHz 32-bit wide ingress and egress parallel TelecomBus line side interfaces.
- Provides capacity to carry an STS-12/STM-4 stream in each 8-bit bus in the TelecomBus interface. The four 8-bit buses can be aggregated to carry an STS-48c/STM-16c stream.

- Provides independent time-slot interchange blocks on the incoming and outgoing TelecomBus interfaces to allow arbitrary arrangement of timeslots at STS-1 granularity.
- Optionally encodes egress data to a set of four working and to a set of four protection 777.6Mbit/s LVDS serial TelecomBus links with 8B/10B-based encoding.
- Optionally decodes ingress data from a set of four working or from a set of four protection 777.6MHz LVDS serial TelecomBus links with 8B/10B-based encoding.
- Provides redundant working and protection transmit LVDS serial TelecomBus streams and redundant receive LVDS serial TelecomBus streams for protection switching purposes.
- Optionally allows selection of either working or protection serial TelecomBus link data, at the STS-1 timeslot granularity, to be directed to the device core for POS/HDLC/ATM processing.
- Provides encoding and decoding of serial TelecomBus control signals at the multiplex section termination (MST) point and high-order path termination (HPT) point.
- Uses 8B/10B-based line coding protocol on the serial links to provide transition density guarantee and DC balance and to offer a greater control character vocabulary than the standard 8B/10B protocol.
- Provides optional PRBS generation for each 8-bit bus on the outgoing parallel TelecomBus interface or for each outgoing LVDS serial TelecomBus link for off-line link verification.
- Provides PRBS detection for each 8-bit bus on the incoming parallel TelecomBus interface or for each incoming LVDS serial TelecomBus link for off-line link verification.
- Provides in-service link verification by optionally overwriting and monitoring the B1 and E1 byte of each constituent STS-1/STM-0 with a unique software programmable byte and its complement.
- Provides pins to coordinate updating of the connection map of the timeslot interchange blocks in the local device, peer and companion PM5310 TBS devices, and companion PM5372 TSE devices.

2.3 DS3 Demapper/Receiver

- Performs STS-1 demapping and destuffing of up to 48 DS3 channels.
- Complies with DS3 to STS-1 asynchronous mapping standard as stated in Bellcore, ANSI and ITU specifications
- Performs majority vote C bit decoding to detect stuff requests
- Extracts DS3 payload from the STS-1 SPE (VC3) via an elastic store
- Uses a simple bit leaking algorithm for the desynchronizer (8 bits are leaked out in four frames, 500 μsec)
- Provides DS3 frame synchronization for C-bit parity DS3 applications as per ANSI-107.
- DS3 Far end alarm channel code detection is provided.

- Provides an integral path maintenance data-link controller with a 128-byte FIFO for each DS3 channel.
- Provides PLCP frame synchronization for DS3 PLCP formatted streams.
- Provides programmable pseudo-random test-sequence detection (up to 2^{32}-1 bit length patterns conforming to ITU-T O.151 standards) and analysis features in DS3 payload.
- Detects and records DS3 alarms, framing errors, parity errors, path parity errors, and FEBE events.

2.4 DS3 Mapper/Transmitter

- Maps a DS3 data stream into an STS-1/STM-0 SPE/VC3.
- Complies with DS3 to STS-1 asynchronous mapping standard as stated in Bellcore, ANSI and ITU specifications
- Accepts DS3 compliant serial data stream with an associated clock (44.736 MHz nominal rate)
- Inserts DS3 AIS (Framed with 1010… repeating data bits) via a microprocessor register bit or TAISGEN input pin
- Performs required C bit encoding for stuff requests
- Sets all fixed stuff (R) bits to zeros or ones per microprocessor control register bit
- Provides DS3 frame insertion for C-bit parity DS3 applications, alarm insertion, and diagnostic features as per ANSI-107.
- DS3 Far end alarm channel code insertion is provided.
- Provides an integral path maintenance data-link controller with a 128-byte FIFO for each DS3 channel.
- Provides frame insertion and path overhead insertion for DS3 based PLCP. In addition, alarm insertion and diagnostic features are provided.
- Provides programmable pseudo-random test sequence generation (up to 2^{32}-1 bit length sequences conforming to ITU-T O.151 standards). Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

2.5 The Receive ATM Processor

- Extracts ATM cells from the received STS-48c/STM16c/STS-12c/STM-4c/STS-3c/STM-1/STS-1/DS3 channel payloads using ATM cell delineation.
- Provides ATM cell payload de-scrambling.
- Performs header check sequence (HCS) error detection and idle/unassigned cell filtering.
- Detects out of cell delineation (OCD) and loss of cell delineation (LCD) alarms.
- Counts number of received cells, idle cells, erred cells and dropped cells.

- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide datapath interfaces (clocked up to 104 MHz) with parity support to read extracted cells from an internal scalable channel FIFO.
- Provides a highly configurable PHY servicing algorithm for POS-PHY Level 3 applications.

2.6 The Receive POS Processor

- Supports packet based link layer protocols using bit and byte synchronous HDLC framing such as PPP, HDLC and Frame Relay.
- Optionally performs self-synchronous POS data de-scrambling on the received STS-48c/STM16c/STS-12c/STM-4c/STS-3c/STM-1/STS-1 channel payloads using the $x^{43}+1$ polynomial.
- Performs flag sequence detection and terminates the received POS/HDLC frames.
- Performs frame check sequence (FCS) validation for CRC-CCITT and CRC-32 polynomials.
- Performs control escape de-stuffing or bit de-stuffing of the POS/HDLC stream.
- Detects for packet abort sequence.
- Checks for minimum and maximum packet lengths. Optionally deletes short packets and marks those exceeding the maximum length as erred.
- Permits FCS stripping on the POS-PHY output data stream.
- Provides a SATURN POS-PHY Level 3 compliant 32-bit datapath interface (clocked up to 104 MHz) with parity support to read packet data from an internal scalable channel FIFO.
- Provides a highly configurable PHY servicing algorithm for POS-PHY Level 3 applications.

2.7 The Transmit ATM Processor

- Provides idle/unassigned cell insertion.
- Optionally provides HCS generation/insertion, and ATM cell payload scrambling.
- Counts the number of transmitted cells.
- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide datapath interfaces (clocked up to 104 MHz) with parity support for writing cells into an internal channel FIFO.

2.8 The Transmit POS Processor

- Supports any packet based link layer protocol using byte synchronous and bit synchronous framing like PPP, HDLC and Frame Relay.
- Optionally performs self-synchronous scrambling using the $1+X^{43}$ polynomial.
- Encapsulates packets within a POS/HDLC frame.
- Performs flag sequence insertion.
- Performs byte stuffing or bit stuffing for transparency processing.

- Optionally performs frame check sequence generation using the CRC-CCITT and CRC-32 polynomials.
- Aborts packets under the direction of the host or when the FIFO underflows.
- Provides a SATURN POS-PHY Level 3 compliant 32-bit wide datapath (clocked up to 104 MHz) with parity support to an internal FIFO buffer.

3 Applications

- ATM and Multi-service Switches, routers, and packet switches
- Channelized ATM and POS interfaces
- SONET/SDH Add/Drop Multiplexers with data processing capabilities

4 References

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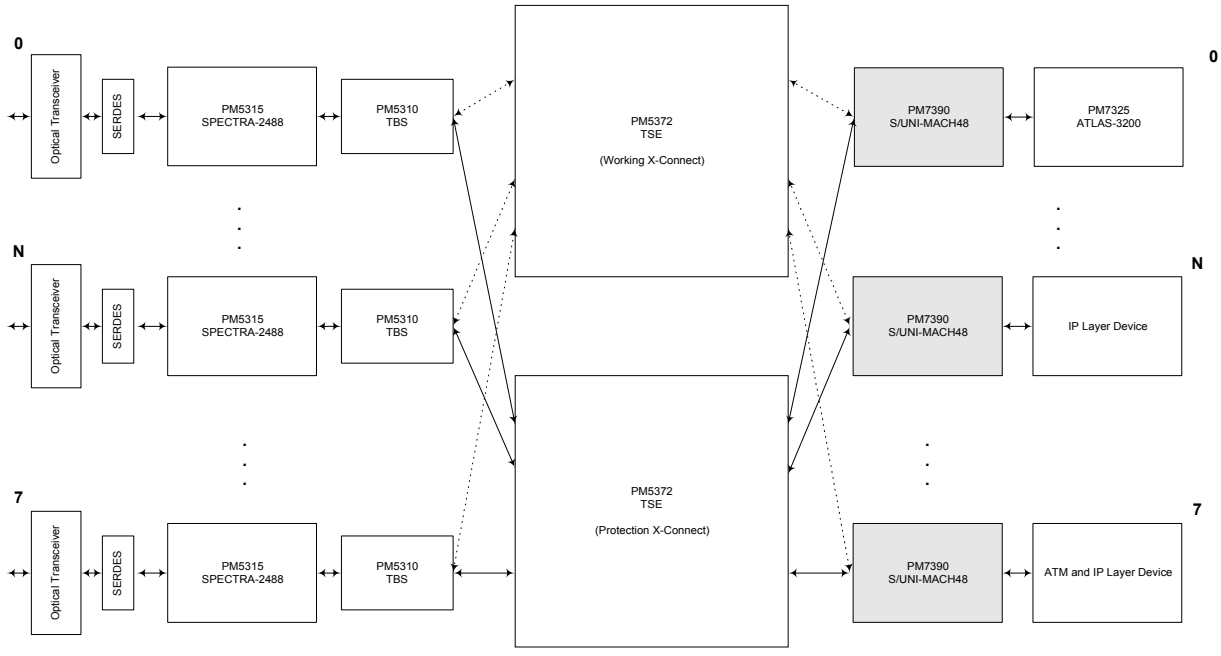
5 Application Examples

The PM7390 S/UNI-MACH48® device is applicable to equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interfaces (UNI), ATM Network-Network Interfaces (NNI), as well as Packet over SONET (POS) interfaces. The POS interface can support several packet based protocols, including the Point-to-Point Protocol (PPP) and HDLC.

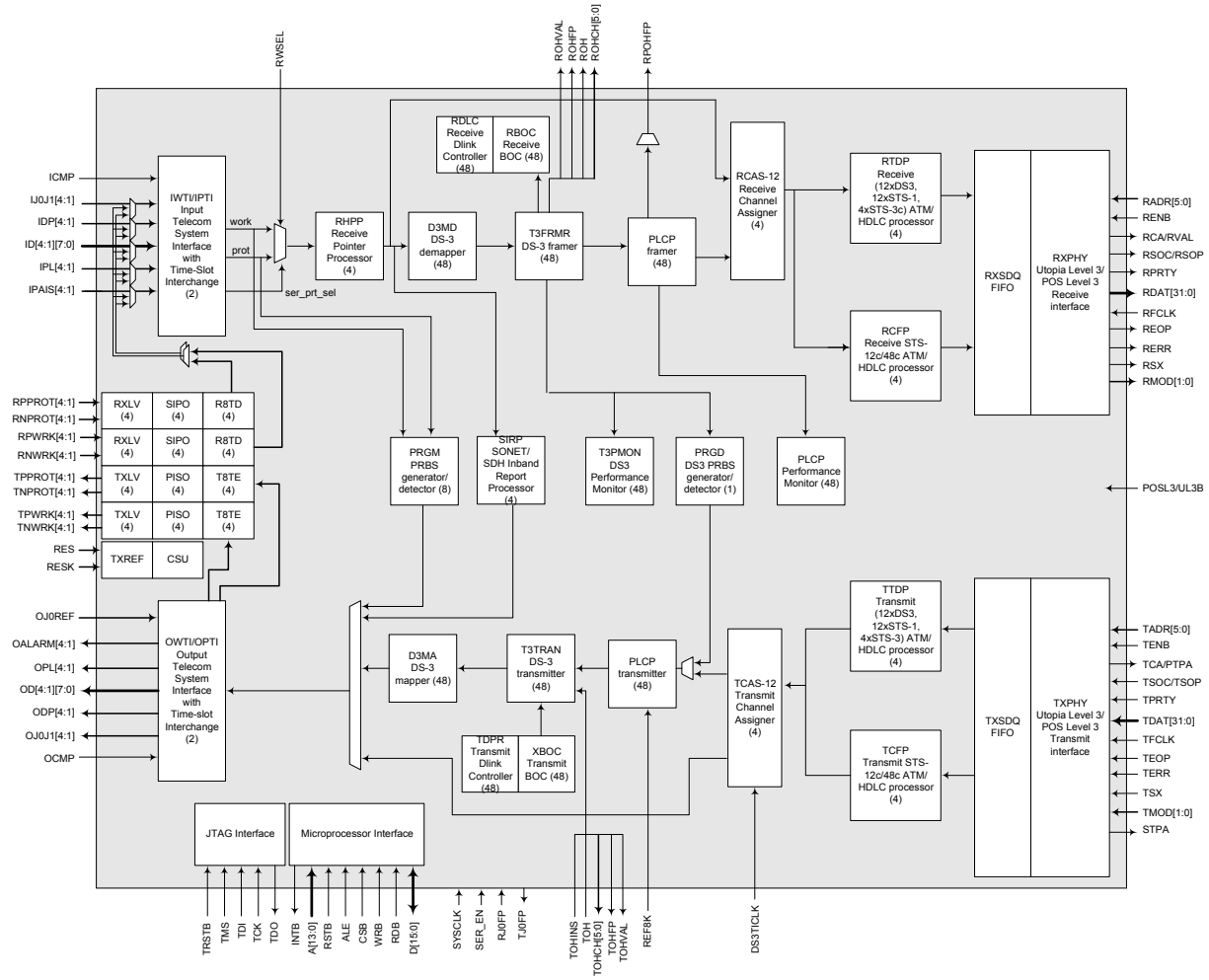
In a typical ATM or POS/HDLC application, the S/UNI-MACH48 performs ATM and POS/HDLC processing on channelized data streams contained within an STS-48/STM-16. The channelized data streams are passed to/from the S/UNI-MACH48 from/to a SONET/SDH framer device like the PM5315 SPECTRA-2488™ device, PM5313 SPECTRA-622™ device, or the PM5316 SPECTRA-4x155™ device. For a system with multiple channelized STS-48 streams, the data streams can pass through a cross-connect switch element (PM5372 TSE™ device) to direct each channel to the appropriate S/UNI-MACH48 or framer.

On the system side, the S/UNI-MACH48 interfaces directly with ATM or POS layer processors and switching or adaptation functions using a UTOPIA Level 3 or POS-PHY Level 3™ 32-bit device (clocked up to 104 MHz) synchronous FIFO style interface. The initial configuration and ongoing control and monitoring of the S/UNI-MACH48 are provided via a generic microprocessor interface.

Figure 1 Multi-Service ATM/POS Switch Port Application

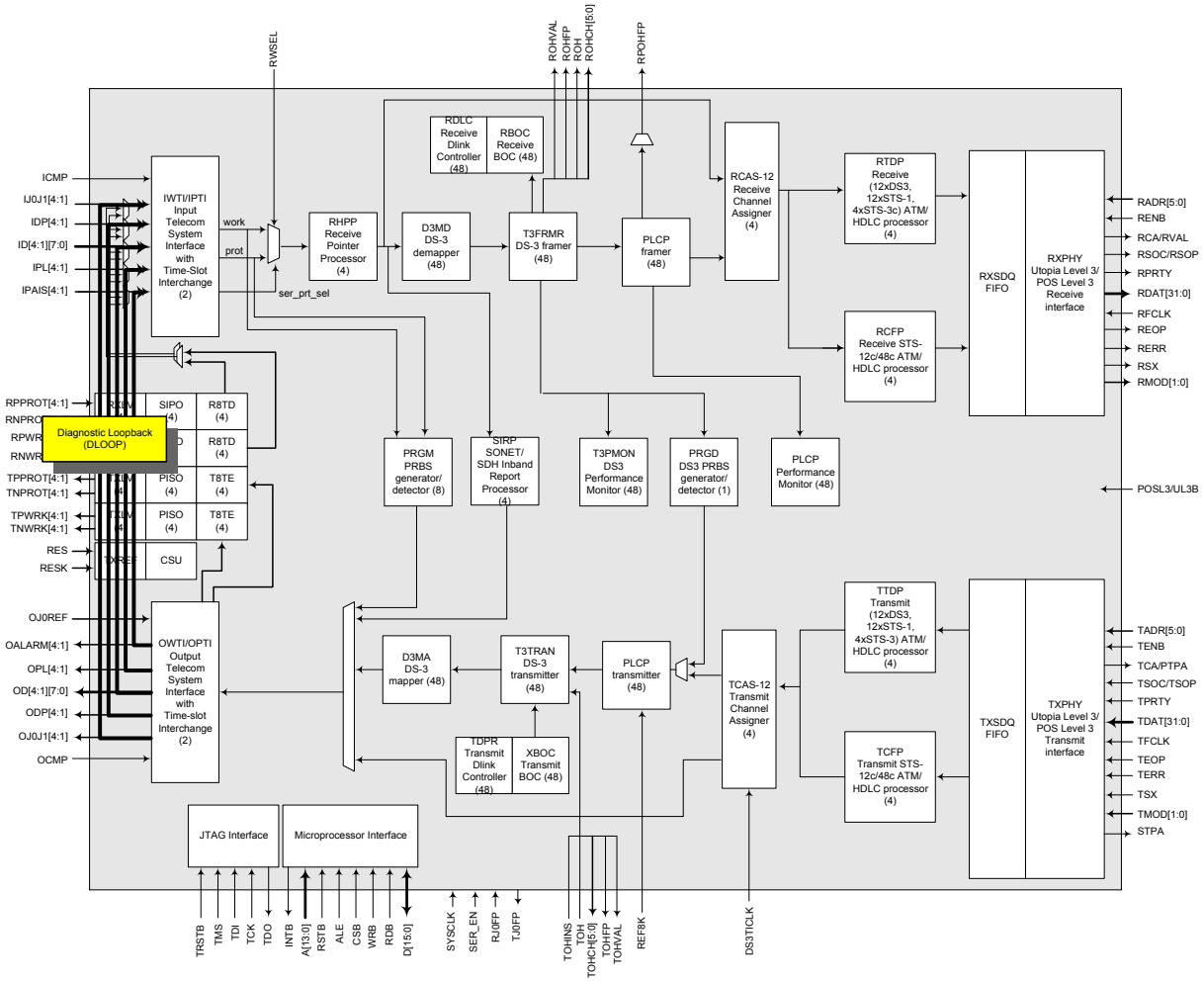


6 Block Diagram

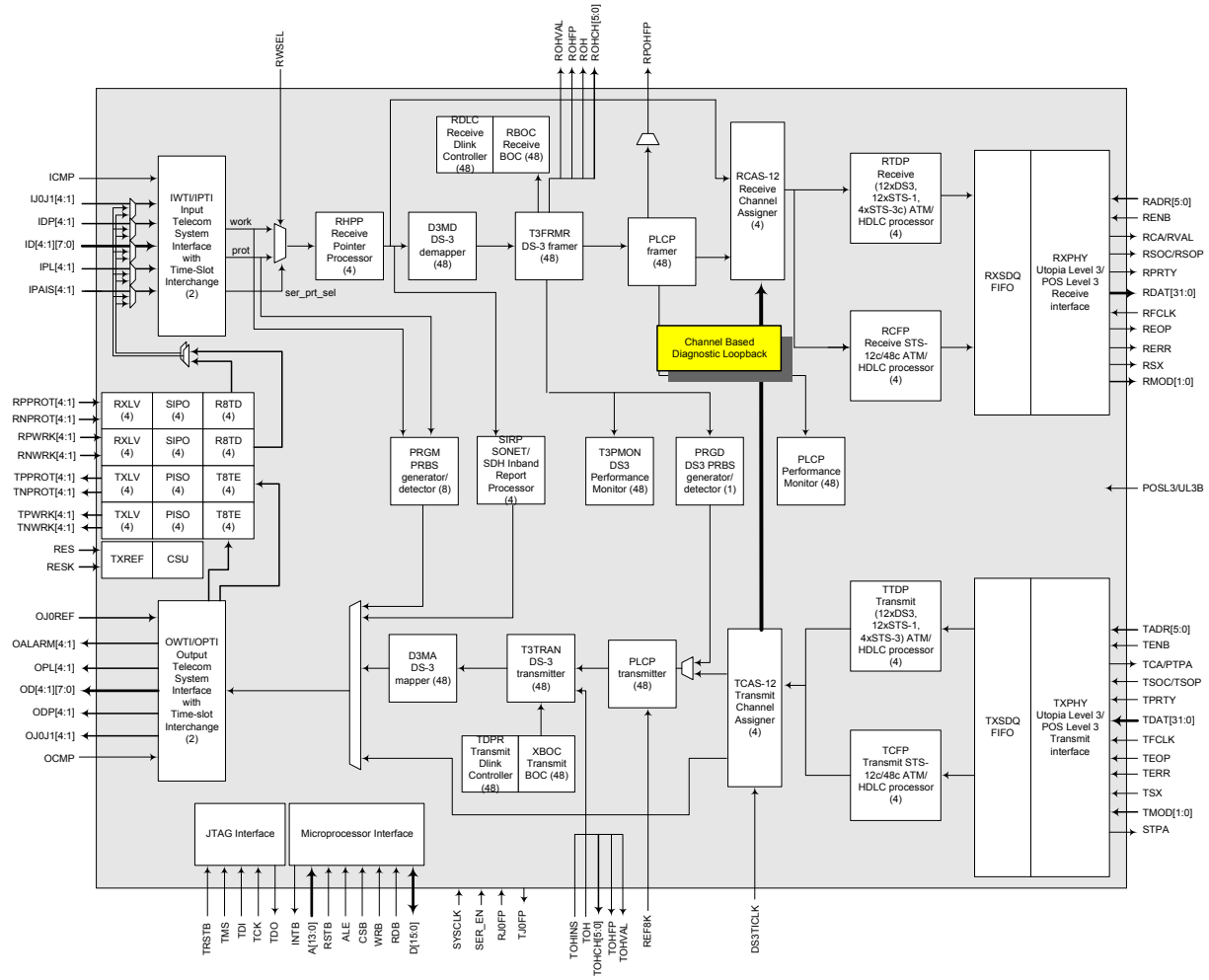


7 Loopback Configurations

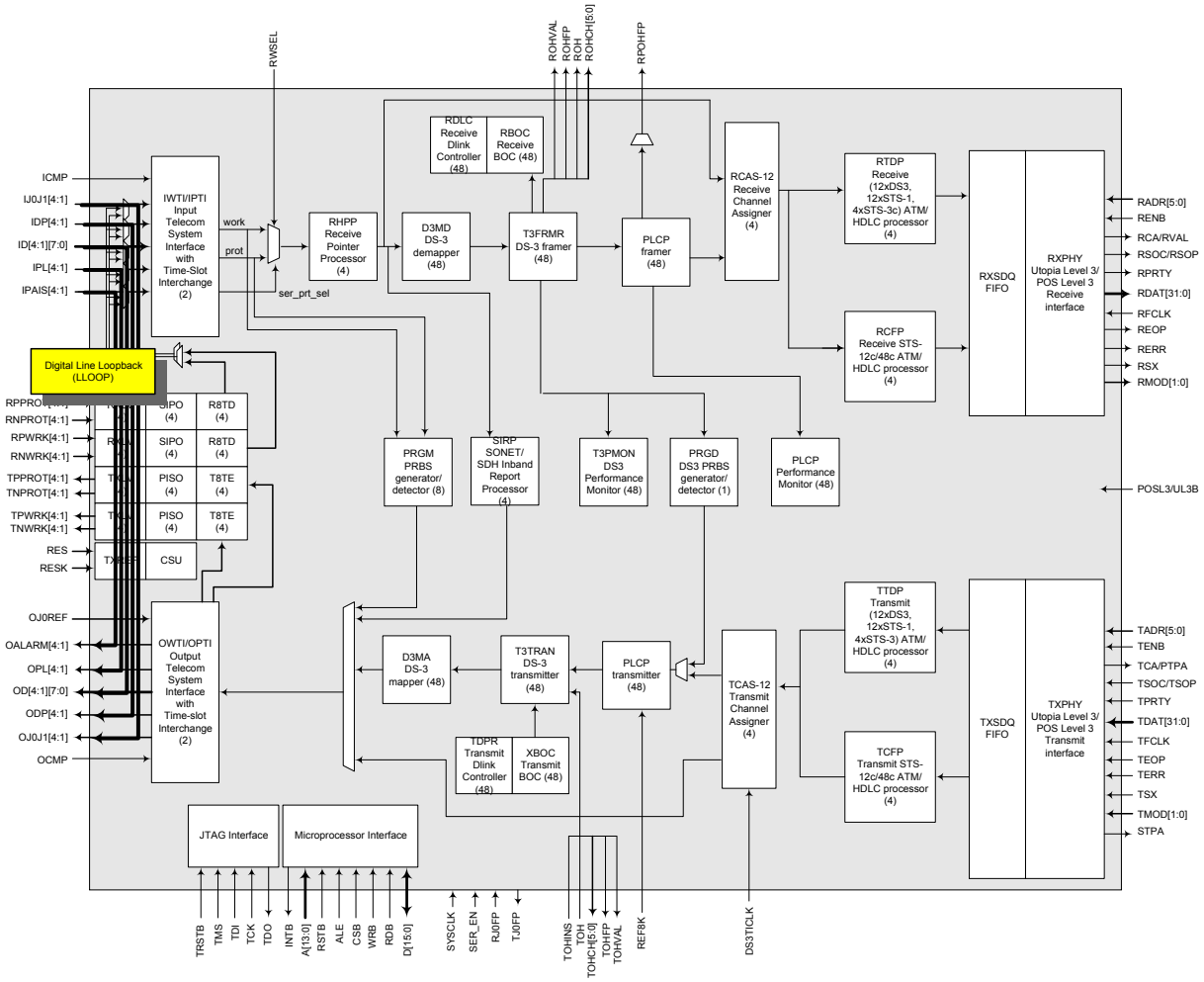
7.1 Parallel TelecomBus Diagnostic Loopback



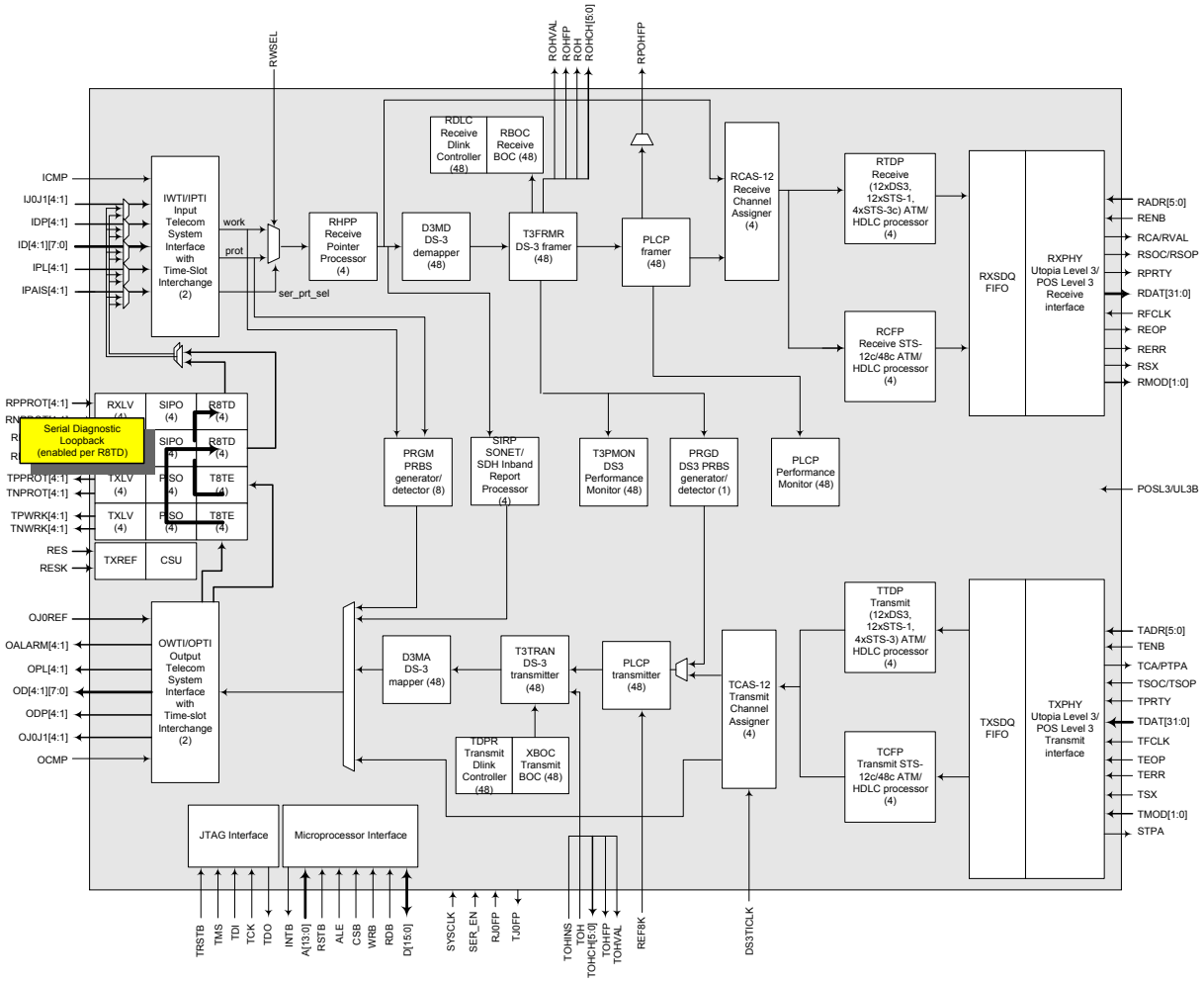
7.2 Channel-Based Diagnostic Loopback (Sub STS-48c Only)



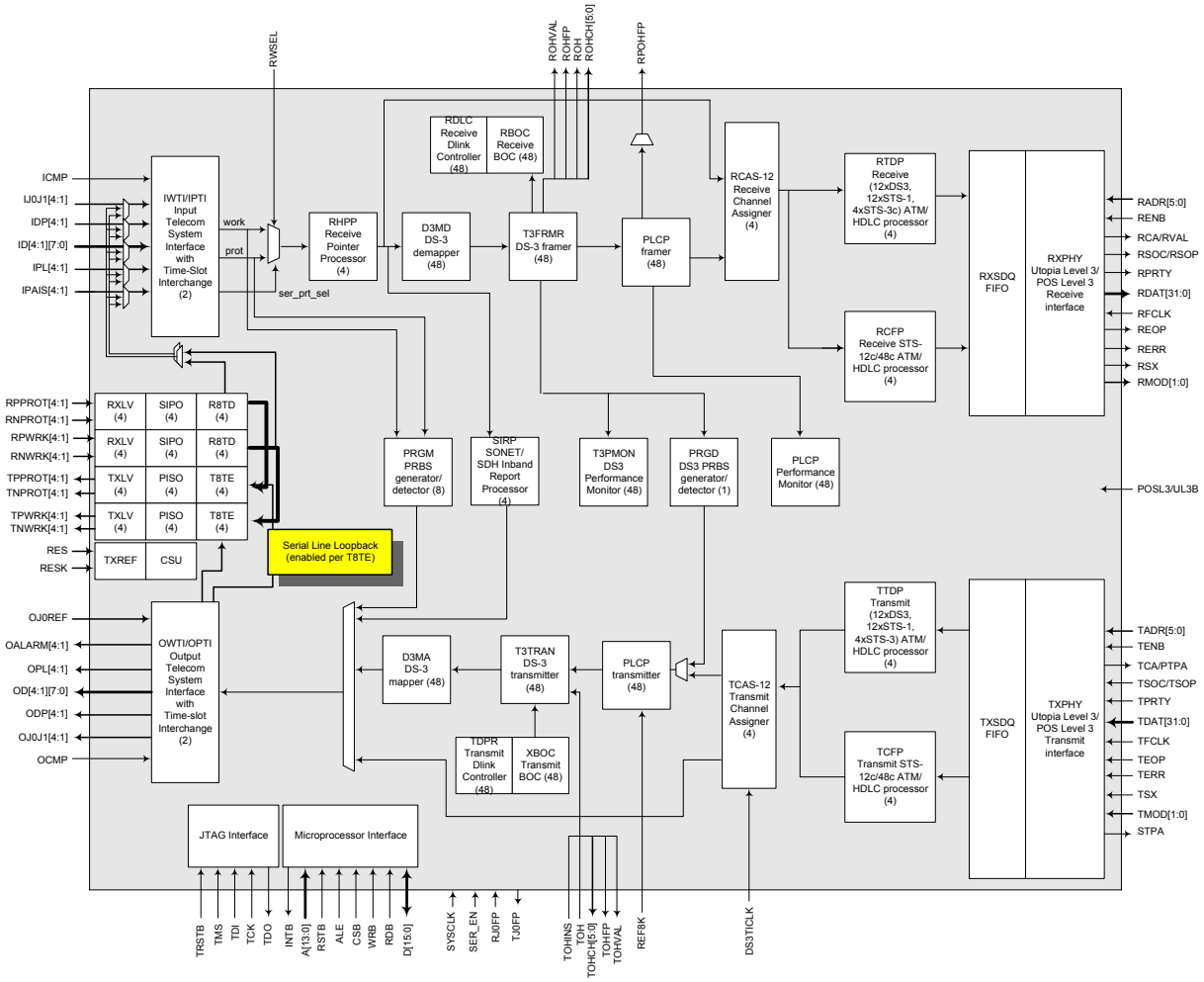
7.3 Parallel TelecomBus Line Loopback



7.4 Serial TelecomBus Diagnostic Loopback



7.5 Serial TelecomBus Line Loopback



8 Description

The PM7390 S/UNI-MACH48 is a monolithic integrated circuit that implements ATM mapping and Packet over SONET/SDH mapping functions for a channelized STS-48/STM-16 stream. The 2.488Gb/s stream can consist of a single STS-48c/STM-16c or a combination of STS-12c/STM-4c, STS-3c/STM-1, STS-1/STM-0, and DS3 channels.

8.1 Receive Direction

The S/UNI-MACH48 can be configured to use either a 77.76 MHz TTL compatible parallel TelecomBus or a set of 777.6 Mbps LVDS compatible serial TelecomBus line-side interface to transmit and receive SONET/SDH data streams.

The incoming TTL compatible parallel TelecomBus can carry an STS-48/STM-16 stream or four STS-12/STM-4 streams that share a common clock and a common transport frame alignment. The parallel TelecomBus interface is compatible with SONET/SDH framers such as the SPECTRA-2488, SPECTRA-622, and SPECTRA-4x155.

Each incoming LVDS compatible serial TelecomBus link carries a constituent STS-12/STM-4 of an STS-48/STM-16 stream. Bytes on the links are carried on an extended 8B/10B character set which encodes TelecomBus data and control signals.

The S/UNI-MACH48 optionally performs AU3/AU4 pointer processing to account for positive and negative pointer justifications on the incoming data streams.

A pseudo-random bit sequence (PRBS) processor is provided to monitor the decoded payload for the $X^{23} + X^{18} + 1$ pattern. The PRBS processor is configurable to handle all legal mixes of STS-1/AU3, STS-3c/AU4, STS-12c/AU4-4c and STS-48c/AU4-16c in the serial TelecomBus or parallel TelecomBus interface. When using the serial TelecomBus, data to the S/UNI-MACH48 core may be sourced from arbitrary time-slots of any of the two sets of LVDS links.

A DS-3 demapper permits extraction of the DS-3 frame from an STS-1 SPE as per Bellcore, ANSI, and ITU specifications. A full featured DS-3 framer provides framing and error accumulation in accordance with ANSI T1.107, and T1.107a. The DS3 framer frames to a DS3 signal with a maximum average reframe time of 1.5 ms and detects framing bit errors, parity errors, path parity errors, AIS, far end receive failure, and idle code. The DS3 overhead bits are extracted and presented on multiplexed serial outputs. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microprocessor port.

PLCP sublayer DS3 processing is also supported. In the PLCP receive direction, framing is provided. BIP-8 error events, frame octet error events and far end block error events are accumulated.

A single DS3 PRBS detectors permits DS3 line error diagnostics on the selected DS3 channel.

The S/UNI-MACH48 allows the SONET/SDH payload to be configured as a single STS-48c/STM-16-16c or as any valid combination of STS-12c/STM-4c, STS-3c/STM-1, STS-1, and DS3 channels. The STS-48c/STM-16-16c channel fills the entire bandwidth of the S/UNI-MACH48 and is assigned to channel number 0. STS-12c/STM-4c channels can be assigned to channels 0, 12, 24, and 36. STS-3c/STM-1 channels can be assigned within a range associated with the STS-12 stream which it belongs to. STS-1/STM-0 and DS3 channels can be assigned to any timeslot not already allocated to others but must also reside within the range of channel values allocated to the STS-12 stream which it belongs to.

When used to implement an ATM UNI or NNI, the S/UNI-MACH48 frames to the ATM payload using cell delineation. The ATM cell payloads are descrambled and are written to a four cell or greater FIFO buffer. The per-channel FIFO size is scalable from 2 cells to 48 cells in size. The total FIFO space available is 192 cells. The received cells are read from the FIFO using a 32-bit wide UTOPIA Level 3 or POS-PHY Level 3 (clocked up to 104 MHz) datapath interface. Counts of received ATM cells and erred ATM headers are accumulated for performance monitoring purposes.

When used to implement packet transmission over a SONET/SDH link, the S/UNI-MACH48 extracts Packet over SONET (POS) and HDLC frames from the SONET/SDH synchronous payload envelope and de-mapped DS3 streams. Frames are verified for correct construction and size. The control escape and bit-stuffing characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive FIFO. FIFO size for each channel is scalable from 128 bytes to 3072 bytes. The total FIFO space available is 12,288 bytes. The received packets are read from the FIFO through a 32-bit POS-PHY Level 3 (clocked up to 104 MHz) system side interface. Valid and FCS erred packet counts are provided for performance monitoring. The S/UNI-MACH48 Packet over SONET implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay.

8.2 Transmit Direction

In the egress direction, the S/UNI-MACH48 transmits the SONET/SDH frame(s) via a parallel TelecomBus interface at 77.76 MHz or a set of 777.6 Mbps LVDS compatible serial TelecomBus links.

Each parallel TelecomBus interface can accommodate a set of four STS-12/STM-4 data streams or an STS-48c/STM-16 data stream. The TelecomBus interface passes appropriate SONET/SDH framing markers along with the data. This allows the S/UNI-MACH48 to interface seamlessly to SONET/SDH framers such as the SPECTRA-2488, SPECTRA-622, and SPECTRA-4x155.

The outgoing LVDS compatible serial TelecomBus stream data is encoded in an extended set of 8B/10B characters and transferred onto two independent sets of 777.6 Mbps LVDS links. Transport and payload frame boundaries, pointer justification events and alarm conditions are marked by 8B/10B control characters. Two sets of links are available. One can be used for working traffic and the other can be used for protection traffic.

Outgoing payload bytes may be optionally overwritten with the $X^{23} + X^{18} + 1$ PRBS pattern for diagnosis of downstream equipment. The PRBS processor is configurable to handle all legal mixes of STS-1/AU3, STS-3c/AU4, STS-12c/AU4-4c and STS-48c/AU4-16c in the incoming TelecomBus interface. A time-slot interchange block is provided to allow arbitrary remapping of streams at STS-1/AU3 granularity. Multicast is supported.

In the DS3 transmit direction, the S/UNI-MACH48 inserts DS3 framing, X, and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for insertion of the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication Signals can be inserted by using internal register bits; other status signals such as the idle signal can be inserted when enabled by internal register bits. The DS-3 frame is mapped into an STS-1 SPE as per Bellcore, ANSI, and ITU specifications.

A single DS3 PRBS generator permits DS3 line error diagnostics at the far end for a selected DS3 channel.

In the PLCP transmit direction, the S/UNI-MACH48 provides overhead insertion using internal registers, DS3 nibble stuffing, automatic BIP-8 octet generation and insertion and automatic far end block error insertion. Diagnostic features for BIP-8 error, framing error and far end block error insertion are also supported.

The S/UNI-MACH48 allows the ATM or POS data streams to be channelized into an STS-48c/STM-16-16c or as any valid combination of STS-12c/STM-4c, STS-3c/STM-1, STS-1, and DS3 channels. The STS-48c/STM-16-16c channel fills the entire bandwidth of the S/UNI-MACH48 and is assigned to channel number 0. STS-12c/STM-4c channels can be assigned to channels 0, 12, 24, and 36. STS-3c/STM-1 channels can be assigned within a range associated with the STS-12 stream which it belongs to. STS-1/STM-0 and DS3 channels can be assigned to any timeslot not already allocated to others but must also reside within the range of channel values allocated to the STS-12 stream which it belongs to

When used to implement an ATM UNI or NNI, ATM cells are written to an internal FIFO using a 32-bit wide UTOPIA Level 3 or POS-PHY Level 3 (clocked up to 104 MHz) datapath interface. The per-channel FIFO size is scalable from 2 cells to 48 cells in size. The total FIFO space available is 192 cells. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI-MACH48 provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement a Packet over SONET/SDH or HDLC link, the S/UNI-MACH48 inserts POS/HDLC frames into the SONET/SDH synchronous payload envelope or DS3 stream. Packets to be transmitted are written into a FIFO through a 32-bit SATURN POS-PHY Level 3 (clocked up to 104 MHz) system side interface. The per-channel FIFO size is scalable from 128 bytes to 3072 bytes in size. The total FIFO space available is 12,288 bytes. POS/HDLC frames are built by inserting the flags, bit stuffs, control escape characters and the FCS fields. Either the CRC-CCITT or CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

8.3 General

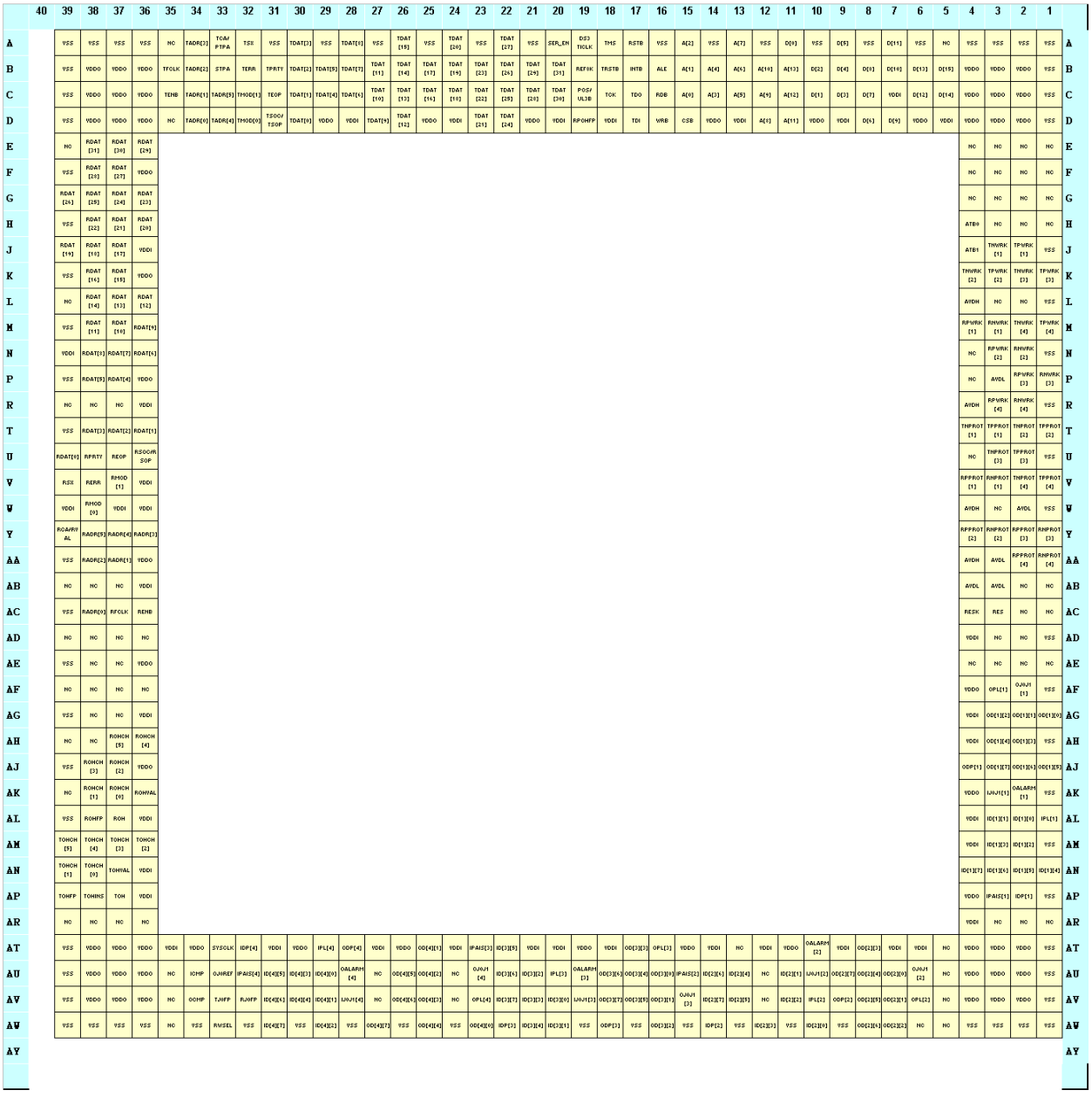
The S/UNI-MACH48 is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The S/UNI-MACH48 also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-MACH48 is implemented in low power, +1.8 Volt, CMOS technology with 3.3V TTL compatible digital inputs and 3.3V TTL/CMOS compatible digital outputs. The S/UNI-MACH48 is packaged in a 560 pin UBGA package.

9 Pin Diagram

The S/UNI-MACH48 is available in a 560 pin UBGA package having a body size of 40 mm by 40 mm and a ball pitch of 1.0 mm.

Figure 2 Pin Diagram – Bottom View



	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		VSS	VSS	VSS	VSS	NC	TADR[3]	TCA/ PTPA	TSX	VSS	TDAT[3]	VSS	TDAT[4]	VSS	TDAT [19]	VSS	TDAT [20]	VSS	TDAT [27]	VSS	SER_EN	DS3 TICLK	TMS	RSTB	VSS	A[2]	VSS	A[7]	VSS	D[0]	VSS	D[5]	VSS	D[11]	VSS	NC	VSS	VSS	VSS	VSS	A
B		VSS	VDDO	VDDO	VDDO	TFCLK	TADR[2]	STPA	TERR	TPRTY	TDAT[2]	TDAT[5]	TDAT[7]	TDAT [11]	TDAT [14]	TDAT [17]	TDAT [18]	TDAT [23]	TDAT [26]	TDAT [29]	TDAT [31]	REFIIC	TRSTB	INTB	ALE	A[1]	A[4]	A[6]	A[10]	A[13]	D[2]	D[4]	D[8]	D[10]	D[13]	D[15]	VDDO	VDDO	VDDO	VSS	B
C		VSS	VDDO	VDDO	VDDO	TENB	TADR[1]	TADR[5]	TMOD[1]	TEOP	TDAT[1]	TDAT[4]	TDAT[6]	TDAT [10]	TDAT [13]	TDAT [16]	TDAT [19]	TDAT [22]	TDAT [25]	TDAT [28]	TDAT [30]	POS/ VL3B	TCK	TDO	RDB	A[0]	A[3]	A[9]	A[5]	A[12]	D[1]	D[3]	D[7]	VDDI	D[12]	D[14]	VDDO	VDDO	VDDO	VSS	C
D		VSS	VDDO	VDDO	VDDO	NC	TADR[0]	TADR[4]	TMOD[0]	TSOC/ TSOP	TDAT[0]	VDDO	VDDI	TDAT[8]	TDAT [12]	VDDO	VDDI	TDAT [21]	TDAT [24]	VDDO	VDDI	RPOHFP	VDDI	TDI	WRB	CSB	VDDO	VDDI	A[8]	A[11]	VDDO	VDDI	D[6]	D[9]	VDDO	VDDI	VDDO	VDDO	VDDO	VSS	D
E		NC	RDAT [31]	RDAT [30]	RDAT [29]																															NC	NC	NC	NC	E
F		VSS	RDAT [28]	RDAT [27]	VDDO																															NC	NC	NC	NC	F
G		RDAT [26]	RDAT [25]	RDAT [24]	RDAT [23]																															NC	NC	NC	NC	G
H		VSS	RDAT [22]	RDAT [21]	RDAT [20]																															ATB9	NC	NC	NC	H
J		RDAT [19]	RDAT [18]	RDAT [17]	VDDI																															ATB1	TNVRK [1]	TPVRK [1]	VSS	J
K		VSS	RDAT [16]	RDAT [15]	VDDO																															TNVRK [2]	TPVRK [2]	TNVRK [3]	TPVRK [3]	K
L		NC	RDAT [14]	RDAT [13]	RDAT [12]																															AVDH	NC	NC	VSS	L
M		VSS	RDAT [11]	RDAT [10]	RDAT[9]																															RPVRK [1]	RNVRK [1]	TNVRK [4]	TPVRK [4]	M
N		VDDI	RDAT[6]	RDAT[7]	RDAT[8]																															NC	RPVRK [2]	RNVRK [2]	VSS	N
P		VSS	RDAT[5]	RDAT[4]	VDDO																															NC	AVDL	RPVRK [3]	RNVRK [3]	P
R		NC	NC	NC	VDDI																															AVDH	RPVRK [4]	RNVRK [4]	VSS	R
T		VSS	RDAT[3]	RDAT[2]	RDAT[1]																															THPROT [1]	TPPROT [1]	THPROT [2]	TPPROT [2]	T
U		RDAT[0]	RPRTY	REOP	RSOC/R SOP																															NC	THPROT [3]	TPPROT [3]	VSS	U
V		RSX	RERR	RMOD [1]	VDDI																															RPPROT [1]	RNPROT [1]	THPROT [4]	TPPROT [4]	V
W		VDDI	RMOD [0]	VDDI	VDDI																															AVDH	NC	AVDL	VSS	W
Y		ROAPRTY AL	RADR[3]	RADR[4]	RADR[3]																															RPPROT [2]	RNPROT [2]	RPPROT [3]	RNPROT [3]	Y
AA		VSS	RADR[2]	RADR[1]	VDDO																															AVDH	AVDL	RPPROT [4]	RNPROT [4]	AA
AB		NC	NC	NC	VDDI																															AVDL	AVDL	NC	NC	AB
AC		VSS	RADR[0]	RFCLK	RENB																															RESK	RES	NC	NC	AC
AD		NC	NC	NC	NC																															VDDI	NC	NC	VSS	AD
AE		VSS	NC	NC	VDDO																															NC	NC	NC	NC	AE
AF		NC	NC	NC	NC																															VDDO	OPL[1]	OJAJ1 [1]	VSS	AF
AG		VSS	NC	NC	VDDI																															VDDI	OD[1][2]	OD[1][1]	OD[1][0]	AG
AH		NC	NC	ROMCH [5]	ROMCH [4]																															VDDI	OD[1][4]	OD[1][3]	VSS	AH
AJ		VSS	ROMCH [3]	ROMCH [2]	VDDO																															ODP[1]	OD[1][7]	OD[1][6]	OD[1][5]	AJ
AK		NC	ROMCH [1]	ROMCH [0]	ROHVAL																															VDDO	LOJAJ[1]	OALARM [1]	VSS	AK
AL		VSS	ROHFP	ROH	VDDI																															VDDI	ID[1][1]	ID[1][0]	IPL[1]	AL
AM		TOHCH [5]	TOHCH [4]	TOHCH [3]	TOHCH [2]																															VDDI	ID[1][3]	ID[1][2]	VSS	AM
AN		TOHCH [1]	TOHCH [0]	TOHVAL	VDDI																															ID[1][7]	ID[1][6]	ID[1][5]	ID[1][4]	AN
AP		TOHFP	TOHINS	TOH	VDDI																															VDDO	IPAIS[1]	IDP[1]	VSS	AP
AR		NC	NC	NC	NC																															VDDI	NC	NC	NC	AR
AT		VSS	VDDO	VDDO	VDDO	VDDI	VDDO	SYSCLK	IDP[4]	VDDI	VDDO	IPL[4]	ODP[4]	VDDI	VDDO	OD[4][1]	VDDI	IPAIS[3]	ID[3][5]	VDDI	VDDI	VDDO	VDDI	OD[3][3]	OPL[3]	VDDO	VDDI	NC	VDDI	VDDO	OALARM [2]	VDDI	OD[3][3]	VDDI	VDDI	NC	VDDO	VDDO	VDDO	VSS	AT
AU		VSS	VDDO	VDDO	VDDO	NC	IOHP	OJAREF	IPAIS[4]	ID[4][5]	ID[4][3]	ID[4][0]	OALARM [4]	NC	OD[4][5]	OD[4][2]	NC	OJAJ1 [4]	ID[3][4]	ID[3][2]	IPL[3]	OALARM [3]	OD[3][6]	OD[3][4]	OD[3][0]	IPAIS[2]	ID[2][6]	ID[2][4]	NC	ID[2][1]	LOJAJ[2]	OD[2][7]	OD[2][4]	OD[2][0]	OJAJ1 [2]	NC	VDDO	VDDO	VDDO	VSS	AU
AV		VSS	VDDO	VDDO	VDDO	NC	IOHP	TJHFP	RJOFP	ID[4][6]	ID[4][4]	ID[4][1]	LOJAJ[4]	NC	OD[4][6]	OD[4][3]	NC	OPL[4]	ID[3][7]	ID[3][3]	ID[3][0]	LOJAJ[3]	OD[3][7]	OD[3][5]	OD[3][1]	OJAJ1 [3]	ID[2][7]	ID[2][5]	NC	ID[2][2]	IPL[2]	ODP[2]	OD[2][5]	OD[2][1]	OPL[2]	NC	VDDO	VDDO	VDDO	VSS	AV
AW		VSS	VSS	VSS	VSS	NC	VSS	RWSEL	VSS	ID[4][7]	VSS	ID[4][2]	VSS	OD[4][7]	VSS	OD[4][4]	VSS	OD[4][0]	IDP[3]	ID[3][4]	ID[3][1]	VSS	ODP[3]	VSS	OD[3][3]	VSS	IDP[2]	VSS	ID[2][3]	VSS	ID[2][0]	VSS	OD[2][6]	OD[2][2]	NC	NC	VSS	VSS	VSS	VSS	AW
AY																																									AY

Figure 3 Pin Diagram – Bottom View (Top,Left Quadrant)

	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
A		VSS	VSS	VSS	VSS	NC	TADR[3]	TCA/ PTPA	TSX	VSS	TDAT[3]	VSS	TDAT[8]	VSS	TDAT [15]	VSS	TDAT [20]	VSS	TDAT [27]	VSS
B		VSS	VDDO	VDDO	VDDO	TFCLK	TADR[2]	STPA	TERR	TPRTY	TDAT[2]	TDAT[5]	TDAT[7]	TDAT [11]	TDAT [14]	TDAT [17]	TDAT [19]	TDAT [23]	TDAT [26]	TDAT [29]
C		VSS	VDDO	VDDO	VDDO	TENB	TADR[1]	TADR[5]	TMOD[1]	TEOP	TDAT[1]	TDAT[4]	TDAT[6]	TDAT [10]	TDAT [13]	TDAT [16]	TDAT [18]	TDAT [22]	TDAT [25]	TDAT [28]
D		VSS	VDDO	VDDO	VDDO	NC	TADR[0]	TADR[4]	TMOD[0]	TSOC/ TSOP	TDAT[0]	VDDO	VDDI	TDAT[9]	TDAT [12]	VDDO	VDDI	TDAT [21]	TDAT [24]	VDDO
E		NC	RDAT [31]	RDAT [30]	RDAT [29]															
F		VSS	RDAT [28]	RDAT [27]	VDDO															
G		RDAT [26]	RDAT [25]	RDAT [24]	RDAT [23]															
H		VSS	RDAT [22]	RDAT [21]	RDAT [20]															
J		RDAT [19]	RDAT [18]	RDAT [17]	VDDI															
K		VSS	RDAT [16]	RDAT [15]	VDDO															
L		NC	RDAT [14]	RDAT [13]	RDAT [12]															
M		VSS	RDAT [11]	RDAT [10]	RDAT[9]															
N		VDDI	RDAT[8]	RDAT[7]	RDAT[6]															
P		VSS	RDAT[5]	RDAT[4]	VDDO															
R		NC	NC	NC	VDDI															
T		VSS	RDAT[3]	RDAT[2]	RDAT[1]															
U		RDAT[0]	RPRTY	REOP	RSOC/RSOP															
V		RSX	RERR	RMOD [1]	VDDI															
W		VDDI	RMOD [0]	VDDI	VDDI															
Y		RCA/RVAL	RADR[5]	RADR[4]	RADR[3]															

Figure 4 Pin Diagram – Bottom View (Top, Right Quadrant)

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
SER_EN	DS3 TICLK	TMS	RSTB	VSS	A[2]	VSS	A[7]	VSS	D[0]	VSS	D[5]	VSS	D[11]	VSS	NC	VSS	VSS	VSS	VSS	A
TDAT [31]	REF8K	TRSTB	INTB	ALE	A[1]	A[4]	A[6]	A[10]	A[13]	D[2]	D[4]	D[8]	D[10]	D[13]	D[15]	VDDO	VDDO	VDDO	VSS	B
TDAT [30]	POS/ UL3B	TCK	TDO	RDB	A[0]	A[3]	A[5]	A[9]	A[12]	D[1]	D[3]	D[7]	VDDI	D[12]	D[14]	VDDO	VDDO	VDDO	VSS	C
VDDI	RPOHFP	VDDI	TDI	WRB	CSB	VDDO	VDDI	A[8]	A[11]	VDDO	VDDI	D[6]	D[9]	VDDO	VDDI	VDDO	VDDO	VDDO	VSS	D
																NC	NC	NC	NC	E
																NC	NC	NC	NC	F
																NC	NC	NC	NC	G
																ATB0	NC	NC	NC	H
																ATB1	TNWRK [1]	TPWRK [1]	VSS	J
																TNWRK [2]	TPWRK [2]	TNWRK [3]	TPWRK [3]	K
																AVDH	NC	NC	VSS	L
																RPWRK [1]	RNWRK [1]	TNWRK [4]	TPWRK [4]	M
																NC	RPWRK [2]	RNWRK [2]	VSS	N
																NC	AVDL	RPWRK [3]	RNWRK [3]	P
																AVDH	RPWRK [4]	RNWRK [4]	VSS	R
																TNPROT[1]	TPPROT[1]	TNPROT[2]	TPPROT[2]	T
																NC	TNPROT[3]	TPPROT[3]	VSS	U
																RPPROT[1]	RNPROT[1]	TNPROT[4]	TPPROT[4]	V
																AVDH	NC	AVDL	VSS	W
																RPPROT[2]	RNPROT[2]	RPPROT[3]	RNPROT[3]	Y

Figure 5 Pin Diagram – Bottom View (Bottom, Left Quadrant)

	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
AA		VSS	RADR[2]	RADR[1]	VDDO															
AB		NC	NC	NC	VDDI															
AC		VSS	RADR[0]	RFCLK	RENB															
AD		NC	NC	NC	NC															
AE		VSS	NC	NC	VDDO															
AF		NC	NC	NC	NC															
AG		VSS	NC	NC	VDDI															
AH		NC	NC	ROHCH [5]	ROHCH [4]															
AJ		VSS	ROHCH [3]	ROHCH [2]	VDDO															
AK		NC	ROHCH [1]	ROHCH [0]	ROHVAL															
AL		VSS	ROHFP	ROH	VDDI															
AM		TOHCH [5]	TOHCH [4]	TOHCH [3]	TOHCH [2]															
AN		TOHCH [1]	TOHCH [0]	TOHVAL	VDDI															
AP		TOHFP	TOHINS	TOH	VDDI															
AR		NC	NC	NC	NC															
AT		VSS	VDDO	VDDO	VDDO	VDDI	VDDO	SYSCLK	IDP[4]	VDDI	VDDO	IPL[4]	ODP[4]	VDDI	VDDO	OD[4][1]	VDDI	IPAIS[3]	ID[3][5]	VDDI
AU		VSS	VDDO	VDDO	VDDO	NC	ICMP	OJ0REF	IPAIS[4]	ID[4][5]	ID[4][3]	ID[4][0]	OALARM[4]	NC	OD[4][5]	OD[4][2]	NC	OJ0J1[4]	ID[3][6]	ID[3][2]
AV		VSS	VDDO	VDDO	VDDO	NC	OCMP	TJ0FP	RJ0FP	ID[4][6]	ID[4][4]	ID[4][1]	IJ0J1[4]	NC	OD[4][6]	OD[4][3]	NC	OPL[4]	ID[3][7]	ID[3][3]
AW		VSS	VSS	VSS	VSS	NC	VSS	RWSEL	VSS	ID[4][7]	VSS	ID[4][2]	VSS	OD[4][7]	VSS	OD[4][4]	VSS	OD[4][0]	IDP[3]	ID[3][4]
AY																				

Figure 6 Pin Diagram – Bottom View (Bottom, Right Quadrant)

																AVDH	AVDL	RPPROT[4]	RNPROT[4]	AA
																AVDL	AVDL	NC	NC	AB
																RESK	RES	NC	NC	AC
																VDDI	NC	NC	VSS	AD
																NC	NC	NC	NC	AE
																VDDO	OPL[1]	OJOJ1[1]	VSS	AF
																VDDI	OD[1][2]	OD[1][1]	OD[1][0]	AG
																VDDI	OD[1][4]	OD[1][3]	VSS	AH
																ODP[1]	OD[1][7]	OD[1][6]	OD[1][5]	AJ
																VDDO	IJOJ1[1]	OALARM[1]	VSS	AK
																VDDI	ID[1][1]	ID[1][0]	IPL[1]	AL
																VDDI	ID[1][3]	ID[1][2]	VSS	AM
																ID[1][7]	ID[1][6]	ID[1][5]	ID[1][4]	AN
																VDDO	IPAIS[1]	IDP[1]	VSS	AP
																VDDI	NC	NC	NC	AR
VDDI	VDDO	VDDI	OD[3][3]	OPL[3]	VDDO	VDDI	NC	VDDI	VDDO	OALARM[2]	VDDI	OD[2][3]	VDDI	VDDI	NC	VDDO	VDDO	VDDO	VSS	AT
IPL[3]	OALARM[3]	OD[3][6]	OD[3][4]	OD[3][0]	IPAIS[2]	ID[2][6]	ID[2][4]	NC	ID[2][1]	IJOJ1[2]	OD[2][7]	OD[2][4]	OD[2][0]	OJOJ1[2]	NC	VDDO	VDDO	VDDO	VSS	AU
ID[3][0]	IJOJ1[3]	OD[3][7]	OD[3][5]	OD[3][1]	OJOJ1[3]	ID[2][7]	ID[2][5]	NC	ID[2][2]	IPL[2]	ODP[2]	OD[2][5]	OD[2][1]	OPL[2]	NC	VDDO	VDDO	VDDO	VSS	AV
ID[3][1]	VSS	ODP[3]	VSS	OD[3][2]	VSS	IDP[2]	VSS	ID[2][3]	VSS	ID[2][0]	VSS	OD[2][6]	OD[2][2]	NC	NC	VSS	VSS	VSS	VSS	AW
																				AY
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

10 Pin Description

Pin Name	Type	Pin No.	Function
Receive System Side Utopia and POS Signals (48 Signals)			
RFCLK	Input	AC37	**The UTOPIA receive FIFO read clock (RFCLK).** RFCLK is used to read ATM cells from the receive cell FIFO. RFCLK is expected to cycle between 60MHz and 104 MHz. **POS-PHY receive FIFO read clock (RFCLK).** This signal is used to read packet data from the packet FIFO. RFCLK is expected to cycle between 60MHz and 104 MHz.
RPRTY	Output	U38	**The UTOPIA receive parity (RPRTY).** The RPRTY signal indicates the parity of the RDAT bus. The RPRTY signal indicates the parity on the RDAT[31:0] bus. Either odd or even parity can be selected. RPRTY is valid only when RENB has been sampled low in the previous clock cycle. RPRTY is updated on the rising edge of RFCLK. **The POS-PHY receive parity (RPRTY).** The RPRTY indicates the parity of the RDAT bus. The RPRTY signal indicates the parity on the RDAT[31:0] bus. Either odd or even parity can be selected. RPRTY is valid only when either RVAL or RSX are asserted. RPRTY is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RDAT[31] RDAT[30] RDAT[29] RDAT[28] RDAT[27] RDAT[26] RDAT[25] RDAT[24] RDAT[23] RDAT[22] RDAT[21] RDAT[20] RDAT[19] RDAT[18] RDAT[17] RDAT[16] RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Output	E38 E37 E36 F38 F37 G39 G38 G37 G36 H38 H37 H36 J39 J38 J37 K38 K37 L38 L37 L36 M38 M37 M36 N38 N37 N36 P38 P37 T38 T37 T36 U39	**UTOPIA receive cell data (RDAT[31:0]).** The RDAT[31:0] bus carries the ATM cell octets that are read from the receive FIFO. RDAT[31:0] is updated on the rising edge of RFCLK. **POS-PHY receive packet data (RDAT[31:0]).** The RDAT[31:0] bus carries the POS packet octets that are read from the receive FIFO. The RDAT[31:0] signals are valid when RVAL and RENB are asserted. RDAT[31:0] is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RENB	Input	AC36	**The UTOPIA receive read enable (RENB).** RENB is used to initiate reads from the receive FIFO. RENB can only be de-asserted as specified in the ATM Forum's UTOPIA Level 3 Specification. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK. **POS-PHY receive read enable (RENB).** RENB is used to initiate reads from the receive FIFO. During a data transfer, RVAL must be monitored since it will indicate if the data is valid. The system may deassert RENB at any time if it is unable to accept more data. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.
RSOC RSOP	Output	U36	**UTOPIA receive start of cell (RSOC).** The RSOC signal marks the start of a cell structure on the RDAT[31:0] bus. The first word of the cell structure is present on the RDAT[31:0] bus when RSOC is high. RSOC is updated on the rising edge of RFCLK. **POS-PHY receive start of packet (RSOP).** RSOP indicates the start of a packet on the RDAT[31:0] bus. RSOP is set high for the first word of a packet on RDAT[31:0]. RSOP is updated on the rising edge of RFCLK

Pin Name	Type	Pin No.	Function
RCA RVAL	Output	Y39	**UTOPIA receive cell available (RCA).** RCA can be polled to provide status indication of when a cell is available in the receive FIFO. RCA will be high two cycles after a channel address is presented on RADR[5:0] to indicate that a cell can be read out of that channel. If no cell is available for that channel, RCA will be low two cycles after RADR[5:0] is presented. RCA is updated on the rising edge of RFCLK. **POS-PHY receive data valid (RVAL).** RVAL indicates the validity of the receive data signals. When RVAL is high, the receive signals RDAT[31:0], RPRTY, RSOP, REOP, RMOD[1:0], and RERR are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will be high when valid data is on the RDAT[31:0] bus. RVAL will transition low when the FIFO does not have data to give. RVAL will remain low until a programmable minimum number of bytes or an end-of-packet (EOP) exists in the receive FIFO. The data available threshold is configurable using the DT[7:0] register bits in the RXSDQ FIFO Data Indirect Available Threshold register. RVAL is updated on the rising edge of RFCLK.
RADR[5] RADR[4] RADR[3] RADR[2] RADR[1] RADR[0]	Input	Y38 Y37 Y36 AA38 AA37 AC38	**UTOPIA receive channel select (RADR[5:0]).** RADR[5:0] is used to select the channel whose cell FIFO status is to be polled using RCA, or to select the channel for which a cell transfer is desired. RADR[5:0] is sampled on the rising edge of RFCLK.
RERR	Output	V38	**POS-PHY receive error (RERR).** RERR indicates that the current packet is invalid due to an error such as invalid FCS, excessive length or received abort. RERR may only assert when REOP is asserted marking the last word of the packet RERR is only used in POS mode and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
REOP	Output	U37	**POS-PHY receive end of packet (REOP).** REOP marks the end of packet on the RDAT[31:0] bus. It is legal for RSOP to be high at the same time REOP is high. REOP is set high to mark the last word of the packet presented on the RDAT[31:0] bus. When REOP is high, RMOD[1:0] specifies if the last word has 1, 2, 3, or 4 valid bytes of data. REOP is only used for POS operation and is updated on the rising edge of RFCLK.
RMOD[1] RMOD[0]	Output	V37 W38	**POS-PHY transmit word modulo (RMOD[1:0]).** RMOD[1:0] indicates the size of the current word when configured for packet mode. During a packet transfer, every word on RDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by RMOD[1:0] RMOD[1:0] = “00” RDAT[31:0] valid RMOD[1:0] = “01” RDAT[31:8] valid RMOD[1:0] = “10” RDAT[31:16] valid RMOD[1:0] = “11” RDAT[31:24] valid RMOD[1:0] is considered valid only when RVAL is asserted. RMOD[1:0] is only used for POS operation and is updated on the rising edge of RFCLK.
RSX	Output	V39	**POS-PHY receive start of transfer (RSX).** RSX is used to indicate the start of a packet transfer. When RSX is high, the channel number being transferred is given on RDAT[31:0]. RSX is only used for POS operation and is updated on the rising edge of RFCLK.
Transmit Utopia and POS Level 3 Signals (49 Signals)			
TFCLK	Input	B35	**UTOPIA transmit FIFO write clock (TFCLK)**. TFCLK is used to write ATM cells to the transmit FIFO. TFCLK is expected to cycle between 60MHz and 104 MHz. **POS-PHY transmit FIFO write clock (TFCLK).** TFCLK is used to write packet data into the packet FIFO. TFCLK is expected to cycle between 60MHz and 104 MHz.

Pin Name	Type	Pin No.	Function
TADR[5] TADR[4] TADR[3] TADR[2] TADR[1] TADR[0]	Input	C33 D33 A34 B34 C34 D34	**UTOPIA transmit channel select (TADR[5:0]).** TADR[5:0] is used to select the channel whose cell FIFO status is to be polled using TCA, or to select the channel for which a cell transfer is desired. TADR[5:0] is sampled on the rising edge of TFCLK. **POS-PHY polled channel select (TADR[5:0]).** TADR[5:0] is used to select the channel whose FIFO status is polled using PTPA. TADR[5:0] is sampled on the rising edge of TFCLK.
TDAT[31] TDAT[30] TDAT[29] TDAT[28] TDAT[27] TDAT[26] TDAT[25] TDAT[24] TDAT[23] TDAT[22] TDAT[21] TDAT[20] TDAT[19] TDAT[18] TDAT[17] TDAT[16] TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	B20 C20 B21 C21 A22 B22 C22 D22 B23 C23 D23 A24 B24 C24 B25 C25 A26 B26 C26 D26 B27 C27 D27 A28 B28 C28 B29 C29 A30 B30 C30 D30	**UTOPIA transmit cell data (TDAT[31:0]).** TDAT[31:0] carries the ATM cell octets that are written to the transmit FIFO. TDAT[31:0] is considered valid only when TENB is simultaneously asserted. TDAT[31:0] is sampled on the rising edge of TFCLK. **POS-PHY transmit packet data (TDAT[31:0]).** TDAT[31:0] carries the POS packet octets that are written to the transmit FIFO. TDAT[31:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[31:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TPRTY	Input	B31	**UTOPIA transmit bus parity (TPRTY).** TPRTY indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are still inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK. **POS-PHY transmit bus parity (TPRTY).** TPRTY indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Packets with parity errors can be optionally aborted by setting the PARERREN bit in the TXPHY. If PARERREN is kept low, the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB or TSX is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
TSOC	Input	D31	**UTOPIA transmit start of cell (TSOC).** TSOC marks the start of a cell structure on the TDAT[31:0] bus. The first word of the cell structure is present on the TDAT[31:0] bus when TSOC is high. TSOC must be present for each cell. TSOC is considered valid only when TENB is simultaneously asserted. TSOC is sampled on the rising edge of TFCLK.
TSOP	Input	D31	**POS-PHY transmit start of packet (TSOP).** TSOP indicates the start of a packet on the TDAT[31:0] bus. TSOP is required to be present at all instances for proper operation. TSOP must be set high for the first word of a packet on TDAT[31:0]. TSOP is considered valid only when TENB is simultaneously asserted. TSOP is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TENB	Input	C35	**UTOPIA transmit write enable (TENB) signal.** TENB is an active low input which is used to initiate writes to the transmit FIFO's. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY and TSOC signals are invalid. When TENB is sampled low, the information sampled on the TDAT, TPRTY and TSOC signals are valid and are written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK. **POS-PHY transmit write enable (TENB).** TENB is an active low input which is used to initiate writes to the transmit FIFO's. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY, TSOP, TEOP, TMOD, and TERR signals are invalid. When TENB is sampled low, the information sampled on the TDAT, TPRTY, TSOP, TEOP, TMOD, and TERR signals are valid and are written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.
TCA PTPA	Output	A33	**UTOPIA transmit cell available (TCA).** TCA can be polled to provide status indication of when room exists to receive a cell in the transmit FIFO. TCA will be high two cycles after a FIFO address is presented on TADR[5:0] to indicate that a cell can be written into that FIFO. If no space is available for that FIFO, TCA will be low two cycles after TADR[5:0] is presented. TCA is updated on the rising edge of TFCLK. **POS-PHY polled transmit packet available (PTPA).** PTPA signal provides status indication on the fill status of the polled (using TADR[5:0]) transmit FIFO. Note that regardless of what fill level PTPA is set to indicate "full" at, the FIFO still has the ability to store data up to its actual capacity. When PTPA transitions high, it indicates that the polled transmit FIFO has enough room to store a configurable number of data bytes. When PTPA transitions low, it indicates that the polled transmit FIFO is either full or near full as configured. PTPA is updated on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TEOP	Input	C31	**POS-PHY transmit end of packet (TEOP).** TEOP marks the end of packet on the TDAT[31:0] bus when configured for packet data. The TEOP signal marks the last word of a packet on the TDAT[31:0] bus. The TMOD[1:0] signal indicates how many bytes are in the last word. It is legal to set TSOP high at the same time as TEOP high in order to support one, two, three, or four byte packets where four bytes is the minimum size after CRC is added. TEOP is only valid when TENB is simultaneously asserted. TEOP is only used for POS operation and is sampled on the rising edge of TFCLK.
STPA	Output	B33	**POS-PHY selected-PHY Transmit Packet Available (STPA).** STPA provides FIFO status indication for the selected channel of the S/UNI-MACH48. STPA is asserted when the minimum number of bytes (user programmable) are available in the transmit FIFO specified by the inband address on TDAT[31:0]. Once asserted, STPA indicates the transmit FIFO is not full. When STPA deassertes, it indicates that the transmit FIFO is full or near full (user programmable). STPA is updated on the rising edge of TFCLK.
TERR	Input	B32	**POS-PHY transmit error (TERR).** TERR is used to indicate that the current packet must be aborted. Packets marked with TERR will be appended the abort sequence when transmitted. TERR should only be asserted during the last word of the packet being transferred on TDAT[31:0]. TERR is only considered valid when TENB and TEOP are simultaneously asserted. TERR is ignored for ATM modes of operation and is sampled on the rising edge of TFCLK.
TSX	Input	A32	**POS-PHY transmit start of transfer (TSX).** TSX is used to indicate the start of a packet transfer. When TSX is high, the channel number to be selected for transfers is expected to be present on TDAT[31:0]. TSX is only used for POS operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TMOD[1] TMOD[0]	Input	C32 D32	**POS-PHY transmit word modulo (TMOD[1:0]).** TMOD[1:0] indicates the size of the current word when configured for packet mode. During a packet transfer, every word on TDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by TMOD[1:0] TMOD[1:0] = “00” TDAT[31:0] valid TMOD[1:0] = “01” TDAT[31:8] valid TMOD[1:0] = “10” TDAT[31:16] valid TMOD[1:0] = “11” TDAT[31:24] valid TMOD[1:0] is considered valid only when TENB is simultaneously asserted. TMOD[1:0] is only used for POS operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
Outgoing TelecomBus Interface (49 Signals) All the TelecomBus output signals can be tri-stated by writing a '1' to the PARDIS bit of register 1.			
OD[4][7] OD[4][6] OD[4][5] OD[4][4] OD[4][3] OD[4][2] OD[4][1] OD[4][0] OD[3][7] OD[3][6] OD[3][5] OD[3][4] OD[3][3] OD[3][2] OD[3][1] OD[3][0] OD[2][7] OD[2][6] OD[2][5] OD[2][4] OD[2][3] OD[2][2] OD[2][1] OD[2][0] OD[1][7] OD[1][6] OD[1][5] OD[1][4] OD[1][3] OD[1][2] OD[1][1] OD[1][0]	Output	AW27 AV26 AU26 AW25 AV25 AU25 AT25 AW23 AV18 AU18 AV17 AU17 AT17 AW16 AV16 AU16 AU9 AW8 AV8 AU8 AT8 AW7 AV7 AU7 AJ3 AJ2 AJ1 AH3 AH2 AG3 AG2 AG1	**Outgoing Data (OD[4:1][7:0]).** The outgoing data buses (OD[4][7:0], OD[3][7:0], OD[2][7:0], OD[1][7:0]) carry the SONET/SDH OC-48 frame data in byte serial format. OD[*x*][7] is the most significant bit, corresponding to bit 1 of each SONET/SDH octet, the bit transmitted first. OD[*x*][0] is the least significant bit, corresponding to bit 8 of each SONET/SDH octet, the bit transmitted last. OD[1][7:0] carries the first STS-12 stream transmitted while OD[4][7:0] carries the last. Each of the four outgoing data buses carries a constituent OC-12 stream. OD[*x*][7:0] are updated on the rising edge of SYSCLK.
ODP[4] ODP[3] ODP[2] ODP[1]	Output	AT28 AW18 AV9 AJ4	**Outgoing Data Parity (ODP[4:1]).** The outgoing data parity bus (ODP[4:1]) reports the parity of the corresponding outgoing data bus (OD[4:1][7:0]). ODP[*x*] reports odd parity relative to OD[*x*][7:0] when the OOP register bit is set high and even parity when the OOP register bit is set low. ODP[*x*] is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
OPL[4] OPL[3] OPL[2] OPL[1]	Output	AV23 AT16 AV6 AF3	**Outgoing Payload Active (OPL[4:1]).** The outgoing payload active bus (OPL[4:1]) distinguishes between transport overhead / section overhead bytes from synchronous payload / high order virtual container bytes in the corresponding outgoing data bus (OD[4:1][7:0]). OPL[*x*] is set high to mark each payload / HO-VC byte on OD[*x*][7:0] and set low to mark each transport overhead / section overhead byte on OD[*x*][7:0]. OPL[4:1] is updated on the rising edge of SYSCLK.
OJ0J1[4] OJ0J1[3] OJ0J1[2] OJ0J1[1]	Output	AU23 AV15 AU6 AF2	**Outgoing Composite Transport and Payload Frame Pulse (OJ0J1[4:1]).** The outgoing composite transport and payload frame pulse bus (OJ0J1[4:1]) identifies the STS/STM frame and the synchronous payload envelope / high order virtual container frame boundaries on the corresponding outgoing data bus (OD[4:1][7:0]). OJ0J1[*x*] is set high when OPL[*x*] is set low to mark the J0 byte of the STS/STM frame on the OD[*x*][7:0] bus. OJ0J1[*x*] is set high when OPL[*x*] is set high to mark the each J1 byte of the SPE / HO-VC frame on the OD[*x*][7:0] bus. The J0 position on OJ0J1[4:1] will be aligned to OJ0REF as configured by the OJ0REFDLY[13:0] bits. OJ0J1[4:1] is updated on the rising edge of SYSCLK.
OALARM[4] OALARM[3] OALARM[2] OALARM[1]	Output	AU28 AU19 AT10 AK2	**Outgoing Alarm (OALARM[4:1]).** The outgoing alarm bus (OALARM[4:1]) identifies STS/STM or tributaries on the corresponding outgoing data bus (OD[4:1][7:0]) that are in AIS state. OALARM[*x*] is set high when the stream on OD[*x*][7:0] is in AIS and is set low when the stream is out of alarm state. OALARM[4:1] is updated on the rising edge of SYSCLK.
OJ0REF	Input	AU33	**Outgoing Transport J0 Frame Pulse Reference (OJ0REF).** The outgoing transport J0 frame pulse reference (OJ0REF) is used to reference the S/UNI-MACH48 to a J0 byte location as configured in the OJ0REFDLY[13:0] bits. OJ0REF is expected to be high for 1 clock cycle every 9720 SYSCLK cycles and aligns the J0 position on OJ0J1[4:1]. OJ0REF is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
Input TelecomBus Interface (48 Signals)			
ID[4][7] ID[4][6] ID[4][5] ID[4][4] ID[4][3] ID[4][2] ID[4][1] ID[4][0] ID[3][7] ID[3][6] ID[3][5] ID[3][4] ID[3][3] ID[3][2] ID[3][1] ID[3][0] ID[2][7] ID[2][6] ID[2][5] ID[2][4] ID[2][3] ID[2][2] ID[2][1] ID[2][0] ID[1][7] ID[1][6] ID[1][5] ID[1][4] ID[1][3] ID[1][2] ID[1][1] ID[1][0]	Input	AW31 AV31 AU31 AV30 AU30 AW29 AV29 AU29 AV22 AU22 AT22 AW21 AV21 AU21 AW20 AV20 AV14 AU14 AV13 AU13 AW12 AV11 AU11 AW10 AN4 AN3 AN2 AN1 AM3 AM2 AL3 AL2	**Incoming Data (ID[4:1][7:0]).** The incoming data buses (ID[4][7:0], ID[3][7:0], ID[2][7:0], ID[1][7:0]) carry the SONET/SDH OC-48 frame data in byte serial format. ID[*x*][7] is the most significant bit, corresponding to bit 1 of each SONET/SDH octet, the bit transmitted first. ID[*x*][0] is the least significant bit, corresponding to bit 8 of each SONET/SDH octet, the bit transmitted last. ID[1][7:0] carries the first STS-12 stream transmitted while ID[4][7:0] carries the last. Each of the four incoming data buses carries a constituent STS-12 stream and share a common transport frame alignment. ID[*x*][7:0] are sampled on the rising edge of SYSCLK.
IDP[4] IDP[3] IDP[2] IDP[1]	Input	AT32 AW22 AW14 AP2	**Incoming Data Parity (IDP[4:1]).** The incoming data parity bus (IDP[4:1]) reports the parity of the corresponding incoming data bus (ID[4:1][7:0], and optionally IJ0J1[4:1] and IPL[4:1]). IDP[*x*] is expected to report odd parity relative to when the IOP register bit is set high and even parity when the IOP register bit is set low. IDP[*x*] is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
IPL[4] IPL[3] IPL[2] IPL[1]	Input	AT29 AU20 AV10 AL1	**Incoming Payload Active (IPL[4:1]).** The incoming payload active bus (IPL[4:1]) distinguishes between transport overhead / section overhead bytes from synchronous payload / high order virtual container bytes in the corresponding incoming data bus (ID[4:1][7:0]). IPL[*x*] is set high mark each payload / HO-VC byte on OD[*x*][7:0] and set low to mark each transport overhead / section overhead byte on ID[*x*][7:0]. IPL[4:1] is sampled on the rising edge of SYSCLK.
IJ0J1[4] IJ0J1[3] IJ0J1[2] IJ0J1[1]	Input	AV28 AV19 AU10 AK3	**Incoming Composite Transport and Payload Frame Pulse (IJ0J1[4:1]).** The incoming composite transport and payload frame pulse bus (IJ0J1[4:1]) identifies the STS/STM frame and the synchronous payload envelop / high order virtual container frame boundaries on the corresponding incoming data bus (ID[4:1][7:0]). IJ0J1[*x*] is set high when IPL[*x*] is set low to mark the J0 byte of the STS/STM frame on the ID[*x*][7:0] bus. IJ0J1[*x*] is set high when IPL[*x*] is set high to mark the each J1 byte of the SPE / HO-VC frame on the ID[*x*][7:0] bus. IJ0J1[1] provides the J0 pulse for all four slices, and therefore must continually provide J0 regardless of whether the data stream is active. IJ0J1[4:2] must be alligned to IJ0J1[1] for the J0 pulse, or their J1 pulses would be out of alignment. IJ0J1[4:1] is sampled on the rising edge of SYSCLK.
IPAIS[4] IPAIS[3] IPAIS[2] IPAIS[1]	Input	AU32 AT23 AU15 AP3	**Incoming High Order Path AIS (IPAIS[4:1]).** The incoming high order path alarm bus (IPAIS[4:1]) identifies STS/STM streams on the corresponding incoming data bus (ID[4:1][7:0]) that are in high order path AIS state. IPAIS[*x*] is set high when the stream on ID[*x*][7:0] is in AIS and is set low when the stream is out of AIS state. IPAIS[4:1] is not used when the RHPP block is enabled (RHPP_EN = 1). IPAIS[4:1] is sampled on the rising edge of SYSCLK.
DS3 Overhead Signals (19 Signals)			
TOHVAL	Output	AN37	**Transmit DS3 Overhead Valid (TOHVAL).** TOHVAL shows whether or not valid data is available on TOHFP and whether TOH and TOHINS can be sampled for the DS3 channel displayed on TOHCH[5:0]. TOHVAL is updated on the rising edge of SYSCLK.
TOHFP	Output	AP39	**Transmit DS3 Overhead Frame Pulse (TOHFP).** TOHFP shows the X1 overhead bit alignment position of the TOH and TOHINS overhead stream for DS3 channel TOHCH[5:0]. This signal is only valid when TOHVAL is logic 1. TOHFP is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
TOHCH[5] TOHCH[4] TOHCH[3] TOHCH[2] TOHCH[1] TOHCH[0]	Output	AM39 AM38 AM37 AM36 AN39 AN38	**Transmit DS3 Overhead Channel (TOHCH[5:0]).** TOHCH[5:0] shows which channel's overhead control information (TOHVAL, TOHFP) is being updated. TOHCH[5:0] is updated on the rising edge of SYSCLK.
TOHINS	Input	AP38	**Transmit DS3 Overhead Insert (TOHINS).** TOHINS is used to determine whether or not the value on the TOH pin is to overwrite the DS3 overhead bit. If TOHINS is logic 1, then the value of TOH will be accepted. If TOHINS is logic 0, then TOH will be ignored and the associated overhead bit will be generated by the S/UNI-MACH48's internal circuitry. TOHINS is only sampled when responding to an asserted TOHVAL indication. TOHINS is sampled on the rising edge of SYSCLK.
TOH	Input	AP37	**Transmit DS3 Overhead (TOH).** TOH provides the state of the DS3 overhead bit which is to be overwritten. TOH is valid only when TOHINS is logic 1 and when responding to an asserted TOHVAL indication. TOH is sampled on the rising edge of SYSCLK.
ROHVAL	Output	AK36	**Receive DS3 Overhead Valid (ROHVAL).** ROHVAL shows whether the signals on ROHFP and ROH contain valid data. When ROHVAL is logic 1, ROHFP and ROH contain valid data for DS3 channel ROHCH[5:0]. ROH is updated on the rising edge of SYSCLK.
ROHFP	Output	AL38	**Receive DS3 Overhead Frame pulse (ROHFP).** ROHFP indicates when ROH gives the state of the X1 bit of DS3 channel ROHCH[5:0]. ROHFP is only valid when ROHVAL is logic 1. ROHFP is updated on the rising edge of SYSCLK.
ROHCH[5] ROHCH[4] ROHCH[3] ROHCH[2] ROHCH[1] ROHCH[0]	Output	AH37 AH36 AJ38 AJ37 AK38 AK37	**Receive DS3 Overhead Channel (ROHCH[5:0]).** The ROHCH[5:0] bus shows which channel's overhead control information (ROHVAL, ROHFP, ROH) is being updated. ROHCH[5:0] is updated on the rising edge of SYSCLK.
ROH	Output	AL37	**Receive DS3 Overhead (ROH).** The ROH signal gives the state of the overhead bit of DS3 channel ROHCH[5:0]. ROH is valid only when ROHVAL is logic 1. ROH is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
PLCP Signals (2 Signals)			
REF8K	Input	B19	**Reference 8 kHz input (REF8K).** The PLCP frame rate can be locked to this external 8 kHz reference. An internal phase-frequency detector compares the transmit PLCP frame rate with the externally applied 8 kHz reference and adjusts the PLCP frame rate appropriately. The REF8K input must transition high once every 125µs for correct operation. The REF8K input is treated as an asynchronous signal and must be "glitch-free".
RPOHFP	Output	D19	**Receive PLCP Frame Pulse (RPOHFP).** RPOHFP shows the PLCP frame pulse for the selected PLCP framer. RPOHFP is logic 1 for a minimum of 1300ns every 125µs and can be treated as an asynchronous "glitch-free" signal.
General (4 Signals)			
SYSCLK	Input	AT33	**System Clock (SYSCLK).** SYSCLK is the master line side clock for the S/UNI-MACH48 device. SYSCLK is nominally a 77.76 MHz clock, with a 50% duty cycle.
POSL3/ UL3B	Input	C19	**Utopia/POS interface select (POSL3/UL3B).** When POSL3/UL3B is set to logic 0, the Utopia Level 3 interface is selected. When set to logic 1, the POS-PHY Level 3 interface is selected.
SER_EN	Input	A20	**Serial Interface Enable (SER_EN).** When SER_EN is logic 0, the line side parallel TelecomBus interface is enabled. When SER_EN is logic 1, the line side serial LVDS interface is enabled.
DS3TICLK	Input	A19	**DS3 Transmit Reference Clock (DS3TICLK).** DS3TICLK is expected to be nominally 44.736 MHz. This is the clock rate at which all the DS3 data streams will be sourced before being mapped into an STS-1/STM-0 timeslot by the DS3 mapper (D3MA) block.

Pin Name	Type	Pin No.	Function
Timeslot Memory Paging (3 Signals)			
ICMP	Input	AU34	**Incoming Connection Memory Page.** The incoming connection memory page select signal (ICMP) controls the selection of the connection memory page in the two Incoming Time-Slot Interchange blocks (IWTI, IPTI). When ICMP is set high, connection memory page 1 is selected. When ICMP is set low, connection memory page 0 is selected. ICMP is sampled at the J0 byte location on the incoming data buses (ID[4:1][7:0]) when the parallel TelecomBus interface is selected (SER_EN is logic 0) or at the J0 byte location as defined by the receive serial interface frame pulse signal (RJ0FP) when the serial LVDS interface is selected (SER_EN is logic 1). Changes to the connection memory page selection is synchronized to the frame boundary of a later transport frame as set by the ICMPDLY bit. ICMP is sampled on the rising edge of SYSCLK.
OCMP	Input	AV34	**Outgoing Connection Memory Page.** The outgoing data bus connection memory page select signal (OCMP) controls the selection of the connection memory page in the two Outgoing Time-Slot Interchange blocks (OWTI and OPTI). When OCMP is set high, connection memory page 1 is selected. When OCMP is set low, connection memory page 0 is selected. OCMP is sampled at the J0 byte location as defined by the OJ0REF input. Changes to the connection memory page selection is synchronized to the transport frame boundary of a later frame as set by the OCMPDLY bit. OCMP is sampled on the rising edge of SYSCLK.
RWSEL	Input	AW33	**Receive Working Serial Data Select.** The receive working serial data select signal (RWSEL) selects between the receive working serial data bus (RPWRK[4:1]/RNWRK[4:1]) and the receive protection serial data bus (RPPROT[4:1]/RNPROT[4:1]). This pin is only used when the LVDS serial interface is enabled (SER_EN is logic 1) and the RWSEL_EN register bit in register 0001H is set to logic 1. When RWSEL is set high, the working serial bus is selected. When RWSEL is set low, the protection serial bus is selected. RWSEL is sampled at the J0 byte location as defined by the receive serial interface frame pulse signal (RJ0FP). Changes to the selection of the working and protection serial streams are synchronized to the J0 byte location of the next frame. RWSEL is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
Receive Serial TelecomBus Interface (17 Signals)			
RPWRK[4] RNWRK[4] RPWRK[3] RNWRK[3] RPWRK[2] RNWRK[2] RPWRK[1] RNWRK[1]	Analog LVDS Input	R3 R2 P2 P1 N3 N2 M4 M3	**Receive Working Serial Data.** The differential receive working serial data links (RPWRK[3:0]/RNWRK[3:0]) carries the receive SONET/SDH STS-48 frame data from an upstream working source, in bit serial format. Each differential pair carries a constituent STS-12 of the receive working stream. Data on RPWRK/RNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. The four differential pairs in RPWRK[3:0]/RNWRK[3:0] are frequency locked but not phase locked. RPWRK[3:0]/RNWRK[3:0] are nominally 777.6 Mbps data streams. RPWRK[3:0]/RNWRK[3:0] may be left floating, or be tied to ground if unused.
RPPROT[4] RNPROT[4] RPPROT[3] RNPROT[3] RPPROT[2] RNPROT[2] RPPROT[1] RNPROT[1]	Analog LVDS Input	AA2 AA1 Y2 Y1 Y4 Y3 V4 V3	**Receive Protect Serial Data.** The differential receive protection serial data links (RPPROT[3:0]/RNPROT[3:0]) carries the receive SONET/SDH STS-48 frame data from an upstream protection source, in bit serial format. Each differential pair carries a constituent STS-12 of the receive protection stream. Data on RPPROT/RNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. The four differential pairs in RPPROT[3:0]/RNPROT[3:0] are frequency locked but not phase locked. RPPROT[3:0]/RNPROT[3:0] are nominally 777.6 Mbps data streams. RPPROT[3:0]/RNPROT[3:0] may be left floating, or be tied to ground if unused.
RJ0FP	Input	AV32	**Receive Serial Interface Frame Pulse.** The receive serial interface frame pulse signal (RJ0FP) provides system timing of the receive serial interface. RJ0FP is expected to be set high once every 9720 SYSCLK cycles, or multiple thereof, to indicate the J0 frame boundary. The RJ0DLY[13:0] register bits are used to align the J0 character on the Receive Serial TelecomBus interface (RPWRK[3:0]/RNWRK[3:0] and RPPROT[3:0]/RNPROT[3:0]) with RJ0FP. This pin is only used when the LVDS serial interface is enabled (SER_EN is logic 1). RJ0FP is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
Transmit Serial TelecomBus Interface (19 Signals)			
TPWRK[4] TNWRK[4] TPWRK[3] TNWRK[3] TPWRK[2] TNWRK[2] TPWRK[1] TNWRK[1]	Analog LVDS Output	M1 M2 K1 K2 K3 K4 J2 J3	**Transmit Working Serial Data.** The differential transmit working serial data links (TPWRK[3:0]/TNWRK[3:0]) carries the transmit SONET/SDH STS-48 frame data to a downstream working sink, in bit serial format. Each differential pair carries a constituent STS-12 of the transmit working stream. Data on TPWRK/TNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. The four differential pairs in TPWRK[3:0]/TNWRK[3:0] are frequency locked but not phase locked. TPWRK[3:0]/TNWRK[3:0] are nominally 777.6 Mbps data streams. TPWRK[3:0]/TNWRK[3:0] may be left floating if unused.
TPPROT[4] TNPROT[4] TPPROT[3] TNPROT[3] TPPROT[2] TNPROT[2] TPPROT[1] TNPROT[1]	Analog LVDS Output	V1 V2 U2 U3 T1 T2 T3 T4	**Transmit Protect Serial Data.** The differential transmit protection serial data links (TPPROT[3:0]/TNPROT[3:0]) carries the transmit SONET/SDH STS-48 frame data to a downstream protection sink, in bit serial format. Each differential pair carries a constituent STS-12 of the transmit protection stream. Data on TPPROT/TNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. The four differential pairs in TPPROT[3:0]/TNPROT[3:0] are frequency locked but not phase locked. TPPROT[3:0]/TNPROT[3:0] are nominally 777.6 Mbps data streams. TPPROT[3:0]/TNPROT[3:0] may be left floating if unused.
TJ0FP	Output	AV33	**Transmit Serial Interface Frame Pulse.** The transmit serial interface frame pulse signal (TJ0FP) provides system timing of the transmit serial interface. TJ0FP is set high once every 9720 SYSCLK cycles to indicate that the J0 frame boundary 8B/10B character has been serialized out on both the differential transmit working LVDS bus (TPWRK[3:0]/TNWRK[3:0]) and the differential transmit protection LVDS bus (TPWRK[3:0]/TNWRK[3:0]). TJ0FP is updated on the rising edge of SYSCLK.
RES	Analog Input	AC3	**Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between these the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force the 0.8V reference voltage onto RES, therefore forcing 252µA of current to flow through the resistor.

Pin Name	Type	Pin No.	Function
RESK	Analog Input	AC4	**Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between these the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force the 0.8V reference voltage onto RES, therefore forcing 252µA of current to flow through the resistor. RESK is electrically connected to AVSS within the block, but should not be connected to AVSS, either on-chip or off-chip.
Microprocessor Interface Signals (36 Signals)			
CSB	Input	D15	**Active-low chip select (CSB).** The CSB signal is low during S/UNI-MACH48 register accesses. If register accesses are to be controlled using the RDB and WRB signals only, CSB must be connected to an inverted version of the RSTB input.
RDB	Input	C16	**Active-low read enable (RDB).** The RDB signal is low during S/UNI-MACH48 register read accesses. The S/UNI-MACH48 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	D16	**Active-low write strobe (WRB).** The WRB signal is low during a S/UNI-MACH48 register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	B5 C5 B6 C6 A7 B7 D7 B8 C8 D8 A9 B9 C9 B10 C10 A11	**The bi-directional data bus (D[15:0]).** D[15:0] is used during S/UNI-MACH48 register read and write accesses.

Pin Name	Type	Pin No.	Function
A[13]/TRS A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	B11 C11 D11 B12 C12 D12 A13 B13 C13 B14 C14 A15 B15 C15	**Address bus (A[13:0]).** A[13:0] selects specific registers during S/UNI-MACH48 register accesses. A[13]/TRS functions as a test mode register select signal. A[13]/TRS is high during test mode register accesses, and is low during normal mode register accesses. A[13]/TRS may be tied low if only normal mode register access is required.
ALE	Input	B16	**Address latch enable (ALE).** ALE is active-high and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-MACH48 to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
RSTB	Input	A17	**Active-low reset (RSTB).** RSTB provides an asynchronous S/UNI-MACH48 reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.
INTB	Output	B17	**Active-low interrupt (INTB).** INTB is set low when a S/UNI-MACH48 interrupt source is active and that source is unmasked. The S/UNI-MACH48 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
JTAG Test Access Port (TAP) (5 Signals)			
TCK	Input	C18	**JTAG test clock (TCK).** TCK provides clock timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	A18	**Test mode select (TMS).** TMS controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	D17	**Test data input (TDI).** TDI carries test data into the S/UNI-MACH48 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Output	C17	**Test data output (TDO).** TDO carries test data out of the S/UNI-MACH48 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when shifting boundary scan data is in progress.

Pin Name	Type	Pin No.	Function
TRSTB	Input	B18	**Active-low test reset (TRSTB).** TRSTB provides an asynchronous S/UNI-MACH48 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB must be connected to the RSTB input.
Analog Test Bus (2 Signals)			
ATB0	Analog I/O	H4	**Analog test bus (ATB0).** ATB0 is used for PMC validation and testing. The ATB0 pin should be grounded in normal operation.
ATB1	Analog I/O	J4	**Analog test bus (ATB1).** ATB1 is used for PMC validation and testing. The ATB1 pin should be grounded in normal operation.
Analog Power (9 Signals)			
AVDH[3] AVDH[2] AVDH[1] AVDH[0]	Power	L4 R4 W4 AA4	The analog high voltage power pins (AVDH[3:0]) should be connected to a well-decoupled +3.3 V DC supply.
AVDL[4] AVDL[3] AVDL[2] AVDL[1] AVDL[0]	Power	P3 W2 AB4 AB3 AA3	The analog low voltage power pins (AVSS[4:0]) should be connected to a well-decoupled +1.8 V DC supply.

Pin Name	Type	Pin No.	Function
Digital Power and Ground (186 Signals)			

Pin Name	Type	Pin No.	Function
VDDO[56:0]	I/O Power	B2 B3 B4 C2 C3 C4 D2 D3 D4 D6 D10 D14 D21 D25 D29 B36 B37 B38 C36 C37 C38 D36 D37 D38 F36 K36 P36 AA36 AE36 AJ36 AT38 AT37 AT36 AU38 AU37 AU36 AV38 AV37 AV36 AT34 AT30 AT26 AT19 AT15 AT11 AV4 AV3 AV2 AU4 AU3 AU2 AT4 AT3 AT2 AP4 AK4 AF4	**I/O power (VDDO).** The VDDO pins should be connected to a well-decoupled +3.3 V power supply.

Pin Name	Type	Pin No.	Function
VDDI[37:0]	Core Power	D5 D9 D13 D18 D20 D24 D28 J36 N39 R36 V36 W36 W37 W39 AB36 AG36 AL36 AN36 AP36 AT35 AT31 AT27 AT24 AT21 AT20 AT18 AT14 AT12 AT9 AT7 AT6 AR4 AM4 AL4 AH4 AG4 AD4 C7	**Core power (VDDI).** The VDDI pins should be connected to a well-decoupled +1.8 V power supply.

Pin Name	Type	Pin No.	Function
VSS[75:0]	Ground	AW39, A1 AW38, A2 AW37, A3 AW36, A4 AW34, A6 AW32, A8 AW30, A10 AW28, A12 AW26, A14 AW24, A16 AW19, A21 AW17, A23 AW15, A25 AW13, A27 AW11, A29 AW9, A31 AW4, A36 AW3, A37 AW2, A38 AA39, A39 AC39, B1 AE39, C1 AG39, AW1 AJ39, D1 AL39, J1 AT39, L1 AU39, N1 AV39, R1 B39, U1 C39, W1 D39, F39 H39, K39 M39, P39 T39, AV1 AU1, AT1 AP1, AM1 AK1, AH1 AF1, AD1	**Ground (VSS).** The VSS pins should be connected to the ground.

Notes on Pin Description:

1. All S/UNI-MACH48 inputs and bi-directional signals present minimum capacitive loading and operate at TTL compatible logic levels and can tolerate 3.3V input levels.
2. The TJ0FP, RDAT[31:0], RPRTY, RSOC/RSOP, REOP, RMOD[1:0], RERR, RCA/RVAL, RSX, RCLK, RFPO, TCA/PTPA, STPA, OD[4:1][7:0], ODP[4:1], OPL[4:1], OJ0J1[4:1], OALARM[4:1], TOHVAL, TOHFP, TOHCH[5:0], RPOHFP, ROHVAL, ROHFP, ROH, and ROHCH[5:1] outputs have a 12mA drive capability. The D[15:0], TDO, and INTB outputs have an 8mA drive capability.
3. It is mandatory that every ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
4. It is mandatory that every 1.8V power pin (VDDI and AVDL) be connected to the 1.8V printed circuit board power plane to ensure reliable device operation.
5. It is mandatory that every 3.3V power pin (VDDO and AVDH) be connected to the 3.3V printed circuit board power planes to ensure reliable device operation.

11 Functional Description

11.1 Input Parallel TelecomBus Interface

The input parallel TelecomBus Interface samples a SONET/SDH stream on 4x8-bit STS-12/STM-4 or 1x32-bit STS-48/STM-16 buses. Markers for J0/J1 byte locations are given to indicate the frame alignment. Payload and non-payload bytes are also marked appropriately. AIS alarm conditions are also given on the interface. The interface is clocked with the 77.76 MHz SYSCLK.

11.2 Input Serial TelecomBus Interface

The input serial TelecomBus Interface samples a SONET/SDH stream on a 4x777.6Mbps LVDS compatible buses. Markers for J0/J1 byte locations are given to indicate the frame alignment. Payload and non-payload bytes are also marked appropriately. AIS alarm conditions are also given on the interface.

11.3 Receive High Order Pointer Processor (RHPP)

The RHPP can process the path overhead of an STS-12 (STM-4) 8-bit serial stream at 77.76 MHz. Four RHPPs can be configured to process the path overhead of an STS-48 (STM-16) 32-bit serial stream at 77.76 MHz.

The RHPP processes the path overhead of any legal mix of STS-1/3c/12c payloads. The STS (VC) payloads are independently floating inside the transport frame and the RHPP must interpret each of the STS-1/3c/12c pointers in order to locate the boundaries of the payloads i.e. the path trace bytes (J1).

The RHPP can be used to process an STS-48c/STM-16c path overhead in a similar manner as an STS-12c/STM-4c.

The RHPP permits the S/UNI-MACH48 to work properly if the J1 markers in the incoming TelecomBus stream(s) are not present. This is required for a drop and continue function where the S/UNI-MACH48 is the drop point and the data stream is routed to another device for the continue function. All SONET/SDH overhead characters remain intact in this format.

11.4 DS3 Demapper (D3MD)

The DS3 Demapper Side (D3MD) block demaps a DS3 signal from an STS-1 (STM-0/AU3) payload. The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. The asynchronous DS3 mapping is shown in Table 1:

Table 1 Asynchronous DS3 Mapping to STS-1 (STM-0/AU3).

J1	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
STS	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
POH	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I

Notes

1. R: Fixed Stuff bit - set to logic ‘0’ or ‘1’
2. C: Stuff Control bit - set to logic ‘1’ for stuff indication
3. S: Stuff Opportunity bit - when stuff control bit is ‘0’, stuff opportunity is I bit
4. O: Overhead communication channel
5. I: DS3 payload information

DS3 Demapper

The D3MD performs majority vote on the received C-bits. If 3 out of 5 C-bits are ‘1’s, the associated S bit is interpreted as a stuff bit. If 3 out of 5 C-bits are ‘0’s, the associated S bit is interpreted as an Information bit. The information bits are written to an elastic store and the Fixed Stuff bits (R) are ignored.

Given an incoming AIS condition on the incoming serial or parallel TelecomBus interface, the D3MD ignores the STS-1 (STM-0/AU3) SPE and writes a DS3 AIS pattern to the elastic store. In addition, the desynchronization algorithm assumes a nominal ratio of data to stuff bits carried in the S bits (1 out of 3 S bits is assumed to be an information (data) bit). DS3 AIS is defined in Table 2.

Table 2 DS3 AIS Format

X (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
X (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
P (p)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
P (p)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (0)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (0)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**

Notes

1. valid M-frame alignment bits (M-bits), M-subframe alignment bits (F-bits), and parity bit of the preceding M-frame (P-bits). The two P-bits are identical, either both are zeros or ones.
2. all the C-bits in the M-frame are set to zeros
3. the X-bits are set to ones
4. the information bit (84 Data bits with repeating sequence of 1010..)

Elastic Store

The elastic store block is provided to buffer for instantaneous frequency differences between the DS-3 stream extracted from the STS-1 (STM-0/AU3) SPE and the incoming reference clock. The DS3 Demapper extracts I bits from the STS-1 (STM-0/AU3) SPE and writes the bits into a 128 bit (16 byte) elastic store. Eight bytes are provided for SONET/SDH overhead (3 bytes for TOH, 1 byte for a positive stuff, 1 byte for POH) and DS3 reserve stuffing bits (2 bytes for R bits, and 3 overhead bits which is rounded-up to 1 byte). The remaining 8 bytes are provided for path pointer adjustments.

Data is read out of the Elastic Store using a divide by 8 version of the input reference 51.84 MHz clock. If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

DS3 Desynchronizer

The Desynchronizer monitors the Elastic Store level to control the de-stuffing algorithm to avoid overflow and underflow conditions. The Desynchronizer assumes a 51.84 MHz.

11.5 DS3 Framer (DS3-FRMR)

The DS3 Framer (DS3-FRMR) Block integrates circuitry required framing to the resulting demapped DS3 bit stream. The DS3-FRMR is directly compatible with C-bit parity DS3 applications.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e., the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and out-of-frame is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the DS3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 Framer Configuration register. The 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation, in the presence of a high bit error rate, than the 3 out of 16 consecutive F-bits ratio. Either out-of-frame criteria allows an out-of-frame defect to be detected quickly when the M-subframe alignment pattern or optionally, when the M-frame alignment pattern is lost.

Also while in-frame, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications are accumulated in the DS3 Performance Monitor (DS3 PMON). Note that the framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the alarm indication signal, and the idle signal) are detected by the DS3-FRMR. The maintenance detection algorithm employs a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate. For AIS, the expected pattern may be selected to be: the framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero; the framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored); or the unframed all-ones signal (with overhead bits equal to ones). Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0. DS3 Loss of Frame detection is provided in a manner compatible with ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms + 75µs ± 75µs. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

Valid X-bits are extracted by the DS3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic 0 (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic 1 (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame.

When the C-bit parity application is enabled, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the Path Maintenance Data Link are received by the Data Link Receiver (RDLC).

The DS3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of OOF or RED, or AIS. The DS3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

Each DS3-FRMR extracts its entire DS3 overhead (56 bits per M-frame – Excluding the F bits) using the ROHVAL, ROHCH[5:0], ROH, and ROHFP outputs of the S/UNI-MACH48. Unused bits are output in the positions of the F framing bits.

The DS3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the DS3-FRMR. Access to these registers is via a generic microprocessor bus.

11.6 DS3 PMON Performance Monitor Accumulator (DS3-PMON)

The DS3 Performance Monitor (DS3-PMON) Block interfaces directly with the DS3 Framer (DS3-FRMR) to accumulate parity error (PERR) events, path parity error (CPERR) events, far end block error (FEBE) events, and framing bit error (FERR) events using saturating counters. The PMON stops accumulating error signal from the DS3 Framer once frame synchronization is lost.

When an accumulation interval is signaled by a write to the DS3-PMON register address space or a write to the S/UNI-MACH48 Global Monitor Update register, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. In addition, a register is provided to indicate changes in the DS3-PMON counters since the last accumulation interval.

11.7 DS3 Bit-Oriented Code Detector (RBOC)

The Bit-Oriented Code Detector is only used in DS3 C-bit Parity.

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) contained in the DS3 C-bit parity far-end alarm and control (FEAC) channel or in the J2 datalink signal stream. The 64^{th} code ("111111") is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes (BOCs) are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") when no valid code is detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code is removed.

11.8 DS3 Facility Data Link Receiver (RDLC)

The RDLC is a microprocessor peripheral used to receive LAPD/HDLC frames on the DS3 C-bit parity Path Maintenance Data Link.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

11.9 SMDS PLCP Layer Receiver (SPLR)

The SMDS PLCP Layer Receiver (SPLR) Block integrates circuitry to support DS3 PLCP frame processing. The SPLR provides framing for PLCP based transmission formats.

The SPLR frames to DS3 based PLCP frames with a maximum average reframe time of 22 µs. Framing is declared (out of frame is removed) upon finding 2 valid, consecutive sets of framing (A1 and A2) octets and 2 valid and sequential path overhead identifier (POHID) octets. While framed, the A1, A2, and POHID octets are examined. OOF is declared when an error is detected in both the A1 and A2 octets or when 2 consecutive POHID octets are found in error. LOF is declared when an OOF state persists for more than 1 ms. If the OOF events are intermittent, the LOF counter is decremented at a rate 1/12 of the incrementing rate. LOF is thus removed when an in-frame state persists for more than 12 ms for a DS3 signal. When LOF is declared, PLCP reframe is initiated.

Framing octet errors and path overhead identifier octet errors are indicated as frame errors. Bit interleaved parity errors and far end block errors are indicated. The yellow signal bit is extracted and accumulated to indicate yellow alarms. Yellow alarm is declared when 10 consecutive yellow signal bits are set to logical 1; it is removed when 10 consecutive received yellow signal bits are set to logical 0. The C1 octet is examined to maintain nibble alignment with the incoming transmission system sublayer bit stream.

11.10 PLCP Performance Monitor (PLCP PMON)

The PLCP Performance Monitor (PLCP PMON) Block interfaces directly to the SPLR to accumulate bit interleaved parity error events, framing octet error events, and far end block error events in saturating counters. When the PLCP framer (SPLR) declares loss of frame, bit interleaved parity error events, framing octet error events, far end block error events, header check sequence error events are not counted.

When an accumulation interval is signaled by a write to the PLCP PMON register address space or to the S/UNI-MACH48 Identification and Global Monitor Update register, the PLCP PMON transfers the current counter values into holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

11.11 DS3 Pseudo-Random Sequence Generator/Detector (PRGD)

The DS3 Pseudo-Random Sequence Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer. Two types of test patterns (pseudo-random and repetitive) conform to ITU-T O.151. The PRGD is used for error diagnostic testing on DS3 channels. There is only one PRGD block to service any one of the 48 possible DS3 channels. The PRGD receiver and transmitter can operate on independent DS3 channels.

The PRGD can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern. The PRGD can perform an auto-synchronization to the expected pattern, and generate interrupts on detection and loss of the specified pattern. The PRGD can accumulate the total number of bits received and the total number of bit errors in two saturating 32-bit counters. The counters accumulate over an interval defined by writes to the S/UNI-MACH48 Global Monitor Update register or by writes to a PRGD accumulation register. When an accumulation is forced by either method, then the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation. In addition to the two counters, a record of the 32 bits received immediately prior to the accumulation is available.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N bits, the PRGD will load N bits from the detected stream, and determine whether the received pattern repeats itself every N subsequent bits. Should it fail to find such a pattern, it will continue loading and checking until it finds a repetitive pattern. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences. Whenever a PRGD accumulation is forced, the PRGD stores a snapshot of the 32 bits received immediately prior to the accumulation. This snapshot may be examined in order to determine the exact nature of the repetitive pattern received by PRGD.

The pseudo-random or repetitive pattern can be inserted/extracted in the DS3 payload. It cannot be inserted into the ATM cell or POS frame payload.

11.12 SONET/SDH PRBS Generator and Monitor (PRGM)

The SONET/SDH Pseudo-Random bit sequence Generator and Monitor (PRGM) block generates and monitors an unframed 2^{23}-1 payload test sequence on the ingress and egress TelecomBus bus timeslots.

The PRGM can generate PRBS in an STS-1/3c/12c/48c (AU3/4/4—4c/4-16c) payload. The path overhead column, the fixed stuff columns #2 to #4 in an STS-12c (AU-4-4c) payload, the fixed stuff columns #2 to16 in an STS-48c (AU-4-16c) payload and the fixed stuff column #30 and #59 in an STS-1 (AU3) payload do not contain any PRBS data.

When processing a concatenated STS-48c (STM-16c) payload, 4 PRGMs are linked in a master/slave configuration. The master PRGM co-ordinates the distributed PRBS generation between itself and the slave PRGMs. Each PRGM generates one quarter of the complete PRBS sequence. To ensure that the slave PRGMs are synchronized with the master PRGM, a signature is continuously broadcasted by the master PRGM to allow the slave PRGMs to check their relative states. A signature mis-match is flagged as an out-of-synch state by the slave PRGM. A re-synchronization of the PRBS generation must be initiated by the master PRGM (under software control).

The PRBS monitor of the PRGM block monitors the recovered payload data for the presence of an unframed 2^{23}-1 test sequence and accumulates pattern errors detected based on this pseudo-random pattern. The PRGM declares synchronization when a sequence of 4 correct pseudo-random patterns (bytes) are detected consecutively. Pattern errors are only counted when the PRGM is in synchronization with the input sequence. When 3 consecutive pattern errors are detected, the PRGM will fall out of synchronization and will continuously attempt to re-synchronize to the input sequence until it is successful.

When processing a concatenated STS-48c (STM-16c) payload, the master PRGM and the slave PRGMs independently monitor one quarter of the complete PRBS sequence. To ensure that the slave PRGMs are synchronized with the master PRGM, the same signature matching will be performed as described for the PRBS generation.

A maskable interrupt is activated to indicate any change in the synchronization status.

11.13 Receive Channel Assigner (RCAS-12)

The Receive Channel Assigner is used to group STS-1/STM-0 system timeslots into channels and transform the internal DS3 serial streams into byte-wide format for processing by the RTDP block. Channel numbers are associated with the Utopia/POS interface RADR[5:0] values.

The RCAS-12 works on an STS-12/STM-4 data stream. It allows the STS-12/STM-4 data stream to be split into DS3, STS-1/STM-0, STS-3c/STM-1, and STS-12c/STM-4 channels. STS-48c/STM-16c data streams do not require processing by the RCAS blocks because no channel division is required.

An RCAS-12 block can assign data streams to one of 12 possible channels. STS-12c/STM-4c channels can be assigned to channels 0, 12, 24, and 36. STS-3c/STM-1 channels can be assigned within a range associated with the STS-12 stream which it belongs to. STS-1/STM-0 and DS3 channels can be assigned to any timeslot not already allocated to others but must also reside within the range of channel values allocated to the STS-12 stream to which it belongs.

An STS-48c stream will occupy all timeslots and will be transmitted across 4 RCAS12 blocks. An STS-48c data stream must be assigned to channel 0.

The line side timeslot mappings can be arbitrary since the IWTI and IPTI blocks can be used to move timeslots.

11.14 Receive Time-sliced Datacom Processor (RTDP)

The Receive Time-sliced Datacom Processor (RTDP) performs both ATM and HDLC processing. It has the capability to process combinations of DS3, STS-1/STM-0, STS-3c/STM-1 channels with aggregate throughput up to STS-12/STM-4 rates.

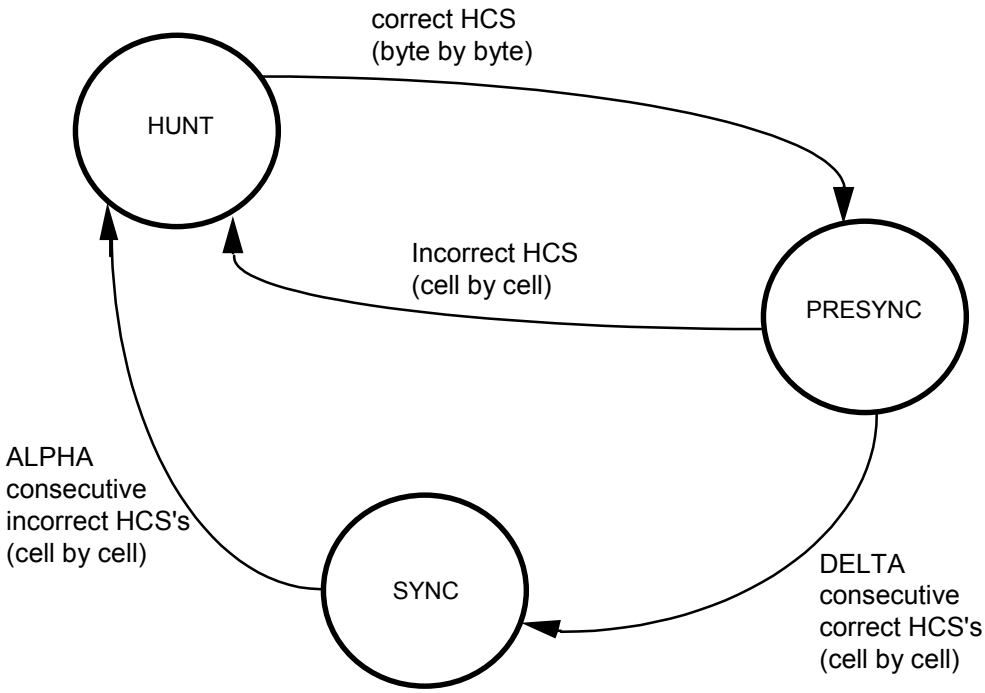
11.14.1 RTDP ATM Processor

In ATM mode, the RTDP performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling

Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the SONET/SDH SPE or DS3 PLCP paylaod, or nibbled aligned to the DS3 framing bit for direct-mapped ATM. The cell delineation algorithm searches the 53 possible cell boundary candidates (or 106 possible nibble-wide candidates for DS3) individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 7

Figure 7 Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 2 µs for the STS-48c/STM-16c rate, 8 µs for the STS-12c/STM-4c rate, 31 µs for the STS-3c/STM-1 rate, 93 µs for the STS-1/STM-0 rate, and 127 µs for DS3 ATM.

Descrambler

The self-synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RTDP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if HCS errors are detected, or if the header contents match the pattern contained in the RTDP Idle Cell Header and Mask register. Idle cell filtering is accomplished by writing the appropriate cell header pattern into the RTDP Idle Cell Header and Mask Pattern and register. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RTDP Idle Cell Header and Mask register allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RTDP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result.

Performance Monitor

The Performance Monitor consists of two 16-bit saturating HCS error event counters, a 32-bit saturating receive cell counter, and a 32-bit saturating Idle cell counter. The first error counter accumulates HCS errors. A 32-bit receive cell counter counts all cells written into the receive FIFO. Filtered Idle cells are counted in another 32-bit counter.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss any counted events.

11.14.2 RTDP Packet Processor

The RTDP performs PPP and HDLC packet extraction, provides FCS error detection, performs packet payload descrambling, and provides performance monitoring functions.

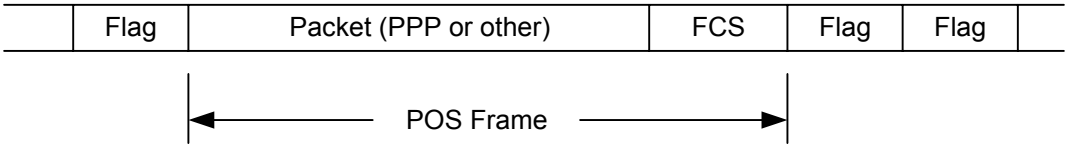
Descrambler

When enabled, the self-synchronous descrambler operates on the PPP Frame data, descrambling the data with the polynomial $x^{43} + 1$. Descrambling is performed on the raw HDLC/PPP data stream, before any PPP frame delineation or byte destuffing is performed. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

PPP/HDLC Frame Delineation

The PPP/HDLC Frame Delineation is performed on the descrambled data and consists of arranging the framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag and Idle Sequences and passes the data onto the Bit or Byte Destuffing block. The PPP/HDLC Frame format is shown on Figure 8.

Figure 8 PPP/HDLC Over SONET Frame Format



In the event of a FIFO overflow caused by the FIFO being full while a packet is being received, the packet is marked with an error so it can be discarded by the system. Subsequent bytes associated with this now aborted frame are discarded. Reception of PPP/HDLC data resumes when a Start of Packet is encountered and the FIFO level is below a programmable Reception Initialization Level.

Byte Destuffing

The byte destuffing algorithm searches the Control Escape character (0x7D). These characters, listed in Table 3, are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XORed with 0x20. Therefore, any escaped data byte will be processed properly by the S/UNI-MACH48.

Table 3 Byte Destuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Aborted Packet	7D-7E

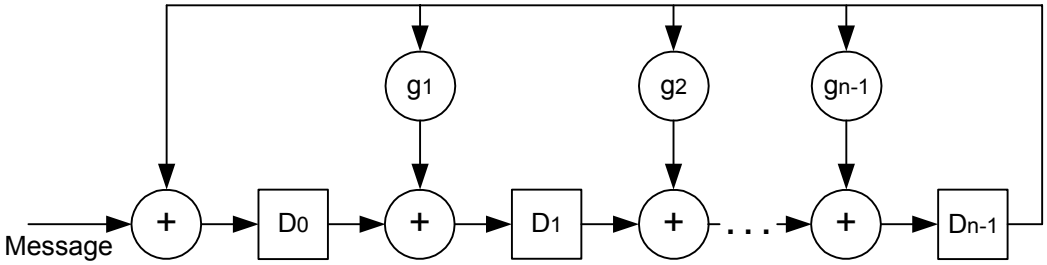
Bit Destuffing

The bit destuffing is used for DS3 HDLC data streams. The logic 0 detected immediately after 5 consecutive logic 1's (aside from Flag or Idle characters) is treated as a zero-stuff bit and is removed before further processing continues. The zero-stuff bits are inserted to assure transition density and for valid detection of Flags and Idle characters.

FCS Check

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, after byte destuffing and data descrambling scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. Packets with FCS errors are marked as such and should be discarded by the system.

Figure 9 CRC Decoder



Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters, one 32-bit saturating received good packet counter, and one 32-bit counter for accumulating packet bytes. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 32-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

The RTDP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but still written into the FIFO. Malformed packets, that is packets that do not at least contain four bytes, are discarded and the MINPLI interrupt will be asserted, but the malformed packet will not be counted. When the packet size exceeds MAXPL[16:0] the packet is marked with an error and the bytes beyond the maximum count are discarded.

11.15 Receive Cell and Frame Processor (RCFP)

The Receive Cell and Frame Processor (RCFP) performs both ATM and PPP processing. It has the capability to process a single STS-12c/STM-4c channel or a single STS-48c/STM-16c channel.

RCFP ATM Cell Processor

In ATM mode, the RCFP performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. Details on each of these functions can be found in the RTDP description.

RCFP POS Frame Processor

The RCFP performs PPP packet extraction, provides FCS error detection, performs packet payload descrambling, and provides performance monitoring functions. Details on each of these functions can be found in the RTDP description. Note that the RCFP only processes byte synchronous PPP, not bit synchronous HDLC.

The RCFP handles malformed packets (smaller than 4 bytes) differently than the RTDP. In the RCFP, the minimum packet violation is counted in MINPL, while for the RTDP, they only cause MINPLI to be asserted. Note that the FCS calculation in the RCFP will proceed independent of any errors detected upstream. Thus, under abort, max length violations, etc, one might also get FCS violations.

11.16 PHY-to-Layer Decoupling FIFO (RXSDQ)

The RXSDQ provides FIFOs for each channel to separate the receive line-side timing from the higher layer ATM system timing. FIFO space can be allocated to different channels in blocks of 16 bytes. The receive FIFO holds a maximium of 768 blocks. For instance, if the S/UNI-MACH48 is configured to carry one STS-12c and 36 STS-1 POS channels, the FIFO can allocate space for 192 blocks for the STS-12c channel and 16 blocks for each of the 36 STS-1s. This would fully utilize the entire FIFO storage space. The maximum value that can be allocated to any single channel is 192 blocks.

The RXPHY provides either a Utopia Level 3 or a POS-PHY Level 3 interface to read data from the FIFO.

ATM Receive FIFO

The Receive FIFO is responsible for holding cells until they are read by Receive System Interface.

Receive FIFO management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions. Upon detection of an overrun, the FIFO discards the current cell and subsequent cells until there is room in the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit and are considered a system error.

POS Receive FIFO

The Receive FIFO block contains storage capacity for 256 octets for each of the 48 possible channels, along with management circuitry for reading and writing the FIFO. The receive FIFO provides for the separation of the physical layer timing from the system timing.

Receive FIFO management functions include filling the receive FIFO, indicating when packets or bytes are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun, the FIFO aborts the current packet and subsequent bytes until there is room in the FIFO. Once enough room is available, as defined by the BT[7:0] register bit settings, the RXSDQ will wait for the next start of packet before writing any data into the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit, and are considered a system error. A FIFO underrun is caused when the System Interface tries to read more data words while the FIFO is empty. This action will be detected and reported through the FUDRI interrupt, but it is not considered a system error. The system will continue to operate normally. In that situation, RVAL can be used by the Link Layer device to find out if valid or invalid data is provided on the System Interface.

11.17 Output Parallel TelecomBus Interface

The Output Parallel TelecomBus Interface maps payload on a SONET/SDH template of 4xSTS-12/STM-4 or 1xSTS-48/STM-16 buses. Markers for J0/J1 byte locations are given to signal the frame alignment. Payload and non-payload bytes are also marked appropriately. Alarm conditions can also be indicated on the interface. The interface is clocked with the 77.76 MHz SYSCLK. The output J0/J1 byte alignment on the parallel TelecomBus is aligned to the input OJ0REF signal.

11.18 Output Serial TelecomBus Interface

The Output Parallel TelecomBus Interface maps payload on a SONET/SDH template of 4x777.6Mbps LVDS compatible bus. Markers for J0/J1 byte locations are given to signal the frame alignment. Payload and non-payload bytes are also marked appropriately. Alarm conditions can also be indicated on the interface. The output J0/J1 byte alignment on the serial TelecomBus is referenced to the input OJ0REF signal.

11.19 DS3 Mapper (D3MA)

The DS3 Mapper (D3MA) block maps a DS3 signal into an STS-1 (STM-0/AU3) payload and compensate for any frequency differences between the incoming DS3 serial bit rate and the available STS-1 (STM-0/AU3) SPE mapped payload capacity. The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. Refer to Table 1 for a description of the DS3 mapping.

DS3 Serializer

Incoming DS3 ATM or packet data is sampled from the TCAS-12 block, deserialized and written into the Elastic Store. The DS3 clock rate is taken from the DS3TICLK input pin of the S/UNI-MACH48.

Elastic Store

The elastic store block is provided to compensate for frequency differences between the DS-3 stream (DS3TICLK) and the STS-1 (STM-0/AU3) SPE capacity (SYSCLK). The DS3 Serializer writes data into the elastic store at the DS3TICLK/8 rate while data is read out at the stuffed STS-1 (STM-0/AU3) byte rate. If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

DS3 Synchronizer

The DS3 Synchronizer performs the mapping of the DS3 into the STS-1 (STM-0/AU3) SPE. The DS3 Synchronizer monitors the Elastic Store level to control the stuffing algorithm to avoid overflow (i.e. run faster) and underflow (i.e. run slower) conditions. The fill level of the elastic store is monitored and stuff opportunities in the DS3 mapping are used to center the Elastic Store. To consume a stuff opportunity, the five C-bits on a row are set to ones and the S bit is used to carry an DS3 information bit. When the S bit is not used to carry information, the C-bits on the row are set to zeros.

11.20 DS3 Transmitter (DS3-TRAN)

The DS3 Transmitter (DS3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream. The DS3-TRAN is directly compatible with C-bit parity DS3 formats.

Status signals such as far end receive failure (FERF), the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of OOF or RED, or AIS by the DS3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the DS3-TRAN. When C-bit parity mode is selected, the path parity bits, and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The path maintenance data link messages are sourced by the TDPR data link transmitter. These overhead signals can also be overwritten by using the TOH and TOHINS inputs.

The DS3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

User control of each of the overhead bits in the DS3 frame is provided. Overhead bits may be inserted on a bit-by-bit basis from a user supplied data stream by using the TOH, TOHINS, TOHFP, TOHCH[5:0], and TOHVAL signals.

11.21 DS3 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator (XBOC) Block transmits 63 of the possible 64 bit oriented codes (BOC) in the C-bit parity Far End Alarm and Control (FEAC) channel. A BOC is a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The code to be transmitted is programmed by writing the XBOC Code Register. The 64th code (111111) is similar to the HDLC idle sequence and is used to disable the transmission of any bit oriented codes. When transmission is disabled, the FEAC channel is set to all ones.

The XBOC allows programmable repetitions of the BOC code. The desired BOC code can be configured to repeat an integer number (N = 1 to 16) of times. An interrupt will signal when the programmed BOC code has been latched and transmission started. The user can then disable BOC transmission at this time to ensure the BOC code is only repeated N times. If the user does not disable BOC transmission, the XBOC will transmit the BOC code another N times.

11.22 DS3 Facility Data Link Transmitter (TDPR)

The DS3 Facility Data Link Transmitter (TDPR) provides a serial data link for the C-bit parity path maintenance data link. The TDPR HDLC facility data link transmission is controlled by the external microprocessor. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) can optionally be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits flags (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the TDPR Transmit Data Register. The TDPR automatically begins transmission of data once at least one complete packet is written into its FIFO. All complete packets of data will be transmitted if no error condition occurs. After the last data byte of a packet, the CRC FCS (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. The TDPR will also force transmission of the FIFO data once the FIFO depth has surpassed the programmable upper limit threshold. Transmission commences regardless of whether or not a packet has been completely written into the FIFO. The user must be careful to avoid overflowing and underflowing the FIFO. Underruns can only occur if the packet length is greater than the programmed upper limit threshold because, in such a case, transmission will begin before a complete packet is stored in the FIFO. All bytes which cause an overflow of the FIFO are ignored.

An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data. Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort sequences (01111111 sequence where the 0 is transmitted first) can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR register bit. An abort sequence will also be transmitted if the user overflows the FIFO with a packet of length greater than 128 bytes. Overflows where other complete packets are still stored in the FIFO will not generate an abort. Only the packet which caused the overflow is corrupted and an interrupt is generated to the user via the OVR register bit. The other packets remain unaffected.

When the TDPR is disabled, a logical 1 (Idle) is inserted in the DS3 path maintenance data link.

11.23 SMDS PLCP Layer Transmitter (SPLT)

The SMDS PLCP Layer Transmitter (SPLT) Block integrates circuitry to support DS3 based PLCP frame insertion.

The SPLT automatically inserts the framing (A1, A2) and path overhead identification (POHID) octets and provides registers or automatic generation of the F1, B1, G1, M2, M1 and C1 octets.

Registers are provided for the path user channel octet (F1) and the path status octet (G1). The bit interleaved parity octet (B1) and the FEBE subfield are automatically inserted.

The DQDB management information octets, M1 and M2 are generated. The type 0 and type 1 patterns described in TA-TSY-000772 are automatically inserted. The type 1 page counter may be reset using a register bit in the SPLT Configuration register. Note that this feature is not required for the ATM Forum compliant DS3 UNI. For this application, the M1 and M2 octets must be set to all zeros.

The PLCP transmit frame C1 cycle/stuff counter octet and the transmit stuffing pattern can be referenced to the REF8K input pin, an internally generated 8 kHz reference synchronized to SYSCLK, or a selected received PLCP frame pulse. Alternatively, a fixed stuffing pattern may be inserted into the C1 cycle/stuff counter octet. In this mode, the C1 stuffing is generated based on the received stuffing pattern as determined by the SPLR block.

When DS3 PLCP format is enabled, the C1 octet indicates the phase of the 375 µs nibble stuffing opportunity cycle. During frame one of the three frame cycle, the pattern FFH is inserted in the C1 octet, indicating a 13 nibble trailer length. During frame two, the pattern 00H is inserted, indicating a 14 nibble trailer length. During frame three, the pattern 66H or 99H is inserted, indicating a 13 or 14 nibble trailer length respectively.

The Zn, growth octets are set to 00H.

11.24 Transmit Channel Assigner (TCAS-12)

The Transmit Channel Assigner is used to map channel numbers from the Utopia/POS interface (TADR[5:0] values) into STS-1 timeslots. It also serializes data to interface the TTDP to the DS3-TRAN blocks.

The TCAS-12 works on an STS-12/STM-4 datastream from an upstream TTDP or TCFP block. It allows the STS-12/STM-4 data stream from the TTDP or TCFP to be split into DS3, STS-1, STS-3c/STM-1, and STS-12c/STM-4 channels. STS-48c/STM-16c data streams do not require processing by the TCAS blocks because no channel division is required.

A TCAS-12 block can assign data streams from one of 12 possible channels. STS-12c/STM-4c timeslots can be taken from channels 0, 12, 24, and 36. STS-3c/STM-1 timeslots can be from a range of channels associated with the STS-12 channel which it belongs to. STS-1/STM-0 and DS3 timeslots can be taken from any channel not already allocated to others but must also reside within the range of timeslot range allocated to the STS-12 channel to which it belongs to

An STS-48c channel will occupy all timeslots and will be transmitted across 4 RCAS12 blocks. An STS-48c data stream must be taken from channel 0.

The timeslot mapping on the line side is arbitrary since the OWTI and OPTI blocks can remap the system side timeslots to any position.

11.25 Transmit Time-sliced Datacom Processor (TTDP)

The Transmit Time-sliced Datacom Processor (TTDP) performs both ATM and PPP/HDLC processing. It has the capability to process multiple sub-STS-12c/STM-4c channels. It can handle combinations of DS3, STS-1/STM-0, STS-3c/STM-1 channels with aggregate throughput up to STS-12/STM-4 rates.

11.25.1 TTDP ATM Processor

In ATM mode, the TTDP performs provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling.

Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler ($x^{43} + 1$ polynomial) described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

11.25.2 TTDP Packet Processor

The TTDP Frame Processor provides rate adaptation by transmitting flag sequences (0x7E) or Idle sequences (0xFF) between packets, provides FCS generation and insertion, performs byte/bit stuffing and data scrambling, and provides performance monitoring functions.

PPP/HDLC Frame Generator

The PPP/HDLC Frame Generator generates packets whose format is shown in Figure 8. Flags or Idle sequences are inserted whenever the Transmit FIFO (TXSDQ) is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packets from the Transmit FIFO and transmits them. In addition, FCS generation, error insertion, bit stuffing (for DS3) or byte stuffing, and scrambling can be optionally enabled.

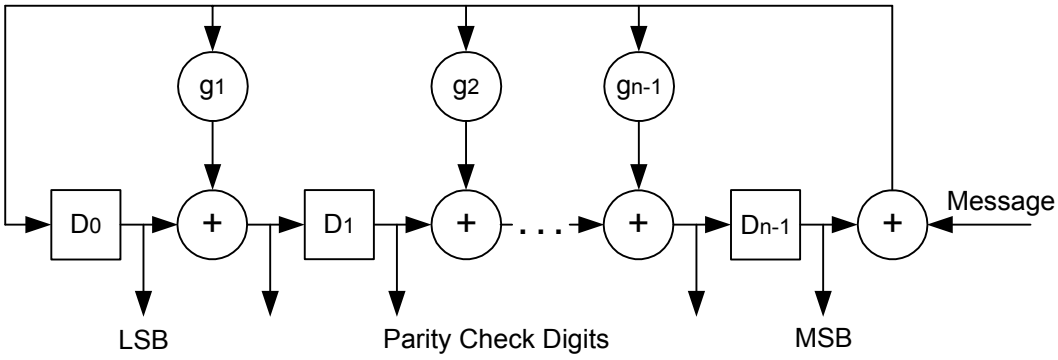
In the event of a FIFO underflow caused by the TXSDQ FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The PPP Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). The bit synchronous HDLC Abort Sequence is 11111111. Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with the Flag Sequence in the outgoing data stream. Transmission of data resumes when a Start of Packet is encountered in the FIFO data stream.

The POS Frame Generator also performs Inter Packet Gapping. This operation consists of inserting a programmable number of Flag and Idle Sequence characters between each PPP/HDLC Frame transmission. This feature allows one to control the system effective data transmission rate if required.

FCS Generator

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the one's complement of the CRC register after calculation ends. FCS calculation and insertion can be disabled.

Figure 10 CRC Generator



An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting the resulting FCS value, before transmission. This should cause an FCS Error at the far end.

Byte Stuffing

The PPP Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are being escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is being escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 4 Byte Stuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Abort Sequence	7D-7E

Bit Stuffing

The bit stuffing procedure is used for DS3 HDLC data streams. A logic 0 bit is inserted after every occurrence of 5 consecutive logic 1's (aside from Flag or Idle characters). The zero-stuff bits are inserted to assure transition density and to ensure Flag and Idle characters are unique.

Data Scrambling

The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

11.26 Transmit Cell and Frame Processor (TCFP)

The Transmit Cell and Frame Processor (TCFP) performs both ATM and PPP processing. It has the capability to process a single STS-12c/STM-4c channel or a single STS-48c/STM-16c channel.

TCFP ATM Cell Processor

In ATM mode, the TCFP provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, performs ATM cell scrambling, and provides performance monitoring functions. Details on each of these functions can be found in the TTDP description.

TCFP PPP Frame Processor

The TCFP provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs byte stuffing and packet data scrambling, and provides performance monitoring functions. Details on each of these functions can be found in the TTDP description. Details on each of these functions can be found in the TTDP description. Note that the TCFP only generates byte synchronous PPP frames, not bit synchronous HDLC frames.

The TCFP behavior differs from that of the TTDP in the behavior of counters for an aborted packet due to under-run. The TCFP counters are not aware of the under-run condition, and thus the Abort counter is not incremented for this condition, and all remaining bytes of the aborted packet are counted.

11.27 Layer-to-PHY Decoupling FIFO (TXSDQ)

The TXSDQ provides FIFOs for each channel to separate the higher layer ATM system timing from line-side timing. Each STS-1/STM-0 or DS3 channel is given a 256 byte (4 ATM cells) FIFO by default. Channels of higher data rates can be given proportionately more FIFO space up to a maximum of 3072 bytes in increments of 16 byte blocks.

The TXPHY provides either a Utopia Level 3 or a POS-PHY Level 3 interface to transfer data to the FIFO.

ATM Transmit FIFO

The Transmit FIFO is responsible for holding cells provided through the Transmit System Interface until they are transmitted. FIFO space can be allocated to different channels in blocks of 16 bytes. The transmit FIFO holds a maximium of 768 blocks (192 ATM cells). For instance, if the S/UNI-MACH48 is configured to carry one STS-12c and 36 STS-1s, the FIFO can allocate space for 48 ATM cells (192 blocks) for the STS-12c channel and 4 ATM cells (16 blocks) for each of the 36 STS-1s. This would fully utilize the entire FIFO storage space. The maximum value that can be allocated to any single channel is 192 blocks (48 ATM cells).

The cells are written in with a single 32-bit data bus running off TFCLK and are read out at the channel rate. Internal read and write pointers track the cells and indicate the fill status of the Transmit FIFO. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing (TFCLK).

POS Transmit FIFO

The Transmit FIFO is responsible for holding packets provided through the Transmit System Interface until they are transmitted. FIFO space can be allocated to different channels in blocks of 16 bytes. The transmit FIFO holds a maximium of 768 blocks. For instance, if the S/UNI-MACH48 is configured to carry one STS-12c and 36 STS-1 POS channels, the FIFO can allocate space for 192 blocks for the STS-12c channel and 16 blocks for each of the 36 STS-1s. This would fully utilize the entire FIFO storage space. The maximum value that can be allocated to any single channel is 192 blocks.

Octets are written in with a single 32-bit data bus running off TFCLK and are read out with a single 32-bit data bus or 4 8-bit data busses at the channel rate. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing.

Internal read and write pointers track the insertion and removal of octets, and indicate the fill status of the Transmit FIFO. These status indications are used to detect underrun and overrun conditions, abort packets as appropriate on both System and Line sides, control flag insertion and to generate the STPA and PTPA outputs.

11.28 ATM UTOPIA and Packet Over SONET POS-PHY System Interfaces (RXPHY and TXPHY)

The S/UNI-MACH48 system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides a 32-bit UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI-MACH48. When configured for POS applications, the system interface provides either a 32-bit POS-PHY Level 3 compliant bus for the transfer of ATM cells and data packets between the link layer device and the S/UNI-MACH48. The link layer device can implement various protocols, including PPP and HDLC.

Receive UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a read clock (RFCLK) and read enable signal (RENB). The interface indicates the start of a cell (RSOC) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA signal indicates when a cell is available for transfer on the receive data bus RDAT[31:0]. The RPRTY signal reports the parity on the RDAT[31:0] bus (selectable as odd or even parity). Read accesses while RCA is deasserted will output invalid data.

Receive POS-PHY Level 3

The interface accepts a read clock (RFCLK) and read enable signal (RENB) when data is read from the receive FIFO (using the rising edge of the RFCLK). The start of packet RSOP marks the first byte of receive packet/cell data on the RDAT[31:0]. The RPRTY signal determine the parity on the RDAT[31:0] bus (selectable as odd or even parity). The end of a packet/cell is indicated by the REOP signal. Signal RERR is provided to indicate that an error in a received packet has occurred (the error may have several causes include an abort sequence or an FCS error). The RVAL signal is used to indicate when RSOP, REOP, RERR and RDAT[31:0] are valid. Read accesses while RVAL is logic 0 are ignored and will output invalid data. RSX indicates the start of a transfer and marks the clock cycle where the in-band channel address is given on the RDAT bus. The RXPHY performs the polling procedure to select which PHY address is serviced.

Transmit UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). To reduce FIFO latency, the FIFO depth at which TCA indicates “full” can be configured from the TXSDQ. If the programmed depth is less than the TXSDQ FIFO capacity, more than one cell may be written after TCA is deasserted as the TXSDQ FIFO still retains its full capacity. The interface provides the transmit cell available status (TCA) which can transition from "available" to "unavailable" when the transmit FIFO is near full or when the FIFO is full and can accept no more writes. The TTDP and TCFP cell processors automatically transmit idle cells until a full cell is available to be transmitted.

The SUNI-MACH48 Transmit UTOPIA Level 3 interface ignores TSOC for the start of cell indication, and uses the sampled high to low transition of TENB as the start of cell. However, if TSOC is missing, a SOPI and EOPI interrupts may be generated, though cells will pass through correctly. TENB must also be asserted (low) for the complete duration of a cell transfer (13 cycles). If TENB is low for other than an integer multiple of 13 cycles, runt cells will be generated. Note that when a runt cell is detected by the Transmit UTOPIA Level 3 interface, the next valid cell will also be discarded.

Transmit POS-PHY Level 3 Interface

The POS-PHY Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of packet/cell (TSOP) indication, the end of packet/cell (TEOP) indication, errored packet (TERR) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). The STPA signal reports the selected transmit FIFO’s fill status (the POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or an entire packet is in the FIFO). The PTPA signal shows the FIFO status for the polled channel. The TSX signal indicates when the in-band channel selection is given on the TDAT bus. This is done at beginning of each transfer sequence. The TMOD signal (Transmit Mod) is provided to indicate whether 1, 2, 3, or 4 bytes are valid of the final word transfer (TEOP is asserted). A packet may be aborted by asserting the TERR signal at the end of the packet.

11.29 SONET/SDH Inband Error Report Processor (SIRP)

The SIRP processes remote alarm indications of in a SONET/SDH data stream. The SIRP may be configured to extract remote defect indications (RDI) and remote error indications (REI) that have been inserted into the G1 byte by an external upstream device. These remote error indications are accumulated and reported at the G1 byte of the associated tributary in the outgoing data stream. Both RDI and extended RDI modes are available. The RDI report can be configured to be maintained asserted for at least 10 frames or 20 frames.

The RDI and REI indications on the transmit data stream can also be asserted manually under microprocessor control.

11.30 Timeslot Interchange (STSI)

An STSI block is used for each of the input and output parallel TelecomBus interfaces. For the serial TelecomBus interfaces, an STSI block is used for each of the input and output working and protection interfaces.

The STSI is used to re-order the timeslots inside a SONET/SDH data stream. The STS-48/STM-16 timeslots can be reordered on an STS-1/STM-0 granularity. Any STS-1/STM-0 can be dropped, moved or copied to one or more STS-1/STM-0 data streams inside a SONET/SDH data stream.

The STSI uses two configuration pages. Either of the two pages specifies the re-ordering operations to be performed on the data streams. In normal operation, one of the pages is active, containing the information used to reorder the current data stream. The other page can be updated by an external microprocessor in the background. When a configuration change is indicated, the two pages are swapped and the most recently updated page becomes the active page. Selection of the page currently in use is made using the ICMP and OCMP pins.

The re-ordering of the input STS-1/STM-0 payload is based on the output STS-1/STM-0 payload, i.e.: each output STS-1/STM-0 time slot is associated with one input STS-1/STM-0 time slot. By defining the re-ordering based on the output STS-1/STM-0 payload, the STSI directly supports multicast and broadcast.

11.31 Receive 8B/10B TelecomBus Decoder (R8TD)

The R8TD is used in the serial TelecomBus interface. The R8TD works in conjunction with an upstream block (PISO) that packs consecutive bits from an incoming 8B/10B serial link into a 10-bit wide stream with arbitrary alignment to the 8B/10B character boundaries.

The R8TD character alignment block uses the K28.5 control character (Comma control / transport frame alignment) to determine 8B/10B character alignment in the incoming stream. When the R8TD character alignment state machine is in the out-of-character-alignment state, it searches for the K28.5 character in all positions of the incoming stream. Upon detecting the K28.5 character, the R8TD will align its internal character boundary, the character alignment state machine will transition to the in-character-alignment state and cease searching for subsequent K28.5 characters. The character alignment block also monitors for line-code violations (LCV) which are accumulated in an internal register. If 5 or more LCVs are detected within a window of 15 characters, the R8TD will enter the out-of-character-alignment state and begin searching for the K28.5 character afresh.

Aligned characters are written into a 24-character FIFO that isolates the incoming timing domain from the outgoing timing domain and provides a means of synchronizing multiple R8TDs outputs.

In order to allow synchronization with other R8TDs that may have slightly different frame alignment and to allow for frame re-alignment, the R8TD frame alignment block monitors the character aligned data stream for the K28.5. An internal frame counter is maintained based on this character. If the K28.5 is found out of place three times then the frame alignment moves to the out-of-frame-alignment state. When in the out-of-frame-alignment state the first K28.5 will be written to the 0 position of the FIFO. The read pointer is then set by the OJ0FP signal to synchronize the output of the K28.5 characters which ensures that signals leaving the multiple R8TDs will have the same alignment.

The R8TD decodes 8B/10B control characters associated with specific SONET/SDH byte positions in an extended TelecomBus stream. In order to identify more SONET/SDH bytes than the 12 control characters available in the standard set, those control characters with balanced line codes for both positive and negative running disparity (K28.0, K28.4, K38.7, K27.7, K29.7 and K30.7) are treated specially, where the positive and negative disparity codes are each associated with a different SONET/SDH byte. The reception of these line-codes will not be considered LCVs due to a mismatch with the running disparity.

The R8TD provides a diagnostic loopback port where the outgoing stream from an associated Transmit 8B/10B Encoder block (T8TE) can be processed in place of the incoming stream.

11.32 Transmit 8B/10B TelecomBus Encoder (T8TE)

The T8TE encodes a data stream into an extended 8B/10B format for transmission on the serial TelecomBus LVDS links. The T8TE encodes TelecomBus control signals such as transport frame and payload boundaries, pointer justification events and alarm conditions into three levels of extended set of 8B/10B characters as well as performing the IEEE mode conversion on data. In order to identify more TelecomBus bytes and events than the 12 control characters available in the standard set, those control characters with balanced line codes for both positive and negative running disparity (K28.0, K28.4, K28.5, k28.6, k28.7, K27.7, K29.7 and K30.7) are treated specially. The positive and negative disparity codes are each associated of a different SONET/SDH byte or event.

The T8TE can be configured to operate in the Loopback mode which allows a line loopback from the associated R8TD block.

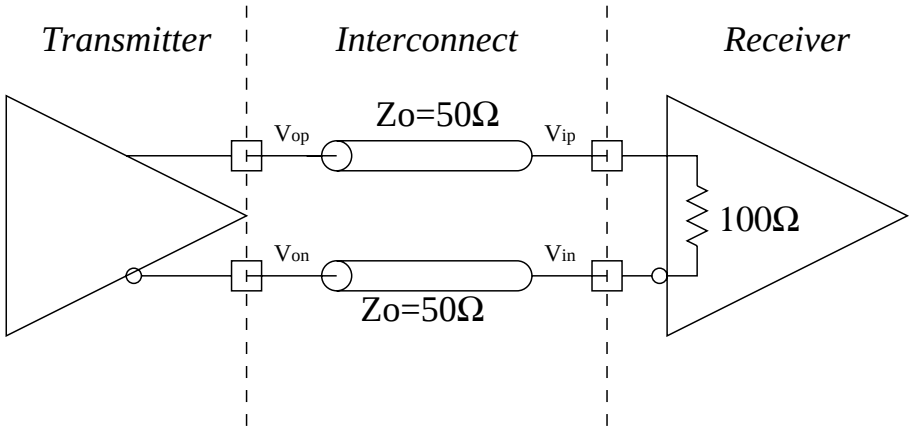
The T8TE uses a FIFO to bridge between the incoming data stream and the outgoing data stream clock domains.

11.33 LVDS Overview

The LVDS family of cells which allow the implementation of 777.6 Mb/s LVDS links. A reference clock of 77.76MHz is required. Four 777.6 Mb/s LVDS form a high-speed serial TelecomBus interface for passing an STS-48 aggregate data stream.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated in Figure 11 below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Figure 11 Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Ten-bit parallel data is sampled by the line rate divided-by-10 clock (77.76MHz SYSCLK) and then serialized at the line rate on the LVDS output pins by a 777.6MHz clock synthesized from SYSCLK. Serial line rate LVDS data is sampled and de-serialized to 10-bit parallel data. Parallel output transfers are synchronized to a gated line rate divided-by-10 clock. The 10-bit data is passed to an 8B/10B decoding block. The gating duty cycle is adjusted such that the throughput of the parallel interface equals the receive input data rate (Line Rate +/- 100ppm). It is expected that the clock source of the transmitter is the same as the clock source of the receiver to ensure the data throughput at both ends of the link are identical.

Data must contain sufficient transition density to allow reliable operation of the data recovery units. 8B/10B block coding and decoding is provided by the T8TE and R8TD blocks.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. Namely, a worst case eye opening of 0.7UI and 100mV differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of backplane connectors and up to 1m of backplane interconnects. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. Due to power constraints, the output differential amplitude is approximately 350mV.

If an LVDS transmitter is not used, its outputs can be left floating. If an LVDS Receiver is not used, its inputs can be left floating provided that the LVDS Receiver is disabled in software to minimize power consumption. Alternatively, the LVDS Receiver's inputs can be tied to ground if the link will not be used. Since these are LVDS receivers and not CMOS, there is no electrical problem in leaving them floating (as opposed to a CMOS input). Power dissipation is the same regardless of whether the input is connected or not, and no damage to the device will occur. If a hot-swap is desired, an LVDS Receiver can be left enabled and it will sync up when the far-end Transmitter is connected.

The LVDS system is comprised of the LVDS Receiver (RXLV), LVDS Transmitter (TXLV),), Transmitter reference (TXREF), data recovery unit (DRU), parallel to serial converter (PISO and Clock Synthesis Unit (CSU).

11.33.1 LVDS Receiver (RXLV)

The RXLV block is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Receiver according to the IEEE 1596.3-1996 LVDS Specification.

The RXLV block is the receiver in Figure 11, accepting up to 777.6 Mb/s LVDS signals from the transmitter, amplifying them and converting them to digital signals, then passing them to a data recovery unit (DRU). Holding to the IEEE 1596.3-1996 specification, the RXLV has a differential input sensitivity better than 100mV, and includes at least 25mV of hysteresis.

11.33.2 LVDS Transmitter (TXLV)

The TXLV block is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Transmitter according to the IEEE 1596.3-1996 LVDS Specification.

The TXLV accepts 777.6 Mbit/s differential data from a "parallel-in, serial-out" (PISO) circuit and then transmits the data off-chip as a low voltage differential signal.

The TXLV uses a reference current and voltage from the TXLVREF block to control the output differential voltage amplitude and the output common-mode voltage.

11.33.3 LVDS Transmit Reference (TXREF)

The TXLVREF provides an on-chip bandgap voltage reference (1.20V ±5%) and a precision current to the TXLV (777.6 Mb/s LVDS Transmitter) blocks. The reference voltage is used to control the common-mode level of the TXLV output, while the reference current is used to control the output amplitude.

The precision currents are generated by forcing the reference voltage across an external, off-chip 4.75kΩ (±1%) resistor. The resulting current is then mirrored through several individual reference current outputs, so each TXLV receives its own reference current.

11.33.4 Data Recovery Unit (DRU)

The DRU is a fully integrated data recovery and serial to parallel converter which can be used for 777.6 Mb/s NRZ data. An 8B/10B block code is used to guarantee transition density for optimal performance.

The DRU recovers data and outputs a 10-bit word synchronized with a line rate divided by 10 gated clock to allow frequency deviations between the data source and the local oscillator. The output clock is not a recovered clock. The DRU accumulates 10 data bits and outputs them on the next clock edge. If 10-bits are not available for transfer at a given clock cycle, the output clock is gated.

The DRU provides moderate high frequency jitter tolerance suitable for inter-chip serial link applications. It can support frequency deviations up to ±100ppm.

11.33.5 Parallel to Serial Converter (PISO)

The PISO is a parallel-to-serial converter designed for high-speed 777.6 Mb/s transmit operation.

11.33.6 Clock Synthesis Unit (CSU)

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 777.6 MHz for the use by the transmitter.

11.34 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-MACH48 identification code is 073900CD hexadecimal.

11.35 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-MACH48. In the following section every register is documented and identified using the register number (REG #). Addresses that are not shown are not used and must be treated as Reserved.

Table 5 Register Memory Map

Address	Register Description
0000	S/UNI-MACH48 Global Performance Monitor Update
0001	S/UNI-MACH48 Master Reset, Configuration, and Global Digital Loopback
0002	S/UNI-MACH48 Receive Timeslot Configuration #1
0003	S/UNI-MACH48 Receive Timeslot Configuration #2
0004	S/UNI-MACH48 Receive Timeslot Configuration #3
0005	S/UNI-MACH48 Receive Timeslot Configuration #4
0006	S/UNI-MACH48 Receive Timeslot Configuration #5
0007	S/UNI-MACH48 Receive Timeslot Configuration #6
0008	S/UNI-MACH48 Transmit Timeslot Configuration #1
0009	S/UNI-MACH48 Transmit Timeslot Configuration #2
000A	S/UNI-MACH48 Transmit Timeslot Configuration #3
000B	S/UNI-MACH48 Transmit Timeslot Configuration #4
000C	S/UNI-MACH48 Transmit Timeslot Configuration #5
000D	S/UNI-MACH48 Transmit Timeslot Configuration #6
000E	S/UNI-MACH48 DS3 PRBS Assignment
000F	S/UNI-MACH48 PLCP Reference and Clock Activity
0010	S/UNI-MACH48 DS3 Automatic Alarm Reporting, LOF Selection, TelecomBus Parity
0011	Receive Serial TelecomBus Synchronization Delay
0012	Miscellaneous
0013	Transmit TelecomBus Synchronization Delay
0014	Software General Purpose Register
0015	S/UNI-MACH48 Interrupt Block Identifier
0016	S/UNI-MACH48 IPTI, IWTI, RXPHY, RXSDQ, RTDPs, and RCFPs Interrupt Indication
0017	S/UNI-MACH48 OPTI, OWTI, TXPHY, TXSDQ, TTDPs, and TCFPs Interrupt Indication
0018	S/UNI-MACH48 SPLR #0-15 Interrupt Indication
0019	S/UNI-MACH48 SPLR #16-31 Interrupt Indication
001A	S/UNI-MACH48 SPLR #32-47 Interrupt Indication
001B	S/UNI-MACH48 DS3 PMON #0-15 Interrupt Indication
001C	S/UNI-MACH48 DS3 PMON #16-31 Interrupt Indication
001D	S/UNI-MACH48 DS3 PMON #32-47 Interrupt Indication
001E	S/UNI-MACH48 D3MA #0-15 Interrupt Indication
001F	S/UNI-MACH48 D3MA #16-31 Interrupt Indication
0020	S/UNI-MACH48 D3MA #32-47 Interrupt Indication
0021	S/UNI-MACH48 D3MD #0-15 Interrupt Indication
0022	S/UNI-MACH48 D3MD #16-31 Interrupt Indication
0023	S/UNI-MACH48 D3MD #32-47 Interrupt Indication
0024	S/UNI-MACH48 XBOC #0-15 Interrupt Indication

Address	Register Description
0025	S/UNI-MACH48 XBOC #16-31 Interrupt Indication
0026	S/UNI-MACH48 XBOC #32-47 Interrupt Indication
0027	S/UNI-MACH48 RBOC #0-15 Interrupt Indication
0028	S/UNI-MACH48 RBOC #16-31 Interrupt Indication
0029	S/UNI-MACH48 RBOC #32-47 Interrupt Indication
002A	S/UNI-MACH48 TDPR #0-15 Interrupt Indication
002B	S/UNI-MACH48 TDPR #16-31 Interrupt Indication
002C	S/UNI-MACH48 TDPR #32-47 Interrupt Indication
002D	S/UNI-MACH48 RDLC #0-15 Interrupt Indication
002E	S/UNI-MACH48 RDLC #16-31 Interrupt Indication
002F	S/UNI-MACH48 RDLC #32-47 Interrupt Indication
0030	S/UNI-MACH48 DS3FRMR #0-15 Interrupt Indication
0031	S/UNI-MACH48 DS3FRMR #16-31 Interrupt Indication
0032	S/UNI-MACH48 DS3FRMR #32-47 Interrupt Indication
0033	S/UNI-MACH48 DS3 LOF #0-15 Interrupt Indication
0034	S/UNI-MACH48 DS3 LOF #16-31 Interrupt Indication
0035	S/UNI-MACH48 DS3 LOF #32-47 Interrupt Indication
0036	S/UNI-MACH48 PLCP PMON #0-15 Interrupt Indication
0037	S/UNI-MACH48 PLCP PMON #16-31 Interrupt Indication
0038	S/UNI-MACH48 PLCP PMON #32-47 Interrupt Indication
0039	S/UNI-MACH48 PRBS Interrupt Indication
003A	S/UNI-MACH48 8B/10B, CSU and DLL Interrupt Indication
003B	S/UNI-MACH48 DS3 #0-15 LOF Status
003C	S/UNI-MACH48 DS3 #16-31 LOF Status
003D	S/UNI-MACH48 DS3 #32-47 LOF Status
003E	S/UNI-MACH48 Device ID #1
003F	S/UNI-MACH48 Device ID #2
0040	RXPHY Configuration
0041	RXPHY Interrupt Status
0042	RXPHY Interrupt Enable
0043	RXPHY Indirect Burst Size
0044	RXPHY Calendar Length
0045	RXPHY Calendar Indirect Address Data
0046	RXPHY Data Type Field
0047	Reserved
0048	TXPHY Configuration
0049	TXPHY Interrupt Status
004A	TXPHY Interrupt Enable
004B	TXPHY Data Type Field

Address	Register Description
004C-004F	Reserved
0050	RXSDQ FIFO Reset
0051	RXSDQ FIFO Interrupt Enable
0052	RXSDQ Reserved
0053	RXSDQ FIFO Overflow Port and Interrupt Indication
0054	RXSDQ FIFO EOP Error Port and Interrupt Indication
0055	RXSDQ FIFO SOP Error Port and Interrupt Indication
0056-0057	RXSDQ Reserved
0058	RXSDQ FIFO Indirect Address
0059	RXSDQ FIFO Indirect Configuration
005A	RXSDQ FIFO Indirect Data Available Threshold
005B	RXSDQ FIFO Indirect Cells and Packets Count
005C	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
005D	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
005E	RXSDQ FIFO Cells and Packets Dropped Aggregate Count
005F	RXSDQ Reserved
0060	TXSDQ FIFO Reset
0061	TXSDQ FIFO Interrupt Enable
0062	TXSDQ Reserved
0063	TXSDQ FIFO Overflow Port and Interrupt Indication
0064	TXSDQ FIFO EOP Error Port and Interrupt Indication
0065	TXSDQ FIFO SOP Error Port and Interrupt Indication
0066-0067	TXSDQ Reserved
0068	TXSDQ FIFO Indirect Address
0069	TXSDQ FIFO Indirect Configuration
006A	TXSDQ FIFO Indirect Data and Buffer Available Thresholds
006B	TXSDQ FIFO Indirect Cells and Packets Count
006C	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
006D	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
006E	TXSDQ FIFO Cells and Packets Dropped Aggregate count
006F	TXSDQ Reserved
RCFP BASE offset = 0070H, 0080H, 0090H, and 00A0H	
00	RCFP Configuration
01	RCFP Interrupt Enable
02	RCFP Interrupt Indication and Status
03	RCFP Minimum Packet Length
04	RCFP Maximum Packet Length
05	RCFP LCD Count Threshold
06	RCFP Idle Cell Header and Mask

Address	Register Description
07	RCFP Receive Byte/Idle Cell Counter (LSB)
08	RCFP Receive Byte/Idle Cell Counter
09	RCFP Receive Byte/Idle Cell Counter (MSB)
0A	RCFP Packet/Cell Counter (LSB)
0B	RCFP Receive Packet/ATM Cell Counter (MSB)
0C	RCFP Receive Erred FCS/HCS Counter
0D	RCFP Receive Aborted Packet Counter
0E	RCFP Receive Minimum Length Packet Error
0F	RCFP Receive Maximum Length Packet Error Counter
TCFP BASE offset = 00B0H, 00C0H, 00D0H, and 00E0H	
00	TCFP Configuration
01	TCFP Interrupt Indication
02	TCFP Idle/Unassigned ATM Cell Header
03	TCFP Diagnostics
04	TCFP Transmit Cell/Packet Counter (LSB)
05	TCFP Transmit Cell/Packet Counter (MSB)
06	TCFP Transmit Byte Counter (LSB)
07	TCFP Transmit Byte Counter
08	TCFP Transmit Byte Counter (MSB)
09	TCFP Aborted Packet Counter
0A-0F	Reserved
RTDP BASE offset = 00F0H, 0110H, 0130H, and 0150H	
00	RTDP Indirect Channel Select
01	RTDP Indirect Configuration
02	RTDP Indirect Minimum Packet Length and Bit Order
03	RTDP Indirect Maximum Packet Length
04	RTDP Indirect LCD Count Threshold
05	RTDP Indirect Idle Cell Header and Mask
06	RTDP Indirect Receive Byte/Idle Cell Counter (LSB)
07	RTDP Indirect Receive Byte/Idle Cell Counter (MSB)
08	RTDP Indirect Packet/Cell Counter (LSB)
09	RTDP Indirect Receive Packet/ATM Cell Counter (MSB)
0A	RTDP Indirect Receive Erred FCS/HCS Counter
0B	RTDP Indirect Receive Aborted Packet Counter
0C	RTDP Indirect Receive Minimum Length Packet Error Counter
0D	RTDP Indirect Receive Maximum Length Packet Error Counter
0E-0F	RTDP Reserved
10	RTDP Interrupt Enable Channels 0 and 1
11	RTDP Interrupt Enable Channels 2 and 3

Address	Register Description
12	RTDP Interrupt Enable Channels 4 and 5
13	RTDP Interrupt Enable Channels 6 and 7
14	RTDP Interrupt Enable Channels 8 and 9
15	RTDP Interrupt Enable Channels 10 and 11
16	RTDP Interrupt Indication Channels 0 and 1
17	RTDP Interrupt Indication Channels 2 and 3
18	RTDP Interrupt Indication Channels 4 and 5
19	RTDP Interrupt Indication Channels 6 and 7
1A	RTDP Interrupt Indication Channels 8 and 9
1B	RTDP Interrupt Indication Channels 10 and 11
1C	RTDP OOF Status
1D	RTDP LOF Status
1E-1F	RTDP Reserved
TTDP BASE offset = 0170H, 0180H, 0190H, and 01A0H	
00	TTDP Indirect Channel Select
01	TTDP Indirect Configuration
02	TTDP Indirect Idle/Unassigned ATM Cell Header
03	TTDP Indirect Diagnostics
04	TTDP Indirect Transmit Cell/Packet Counter (LSB)
05	TTDP Indirect Transmit Cell/Packet Counter (MSB)
06	TTDP Indirect Transmit Byte Counter (LSB)
07	TTDP Indirect Transmit Byte Counter (MSB)
08	TTDP Indirect Aborted Packet Counter
09	TTDP CRC Error Mask
0A	TTDP Interrupt Enable 1
0B	TTDP Interrupt Enable 2
0C	TTDP Interrupt 1
0D	TTDP Interrupt 2
0E	TTDP Transmit Off
0F	Reserved
RCAS12 BASE offset = 01B0H, 01C0H, 01D0H, and 01E0H	
00	RCAS12 Channel Disable
01	RCAS12 Channel Loopback Enable
02	RCAS12 Timeslot 0 Configuration
03	RCAS12 Timeslot 1 Configuration
04	RCAS12 Timeslot 2 Configuration
05	RCAS12 Timeslot 3 Configuration
06	RCAS12 Timeslot 4 Configuration
07	RCAS12 Timeslot 5 Configuration

Address	Register Description
08	RCAS12 Timeslot 6 Configuration
09	RCAS12 Timeslot 7 Configuration
0A	RCAS12 Timeslot 8 Configuration
0B	RCAS12 Timeslot 9 Configuration
0C	RCAS12 Timeslot 10 Configuration
0D	RCAS12 Timeslot 11 Configuration
0E-0F	Reserved
TCAS12 BASE offset = 01F0H, 0200H, 0210H, and 0220H	
00	TCAS12 Channel Configuration
01	TCAS12 OALARM Configuration
02	TCAS12 Timeslot 0 Configuration
03	TCAS12 Timeslot 1 Configuration
04	TCAS12 Timeslot 2 Configuration
05	TCAS12 Timeslot 3 Configuration
06	TCAS12 Timeslot 4 Configuration
07	TCAS12 Timeslot 5 Configuration
08	TCAS12 Timeslot 6 Configuration
09	TCAS12 Timeslot 7 Configuration
0A	TCAS12 Timeslot 8 Configuration
0B	TCAS12 Timeslot 9 Configuration
0C	TCAS12 Timeslot 10 Configuration
0D	TCAS12 Timeslot 11 Configuration
0E	TCAS12 Idle Timeslot Fill Data
0E-0F	Reserved
DS3 BASE offset = 0230H + N*60H (N = 0 to 2FH)	
00	SPLR Configuration
01	SPLR Interrupt Enable
02	SPLR Interrupt Status
03	SPLR Status
04	SPLT Configuration
05	SPLT Control
06	SPLT Diagnostics and G1 Octet
07	SPLT F1 Octet
08	DS3 FRMR Configuration
09	DS3 FRMR Interrupt Enable (ACE=0)
09	DS3 FRMR Additional Configuration Register (ACE=1)
0A	DS3 FRMR Interrupt Status
0B	DS3 FRMR Status
0C	DS3 TRAN Configuration

Address	Register Description
0D	DS3 TRAN Diagnostic
0E	Reserved
0F	Reserved
10	RDLC Configuration
11	RDLC Interrupt Control
12	RDLC Status
13	RDLC Data
14	RDLC Primary Address Match
15	RDLC Secondary Address Match
16	Reserved
17	Reserved
18	TDPR Configuration
19	TDPR Upper Transmit Threshold
1A	TDPR Lower Interrupt Threshold
1B	TDPR Interrupt Enable
1C	TDPR Interrupt Status/UDR Clear
1D	TDPR Transmit Data
1E	Reserved
1F	Reserved
20	RBOC Configuration/Interrupt Enable
21	RBOC Interrupt Status
22	Reserved
23	Reserved
24	XBOC Control
25	XBOC Bit Oriented Code
26-30	Reserved
31	DS3 PMON Interrupt Enable/Status
32	Reserved
33	Reserved
34	Reserved
35	Reserved
36	DS3 PMON Framing Bit Error Event Count (LSB)
37	DS3 PMON Framing Bit Error Event Count (MSB)
38	Reserved
39	Reserved
3A	DS3 PMON Parity Error Event Count LSB
3B	DS3 PMON Parity Error Event Count (MSB)
3C	DS3 PMON Path Parity Error Event Count LSB
3D	DS3 PMON Path Parity Error Event Count (MSB)

Address	Register Description
3E	DS3 PMON FEBE Event Count (LSB)
3F	DS3 PMON FEBE Event Count (MSB
40	Reserved
41	PLCP PMON Interrupt Enable/Status
42	Reserved
43	Reserved
44	Reserved
45	Reserved
46	Reserved
47	Reserved
48	PLCP PMON FEBE Count (LSB)
49	PLCP PMON FEBE Count (MSB)
4A	PLCP PMON B1 Error Count LSB
4B	PLCP PMON B1 Error Count (MSB)
4C	PLCP PMON Framing Error Event Count LSB
4D	PLCP PMON Framing Error Event Count (MSB)
4E	Reserved
4F	Reserved
50	D3MD Configuration
51	D3MD Interrupt Status
52	D3MD Interrupt Enable
53	Reserved
54	D3MA Configuration
55	D3MA Interrupt Status
56	D3MA Interrupt Enable
57-5F	Reserved
. . .	. . .
1430-14BF	Reserved
SIRP BASE offset = 14C0H, 14D0H, 14E0H,14F0H	
00	SIRP Timeslot 0 Configuration
01	SIRP Timeslot 1 Configuration
02	SIRP Timeslot 2 Configuration
03	SIRP Timeslot 3 Configuration
04	SIRP Timeslot 4 Configuration
05	SIRP Timeslot 5 Configuration
06	SIRP Timeslot 6 Configuration
07	SIRP Timeslot 7 Configuration

Address	Register Description	
08	SIRP Timeslot 8 Configuration	
09	SIRP Timeslot 9 Configuration	
0A	SIRP Timeslot A Configuration	
0B	SIRP Timeslot B Configuration	
0C	SIRP LCD RDI Value Register	
0D-0F	SIRP Reserved	
. . .	. . .	
1500	PRGD Control	
1501	PRGD Interrupt Enable/Status	
1502	PRGD Length	
1503	PRGD Tap	
1504	PRGD Error Insertion Register	
1505	PRGD Reserved	
1506	PRGD Reserved	
1507	PRGD Reserved	
1508	PRGD Pattern Insertion #1	
1509	PRGD Pattern Insertion #2	
150A	PRGD Pattern Insertion #3	
150B	PRGD Pattern Insertion #4	
150C	PRGD Pattern Detector #1	
150D	PRGD Pattern Detector #2	
150E	PRGD Pattern Detector #3	
150F	PRGD Pattern Detector #4	
PRGM BASE offset = 1510H, 1520H, 1530H,1540H, 1550H, 1560H, 1570H, and 1580H		
00	PRGM Indirect Address	
01	PRGM Indirect Data	
	PRGM Indirect Register 0	Monitor Timeslot Configuration Page
	PRGM Indirect Register 1	Monitor PRBS[22:7] Accumulator Page
	PRGM Indirect Register 2	Monitor PRBS[6:0] Accumulator Page
	PRGM Indirect Register 3	Monitor B1/E1 Value Page
	PRGM Indirect Register 4	Monitor Error Count Page
	PRGM Indirect Register 5	Monitor Received B1/E1 Bytes Page
	PRGM Indirect Register 8	Generator Timeslot Configuration Page
	PRGM Indirect Register 9	Generator PRBS[22:7] Accumulator Page
	PRGM Indirect Register A	Generator PRBS[6:0] Accumulator Page
	PRGM Indirect Register B	Generator B1/E1 Value Page
02	PRGM Generator Payload Configuration	

Address	Register Description	
03	PRGM Monitor Payload Configuration	
04	PRGM Monitor Byte Error Interrupt Status	
05	PRGM Monitor Byte Error Interrupt Enable	
06	PRGM Monitor B1/E1 Bytes Interrupt Status	
07	PRGM Monitor B1/E1 Bytes Interrupt Enable	
08	PRGM Reserved	
09	PRGM Monitor Synchronization Interrupt Status	
0A	PRGM Monitor Synchronization Interrupt Enable	
0B	PRGM Monitor Synchronization Status	
0C	PRGM Performance Counters Transfer Trigger	
0D-0F	PRGM Reserved	
RHPP Base offset = 1600H, 1680H, 1700H, 1780H		
00	RHPP Indirect Address	
01	RHPP Indirect Data	
	RHPP Indirect Register 0	Pointer Interpreter Configuration
	RHPP Indirect Register 1	Pointer Interpreter Configuration
	RHPP Indirect Register 2	Pointer Value and ERDI
	RHPP Indirect Register 3	Reserved
	RHPP Indirect Register 4	Reserved
	RHPP Indirect Register 5	Pointer Interpreter Status
	RHPP Indirect Register 6	Reserved
	RHPP Indirect Register 7	Path REI Error Counter
	RHPP Indirect Register 8	Reserved
	RHPP Indirect Register 9	Reserved
02	RHPP Payload Configuration	
03	RHPP Counters update	
04	RHPP Path Interrupt Status	
05	RHPP Pointer Concatenation processing Disable	
06-07	RHPP Reserved	
08	RHPP Pointer Interpreter Status STS-1/STM-0 #0	
09	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #0	
0A	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #0	
0B-0F	RHPP Reserved STS-1/STM-0 #0	
10	RHPP Pointer Interpreter Status STS-1/STM-0 #1	
11	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #1	
12	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #1	
13-17	RHPP Reserved STS-1/STM-0 #1	
18	RHPP Pointer Interpreter Status STS-1/STM-0 #2	

Address	Register Description
19	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #2
1A	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #2
1B-1F	RHPP Reserved STS-1/STM-0 #2
. . .	. . .
60	RHPP Pointer Interpreter Status STS-1/STM-0 #11
61	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #11
62	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #11
63-7F	RHPP Reserved
STSI BASE: **IWTI offset = 1800H** **IPTI offset = 1808H** **OWTI offset = 1810H** **OPTI offset = 1818H**	
00	STSI Indirect Address
01	STSI Indirect Data
02	STSI Configuration
03	STSI Interrupt Status
04-07	STSI Reserved
R8TD BASE offset = 1820H, 1828H, 1830H, 1838H, 1840H, 1848H, 1850H, 1858H	
00	R8TD Control and Status
01	R8TD Interrupt Status
02	R8TD Line Code Violation Count
03	R8TD Analog Control 1
04	R8TD Analog Control 2
05	R8TD Analog Control 3
06	R8TD Reserved
07	R8TD Reserved
T8TE BASE offset = 1860H, 1868H, 1870H, 1878H, 1880H, 1888H, 1890H, 1898H	
00	T8TE Control and Status
01	T8TE Interrupt Status
02	T8TE TelecomBus Mode #1
03	T8TE TelecomBus Mode #2
04	T8TE Test Pattern
05	T8TE Analog Control
06	T8TE DTB Bus
07	T8TE Reserved
18A0-18AB	DLL Reserved
18AC	CSTR Control

Address	Register Description
18AD	CSTR Interrupt Enable and CSU Lock Status
18AE	CSTR CSU Lock Interrupt Indication
18AF	CSTR Reserved
18B0-BF	Reserved
1900	S/UNI-MACH48 Channel #0 Dropped Cell/Packet Counter
1901	S/UNI-MACH48 Channel #1 Dropped Cell/Packet Counter
1902	S/UNI-MACH48 Channel #2 Dropped Cell/Packet Counter
1903	S/UNI-MACH48 Channel #3 Dropped Cell/Packet Counter
1904	S/UNI-MACH48 Channel #4 Dropped Cell/Packet Counter
1905	S/UNI-MACH48 Channel #5 Dropped Cell/Packet Counter
1906	S/UNI-MACH48 Channel #6 Dropped Cell/Packet Counter
1907	S/UNI-MACH48 Channel #7 Dropped Cell/Packet Counter
1908	S/UNI-MACH48 Channel #8 Dropped Cell/Packet Counter
1909	S/UNI-MACH48 Channel #9 Dropped Cell/Packet Counter
190A	S/UNI-MACH48 Channel #10 Dropped Cell/Packet Counter
190B	S/UNI-MACH48 Channel #11 Dropped Cell/Packet Counter
190C	S/UNI-MACH48 Channel #12 Dropped Cell/Packet Counter
190D	S/UNI-MACH48 Channel #13 Dropped Cell/Packet Counter
190E	S/UNI-MACH48 Channel #14 Dropped Cell/Packet Counter
190F	S/UNI-MACH48 Channel #15 Dropped Cell/Packet Counter
1910	S/UNI-MACH48 Channel #16 Dropped Cell/Packet Counter
1911	S/UNI-MACH48 Channel #17 Dropped Cell/Packet Counter
1912	S/UNI-MACH48 Channel #18 Dropped Cell/Packet Counter
1913	S/UNI-MACH48 Channel #19 Dropped Cell/Packet Counter
1914	S/UNI-MACH48 Channel #20 Dropped Cell/Packet Counter
1915	S/UNI-MACH48 Channel #21 Dropped Cell/Packet Counter
1916	S/UNI-MACH48 Channel #22 Dropped Cell/Packet Counter
1917	S/UNI-MACH48 Channel #23 Dropped Cell/Packet Counter
1918	S/UNI-MACH48 Channel #24 Dropped Cell/Packet Counter
1919	S/UNI-MACH48 Channel #25 Dropped Cell/Packet Counter
191A	S/UNI-MACH48 Channel #26 Dropped Cell/Packet Counter
191B	S/UNI-MACH48 Channel #27 Dropped Cell/Packet Counter
191C	S/UNI-MACH48 Channel #28 Dropped Cell/Packet Counter
191D	S/UNI-MACH48 Channel #29 Dropped Cell/Packet Counter
191E	S/UNI-MACH48 Channel #30 Dropped Cell/Packet Counter
191F	S/UNI-MACH48 Channel #31 Dropped Cell/Packet Counter
1920	S/UNI-MACH48 Channel #32 Dropped Cell/Packet Counter
1921	S/UNI-MACH48 Channel #33 Dropped Cell/Packet Counter
1922	S/UNI-MACH48 Channel #34 Dropped Cell/Packet Counter

Address	Register Description
1923	S/UNI-MACH48 Channel #35 Dropped Cell/Packet Counter
1924	S/UNI-MACH48 Channel #36 Dropped Cell/Packet Counter
1925	S/UNI-MACH48 Channel #37 Dropped Cell/Packet Counter
1926	S/UNI-MACH48 Channel #38 Dropped Cell/Packet Counter
1927	S/UNI-MACH48 Channel #39 Dropped Cell/Packet Counter
1928	S/UNI-MACH48 Channel #40 Dropped Cell/Packet Counter
1929	S/UNI-MACH48 Channel #41 Dropped Cell/Packet Counter
192A	S/UNI-MACH48 Channel #42 Dropped Cell/Packet Counter
192B	S/UNI-MACH48 Channel #43 Dropped Cell/Packet Counter
192C	S/UNI-MACH48 Channel #44 Dropped Cell/Packet Counter
192D	S/UNI-MACH48 Channel #45 Dropped Cell/Packet Counter
192E	S/UNI-MACH48 Channel #46 Dropped Cell/Packet Counter
192F	S/UNI-MACH48 Channel #47 Dropped Cell/Packet Counter
1930	S/UNI-MACH48 Drop Counter Interrupt Enable #1
1931	S/UNI-MACH48 Drop Counter Interrupt Enable #2
1932	S/UNI-MACH48 Drop Counter Interrupt Enable #3
1933	S/UNI-MACH48 Drop Counter Interrupt #1
1934	S/UNI-MACH48 Drop Counter Interrupt #2
1935	S/UNI-MACH48 Drop Counter Interrupt #3
1936-1FFF	Reserved
2000	S/UNI-MACH48 Master Test Register
2001	S/UNI-MACH48 Test Mode Address Force Enable
2002	S/UNI-MACH48 Test Mode Address Force Value
2003	S/UNI-MACH48 Analog Block Test
2004 – 3FFF	Reserved for Test

Notes on Register Memory Map:

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[13] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

12 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI-MACH48. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-MACH48 to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-MACH48 operation unless otherwise noted. Performance monitoring counter registers are a common exception.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-MACH48 operates as intended, reserved register bits must be written with their default value as indicated by the register bit description.

Register 0000H: S/UNI-MACH48 Global Performance Monitor Update

Bit	Type	Function	Default
Bit 15	R	TIP	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a global performance monitor update by simultaneously loading all the performance meter registers in the RXSDQ, TXSDQ, TTDP, TCFP, RTDP, RCFP, DS3 PMON, PLCP PMON, R8TD, T8TE, RHPP, PRGD, and PRGM blocks, and the Per-Channel Dropped Cell/Packet Counters.

TIP

The TIP bit is set to a logic one when the performance meter registers are being loaded. Writing to this register with DRESET equal to logic 0 initiates an accumulation interval transfer and loads all the performance meter registers in the S/UNI-MACH48.

TIP remains logic 1 while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Register 0001H: S/UNI-MACH48 Master Reset, Configuration, and Global Digital Loopback

Bit	Type	Function	Default
Bit 15	R/W	DRESET	0
Bit 14	R/W	ARESET	1
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	DS3LOFEN	0
Bit 10	R/W	INTDIS	0
Bit 9	R/W	PARDIS	0
Bit 8	R/W	SEREN	X
Bit 7	R/W	POSL3	X
Bit 6	R/W	RHPP_EN	1
Bit 5	R/W	DLINV	0
Bit 4	R/W	RWSEL_EN	1
Bit 3	R/W	RX48C	1
Bit 2	R/W	TX48C	1
Bit 1	R/W	DLOOP	0
Bit 0	R/W	LLOOP	0

This register allows the configuration of S/UNI-MACH48 features.

LLOOP

The LLOOP bit is used to enable line-loopback. When LLOOP is logic 1, line-loopback is enabled and IJ0J1[4:1], IDP[4:1], ID[4:1][7:0], IPL[4:1], and IPAIS[4:1] are directed to OJ0J1[4:1], ODP[4:1], OD[4:1][7:0], OPL[4:1], and OALARM[4:1] respectively. When LLOOP is logic 0, line-loopback is not enabled.

DLOOP

The DLOOP bit is used to enable parallel diagnostic-loopback. When DLOOP is logic 1, parallel diagnostic-loopback is enabled and OJ0J1[4:1], ODP[4:1], OD[4:1][7:0], OPL[4:1], and OALARM[4:1] replace IJ0J1[4:1], IDP[4:1], ID[4:1][7:0], IPL[4:1], and IPAIS[4:1] respectively. When DLOOP is logic 0, parallel diagnostic-loopback is not enabled. Note that when DLOOP is logic 1, parallel diagnostic loopback is enabled regardless of any other settings including SEREN or DLBEN in the R8TD.

TX48C

The TX48C bit is used to select STS-48c/STM-16c operation. When TX48C is logic 1, the transmit data stream is treated as a single STS-48c/STM-16c channel. When TX48C is logic 0, the transmit system side timeslots are configured using the TS***xy***[1:0] bits (where ***x*** = 0, 1, 2, ..16 and ***y*** = 1, 2, 3, or 4) in the S/UNI-MACH48 Transmit Timeslot Configuration Registers.

RX48C

The RX48C bit is used to selected STS-48c/STM-16c operation. When RX48C is logic 1, the receive data stream is treated as a single STS-48c/STM-16c channel. When RX48C is logic 0, the receive data stream timeslots are configured using the RS***xy***[1:0] bits (where ***x*** = 1, 2, ..16 and ***y*** = 1, 2, 3, or 4) in the S/UNI-MACH48 Receive Timeslot Configuration Registers.

RWSEL_EN

The RWSEL_EN bit is used to enable the RWSEL input pin. When RWSEL_EN is logic 1, the RWSEL input signal is used to globally select between the working RPWRK/RNWRK[4:1] and protection RPPROT/RNPROT[4:1] serial TelecomBus links. When RWSEL_EN is logic 0, the RWSEL input is ignored and selection between the working and protection serial TelecomBus links can be done on a per timeslot basis using the SER_PRT_SEL register bit in the IWTI block. **If both the SEREN bit and the SEREN pin are logic 0 (Parallel TelecomBus Mode), then RWSEL_EN must be logic 0 for proper operation**.

DLINV

The DLINV bit provides polarity control for the DS3 C-bit Parity path maintenance data link which is located in the 3 C-bits of M-subframe 5. When a logic 1 is written to DLINV, the path maintenance data link is inverted before being processed. The rationale behind this bit is as follows: currently ANSI standard T1.107 specifies that the C-bits (which carry the path maintenance data link) be set to all zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all ones) should be transmitted. By inverting the data link, the all zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully. Although this inversion is currently not specified in ANSI T1.107a, this bit is provided to safe-guard the S/UNI-MACH48 in case the inversion is required in the future.

HPP_EN

The high-order path processor enable (RHPP_EN) bit is used to select whether or not the J1 indications are given on the incoming parallel or serial TelecomBus interfaces or if the RHPP block must be used to find them. When RHPP_EN is logic 1, then the RHPP block will extract the SONET/SDH pointers and track positive and negative justifications. If RHPP_EN is logic 0, then, then the J1 indications must be given on the TelecomBus interface.

POSL3

The POS-PHY Level 3 Select bit (POSL3) is OR'ed with the POS/UL3B pin to select POS-PHY Level 3 mode on the system interface. When POSL3 or POS/UL3B are logic 1, the system bus operates in POS-PHY Level 3 mode. When both POSL3 and POS/UL3B are logic 0, the bus operates as a UTOPIA Level 3 bus. Reading this bit gives the mode of the bus, (ie, the OR of the pin and the bit). The default state of this register bit is logic 0.

SEREN

The Serial TelecomBus Enable bit (SEREN) is OR'ed with the SEREN pin to enable the Serial TelecomBus interface. When the SEREN bit or the SEREN pin are logic 1, the Serial TelecomBus is selected, and the Parallel TelecomBus is ignored. When both the SEREN bit and the SEREN pin are logic 0, the Parallel TelecomBus is selected, and the Serial TelecomBus is ignored. Reading this bit gives the mode of the TelecomBus interface, (ie, the OR of the pin and the bit). The default state of this register bit is logic 0. If parallel TelecomBus mode is selected (SEREN = 0) then RWSEL_EN must be logic 0 for proper operation.

PARDIS

The Parallel TelecomBus disable bit (PARDIS) holds the Parallel TelecomBus interface tristate (High Z) when logic 1.

INTDIS

The Interrupt disable bit (INTDIS) holds the interrupt pin INTB inactive (High Z) when logic 1. This bit does not clear any interrupt enables. It just blocks interrupts at the top level. Interrupt registers can still be polled and cleared normally.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

DS3LOFEN

When logic 1, the DS3 LOF Interrupt Enable (DS3LOFEN) bit allows a change in the LOF status of any enabled DS3 Receiver to cause a system interrupt. When DS3LOFEN is logic 0, the LOF status, and status change bits can still be polled by software, but they will not result in a system interrupt (INTB). The LOF Status bits are in registers: 3BH, 3CH, and 3DH and the LOF STatus change bits are in registers: 33H, 34H, 35H.

ARESET

The ARESET bit allows the analog circuitry in the S/UNI-MACH48 to be reset under software control. If the ARESET bit is a logic one, all the S/UNI-MACH48 analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-MACH48 out of reset. Holding the S/UNI-MACH48 in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET bit, thus negating the analog software reset.

DRESET

The DRESET bit allows the digital circuitry in the S/UNI-MACH48 to be reset under software control. If the DRESET bit is a logic one, all the S/UNI-MACH48 digital circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-MACH48 out of reset. Holding the S/UNI-MACH48 in a reset state places it into a low power, digital stand-by mode. A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register 0002H: S/UNI-MACH48 Receive Timeslot Configuration #1

Bit	Type	Function	Default
Bit 15	R/W	RS4_2[1]	0
Bit 14	R/W	RS4_2[0]	0
Bit 13	R/W	RS3_2[1]	0
Bit 12	R/W	RS3_2[0]	0
Bit 11	R/W	RS2_2[1]	0
Bit 10	R/W	RS2_2[0]	0
Bit 9	R/W	RS1_2[1]	0
Bit 8	R/W	RS1_2[0]	0
Bit 7	R/W	RS4_1[1]	0
Bit 6	R/W	RS4_1[0]	0
Bit 5	R/W	RS3_1[1]	0
Bit 4	R/W	RS3_1[0]	0
Bit 3	R/W	RS2_1[1]	0
Bit 2	R/W	RS2_1[0]	0
Bit 1	R/W	RS1_1[1]	0
Bit 0	R/W	RS1_1[0]	0

This register configures the receive system-side timeslots Sx,y (see Table 52) for DS3, STS-1/STM-0, STS-3c/STM-1, or STS-12c/STM-4c rates. This register is ignored for STS-48c/STM-16c rates. The system-side timeslots are after the ingress time-slot interchange function.

RS***x_y***[1:0]

The RS***x_y***[1:0] bits configure the receive system-side timeslot S***x,y*** to the desired rate as shown Table 6.

Table 6 Receive Timeslot Configuration for Different Traffic Types

RS*x,y*[1:0]	Configuration
00	STS-12c/STM-4c
01	STS-3c/STM-1
10	STS-1/STM-0
11	DS3

The RS***x,y***[1:0] bits are only valid when RX48C is logic 0. The receive timeslot positions are as shown in Table 52. **The timeslot positions referenced here are post IWTI and post IPTI**. That is, they are the positions after the ingress data has passed through the TimeSlot Interchange function in the IWTI or IPTI. The definitions for S***x,y*** can be found in Section 14.9.2.

The valid combinations for different timeslot mappings are given in Table 7.

Table 7 Valid Receive Timeslot Mappings

Rate	Valid Mappings
STS-48c	All S***x,y***
STS-12c	(S1,1 S2,1 S3,1 S4,1 S1,2 S2,2 S3,2 S4,2 S1,3 S2,3 S3,3 and S4,3) (S5,1 S6,1 S7,1 S8,1 S5,2 S6,2 S7,2 S8,2 S5,3 S6,3 S7,3 and S8,3) (S9,1 S10,1 S11,1 S12,1 S9,2 S10,2 S11,2 S12,2 S9,3 S10,3 S11,3 and S12,3) (S13,1 S14,1 S15,1 S16,1 S13,2 S14,2 S15,2 S16,2 S13,3 S14,3 S15,3 and S16,3)
STS-3c	S1,1 S1,2 S1,3 S2,1 S2,2 S2,3 S3,1 S3,2 S3,3 S4,1 S4,2 S4,3 S5,1 S5,2 S5,3 S6,1 S6,2 S6,3 S7,1 S7,2 S7,3 S8,1 S8,2 S8,3 S9,1 S9,2 S9,3 S10,1 S10,2 S10,3 S11,1 S11,2 S11,3 S12,1 S12,2 S12,3 S13,1 S13,2 S13,3 S14,1 S14,2 S14,3 S15,1 S15,2 S15,3 S16,1 S16,2 S16,3
STS-1	Any S***x,y*** unoccupied by an STS-12c or an STS-3c
DS3	Any ***Sx,y*** unoccupied by an STS-12c, STS-3c, or STS-1

Register 0003H: S/UNI-MACH48 Receive Timeslot Configuration #2

Bit	Type	Function	Default
Bit 15	R/W	RS8_1[1]	0
Bit 14	R/W	RS8_1[0]	0
Bit 13	R/W	RS7_1[1]	0
Bit 12	R/W	RS7_1[0]	0
Bit 11	R/W	RS6_1[1]	0
Bit 10	R/W	RS6_1[0]	0
Bit 9	R/W	RS5_1[1]	0
Bit 8	R/W	RS5_1[0]	0
Bit 7	R/W	RS4_3[1]	0
Bit 6	R/W	RS4_3[0]	0
Bit 5	R/W	RS3_3[1]	0
Bit 4	R/W	RS3_3[0]	0
Bit 3	R/W	RS2_3[1]	0
Bit 2	R/W	RS2_3[0]	0
Bit 1	R/W	RS1_3[1]	0
Bit 0	R/W	RS1_3[0]	0

Register 0004H: S/UNI-MACH48 Receive Timeslot Configuration #3

Bit	Type	Function	Default
Bit 15	R/W	RS8_3[1]	0
Bit 14	R/W	RS8_3[0]	0
Bit 13	R/W	RS7_3[1]	0
Bit 12	R/W	RS7_3[0]	0
Bit 11	R/W	RS6_3[1]	0
Bit 10	R/W	RS6_3[0]	0
Bit 9	R/W	RS5_3[1]	0
Bit 8	R/W	RS5_3[0]	0
Bit 7	R/W	RS8_2[1]	0
Bit 6	R/W	RS8_2[0]	0
Bit 5	R/W	RS7_2[1]	0
Bit 4	R/W	RS7_2[0]	0
Bit 3	R/W	RS6_2[1]	0
Bit 2	R/W	RS6_2[0]	0
Bit 1	R/W	RS5_2[1]	0
Bit 0	R/W	RS5_2[0]	0

Register 0005H: S/UNI-MACH48 Receive Timeslot Configuration #4

Bit	Type	Function	Default
Bit 15	R/W	RS12_2[1]	0
Bit 14	R/W	RS12_2[0]	0
Bit 13	R/W	RS11_2[1]	0
Bit 12	R/W	RS11_2[0]	0
Bit 11	R/W	RS10_2[1]	0
Bit 10	R/W	RS10_2[0]	0
Bit 9	R/W	RS9_2[1]	0
Bit 8	R/W	RS9_2[0]	0
Bit 7	R/W	RS12_1[1]	0
Bit 6	R/W	RS12_1[0]	0
Bit 5	R/W	RS11_1[1]	0
Bit 4	R/W	RS11_1[0]	0
Bit 3	R/W	RS10_1[1]	0
Bit 2	R/W	RS10_1[0]	0
Bit 1	R/W	RS9_1[1]	0
Bit 0	R/W	RS9_1[0]	0

Register 0006H: S/UNI-MACH48 Receive Timeslot Configuration #5

Bit	Type	Function	Default
Bit 15	R/W	RS16_1[1]	0
Bit 14	R/W	RS16_1[0]	0
Bit 13	R/W	RS15_1[1]	0
Bit 12	R/W	RS15_1[0]	0
Bit 11	R/W	RS14_1[1]	0
Bit 10	R/W	RS14_1[0]	0
Bit 9	R/W	RS13_1[1]	0
Bit 8	R/W	RS13_1[0]	0
Bit 7	R/W	RS12_3[1]	0
Bit 6	R/W	RS12_3[0]	0
Bit 5	R/W	RS11_3[1]	0
Bit 4	R/W	RS11_3[0]	0
Bit 3	R/W	RS10_3[1]	0
Bit 2	R/W	RS10_3[0]	0
Bit 1	R/W	RS9_3[1]	0
Bit 0	R/W	RS9_3[0]	0

Register 0007H: S/UNI-MACH48 Receive Timeslot Configuration #6

Bit	Type	Function	Default
Bit 15	R/W	RS16_3[1]	0
Bit 14	R/W	RS16_3[0]	0
Bit 13	R/W	RS15_3[1]	0
Bit 12	R/W	RS15_3[0]	0
Bit 11	R/W	RS14_3[1]	0
Bit 10	R/W	RS14_3[0]	0
Bit 9	R/W	RS13_3[1]	0
Bit 8	R/W	RS13_3[0]	0
Bit 7	R/W	RS16_2[1]	0
Bit 6	R/W	RS16_2[0]	0
Bit 5	R/W	RS15_2[1]	0
Bit 4	R/W	RS15_2[0]	0
Bit 3	R/W	RS14_2[1]	0
Bit 2	R/W	RS14_2[0]	0
Bit 1	R/W	RS13_2[1]	0
Bit 0	R/W	RS13_2[0]	0

These registers configure the receive system-side timeslots Sx,y (see Table 52) for DS3, STS-1/STM-0, STS-3c/STM-1, or STS-12c/STM-4c rates. This register is ignored for STS-48c/STM-16c rates. The system-side timeslots are after the ingress time-slot interchange function.

RS***x_y***[1:0]

The RS***x_y***[1:0] bits configure the receive system-side timeslot S***x,y*** to the desired rate as shown in Table 6.

The RS***x,y***[1:0] bits are only valid when RX48C is logic 0. The receive timeslot positions are as shown in Table 52. **The timeslot positions referenced here are post IWTI and post IPTI**. That is, they are the positions after the ingress data has passed through the TimeSlot Interchange function in the IWTI or IPTI. The definitions for S***x,y*** can be found in Section 14.9.2.

The valid combinations for different timeslot mappings are given in Table 7.

Register 0008H: S/UNI-MACH48 Transmit Timeslot Configuration #1

Bit	Type	Function	Default
Bit 15	R/W	TS4_2[1]	0
Bit 14	R/W	TS4_2[0]	0
Bit 13	R/W	TS3_2[1]	0
Bit 12	R/W	TS3_2[0]	0
Bit 11	R/W	TS2_2[1]	0
Bit 10	R/W	TS2_2[0]	0
Bit 9	R/W	TS1_2[1]	0
Bit 8	R/W	TS1_2[0]	0
Bit 7	R/W	TS4_1[1]	0
Bit 6	R/W	TS4_1[0]	0
Bit 5	R/W	TS3_1[1]	0
Bit 4	R/W	TS3_1[0]	0
Bit 3	R/W	TS2_1[1]	0
Bit 2	R/W	TS2_1[0]	0
Bit 1	R/W	TS1_1[1]	0
Bit 0	R/W	TS1_1[0]	0

This register configures the receive system-side timeslots Sx,y (see Table 52) for DS3, STS-1/STM-0, STS-3c/STM-1, or STS-12c/STM-4c rates. This register is ignored for STS-48c/STM-16c rates. The system-side timeslots are before the egress time-slot interchange function.

TS***x_y***[1:0]

The TS***x_y***[1:0] bits configure the transmit system-side timeslot S***x,y*** to the desired rate as shown Table 8.

Table 8 Transmit Timeslot Configuration for Different Traffic Types

TS*x,y*[1:0]	Configuration
00	STS-12c/STM-4c
01	STS-3c/STM-1
10	STS-1/STM-0
11	DS3

The TS***x,y***[1:0] bits are only valid when TX48C is logic 0. The transmit timeslot positions are as shown in Table 52. **The timeslot positions referenced here are pre OWTI and pre OPTI**. That is, they are the positions before the egress data has passed through the TimeSlot Interchange function in the OWTI or OPTI. The definitions for S***x,y*** can be found in Section 14.9.2.

The valid combinations for different timeslot mappings are given in Table 9.

Table 9 Valid Transmit Timeslot Mappings

Rate	Valid Mappings
STS-48c	All S***x,y***
STS-12c	(S1,1 S2,1 S3,1 S4,1 S1,2 S2,2 S3,2 S4,2 S1,3 S2,3 S3,3 and S4,3) (S5,1 S6,1 S7,1 S8,1 S5,2 S6,2 S7,2 S8,2 S5,3 S6,3 S7,3 and S8,3) (S9,1 S10,1 S11,1 S12,1 S9,2 S10,2 S11,2 S12,2 S9,3 S10,3 S11,3 and S12,3) (S13,1 S14,1 S15,1 S16,1 S13,2 S14,2 S15,2 S16,2 S13,3 S14,3 S15,3 and S16,3)
STS-3c	S1,1 S1,2 S1,3 S2,1 S2,2 S2,3 S3,1 S3,2 S3,3 S4,1 S4,2 S4,3 S5,1 S5,2 S5,3 S6,1 S6,2 S6,3 S7,1 S7,2 S7,3 S8,1 S8,2 S8,3 S9,1 S9,2 S9,3 S10,1 S10,2 S10,3 S11,1 S11,2 S11,3 S12,1 S12,2 S12,3 S13,1 S13,2 S13,3 S14,1 S14,2 S14,3 S15,1 S15,2 S15,3 S16,1 S16,2 S16,3
STS-1	Any S***x,y*** unoccupied by an STS-12c or an STS-3c
DS3	Any ***Sx,y*** unoccupied by an STS-12c, STS-3c, or STS-1

Register 0009H: S/UNI-MACH48 Transmit Timeslot Configuration #2

Bit	Type	Function	Default
Bit 15	R/W	TS8_1[1]	0
Bit 14	R/W	TS8_1[0]	0
Bit 13	R/W	TS7_1[1]	0
Bit 12	R/W	TS7_1[0]	0
Bit 11	R/W	TS6_1[1]	0
Bit 10	R/W	TS6_1[0]	0
Bit 9	R/W	TS5_1[1]	0
Bit 8	R/W	TS5_1[0]	0
Bit 7	R/W	TS4_3[1]	0
Bit 6	R/W	TS4_3[0]	0
Bit 5	R/W	TS3_3[1]	0
Bit 4	R/W	TS3_3[0]	0
Bit 3	R/W	TS2_3[1]	0
Bit 2	R/W	TS2_3[0]	0
Bit 1	R/W	TS1_3[1]	0
Bit 0	R/W	TS1_3[0]	0

Register 000AH: S/UNI-MACH48 Receive Timeslot Configuration #3

Bit	Type	Function	Default
Bit 15	R/W	TS8_3[1]	0
Bit 14	R/W	TS8_3[0]	0
Bit 13	R/W	TS7_3[1]	0
Bit 12	R/W	TS7_3[0]	0
Bit 11	R/W	TS6_3[1]	0
Bit 10	R/W	TS6_3[0]	0
Bit 9	R/W	TS5_3[1]	0
Bit 8	R/W	TS5_3[0]	0
Bit 7	R/W	TS8_2[1]	0
Bit 6	R/W	TS8_2[0]	0
Bit 5	R/W	TS7_2[1]	0
Bit 4	R/W	TS7_2[0]	0
Bit 3	R/W	TS6_2[1]	0
Bit 2	R/W	TS6_2[0]	0
Bit 1	R/W	TS5_2[1]	0
Bit 0	R/W	TS5_2[0]	0

Register 000BH: S/UNI-MACH48 Transmit Timeslot Configuration #4

Bit	Type	Function	Default
Bit 15	R/W	TS12_2[1]	0
Bit 14	R/W	TS12_2[0]	0
Bit 13	R/W	TS11_2[1]	0
Bit 12	R/W	TS11_2[0]	0
Bit 11	R/W	TS10_2[1]	0
Bit 10	R/W	TS10_2[0]	0
Bit 9	R/W	TS9_2[1]	0
Bit 8	R/W	TS9_2[0]	0
Bit 7	R/W	TS12_1[1]	0
Bit 6	R/W	TS12_1[0]	0
Bit 5	R/W	TS11_1[1]	0
Bit 4	R/W	TS11_1[0]	0
Bit 3	R/W	TS10_1[1]	0
Bit 2	R/W	TS10_1[0]	0
Bit 1	R/W	TS9_1[1]	0
Bit 0	R/W	TS9_1[0]	0

Register 000CH: S/UNI-MACH48 Transmit Timeslot Configuration #5

Bit	Type	Function	Default
Bit 15	R/W	TS16_1[1]	0
Bit 14	R/W	TS16_1[0]	0
Bit 13	R/W	TS15_1[1]	0
Bit 12	R/W	TS15_1[0]	0
Bit 11	R/W	TS14_1[1]	0
Bit 10	R/W	TS14_1[0]	0
Bit 9	R/W	TS13_1[1]	0
Bit 8	R/W	TS13_1[0]	0
Bit 7	R/W	TS12_3[1]	0
Bit 6	R/W	TS12_3[0]	0
Bit 5	R/W	TS11_3[1]	0
Bit 4	R/W	TS11_3[0]	0
Bit 3	R/W	TS10_3[1]	0
Bit 2	R/W	TS10_3[0]	0
Bit 1	R/W	TS9_3[1]	0
Bit 0	R/W	TS9_3[0]	0

Register 000DH: S/UNI-MACH48 Receive Timeslot Configuration #6

Bit	Type	Function	Default
Bit 15	R/W	TS16_3[1]	0
Bit 14	R/W	TS16_3[0]	0
Bit 13	R/W	TS15_3[1]	0
Bit 12	R/W	TS15_3[0]	0
Bit 11	R/W	TS14_3[1]	0
Bit 10	R/W	TS14_3[0]	0
Bit 9	R/W	TS13_3[1]	0
Bit 8	R/W	TS13_3[0]	0
Bit 7	R/W	TS16_2[1]	0
Bit 6	R/W	TS16_2[0]	0
Bit 5	R/W	TS15_2[1]	0
Bit 4	R/W	TS15_2[0]	0
Bit 3	R/W	TS14_2[1]	0
Bit 2	R/W	TS14_2[0]	0
Bit 1	R/W	TS13_2[1]	0
Bit 0	R/W	TS13_2[0]	0

These registers configure the transmit system-side timeslots Sx,y (see Table 52) for DS3, STS-1/STM-0, STS-3c/STM-1, or STS-12c/STM-4c rates. This register is ignored for STS-48c/STM-16c rates. The system-side timeslots are before the egress time-slot interchange function.

TS***x_y***[1:0]

The TS***x_y***[1:0] bits configure the transmit system-side timeslot S***x,y*** to the desired rate as shown in Table 8.

The TS***x,y***[1:0] bits are only valid when RX48C is logic 0. The receive timeslot positions are as shown in Table 52. **The timeslot positions referenced here are pre PWTI and pre OPTI**. That is, they are the positions before the egress data has passed through the TimeSlot Interchange function in the OWTI or OPTI. The definitions for S***x,y*** can be found in Section 14.9.2.

The valid combinations for different timeslot mappings are given in Table 9.

Register 000EH: S/UNI-MACH48 DS3 PRBS Assignment

Bit	Type	Function	Default
Bit 15	R/W	TPRGD_EN	0
Bit 14		Unused	X
Bit 13	R/W	TPRGDTS[5]	0
Bit 12	R/W	TPRGDTS[4]	0
Bit 11	R/W	TPRGDTS[3]	0
Bit 10	R/W	TPRGDTS[2]	0
Bit 9	R/W	TPRGDTS[1]	0
Bit 8	R/W	TPRGDTS[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RPRGDTS[5]	0
Bit 4	R/W	RPRGDTS[4]	0
Bit 3	R/W	RPRGDTS[3]	0
Bit 2	R/W	RPRGDTS[2]	0
Bit 1	R/W	RPRGDTS[1]	0
Bit 0	R/W	RPRGDTS[0]	0

This register is used to assign the timeslot which the DS3 transmit and receive PRBS generator/detector has effect on.

RPRGDTS[5:0]

The RPRGDTS[5:0] bits contain the value of the timeslot which the PRGD block's DS3 PRBS detector is assigned to. For valid operation, the RS***x,y***[1:0] bits associated with timeslot S***x,y*** must be set to 'b11 (DS3). Table 52 shows the receive timeslot map.

TPRGDTS[5:0]

The TPRGDTS[5:0] bits contain the value of the timeslot which the PRGD block's DS3 PRBS transmitter is assigned to. For valid operation, the TS***x,y***[1:0] bits associated with timeslot S***x,y*** must be set to 'b11 (DS3). Table 52 shows the transmit timeslot map.

TPRGD_EN

The TPRGD_EN bit enables the insertion of PRBS data into the DS3 block selected by the TPRGDTS[5:0] bits. When TPRGD_EN is logic 1, the PRBS transmitter is enabled. When TPRGD_EN is logic 0, the PRBS transmitter is disabled, and DS3 data flows normally.

Register 000FH: S/UNI-MACH48 PLCP Reference and Clock Activity

Bit	Type	Function	Default
Bit 15	R/W	8KI_SEL[1]	0
Bit 14	R/W	8KI_SEL[0]	0
Bit 13	R/W	8KO_SEL[5]	0
Bit 12	R/W	8KO_SEL[4]	0
Bit 11	R/W	8KO_SEL[3]	0
Bit 10	R/W	8KO_SEL[2]	0
Bit 9	R/W	8KO_SEL[1]	0
Bit 8	R/W	8KO_SEL[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SYSCLKA	X
Bit 2	R	RFCLKA	X
Bit 1	R	TFCLKA	X
Bit 0	R	DS3TICLKA	X

This register is used to verify clock activity and select the 8kHz reference for the S/UNI-MACH48.

DS3TICLKA

The DS3TICLK active (DS3TICLKA) bit monitors for low to high transitions on the DS3TICLK clock input. DS3TICLKA is set to logic 1 on a rising edge of DS3TICLK, and is cleared to logic 0 when this register is read.

TFCLKA

The TFCLK active (TFCLKA) bit monitors for low to high transitions on the TFCLK clock input. TFCLKA is set to logic 1 on a rising edge of TFCLK, and is cleared to logic 0 when this register is read.

RFCLKA

The RFCLK active (RFCLKA) bit monitors for low to high transitions on the RFCLK clock input. RFCLKA is set to logic 1 on a rising edge of RFCLK, and is cleared to logic 0 when this register is read.

SYSCLKA

The SYSCLK active (SYSCLKA) bit monitors for low to high transitions on the SYSCLK clock input. SYSCLKA is set to logic 1 on a rising edge of SYSCLK, and cleared to is logic 0 when this register is read.

8KO_SEL[5:0]

The 8 kHz output reference select (8KO_SEL[5:0]) bits select which of the 48 PLCP framer's frame pulse is output on RPOHFP. Frame realignments may cause disruptions in the integrity of this 8 kHz signal. The value corresponds to the system side timeslot assignments shown on Table 52 and referenced in Section 12.7. An 8KO_SEL[5:0] value of 0 corresponds to the PLCP framer residing at the DS3_BASE offset of 0. An 8KO_SEL[5:0] value of 2FH corresponds to the PLCP framer residing at highest DS3_BASE offset value. Legal values of 8KO_SEL[5:0] are from 0 to 2FH.

8KI_SEL[1:0]

The 8 kHz input reference select (8KI_SEL[1:0]) bits select the 8 kHz reference source used to lock the PLCP transmitted frame rate. The selection is shown in Table 10.

Table 10 8 KHz Reference Selection

8KI_SEL[1:0]	8 KHz Reference Source
00	REF8K
01	RPOHFP of corresponding SPLR block
10	Internal 8 kHz reference generated from SYSCLK and initiated by OJ0REF
11	Reserved

Register 0010H: S/UNI-MACH48 DS3 Automatic Alarm Reporting, DS3 LOF Selection, TelecomBus Parity

Bit	Type	Function	Default
Bit 15	R	IPI	X
Bit 14	R/W	IPE	0
Bit 13	R/W	ODDPG	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	INCPL	0
Bit 10	R/W	INCJ0J1	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	DS3LOF[1]	0
Bit 6	R/W	DS3LOF[0]	0
Bit 5	R/W	PLCP_FEBEN	0
Bit 4	R/W	LCDEN	0
Bit 3	R/W	AISEN	0
Bit 2	R/W	REDEN	0
Bit 1	R/W	OOFEN	0
Bit 0	R/W	FEBEN	0

This register is used to enable automatic error reporting due to DS3 far end errors

FEBEN

The FEBEN bit enables the detection of DS3 framing bit errors or C-bit parity errors to generate a FEBE indication in the transmit stream. When FEBEN is logic 1, assertion of a C-bit parity error or a framing bit error indication by the DS3 FRMR causes a FEBE to be transmitted by the corresponding DS3 TRAN. When FEBEN is logic 0, assertion of the errors does not cause transmission of a FEBE.
Note that the FEBE is generated on the DS3 TRAN which occupies the same system side timeslot as the DS3 FRMR.

OOFEN

The OOFEN bit enables the receive out of frame indication to automatically generate a FERF indication in the transmit stream. This bit operates only when the REDEN bit is logic 0. When OOFEN is logic 1, assertion of the OOF indication by the DS3 FRMR causes a FERF to be transmitted by the corresponding DS3 TRAN for the duration of the OOF assertion. When OOFEN is logic 0, assertion of the OOF indication does not cause transmission of a FERF.

Note that the FERF is generated on the DS3 TRAN which occupies the same system side timeslot as the DS3 FRMR.

REDEN

The REDEN bit enables the receive RED alarm (persistent out of frame) indication to automatically generate a FERF indication in the DS3 transmit stream. When REDEN is logic 1, assertion of the RED indication by the DS3 FRMR causes a FERF to be transmitted by the corresponding DS3 TRAN for the duration of the RED assertion. Also, the OOFEN bit is internally forced to logic 0 when REDEN is logic 1. When REDEN is logic 0, assertion of the RED indication does not cause transmission of a FERF.
Note that the FERF is generated on the DS3 TRAN which occupies the same system side timeslot as the DS3 FRMR.

AISEN

The AISEN bit enables the receive alarm indication signal to automatically generate a FERF indication in the transmit stream. When AISEN is logic 1, assertion of the AIS indication by the DS3 FRMR causes a FERF to be transmitted by the corresponding DS3 TRAN for the duration of the AIS assertion. When AISEN is logic 0, assertion of the AIS indication does not cause transmission of a FERF.
Note that the FERF is generated on the DS3 TRAN which occupies the same system side timeslot as the DS3 FRMR.

LCDEN

The LCDEN bit enables the Loss of Cell Delineation state to generate a FERF in the transmit DS3 data stream. When LCDEN is logic 1, assertion of the LCD condition by the corresponding RTDP causes a FERF to be transmitted by the corresponding DS3 TRAN for the duration of the LCD assertion. When LCDEN is logic 0, assertion of the LCD condition does not cause transmission of a FERF.
Note that the FERF is generated on the DS3 TRAN which occupies the same system side timeslot as the DS3 FRMR which feeds the RTDP.

PLCP_FEBEN

The PLCP_FEBEN bit enables BIP8 errors in the PLCP frame to automatically generate appropriate FEBE indications in the transmit PLCP stream. When PLCP_FEBE is logic 1, detection of BIP8 errors by the SPLR causes the correct FEBE count to be transmitted by the corresponding SPLT. When PLCP_FEBEN is logic 0, assertion of the BIP8 errors does not cause transmission of the FEBE.
Note that the FEBE is generated on the SPLT which occupies the same system side timeslot as the SPLR.

DS3LOF[1:0]

The DS3LOF[1:0] bits determine the integration period used for asserting and de-asserting DS3 Loss of Frame. DS3 LOF events and status are given in the S/UNI-MACH48 DS3 LOF Interrupt Indication and S/UNI-MACH48 DS3 LOF Status registers for each DS3 stream. The integration times are selected as follows:

Table 11 DS3 LOF Integration Period Configuration

DS3LOF[1:0]	Integration Period
00	3ms
01	2ms
10	1ms
11	Reserved

INCJ0J1

The INCJ0J1 bit controls the whether the composite timing signals (IJ0J1[4:1], OJ0J1[4:1]) in the incoming and outgoing parallel TelecomBuses are used to calculate the corresponding parity signals (IDP[4:1], ODP[4:1]). When INCJ0J1 is set logic 1, the parity signal set includes the IJ0J1[4:1] and OJ0J1[4:1] signal. When INCJ0J1 is logic 0, parity is calculated without regard to the state of the corresponding IJ0J1[4:1] or OJ0J1[4:1] signal on the buses.

INCPL

The INCPL bit controls the whether the payload active signal (IPL[4:1], OPL[4:1]) in the incoming and outgoing TelecomBuses are used to calculate the corresponding parity signals (IDP[4:1] and ODP[4:1] respectively). When INCPL is set logic 1, the parity signal set includes the corresponding IPL[4:1] or OPL[4:1] signal. When INCPL is logic 0, parity is calculated without regard to the state of the corresponding IPL[4:1] or OPL[4:1] signal on the buses.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

ODDPG

The ODDPG bit controls the parity generated on the outgoing TelecomBus and parity signals (ODP[4:1]). When logic 1, the ODDPG bit configures the bus parity including the corresponding parity signal to be odd. When logic 0, the ODDPG bit configures the bus parity to be even.

IPE

The IPE bit controls the assertion of interrupts when a parity error is detected on the incoming TelecomBus. When IPE is logic 1, an interrupt will be asserted (INTB set logic 0) when a parity error has been detected in the incoming TelecomBus. When IPE is logic 0, incoming bus parity errors will not affect the interrupt output.

IPI

The incoming parallel TelecomBus parity interrupt status bit (IPI) reports the status of the incoming bus parity interrupt. IPI is logic 1 when the current incomming parity is different from the previous parity. This bit and the interrupt are cleared when this register is read. Note, IPI is only valid when operating in parallel TelecomBus mode. The occurrence of parity error events is usually an indication of mis-configured parity generation/detection or actual hardware problem at the incoming bus input.

Register 0011H: Receive Serial TelecomBus Synchronization Delay

Bit	Type	Function	Default
Bit 15	R/W	ICMPDLY	1
Bit 14		Unused	X
Bit 13	R/W	RJ0DLY[13]	0
Bit 12	R/W	RJ0DLY[12]	0
Bit 11	R/W	RJ0DLY[11]	0
Bit 10	R/W	RJ0DLY[10]	0
Bit 9	R/W	RJ0DLY[9]	0
Bit 8	R/W	RJ0DLY[8]	0
Bit 7	R/W	RJ0DLY[7]	0
Bit 6	R/W	RJ0DLY[6]	0
Bit 5	R/W	RJ0DLY[5]	0
Bit 4	R/W	RJ0DLY[4]	0
Bit 3	R/W	RJ0DLY[3]	0
Bit 2	R/W	RJ0DLY[2]	0
Bit 1	R/W	RJ0DLY[1]	0
Bit 0	R/W	RJ0DLY[0]	0

This register controls the delay from the RJ0FP input signal to the time when the S/UNI-MACH48 may safely process the J0 characters delivered by the receive working serial data links (RPWRK[4:1]/RNWRK[4:1]) and the receive protect serial data links (RPPROT[4:1]/RNPROT[4:1]).

RJ0DLY[13:0]

The receive transport frame delay bits (RJ0FP[13:0]) controls the delay, in SYSCLK cycles, inserted by the S/UNI-MACH48 before processing the J0 characters delivered by the two sets of the receive serial data links (RPWRK[4:1]/RNWRK[4:1], and RPPROT[4:1]/RNPROT[4:1]). RJ0DLY is set such that after the specified delay, all active receive links would have delivered the J0 character. The relationships of RJ0FP, RJ0DLY[13:0] and the system configuration are described in the Functional Timing section.

Valid values of RJ0DLY[13:0] are 0000H to 25F7H.

ICMPDLY

When ICMPDLY is set to ‘1’, the ICMP signal is sampled twice on IJ0 or RJ0FP (depending on Serial/Parallel Mode), so the page switch will be expected after two RJ0FP/IJ0 pulses and one internal J0 pulse. When ICMPDLY is set to ‘0’, the ICMP signal is sampled once on IJ0 or RJ0FP, so the page switch will be expected after one RJ0FP/IJ0 pulse and one internal J0 pulse.

This bit allows fine tuning of the expected response to ICMP changes when the RJ0DLY bits move the internal J0 pulse from its default location. ICMPDLY should be set to '1' when S/UNI-MACH48 and PM5372 TSE or PM5310 TBS share a common ICMP.

Register 0012H: Miscellaneous

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	OPTI_MODE[1]	1
Bit 6	R/W	OPTI_MODE[0]	1
Bit 5	R/W	OWTI_MODE[1]	1
Bit 4	R/W	OWTI_MODE[0]	1
Bit 3	R/W	IPTI_MODE[1]	1
Bit 2	R/W	IPTI_MODE[0]	0
Bit 1	R/W	IWTI_MODE[1]	1
Bit 0	R/W	IWTI_MODE[0]	0

More information on the IWTI, IPTI, OWTI, and OPTI mappings can be found in Section 14.9.

IWTI_MODE[1:0]

The IWTI mode bits (IWTI_MODE[1:0]) permit setting of standard timeslot maps in the IWTI block without configuring each STS-1 timeslot.

Table 12 Incoming STSI Mapping Modes

IWTI_MODE[1:0]	IWTI Operation
00	User configured timeslot mapping
01	Bypass mode (no remapping)
10	STS-48c mode
11	Reserved

IPTI_MODE[1:0]

The IPTI mode bits (IPTI_MODE[1:0]) permit setting of standard timeslot maps in the IPTI block without configuring each STS-1 timeslot. The operation modes are identical to those listed for IWTI_MODE[1:0].

OWTI_MODE[1:0]

The OWTI mode bits (OWTI_MODE[1:0]) permit setting of standard timeslot maps in the OWTI block without configuring each STS-1 timeslot.

Table 13 Outgoing STSI Mapping Modes

OWTI_MODE[1:0]	OWTI Operation
00	User configured timeslot mapping
01	Bypass mode (no remapping)
10	Reserved
11	STS-48c mode

OPTI_MODE[1:0]

The OPTI mode bits (OPTI_MODE[1:0]) permit setting of standard timeslot maps in the OPTI block without configuring each STS-1 timeslot. The operation modes are identical to those listed for OWTI_MODE[1:0].

Reserved

The Reserved bit must be set to logic 1 for proper operation.

Register 0013H: Transmit TelecomBus Synchronization Delay

Bit	Type	Function	Default
Bit 15	R/W	OCMPDLY	0
Bit 14		Unused	X
Bit 13	R/W	OJ0REFDLY[13]	0
Bit 12	R/W	OJ0REFDLY[12]	0
Bit 11	R/W	OJ0REFDLY[11]	0
Bit 10	R/W	OJ0REFDLY[10]	0
Bit 9	R/W	OJ0REFDLY[9]	0
Bit 8	R/W	OJ0REFDLY[8]	0
Bit 7	R/W	OJ0REFDLY[7]	0
Bit 6	R/W	OJ0REFDLY[6]	0
Bit 5	R/W	OJ0REFDLY[5]	0
Bit 4	R/W	OJ0REFDLY[4]	0
Bit 3	R/W	OJ0REFDLY[3]	0
Bit 2	R/W	OJ0REFDLY[2]	0
Bit 1	R/W	OJ0REFDLY[1]	0
Bit 0	R/W	OJ0REFDLY[0]	0

This register controls the delay from the OJ0REF input signal to the time when the S/UNI-MACH48 produces the J0 pulse on the transmit parallel TelecomBus interface and the J0 character on the transmit working serial data links (TPWRK[4:1]/TNWRK[4:1]) and the transmit protect serial data links (TPPROT[4:1]/TNPROT[4:1]).

OJ0REFDLY[13:0]

The transmit transport frame delay bits (OJ0REFDLY [13:0]) control the delay, in SYSCLK cycles, inserted by the S/UNI-MACH48 between receiving a reference J0 frame pulse on OJ0REF, and presenting the outgoing J0 transmit frame pulse on OJ0J1[4:1] or J0 character on TPWRK[4:1]/TNWRK[4:1] and TPPROT[4:1]/TNPROT[4:1]. OJ0REFDLY is set such that after the specified delay, OJ0J1[4:1] will have the J0 frame pulse on it. The relationships of OJ0REF, OJ0REFDLY [13:0] and the system configuration are described in the Functional Timing section.

Valid values of OJ0REFDLY [13:0] are 0000H to 25F7H.

OCMPDLY

When OCMPDLY is set to ‘1’, the OCMP signal is sampled twice on OJ0REF, so the page switch will be expected after two OJ0REF pulses and one internal OJ0 pulse. When OCMPDLY is set to ‘0’, the OCMP signal is sampled once on OJ0REF, so the page switch will be expected after one OJ0REF pulse and one internal OJ0 pulse.

This bit allows fine tuning of the expected response to OCMP changes when the OJ0REFDLY bits move the internal OJ0 pulse from its default location. OCMPDLY should be set to '1' when S/UNI-MACH48 and PM5372 TSE or PM5310 TBS share a common OCMP.

Register 0014H: Software General Purpose Register

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

This register is included for software applications that may want a general purpose register. Writes to this register have no effect on the function of the S/UNI-MACH48 device.

FREE[7:0]

The FREE[7:0] register bits do not perform any function. They are free for user defined read/write operations.

Register 0015H: S/UNI-MACH48 Interrupt Block Identifier

Bit	Type	Function	Default
Bit 15	R	ID_DROPI	X
Bit 14	R	ID_MACHI	X
Bit 13	R	ID_LINEI	X
Bit 12	R	ID_PRBS_PPI	X
Bit 11	R	ID_PLCPPMONI	X
Bit 10	R	ID_DS3FRMI	X
Bit 9	R	ID_RDLCI	X
Bit 8	R	ID_TDPRI	X
Bit 7	R	ID_RBOCI	X
Bit 6	R	ID_XBOCI	X
Bit 5	R	ID_D3MDI	X
Bit 4	R	ID_D3MAI	X
Bit 3	R	ID_DS3PMONI	X
Bit 2	R	ID_SPLRI	X
Bit 1	R	ID_TXI	X
Bit 0	R	ID_RXI	X

This register allows the source of an active interrupt to be identified down to the block function level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

ID_RXI

The ID_RXI bit is logic 1 when an interrupt request is active from one of the RXPHY, RXSDQ, RCFP, or RTDP blocks. The particular block which set the interrupt can be identified by reading the S/UNI-MACH48 IPTI, IWTI, RXPHY, RXSDQ, RTDPs, and RCFPs Interrupt Indication register. The ID_RXI bit is cleared when the interrupt is cleared.

ID_TXI

The ID_TXI bit is logic 1 when an interrupt request is active from one of the TXPHY, TXSDQ, TCFP, or TTDP blocks. The particular block which set the interrupt can be identified by reading the S/UNI-MACH48 OPTI, OWTI, TXPHY, TXSDQ, TTDPs, and TCFPs Interrupt Indication register. The ID_TXI bit is cleared when the interrupt is cleared.

ID_SPLRI

The ID_SPLRI bit is logic 1 when an interrupt request is active from one of the SPLR blocks. The particular SPLR which set the interrupt can be identified by reading the S/UNI-MACH48 SPLR Interrupt Indication registers. The ID_SPLRI bit is cleared when the interrupt is cleared.

ID_DS3PMONI

The ID_DS3PMONI bit is logic 1 when an interrupt request is active from one of the DS3 PMON blocks. The particular DS3 PMON which set the interrupt can be identified by reading the S/UNI-MACH48 DS3 PMON Interrupt Indication registers. The ID_DS3PMONI bit is cleared when the interrupt is cleared.

ID_D3MAI

The ID_D3MAI bit is logic 1 when an interrupt request is active from one of the D3MA blocks. The particular D3MA which set the interrupt can be identified by reading the S/UNI-MACH48 D3MA Interrupt Indication registers. The ID_D3MAI bit is cleared when the interrupt is cleared.

ID_D3MDI

The ID_D3MDI bit is logic 1 when an interrupt request is active from one of the D3MD blocks. The particular D3MD which set the interrupt can be identified by reading the S/UNI-MACH48 D3MD Interrupt Indication registers. The ID_D3MDI bit is cleared when the interrupt is cleared.

ID_XBOCI

The ID_XBOCI bit is logic 1 when an interrupt request is active from one of the XBOC blocks. The particular XBOC which set the interrupt can be identified by reading the S/UNI-MACH48 XBOC Interrupt Indication registers. The ID_XBOCI bit is cleared when this register is read.

ID_RBOCI

The ID_RBOCI bit is logic 1 when an interrupt request is active from one of the RBOC blocks. The particular RBOC which set the interrupt can be identified by reading the S/UNI-MACH48 RBOC Interrupt Indication registers. The ID_RBOCI bit is cleared when the interrupt is cleared.

ID_TDPRI

The ID_TDPRI bit is logic 1 when an interrupt request is active from one of the TDPR blocks. The particular TDPR which set the interrupt can be identified by reading the S/UNI-MACH48 TDPR Interrupt Indication registers. The ID_TDPRI bit is cleared when the interrupt is cleared.

ID_RDLCI

The ID_RDLCI bit is logic 1 when an interrupt request is active from one of the RDLC blocks. The particular RDLC which set the interrupt can be identified by reading the S/UNI-MACH48 RDLC Interrupt Indication registers. The ID_RDLCI bit is cleared when the interrupt is cleared.

ID_DS3FRMI

The ID_DS3FRMI bit is logic 1 when an interrupt request is active from one of the DS3 FRMR blocks. The particular DS3 FRMR which set the interrupt can be identified by reading the S/UNI-MACH48 DS3 FRMR Interrupt Indication registers. The ID_DS3FRMRI bit is cleared when the interrupt is cleared.

ID_PLCPPMONI

The ID_PLCPPMONI bit is logic 1 when an interrupt request is active from one of the PLCP PMON blocks. The particular PLCP PMON which set the interrupt can be identified by reading the S/UNI-MACH48 PLCP PMON Interrupt Indication registers. The ID_PLCPPMONI bit is cleared when the interrupt is cleared.

ID_PRBS_PPI

The ID_PRBS_PPI bit is logic 1 when an interrupt request is active from one of the psuedo-random bit processor (PRGM or PRGD) blocks or from an RHPP block. The particular PRGM, RHPP, or PRGD which set the interrupt can be identified by reading the S/UNI-MACH48 PRBS and RHPP Interrupt Indication register. The ID_PRBS_PPI bit is cleared when the interrupt is cleared.

ID_LINEI

The ID_LINEI bit is logic 1 when an interrupt request is active from one of the R8TD 8B/10B decoder blocks, the CSTR clock synthesizer unit (CSU) wrapper block, one of the DLLs, or one of the SIRP blocks. The particular R8TD or CSTR or SIRP block which set the interrupt can be identified by reading the S/UNI-MACH48 8B/10B, CSTR, and Inband Error Interrupt Indication registers. The ID_LINEI bit is cleared when the interrupt is cleared.

ID_MACHI

The ID_MACHI bit is logic 1 when an interrupt request is active from a S/UNI-MACH48 top-level function. The TelecomBus Parity function can be found at register 0010H and the DS3 LOF function can be found at registers 0033H, 0034H, and 0035H. The ID_ MACHI bit is cleared when the interrupt is cleared.

ID_DROPI

The ID_DROPI bit is logic 1 when an interrupt request is active from the per-channel dropped cell/packet indicators. The per-channel dropped cell/packet interrupts can be found at registers 1933H to 1935H. The ID_ DROPI bit is cleared when the interrupt is cleared.

Register 0016H: S/UNI-MACH48 IPTI, IWTI, RXPHY, RXSDQ, RTDPs, and RCFPs Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	IPTII	X
Bit 10	R	IWTII	X
Bit 9	R	RXPHYI	X
Bit 8	R	RXSDQI	X
Bit 7	R	RTDP4I	X
Bit 6	R	RTDP3I	X
Bit 5	R	RTDP2I	X
Bit 4	R	RTDP1I	X
Bit 3	R	RCFP4I	X
Bit 2	R	RCFP3I	X
Bit 1	R	RCFP2I	X
Bit 0	R	RCFP1I	X

This register is used to indicate interrupts generated from blocks associated with the receive UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

RCFP***x***I

The RCFP #***x*** interrupt event indication (RCFP***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RCFP #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

RTDP***x***I

The RTDP #***x*** interrupt event indication (RTDP***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RTDP #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

RXSDQI

The RXSDQ interrupt event indication (RXSDQI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system FIFO RXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

RXPHYI

The RXPHY interrupt event indication (RXPHYI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system UTOPIA/POS-PHY interface RXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

IWTII

The IWTI interrupt event indication (IWTII) transitions to logic 1 when a hardware interrupt event is sourced from the IWTI block. This bit is cleared to logic 0 when the interrupt is cleared.

IPTII

The IPTI interrupt event indication (IPTII) transitions to logic 1 when a hardware interrupt event is sourced from the IPTI block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0017H: S/UNI-MACH48 OPTI, OWTI, TXPHY, TXSDQ, TTDPs, and TCFPs Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	OPTII	X
Bit 10	R	OWTII	X
Bit 9	R	TXPHYI	X
Bit 8	R	TXSDQI	X
Bit 7	R	TTDP4I	X
Bit 6	R	TTDP3I	X
Bit 5	R	TTDP2I	X
Bit 4	R	TTDP1I	X
Bit 3	R	TCFP4I	X
Bit 2	R	TCFP3I	X
Bit 1	R	TCFP2I	X
Bit 0	R	TCFP1I	X

This register is used to indicate interrupts generated from blocks associated with the transmit UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

TCFP***x***I

The TCFP #***x*** interrupt event indication (TCFP***x***I) transitions to logic 1 when a hardware interrupt event is sourced from TCFP #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

TTDP***x***I

The TTDP #***x*** interrupt event indication (TTDP***x***I) transitions to logic 1 when a hardware interrupt event is sourced from TTDP #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

TXSDQI

The TXSDQ interrupt event indication (TXSDQI) transitions to logic 1 when a hardware interrupt event is sourced from the transmit system FIFO TXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

TXPHYI

The TXPHY interrupt event indication (TXPHYI) transitions to logic 1 when a hardware interrupt event is sourced from the transmit system UTOPIA/POS-PHY interface TXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

OWTII

The OWTI interrupt event indication (OWTII) transitions to logic 1 when a hardware interrupt event is sourced from the OWTI block. This bit is cleared to logic 0 when the interrupt is cleared.

OPTII

The OPTI interrupt event indication (OPTII) transitions to logic 1 when a hardware interrupt event is sourced from the OPTI block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0018H: S/UNI-MACH48 SPLR #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	SPLR15I	X
Bit 14	R	SPLR14I	X
Bit 13	R	SPLR13I	X
Bit 12	R	SPLR12I	X
Bit 11	R	SPLR11I	X
Bit 10	R	SPLR10I	X
Bit 9	R	SPLR9I	X
Bit 8	R	SPLR8I	X
Bit 7	R	SPLR7I	X
Bit 6	R	SPLR6I	X
Bit 5	R	SPLR5I	X
Bit 4	R	SPLR4I	X
Bit 3	R	SPLR3I	X
Bit 2	R	SPLR2I	X
Bit 1	R	SPLR1I	X
Bit 0	R	SPLR0I	X

This register is used to indicate interrupts generated from the SPLR blocks.

SPLR***x***I

The SPLR #***x*** interrupt event indication (SPLR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from SPLR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0019H: S/UNI-MACH48 SPLR #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	SPLR31I	X
Bit 14	R	SPLR30I	X
Bit 13	R	SPLR29I	X
Bit 12	R	SPLR28I	X
Bit 11	R	SPLR27I	X
Bit 10	R	SPLR26I	X
Bit 9	R	SPLR25I	X
Bit 8	R	SPLR24I	X
Bit 7	R	SPLR23I	X
Bit 6	R	SPLR22I	X
Bit 5	R	SPLR21I	X
Bit 4	R	SPLR20I	X
Bit 3	R	SPLR19I	X
Bit 2	R	SPLR18I	X
Bit 1	R	SPLR17I	X
Bit 0	R	SPLR16I	X

This register is used to indicate interrupts generated from the SPLR blocks.

SPLR***x***I

The SPLR #***x*** interrupt event indication (SPLR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from SPLR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 001AH: S/UNI-MACH48 SPLR #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	SPLR47I	X
Bit 14	R	SPLR46I	X
Bit 13	R	SPLR45I	X
Bit 12	R	SPLR44I	X
Bit 11	R	SPLR43I	X
Bit 10	R	SPLR42I	X
Bit 9	R	SPLR41I	X
Bit 8	R	SPLR40I	X
Bit 7	R	SPLR39I	X
Bit 6	R	SPLR38I	X
Bit 5	R	SPLR37I	X
Bit 4	R	SPLR36I	X
Bit 3	R	SPLR35I	X
Bit 2	R	SPLR34I	X
Bit 1	R	SPLR33I	X
Bit 0	R	SPLR32I	X

This register is used to indicate interrupts generated from the SPLR blocks.

SPLR*x*I

The SPLR #***x*** interrupt event indication (SPLR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from SPLR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 001BH: S/UNI-MACH48 DS3 PMON #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3PMON15I	X
Bit 14	R	DS3PMON14I	X
Bit 13	R	DS3PMON13I	X
Bit 12	R	DS3PMON12I	X
Bit 11	R	DS3PMON11I	X
Bit 10	R	DS3PMON10I	X
Bit 9	R	DS3PMON9I	X
Bit 8	R	DS3PMON8I	X
Bit 7	R	DS3PMON7I	X
Bit 6	R	DS3PMON6I	X
Bit 5	R	DS3PMON5I	X
Bit 4	R	DS3PMON4I	X
Bit 3	R	DS3PMON3I	X
Bit 2	R	DS3PMON2I	X
Bit 1	R	DS3PMON1I	X
Bit 0	R	DS3PMON0I	X

This register is used to indicate interrupts generated from the DS3 PMON blocks.

DS3PMON***x***I

The DS3 PMON #***x*** interrupt event indication (DS3PMON***x***I) transitions to logic 1 when a hardware interrupt event is sourced from DS3 PMON #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 001CH: S/UNI-MACH48 DS3 PMON #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3PMON31I	X
Bit 14	R	DS3PMON30I	X
Bit 13	R	DS3PMON29I	X
Bit 12	R	DS3PMON28I	X
Bit 11	R	DS3PMON27I	X
Bit 10	R	DS3PMON26I	X
Bit 9	R	DS3PMON25I	X
Bit 8	R	DS3PMON24I	X
Bit 7	R	DS3PMON23I	X
Bit 6	R	DS3PMON22I	X
Bit 5	R	DS3PMON21I	X
Bit 4	R	DS3PMON20I	X
Bit 3	R	DS3PMON19I	X
Bit 2	R	DS3PMON18I	X
Bit 1	R	DS3PMON17I	X
Bit 0	R	DS3PMON16I	X

This register is used to indicate interrupts generated from the DS3 PMON blocks.

S3PMON***x***I

The DS3 PMON #***x*** interrupt event indication (DS3PMON***x***I) transitions to logic 1 when a hardware interrupt event is sourced from DS3 PMON #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 001DH: S/UNI-MACH48 DS3 PMON #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3PMON47I	X
Bit 14	R	DS3PMON46I	X
Bit 13	R	DS3PMON45I	X
Bit 12	R	DS3PMON44I	X
Bit 11	R	DS3PMON43I	X
Bit 10	R	DS3PMON42I	X
Bit 9	R	DS3PMON41I	X
Bit 8	R	DS3PMON40I	X
Bit 7	R	DS3PMON39I	X
Bit 6	R	DS3PMON38I	X
Bit 5	R	DS3PMON37I	X
Bit 4	R	DS3PMON36I	X
Bit 3	R	DS3PMON35I	X
Bit 2	R	DS3PMON34I	X
Bit 1	R	DS3PMON33I	X
Bit 0	R	DS3PMON32I	X

DS3PMON***x***I

The DS3 PMON #***x*** interrupt event indication (DS3PMON***x***I) transitions to logic 1 when a hardware interrupt event is sourced from DS3 PMON #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.This register is used to indicate interrupts generated from the DS3 PMON blocks.

Register 001EH: S/UNI-MACH48 D3MA #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	D3MA15I	X
Bit 14	R	D3MA14I	X
Bit 13	R	D3MA13I	X
Bit 12	R	D3MA12I	X
Bit 11	R	D3MA11I	X
Bit 10	R	D3MA10I	X
Bit 9	R	D3MA9I	X
Bit 8	R	D3MA8I	X
Bit 7	R	D3MA7I	X
Bit 6	R	D3MA6I	X
Bit 5	R	D3MA5I	X
Bit 4	R	D3MA4I	X
Bit 3	R	D3MA3I	X
Bit 2	R	D3MA2I	X
Bit 1	R	D3MA1I	X
Bit 0	R	D3MA0I	X

This register is used to indicate interrupts generated from the D3MA blocks.

D3MA***x***I

The D3MA #***x*** interrupt event indication (D3MA***x***I) transitions to logic 1 when a hardware interrupt event is sourced from D3MA #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 001FH: S/UNI-MACH48 D3MA #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	D3MA31I	X
Bit 14	R	D3MA30I	X
Bit 13	R	D3MA29I	X
Bit 12	R	D3MA28I	X
Bit 11	R	D3MA27I	X
Bit 10	R	D3MA26I	X
Bit 9	R	D3MA25I	X
Bit 8	R	D3MA24I	X
Bit 7	R	D3MA23I	X
Bit 6	R	D3MA22I	X
Bit 5	R	D3MA21I	X
Bit 4	R	D3MA20I	X
Bit 3	R	D3MA19I	X
Bit 2	R	D3MA18I	X
Bit 1	R	D3MA17I	X
Bit 0	R	D3MA16I	X

This register is used to indicate interrupts generated from the D3MA blocks.

D3MA***x***I

The D3MA #***x*** interrupt event indication (D3MA***x***I) transitions to logic 1 when a hardware interrupt event is sourced from D3MA #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0020H: S/UNI-MACH48 D3MA #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	D3MA47I	X
Bit 14	R	D3MA46I	X
Bit 13	R	D3MA45I	X
Bit 12	R	D3MA44I	X
Bit 11	R	D3MA43I	X
Bit 10	R	D3MA42I	X
Bit 9	R	D3MA41I	X
Bit 8	R	D3MA40I	X
Bit 7	R	D3MA39I	X
Bit 6	R	D3MA38I	X
Bit 5	R	D3MA37I	X
Bit 4	R	D3MA36I	X
Bit 3	R	D3MA35I	X
Bit 2	R	D3MA34I	X
Bit 1	R	D3MA33I	X
Bit 0	R	D3MA32I	X

This register is used to indicate interrupts generated from the D3MA blocks.

D3MA***x***I

The D3MA #***x*** interrupt event indication (D3MA***x***I) transitions to logic 1 when a hardware interrupt event is sourced from D3MA #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0021H: S/UNI-MACH48 D3MD #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	D3MD15I	X
Bit 14	R	D3MD14I	X
Bit 13	R	D3MD13I	X
Bit 12	R	D3MD12I	X
Bit 11	R	D3MD11I	X
Bit 10	R	D3MD10I	X
Bit 9	R	D3MD9I	X
Bit 8	R	D3MD8I	X
Bit 7	R	D3MD7I	X
Bit 6	R	D3MD6I	X
Bit 5	R	D3MD5I	X
Bit 4	R	D3MD4I	X
Bit 3	R	D3MD3I	X
Bit 2	R	D3MD2I	X
Bit 1	R	D3MD1I	X
Bit 0	R	D3MD0I	X

This register is used to indicate interrupts generated from the D3MD blocks.

D3MD***x***I

The D3MD #***x*** interrupt event indication (D3MD***x***I) transitions to logic 1 when a hardware interrupt event is sourced from D3MD #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0022H: S/UNI-MACH48 D3MD #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	D3MD31I	X
Bit 14	R	D3MD30I	X
Bit 13	R	D3MD29I	X
Bit 12	R	D3MD28I	X
Bit 11	R	D3MD27I	X
Bit 10	R	D3MD26I	X
Bit 9	R	D3MD25I	X
Bit 8	R	D3MD24I	X
Bit 7	R	D3MD23I	X
Bit 6	R	D3MD22I	X
Bit 5	R	D3MD21I	X
Bit 4	R	D3MD20I	X
Bit 3	R	D3MD19I	X
Bit 2	R	D3MD18I	X
Bit 1	R	D3MD17I	X
Bit 0	R	D3MD16I	X

This register is used to indicate interrupts generated from the D3MD blocks.

D3MD***x***I

The D3MD #***x*** interrupt event indication (D3MD***x***I) transitions to logic 1 when a hardware interrupt event is sourced from D3MD #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0023H: S/UNI-MACH48 D3MD #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	D3MD47I	X
Bit 14	R	D3MD46I	X
Bit 13	R	D3MD45I	X
Bit 12	R	D3MD44I	X
Bit 11	R	D3MD43I	X
Bit 10	R	D3MD42I	X
Bit 9	R	D3MD41I	X
Bit 8	R	D3MD40I	X
Bit 7	R	D3MD39I	X
Bit 6	R	D3MD38I	X
Bit 5	R	D3MD37I	X
Bit 4	R	D3MD36I	X
Bit 3	R	D3MD35I	X
Bit 2	R	D3MD34I	X
Bit 1	R	D3MD33I	X
Bit 0	R	D3MD32I	X

This register is used to indicate interrupts generated from the D3MD blocks.

D3MD***x***I

The D3MD #***x*** interrupt event indication (D3MD***x***I) transitions to logic 1 when a hardware interrupt event is sourced from D3MD #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0024H: S/UNI-MACH48 XBOC #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	XBOC15I	X
Bit 14	R	XBOC14I	X
Bit 13	R	XBOC13I	X
Bit 12	R	XBOC12I	X
Bit 11	R	XBOC11I	X
Bit 10	R	XBOC10I	X
Bit 9	R	XBOC9I	X
Bit 8	R	XBOC8I	X
Bit 7	R	XBOC7I	X
Bit 6	R	XBOC6I	X
Bit 5	R	XBOC5I	X
Bit 4	R	XBOC4I	X
Bit 3	R	XBOC3I	X
Bit 2	R	XBOC2I	X
Bit 1	R	XBOC1I	X
Bit 0	R	XBOC0I	X

This register is used to indicate interrupts generated from the XBOC blocks.

XBOC***x***I

The XBOC #***x*** interrupt event indication (XBOC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from XBOC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0025H: S/UNI-MACH48 XBOC #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	XBOC31I	X
Bit 14	R	XBOC30I	X
Bit 13	R	XBOC29I	X
Bit 12	R	XBOC28I	X
Bit 11	R	XBOC27I	X
Bit 10	R	XBOC26I	X
Bit 9	R	XBOC25I	X
Bit 8	R	XBOC24I	X
Bit 7	R	XBOC23I	X
Bit 6	R	XBOC22I	X
Bit 5	R	XBOC21I	X
Bit 4	R	XBOC20I	X
Bit 3	R	XBOC19I	X
Bit 2	R	XBOC18I	X
Bit 1	R	XBOC17I	X
Bit 0	R	XBOC16I	X

This register is used to indicate interrupts generated from the XBOC blocks.

XBOC***x***I

The XBOC #***x*** interrupt event indication (XBOC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from XBOC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0026H: S/UNI-MACH48 XBOC #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	XBOC47I	X
Bit 14	R	XBOC46I	X
Bit 13	R	XBOC45I	X
Bit 12	R	XBOC44I	X
Bit 11	R	XBOC43I	X
Bit 10	R	XBOC42I	X
Bit 9	R	XBOC41I	X
Bit 8	R	XBOC40I	X
Bit 7	R	XBOC39I	X
Bit 6	R	XBOC38I	X
Bit 5	R	XBOC37I	X
Bit 4	R	XBOC36I	X
Bit 3	R	XBOC35I	X
Bit 2	R	XBOC34I	X
Bit 1	R	XBOC33I	X
Bit 0	R	XBOC32I	X

This register is used to indicate interrupts generated from the XBOC blocks.

XBOC***x***I

The XBOC #***x*** interrupt event indication (XBOC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from XBOC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0027H: S/UNI-MACH48 RBOC #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	RBOC15I	X
Bit 14	R	RBOC14I	X
Bit 13	R	RBOC13I	X
Bit 12	R	RBOC12I	X
Bit 11	R	RBOC11I	X
Bit 10	R	RBOC10I	X
Bit 9	R	RBOC9I	X
Bit 8	R	RBOC8I	X
Bit 7	R	RBOC7I	X
Bit 6	R	RBOC6I	X
Bit 5	R	RBOC5I	X
Bit 4	R	RBOC4I	X
Bit 3	R	RBOC3I	X
Bit 2	R	RBOC2I	X
Bit 1	R	RBOC1I	X
Bit 0	R	RBOC0I	X

This register is used to indicate interrupts generated from the RBOC blocks.

RBOC***x***I

The RBOC #***x*** interrupt event indication (RBOC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RBOC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0028H: S/UNI-MACH48 RBOC #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	RBOC31I	X
Bit 14	R	RBOC30I	X
Bit 13	R	RBOC29I	X
Bit 12	R	RBOC28I	X
Bit 11	R	RBOC27I	X
Bit 10	R	RBOC26I	X
Bit 9	R	RBOC25I	X
Bit 8	R	RBOC24I	X
Bit 7	R	RBOC23I	X
Bit 6	R	RBOC22I	X
Bit 5	R	RBOC21I	X
Bit 4	R	RBOC20I	X
Bit 3	R	RBOC19I	X
Bit 2	R	RBOC18I	X
Bit 1	R	RBOC17I	X
Bit 0	R	RBOC16I	X

This register is used to indicate interrupts generated from the RBOC blocks.

RBOC***x***I

The RBOC #***x*** interrupt event indication (RBOC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RBOC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0029H: S/UNI-MACH48 RBOC #31-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	RBOC47I	X
Bit 14	R	RBOC46I	X
Bit 13	R	RBOC45I	X
Bit 12	R	RBOC44I	X
Bit 11	R	RBOC43I	X
Bit 10	R	RBOC42I	X
Bit 9	R	RBOC41I	X
Bit 8	R	RBOC40I	X
Bit 7	R	RBOC39I	X
Bit 6	R	RBOC38I	X
Bit 5	R	RBOC37I	X
Bit 4	R	RBOC36I	X
Bit 3	R	RBOC35I	X
Bit 2	R	RBOC34I	X
Bit 1	R	RBOC33I	X
Bit 0	R	RBOC32I	X

This register is used to indicate interrupts generated from the RBOC blocks.

RBOC***x***I

The RBOC #***x*** interrupt event indication (RBOC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RBOC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 002AH: S/UNI-MACH48 TDPR #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	TDPR15I	X
Bit 14	R	TDPR14I	X
Bit 13	R	TDPR13I	X
Bit 12	R	TDPR12I	X
Bit 11	R	TDPR11I	X
Bit 10	R	TDPR10I	X
Bit 9	R	TDPR9I	X
Bit 8	R	TDPR8I	X
Bit 7	R	TDPR7I	X
Bit 6	R	TDPR6I	X
Bit 5	R	TDPR5I	X
Bit 4	R	TDPR4I	X
Bit 3	R	TDPR3I	X
Bit 2	R	TDPR2I	X
Bit 1	R	TDPR1I	X
Bit 0	R	TDPR0I	X

This register is used to indicate interrupts generated from the TDPR blocks.

TDPR***x***I

The TDPR #***x*** interrupt event indication (TDPR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from TDPR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 002BH: S/UNI-MACH48 TDPR #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	TDPR31I	X
Bit 14	R	TDPR30I	X
Bit 13	R	TDPR29I	X
Bit 12	R	TDPR28I	X
Bit 11	R	TDPR27I	X
Bit 10	R	TDPR26I	X
Bit 9	R	TDPR25I	X
Bit 8	R	TDPR24I	X
Bit 7	R	TDPR23I	X
Bit 6	R	TDPR22I	X
Bit 5	R	TDPR21I	X
Bit 4	R	TDPR20I	X
Bit 3	R	TDPR19I	X
Bit 2	R	TDPR18I	X
Bit 1	R	TDPR17I	X
Bit 0	R	TDPR16I	X

This register is used to indicate interrupts generated from the TDPR blocks.

TDPR***x***I

The TDPR #***x*** interrupt event indication (TDPR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from TDPR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 002CH: S/UNI-MACH48 TDPR #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	TDPR47I	X
Bit 14	R	TDPR46I	X
Bit 13	R	TDPR45I	X
Bit 12	R	TDPR44I	X
Bit 11	R	TDPR43I	X
Bit 10	R	TDPR42I	X
Bit 9	R	TDPR41I	X
Bit 8	R	TDPR40I	X
Bit 7	R	TDPR39I	X
Bit 6	R	TDPR38I	X
Bit 5	R	TDPR37I	X
Bit 4	R	TDPR36I	X
Bit 3	R	TDPR35I	X
Bit 2	R	TDPR34I	X
Bit 1	R	TDPR33I	X
Bit 0	R	TDPR32I	X

This register is used to indicate interrupts generated from the TDPR blocks.

TDPR***x***I

The TDPR #***x*** interrupt event indication (TDPR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from TDPR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 002DH: S/UNI-MACH48 RDLC #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	RDLC15I	X
Bit 14	R	RDLC14I	X
Bit 13	R	RDLC13I	X
Bit 12	R	RDLC12I	X
Bit 11	R	RDLC11I	X
Bit 10	R	RDLC10I	X
Bit 9	R	RDLC9I	X
Bit 8	R	RDLC8I	X
Bit 7	R	RDLC7I	X
Bit 6	R	RDLC6I	X
Bit 5	R	RDLC5I	X
Bit 4	R	RDLC4I	X
Bit 3	R	RDLC3I	X
Bit 2	R	RDLC2I	X
Bit 1	R	RDLC1I	X
Bit 0	R	RDLC0I	X

This register is used to indicate interrupts generated from the RDLC blocks.

RDLC***x***I

The RDLC #***x*** interrupt event indication (RDLC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RDLC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 002EH: S/UNI-MACH48 RDLC #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	RDLC31I	X
Bit 14	R	RDLC30I	X
Bit 13	R	RDLC29I	X
Bit 12	R	RDLC28I	X
Bit 11	R	RDLC27I	X
Bit 10	R	RDLC26I	X
Bit 9	R	RDLC25I	X
Bit 8	R	RDLC24I	X
Bit 7	R	RDLC23I	X
Bit 6	R	RDLC22I	X
Bit 5	R	RDLC21I	X
Bit 4	R	RDLC20I	X
Bit 3	R	RDLC19I	X
Bit 2	R	RDLC18I	X
Bit 1	R	RDLC17I	X
Bit 0	R	RDLC16I	X

This register is used to indicate interrupts generated from the RDLC blocks.

RDLC***x***I

The RDLC #***x*** interrupt event indication (RDLC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RDLC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 002FH: S/UNI-MACH48 RDLC #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	RDLC47I	X
Bit 14	R	RDLC46I	X
Bit 13	R	RDLC45I	X
Bit 12	R	RDLC44I	X
Bit 11	R	RDLC43I	X
Bit 10	R	RDLC42I	X
Bit 9	R	RDLC41I	X
Bit 8	R	RDLC40I	X
Bit 7	R	RDLC39I	X
Bit 6	R	RDLC38I	X
Bit 5	R	RDLC37I	X
Bit 4	R	RDLC36I	X
Bit 3	R	RDLC35I	X
Bit 2	R	RDLC34I	X
Bit 1	R	RDLC33I	X
Bit 0	R	RDLC32I	X

This register is used to indicate interrupts generated from the RDLC blocks.

RDLC***x***I

The RDLC #***x*** interrupt event indication (RDLC***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RDLC #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0030H: S/UNI-MACH48 DS3FRMR #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3FRMR15I	X
Bit 14	R	DS3FRMR14I	X
Bit 13	R	DS3FRMR13I	X
Bit 12	R	DS3FRMR12I	X
Bit 11	R	DS3FRMR11I	X
Bit 10	R	DS3FRMR10I	X
Bit 9	R	DS3FRMR9I	X
Bit 8	R	DS3FRMR8I	X
Bit 7	R	DS3FRMR7I	X
Bit 6	R	DS3FRMR6I	X
Bit 5	R	DS3FRMR5I	X
Bit 4	R	DS3FRMR4I	X
Bit 3	R	DS3FRMR3I	X
Bit 2	R	DS3FRMR2I	X
Bit 1	R	DS3FRMR1I	X
Bit 0	R	DS3FRMR0I	X

This register is used to indicate interrupts generated from the DS3FRMR blocks.

DS3FRMR***x***I

The DS3FRMR #***x*** interrupt event indication (DS3FRMR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from DS3FRMR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0031H: S/UNI-MACH48 DS3FRMR #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3FRMR31I	X
Bit 14	R	DS3FRMR30I	X
Bit 13	R	DS3FRMR29I	X
Bit 12	R	DS3FRMR28I	X
Bit 11	R	DS3FRMR27I	X
Bit 10	R	DS3FRMR26I	X
Bit 9	R	DS3FRMR25I	X
Bit 8	R	DS3FRMR24I	X
Bit 7	R	DS3FRMR23I	X
Bit 6	R	DS3FRMR22I	X
Bit 5	R	DS3FRMR21I	X
Bit 4	R	DS3FRMR20I	X
Bit 3	R	DS3FRMR19I	X
Bit 2	R	DS3FRMR18I	X
Bit 1	R	DS3FRMR17I	X
Bit 0	R	DS3FRMR16I	X

This register is used to indicate interrupts generated from the DS3FRMR blocks.

DS3FRMR***x***I

The DS3FRMR #***x*** interrupt event indication (DS3FRMR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from DS3FRMR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0032H: S/UNI-MACH48 DS3FRMR #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3FRMR47I	X
Bit 14	R	DS3FRMR46I	X
Bit 13	R	DS3FRMR45I	X
Bit 12	R	DS3FRMR44I	X
Bit 11	R	DS3FRMR43I	X
Bit 10	R	DS3FRMR42I	X
Bit 9	R	DS3FRMR41I	X
Bit 8	R	DS3FRMR40I	X
Bit 7	R	DS3FRMR39I	X
Bit 6	R	DS3FRMR38I	X
Bit 5	R	DS3FRMR37I	X
Bit 4	R	DS3FRMR36I	X
Bit 3	R	DS3FRMR35I	X
Bit 2	R	DS3FRMR34I	X
Bit 1	R	DS3FRMR33I	X
Bit 0	R	DS3FRMR32I	X

This register is used to indicate interrupts generated from the DS3FRMR blocks.

DS3FRMR***x***I

The DS3FRMR #***x*** interrupt event indication (DS3FRMR***x***I) transitions to logic 1 when a hardware interrupt event is sourced from DS3FRMR #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0033H: S/UNI-MACH48 DS3 LOF #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3LOF15I	X
Bit 14	R	DS3LOF14I	X
Bit 13	R	DS3LOF13I	X
Bit 12	R	DS3LOF12I	X
Bit 11	R	DS3LOF11I	X
Bit 10	R	DS3LOF10I	X
Bit 9	R	DS3LOF9I	X
Bit 8	R	DS3LOF8I	X
Bit 7	R	DS3LOF7I	X
Bit 6	R	DS3LOF6I	X
Bit 5	R	DS3LOF5I	X
Bit 4	R	DS3LOF4I	X
Bit 3	R	DS3LOF3I	X
Bit 2	R	DS3LOF2I	X
Bit 1	R	DS3LOF1I	X
Bit 0	R	DS3LOF0I	X

This register is used to indicate interrupts generated from the DS3 LOF events.

DS3LOF***x***I

The DS3LOF #***x*** interrupt event indication (DS3LOF***x***I) transitions to logic 1 when a DS3 LOF state is detected or cleared on the DS3FRMR#***x*** data stream. This bit is cleared to logic 0 when this register is read. The status of the DS3 LOF state can be read from the corresponding bit of register 003BH.

Register 0034H: S/UNI-MACH48 DS3 LOF #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3LOF31I	X
Bit 14	R	DS3LOF30I	X
Bit 13	R	DS3LOF29I	X
Bit 12	R	DS3LOF28I	X
Bit 11	R	DS3LOF27I	X
Bit 10	R	DS3LOF26I	X
Bit 9	R	DS3LOF25I	X
Bit 8	R	DS3LOF24I	X
Bit 7	R	DS3LOF23I	X
Bit 6	R	DS3LOF22I	X
Bit 5	R	DS3LOF21I	X
Bit 4	R	DS3LOF20I	X
Bit 3	R	DS3LOF19I	X
Bit 2	R	DS3LOF18I	X
Bit 1	R	DS3LOF17I	X
Bit 0	R	DS3LOF16I	X

This register is used to indicate interrupts generated from the DS3 LOF events.

DS3LOF***x***I

The DS3LOF #***x*** interrupt event indication (DS3LOF***x***I) transitions to logic 1 when a DS3 LOF state is detected or cleared on the DS3FRMR#***x*** data stream. This bit is cleared to logic 0 when this register is read. The status of the DS3 LOF state can be read from the corresponding bit of register 003CH.

Register 0035H: S/UNI-MACH48 DS3 LOF #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DS3LOF47I	X
Bit 14	R	DS3LOF46I	X
Bit 13	R	DS3LOF45I	X
Bit 12	R	DS3LOF44I	X
Bit 11	R	DS3LOF43I	X
Bit 10	R	DS3LOF42I	X
Bit 9	R	DS3LOF41I	X
Bit 8	R	DS3LOF40I	X
Bit 7	R	DS3LOF39I	X
Bit 6	R	DS3LOF38I	X
Bit 5	R	DS3LOF37I	X
Bit 4	R	DS3LOF36I	X
Bit 3	R	DS3LOF35I	X
Bit 2	R	DS3LOF34I	X
Bit 1	R	DS3LOF33I	X
Bit 0	R	DS3LOF32I	X

This register is used to indicate interrupts generated from the DS3 LOF events.

DS3LOF***x***I

The DS3LOF #***x*** interrupt event indication (DS3LOF***x***I) transitions to logic 1 when a DS3 LOF state is detected or cleared on the DS3FRMR#***x*** data stream. This bit is cleared to logic 0 when this register is read. The status of the DS3 LOF state can be read from the corresponding bit of register 003DH.

Register 0036H: S/UNI-MACH48 PLCP PMON #0-15 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	PLCPPMON15I	X
Bit 14	R	PLCPPMON14I	X
Bit 13	R	PLCPPMON13I	X
Bit 12	R	PLCPPMON12I	X
Bit 11	R	PLCPPMON11I	X
Bit 10	R	PLCPPMON10I	X
Bit 9	R	PLCPPMON9I	X
Bit 8	R	PLCPPMON8I	X
Bit 7	R	PLCPPMON7I	X
Bit 6	R	PLCPPMON6I	X
Bit 5	R	PLCPPMON5I	X
Bit 4	R	PLCPPMON4I	X
Bit 3	R	PLCPPMON3I	X
Bit 2	R	PLCPPMON2I	X
Bit 1	R	PLCPPMON1I	X
Bit 0	R	PLCPPMON0I	X

This register is used to indicate interrupts generated from the PLCP PMON blocks.

PLCPPMON***x***I

The PLCP PMON #***x*** interrupt event indication (PLCPPMON***x***I) transitions to logic 1 when a hardware interrupt event is sourced from PLCP PMON #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0037H: S/UNI-MACH48 PLCP PMON #16-31 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	PLCPPMON31I	X
Bit 14	R	PLCPPMON30I	X
Bit 13	R	PLCPPMON29I	X
Bit 12	R	PLCPPMON28I	X
Bit 11	R	PLCPPMON27I	X
Bit 10	R	PLCPPMON26I	X
Bit 9	R	PLCPPMON25I	X
Bit 8	R	PLCPPMON24I	X
Bit 7	R	PLCPPMON23I	X
Bit 6	R	PLCPPMON22I	X
Bit 5	R	PLCPPMON21I	X
Bit 4	R	PLCPPMON20I	X
Bit 3	R	PLCPPMON19I	X
Bit 2	R	PLCPPMON18I	X
Bit 1	R	PLCPPMON17I	X
Bit 0	R	PLCPPMON16I	X

This register is used to indicate interrupts generated from the PLCP PMON blocks.

PLCPPMON***x***I

The PLCP PMON #***x*** interrupt event indication (PLCPPMON***x***I) transitions to logic 1 when a hardware interrupt event is sourced from PLCP PMON #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0038H: S/UNI-MACH48 PLCP PMON #32-47 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	PLCPPMON47I	X
Bit 14	R	PLCPPMON46I	X
Bit 13	R	PLCPPMON45I	X
Bit 12	R	PLCPPMON44I	X
Bit 11	R	PLCPPMON43I	X
Bit 10	R	PLCPPMON42I	X
Bit 9	R	PLCPPMON41I	X
Bit 8	R	PLCPPMON40I	X
Bit 7	R	PLCPPMON39I	X
Bit 6	R	PLCPPMON38I	X
Bit 5	R	PLCPPMON37I	X
Bit 4	R	PLCPPMON36I	X
Bit 3	R	PLCPPMON35I	X
Bit 2	R	PLCPPMON34I	X
Bit 1	R	PLCPPMON33I	X
Bit 0	R	PLCPPMON32I	X

This register is used to indicate interrupts generated from the PLCP PMON blocks.

DS3PMON***x***I

The PLCP PMON #***x*** interrupt event indication (PLCPPMON***x***I) transitions to logic 1 when a hardware interrupt event is sourced from PLCP PMON #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0039H: S/UNI-MACH48 PRBS and RHPP Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	RHPP3I	X
Bit 14	R	RHPP2I	X
Bit 13	R	RHPP1I	X
Bit 12	R	RHPP0I	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	PRGDI	X
Bit 8		Unused	X
Bit 7	R	PRGM7I	X
Bit 6	R	PRGM6I	X
Bit 5	R	PRGM5I	X
Bit 4	R	PRGM4I	X
Bit 3	R	PRGM3I	X
Bit 2	R	PRGM2I	X
Bit 1	R	PRGM1I	X
Bit 0	R	PRGM0I	X

This register is used to indicate interrupts generated from the PRBS processor blocks.

PRGM***x***I

The PRGM #***x*** interrupt event indication (PRGM***x***I) transitions to logic 1 when a hardware interrupt event is sourced from PRGM #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

PRGDI

The PRGD interrupt event indication (PRGDI) transitions to logic 1 when a hardware interrupt event is sourced from PRGD block. This bit is cleared to logic 0 when the interrupt is cleared.

RHPP***x***I

The RHPP #***x*** interrupt event indication (RHPP***x***I) transitions to logic 1 when a hardware interrupt event is sourced from RHPP #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 003AH: S/UNI-MACH48 8B/10B, CSTR, and DLL Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	DLL_SYSCLKI	X
Bit 14	R	DLL_TFCLKI	X
Bit 13	R	DLL_RFCLKI	X
Bit 12	R	CSTRI	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	R8TD7I	X
Bit 6	R	R8TD6I	X
Bit 5	R	R8TD5I	X
Bit 4	R	R8TD4I	X
Bit 3	R	R8TD3I	X
Bit 2	R	R8TD2I	X
Bit 1	R	R8TD1I	X
Bit 0	R	R8TD0I	X

This register is used to indicate interrupts generated from the R8TD 8B/10B decoder blocks, the Clock Synthesizer (CSU) block and the SIRP blocks.

R8TD***x***I

The R8TD #***x*** interrupt event indication (R8TD***x***I) transitions to logic 1 when a hardware interrupt event is sourced from R8TD #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

CSTRI

The CSU Lock interrupt event indication (CSTRI) transitions to logic 1 when a hardware interrupt event is sourced from the CSU wrapper (CSTR) block. This bit is cleared to logic 0 when the interrupt is cleared.

DLL_RFCLKI

The DLL_RFCLK interrupt event indication (DLL_RFCLKI) transitions to logic 1 when a hardware interrupt event is sourced from the RFCLK DLL block. This bit is cleared to logic 0 when the interrupt is cleared.

DLL_TFCLKI

The DLL_TFCLK interrupt event indication (DLL_TFCLKI) transitions to logic 1 when a hardware interrupt event is sourced from the TFCLK DLL block. This bit is cleared to logic 0 when the interrupt is cleared.

DLL_SYSCLKI

The DLL_SYSCLK interrupt event indication (DLL_SYSCLKI) transitions to logic 1 when a hardware interrupt event is sourced from the SYSCLK DLL block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 003BH: S/UNI-MACH48 DS3 #0-15 LOF Status

Bit	Type	Function	Default
Bit 15	R	DS3LOF15V	X
Bit 14	R	DS3LOF14V	X
Bit 13	R	DS3LOF13V	X
Bit 12	R	DS3LOF12V	X
Bit 11	R	DS3LOF11V	X
Bit 10	R	DS3LOF10V	X
Bit 9	R	DS3LOF9V	X
Bit 8	R	DS3LOF8V	X
Bit 7	R	DS3LOF7V	X
Bit 6	R	DS3LOF6V	X
Bit 5	R	DS3LOF5V	X
Bit 4	R	DS3LOF4V	X
Bit 3	R	DS3LOF3V	X
Bit 2	R	DS3LOF2V	X
Bit 1	R	DS3LOF1V	X
Bit 0	R	DS3LOF0V	X

This register is used to indicate the current DS3 LOF status.

DS3LOF***x***V

The DS3LOF #***x*** status (DS3LOF***x***V) is logic 1 when the DS3 data stream is in Loss Of Frame state. It is logic 0 when the DS3 data stream is not in Loss of Frame State.

Register 003CH: S/UNI-MACH48 DS3 #16-31 LOF Status

Bit	Type	Function	Default
Bit 15	R	DS3LOF31V	X
Bit 14	R	DS3LOF30V	X
Bit 13	R	DS3LOF29V	X
Bit 12	R	DS3LOF28V	X
Bit 11	R	DS3LOF27V	X
Bit 10	R	DS3LOF26V	X
Bit 9	R	DS3LOF25V	X
Bit 8	R	DS3LOF24V	X
Bit 7	R	DS3LOF23V	X
Bit 6	R	DS3LOF22V	X
Bit 5	R	DS3LOF21V	X
Bit 4	R	DS3LOF20V	X
Bit 3	R	DS3LOF19V	X
Bit 2	R	DS3LOF18V	X
Bit 1	R	DS3LOF17V	X
Bit 0	R	DS3LOF16V	X

This register is used to indicate the current DS3 LOF status.

DS3LOF***x***V

The DS3LOF #***x*** status (DS3LOF***x***V) is logic 1 when the DS3 data stream is in Loss Of Frame state. It is logic 0 when the DS3 data stream is not in Loss of Frame State.

Register 003DH: S/UNI-MACH48 DS3 #32-47 LOF Status

Bit	Type	Function	Default
Bit 15	R	DS3LOF47V	X
Bit 14	R	DS3LOF46V	X
Bit 13	R	DS3LOF45V	X
Bit 12	R	DS3LOF44V	X
Bit 11	R	DS3LOF43V	X
Bit 10	R	DS3LOF42V	X
Bit 9	R	DS3LOF41V	X
Bit 8	R	DS3LOF40V	X
Bit 7	R	DS3LOF39V	X
Bit 6	R	DS3LOF38V	X
Bit 5	R	DS3LOF37V	X
Bit 4	R	DS3LOF36V	X
Bit 3	R	DS3LOF35V	X
Bit 2	R	DS3LOF34V	X
Bit 1	R	DS3LOF33V	X
Bit 0	R	DS3LOF32V	X

This register is used to indicate the current DS3 LOF status.

DS3LOF***x***V

The DS3LOF #***x*** status (DS3LOF***x***V) is logic 1 when the DS3 data stream is in Loss Of Frame state. It is logic 0 when the DS3 data stream is not in Loss of Frame State.

Register 003EH: S/UNI-MACH48 Device ID #1

Bit	Type	Function	Default
Bit 15	R	DEVICEID[15]	0
Bit 14	R	DEVICEID[14]	1
Bit 13	R	DEVICEID[13]	1
Bit 12	R	DEVICEID[12]	1
Bit 11	R	DEVICEID[11]	0
Bit 10	R	DEVICEID[10]	0
Bit 9	R	DEVICEID[9]	1
Bit 8	R	DEVICEID[8]	1
Bit 7	R	DEVICEID[7]	1
Bit 6	R	DEVICEID[6]	0
Bit 5	R	DEVICEID[5]	0
Bit 4	R	DEVICEID[4]	1
Bit 3	R	DEVICEID[3]	0
Bit 2	R	DEVICEID[2]	0
Bit 1	R	DEVICEID[1]	0
Bit 0	R	DEVICEID[0]	0

This register is used to allow software to determine the identity of this device.

DEVICEID[15:0]

For the S/UNI-MACH48 device, these bits will be read as the hexadecimal number 7390.

Register 003FH: S/UNI-MACH48 Device ID #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	DEVICEREV[3]	X
Bit 2	R	DEVICEREV[2]	X
Bit 1	R	DEVICEREV[1]	X
Bit 0	R	DEVICEREV[0]	X

This register is used to allow software to determine the revision number of this device.

DEVICEREV[3:0]

The Device Revision bits (DEVICEREV[3:0] can be read by software to find the device revision of this part. “0010” corresponds to revision C.

Register 0040H: RXPHY Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	RSXPAUSE[1]	0
Bit 12	R/W	RSXPAUSE[0]	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	RXPRST	1

RXPRST

The RXPRST bit is used to reset the RXPHY circuitry. When RXPRST is set to logic zero, the RXPHY operates normally. When RXPRST is set to logic one, the RXPHY ignores all pin inputs but the register bits may be accessed for purposes of initialization. The RXPHY deasserts all outputs until a logic zero is written to RXPRST.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is generated by the RXPHY for the UL3 or POS L3 interface. When set to logic 1, odd parity is generated. When set to logic 0, even parity is generated. This bit is global and affects all PHY channels.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

RSXPAUSE[1:0]

RSXPAUSE bits control the number of additional clocks to pause between transfers as per POS-PHY Level 3 specification. These bits are effective in PL3 mode only. The default setting is '00' meaning the minimal pause of 2 dead cycles and one RSX cycle will occur between transfers resulting in maximum bandwidth usage. As setting of '01' indicates 1 additional clock between transfers and a setting of '10' indicates 2 additional clocks between transfers. The setting of '11' is reserved. Note that the additional clock cycles are inserted in the RSX pulse, effectively widening the pulse. These bits cannot be changed during operation and can only be changed when RXPRST is logic one.

Register 0041H: RXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

In UTOPIA, the RENB was detected as being deasserted before appropriate time at end of the cell transfer. The cell will continue to be transferred as per the Utopia Level 3 specification, but this indicates that there may be a configuration mismatch between the RXPHY and the downstream device. A possible cause is the incorrect setting of the size of the cell expected by this interface. The RUNTCELLI bit is cleared when it is read.

Register 0042H: RXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RUNTCELLE	0

RUNTCELLE

The RUNTCELLE bit is used to enable RUNTCELLI signal to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Register 0043H: RXPHY Indirect Burst Size

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CONFIG_RWB	0
Bit 13	R/W	PHY_ADDR[5]	0
Bit 12	R/W	PHY_ADDR[4]	0
Bit 11	R/W	PHY_ADDR[3]	0
Bit 10	R/W	PHY_ADDR[2]	0
Bit 9	R/W	PHY_ADDR[1]	0
Bit 8	R/W	PHY_ADDR[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	BURST_SIZE[3]	X
Bit 2	R/W	BURST_SIZE[2]	X
Bit 1	R/W	BURST_SIZE[1]	X
Bit 0	R/W	BURST_SIZE[0]	X

The RXPHY Indirect Burst Size register is an indirect address and data register. The register is used only in POS-PHY mode of operation.

BURST_SIZE[3:0]

The BURST_SIZE data register is provided to program the allowable burst size for the PHY. The size of a burst is BURST_SIZE + 1. For example, a BURST_SIZE[3:0] = “0000” indicates a burst size of one block. A block is equal to 16 bytes and takes 4 clocks to transfer. The 4 bits of Burst Size allow the maximum burst to be 16 blocks (256 bytes), per PHY. This register is used only in POS-PHY L3 mode. BURST_SIZE[3:0] defaults to “0011”, but this default value is only observable if RFCLK is toggling. See the bit description for DT (register 005AH) and section 14.16 for more details on setting these bits.

PHY_ADDR[5:0]

The PHY_ADDR bits are an indirect address that is used with BURST_SIZE data. The two allow indirect address reads and writes using a small amount of external address space. The PHY_ADDR is used with CONFIG_RWB and BUSY to command reads and writes. Valid values for PHY_ADDR[5:0] are from 0 to 2FH.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data for PHY_ADDR and will be placed in the BURST_SIZE register. A value of '0' means that a write of the information in BURST_SIZE will be performed for PHY channel address PHY_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0044H: RXPHY Calendar Length

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	CALENDAR_LENGTH[6]	0
Bit 5	R/W	CALENDAR_LENGTH[5]	0
Bit 4	R/W	CALENDAR_LENGTH[4]	0
Bit 3	R/W	CALENDAR_LENGTH[3]	0
Bit 2	R/W	CALENDAR_LENGTH[2]	0
Bit 1	R/W	CALENDAR_LENGTH[1]	0
Bit 0	R/W	CALENDAR_LENGTH[0]	0

CALENDAR_LENGTH[6:0]

The CALENDAR_LENGTH register is provided to program the length of calendar used for servicing up to a maximum of 128 entries. (See Register 0045H RXPHY Calendar Indirect Address Data). The number of entries is equal to CALENDAR_LENGTH + 1.

Register 0045H: RXPHY Calendar Indirect Address Data

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CALENDAR_ADDR[6]	0
Bit 13	R/W	CALENDAR_ADDR[5]	0
Bit 12	R/W	CALENDAR_ADDR[4]	0
Bit 11	R/W	CALENDAR_ADDR[3]	0
Bit 10	R/W	CALENDAR_ADDR[2]	0
Bit 9	R/W	CALENDAR_ADDR[1]	0
Bit 8	R/W	CALENDAR_ADDR[0]	0
Bit 7	R/W	CONFIG_RWB	0
Bit 6		Unused	X
Bit 5	R/W	CALENDAR_DATA[5]	X
Bit 4	R/W	CALENDAR_DATA[4]	X
Bit 3	R/W	CALENDAR_DATA[3]	X
Bit 2	R/W	CALENDAR_DATA[2]	X
Bit 1	R/W	CALENDAR_DATA[1]	X
Bit 0	R/W	CALENDAR_DATA[0]	X

The RXPHY Calendar Indirect Address Data register is an indirect address and data register. The register is used in POS mode of operation.CALENDAR_DATA[5:0]

The CALENDAR_DATA register is provided to program the PHY address number to be serviced in the calendar sequence. The calendar consists of a maximum of 128 entries where the CALENDAR_ADDR is used to access one of the 128 (or less) entries to either write or read CALENDAR_DATA. CALENDAR_DATA is the PHY address to be serviced during the sequence associated with CALENDAR_ADDR. The length of the calendar is set in the RXPHY Calendar Length register. CALENDAR_DATA[5:0] defaults to “000000”, but this default value is only observable if RFCLK is toggling.

CALENDAR_ADDR[6:0]

The CALENDAR_ADDR register is an indirect address register that is used with CALENDAR_DATA register. The two registers together allow indirect address reads and writes using a small amount of external address space. The CALENDAR_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data at CALENDAR_ADDR and will be placed in the CALENDAR_DATA register. A value of '0' means that a write of the information in CALENDAR_DATA will be performed at address CALENDAR_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0046H: RXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	POS_FIELD[7]	0
Bit 14	R/W	POS_FIELD[6]	0
Bit 13	R/W	POS_FIELD[5]	0
Bit 12	R/W	POS_FIELD[4]	0
Bit 11	R/W	POS_FIELD[3]	0
Bit 10	R/W	POS_FIELD[2]	0
Bit 9	R/W	POS_FIELD[1]	0
Bit 8	R/W	POS_FIELD[0]	1
Bit 7	R/W	ATM_FIELD[7]	0
Bit 6	R/W	ATM_FIELD[6]	0
Bit 5	R/W	ATM_FIELD[5]	0
Bit 4	R/W	ATM_FIELD[4]	0
Bit 3	R/W	ATM_FIELD[3]	0
Bit 2	R/W	ATM_FIELD[2]	0
Bit 1	R/W	ATM_FIELD[1]	0
Bit 0	R/W	ATM_FIELD[0]	0

The RXPHY Data Type Field is used in POS-PHY L3 mode of operation only and is provided as a means to identify the type of traffic, ATM or packet, being sent over the POS-PHY L3 interface. Selection of ATM and packet PHYs is done using the POS_SEL bits in the RXSDQ FIFO Indirect Configuration register.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cell transfers over the POS-PHY L3 interface. When the outgoing data is an ATM cell, then the ATM_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (ie. when RSX is logic 1).

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data transfers over the POS-PHY L3 interface. When the outgoing data is of type packet, then the POS_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (ie. when RSX is logic 1).

Register 0048H: TXPHY Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved0	0
Bit 8	R/W	Reserved1	0
Bit 7	R/W	TPAHOLD	0
Bit 6	R/W	INBANDADDR	1
Bit 5	R/W	Reserved0	0
Bit 4	R/W	Reserved0	0
Bit 3	R/W	PARERREN	0
Bit 2	R/W	Reserved0	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	TXPRST	1

TXPRST

The TXPRST bit is used to reset the TXPHY circuitry. When TXPRST is set to logic zero, the TXPHY operates normally. When TXPRST is set to logic one, the TXPHY ignores all pin inputs but the registers may be accessed for purposes of initialization. The TXPHY deasserts all outputs until a logic zero is written to TXPRST.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is generated by the TXPHY. When set to logic 1, odd parity is expected. When set to logic 0, even parity is expected. This bit is global and affects all PHY channels.

PARERREN

When set to logic 1, PARERREN will enable the TXPHY to pass an error signal to the TXSDQ upon detection of a parity error. This will cause the packet to be aborted by the cell processor. This bit has no effect on ATM cells with parity errors. If PARERREN is set to logic 0, parity errors will not disrupt the transmission of a packet. They will only cause an interrupt (if enabled).

INBANDADDR

The INBANDADDR bit is used only in POS-PHY L3 mode to indicate whether the in-band address is expected on the interface. This bit is useful in single PHY applications where the in-band addressing is optional (address 0 is assumed) and the Link Layer device does not send an address in band since there is only one PHY. This bit can only be changed when TXPRST is logic 1. Note that regardless of the value of INBANDADDR, PTPA will reflect the address value on the TADR pins.

TPAHOLD

The TPAHOLD bit is used only in POS-PHY mode to control the STPA and PTPA signal response time.

TPAHOLD can only be set to logic 1 if the upstream device is working in burst-transfer mode (TENB is deasserted between each burst). In this mode, the PTPA (if polled) for the channel will deassert within 1 clock cycle of the write which causes the FIFO fill level to cross its buffer available threshold.

When TPAHOLD is set to logic 0, PTPA (if polled) for the channel will deassert 5 clock cycles after the write which causes the FIFO fill level to cross its buffer available threshold.

See Section 15.8.2 for more details.

This bit cannot be changed during operation and can only be changed when TXPRST is logic one.

Reserved0

The Reserved0 bits must be set to logic 0 for proper operation.

Reserved1

The Reserved1 bit must be set to logic 1 for proper operation.

Register 0049H: TXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TDTFERRI	X
Bit 1	R	TPARERRI	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

The RUNTCELLI bit indicates that TENB was detected as being deasserted before the end of the cell transfer when operating in Utopia L3 mode. This will result in a partial cell transfer and an erred cell will passed to the TXSDQ. Possible causes are incorrect setting in the size of the cell expected by this interface. The RUNTCELLI bit is cleared when this register is read.

TPARERRI

The TPARERR bit is used to indicate that a Parity Error was observed on the incoming TDAT bus since the last time the interrupt was read. The packet will be marked erred and sent on to the TXSDQ. ATM cell transmission is not affected by parity errors. The TPARERRI bit is cleared when this register is read.

TDTFERRI

The TDTFERR bit is used to indicate that a Data Field mismatch was observed on the incoming TDAT[31:24] bus compared to the ATM/packet selection for that PHY configuration (selection done using the POS_SEL bits in the TXSDQ FIFO Indirect Configuration register). This bit is cleared on microprocessor read.

Register 004AH: TXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	TDTFERRE	0
Bit 1	R/W	TPARERRE	0
Bit 0	R/W	RUNTCELLE	0

RUNTCELLE

The RUNTCELLE bit is used to enable the detection of the runt cell condition (RUNTCELLI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

TPARERRE

The TPARERRE bit is used to enable the detection of a parity error (TPARERRI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

TDTFERRE

The TDTFERRE bit is used to enable the TDFTERRI interrupt status bit to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Register 004BH: TXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	POS_FIELD[7]	0
Bit 14	R/W	POS_FIELD[6]	0
Bit 13	R/W	POS_FIELD[5]	0
Bit 12	R/W	POS_FIELD[4]	0
Bit 11	R/W	POS_FIELD[3]	0
Bit 10	R/W	POS_FIELD[2]	0
Bit 9	R/W	POS_FIELD[1]	0
Bit 8	R/W	POS_FIELD[0]	1
Bit 7	R/W	ATM_FIELD[7]	0
Bit 6	R/W	ATM_FIELD[6]	0
Bit 5	R/W	ATM_FIELD[5]	0
Bit 4	R/W	ATM_FIELD[4]	0
Bit 3	R/W	ATM_FIELD[3]	0
Bit 2	R/W	ATM_FIELD[2]	0
Bit 1	R/W	ATM_FIELD[1]	0
Bit 0	R/W	ATM_FIELD[0]	0

The TXPHY Data Type Field is used in POS-PHY L3 mode of operation only and is provided as a means to identify the type of traffic, ATM or packet, being sent over the POS-PHY L3 interface. Selection of ATM and packet PHYs is done using the POS_SEL bit in the TXSDQ FIFO Indirect Configuration register.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify an ATM cell being transferred over the POS-PHY L3 interface. When the incoming data is of type ATM cell, then the value of TDAT[31:24] at the cycle in which the in-band address is inserted on TDAT[5:0] (ie. when TSX = 1) should match ATM_FIELD[7:0]. Otherwise, an interrupt is signaled to indicate a data type mismatch.

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data being transferred over the POS-PHY L3 interface. When the incoming data is of type packet, then the value of TDAT[31:24] at the cycle in which the in-band address is inserted on TDAT[5:0] (ie. When TSX = 1) should match POS_FIELD[7:0]. Otherwise, an interrupt is signaled to indicate a data type mismatch.

Register 0050H: RXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	RXSDQTIP	X
Bit 0	R/W	SDQRST	1

SDQRST

This bit is used to reset the RXSDQ. The RXSDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

RXSDQTIP

The RXSDQTIP bit indicates that the RXSDQ counters are in the process of being transferred to their holding registers. A transfer is initialized by writing to the S/UNI-MACH48 Global Performance Monitor Update register (0000H). RXSDQTIP is logic 1 while a transfer is in progress. It returns to logic 0 when the transfer is completed.

Register 0051H: RXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	OFLE	0

OFLE

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

Reserved

This bit should be set to logic 0 for proper operation.

Register 0053H: RXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	OFLI	X

OFLI

This bit is set when any of the configured FIFOs overflows. The FIFO number that caused this interrupt is available in OFL_FIFO[5:0]. This bit is cleared when read by the user. This overflow indication can be set by each byte of a cell or packet that is being written into a full FIFO, so multiple interrupts can be generated for the same cell or packet if the interrupt indication is read too quickly.

OFL_FIFO[5:0]

These bits are used to indicate the FIFO number which overflowed and set the OFLI indication. These bits are valid only when OFLI is logic 1. If multiple FIFOs overflow before this interrupt is serviced, OFL_FIFO[5:0] will indicate the FIFO that first overflowed.

Register 0054H: RXSDQ FIFO EOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	Reserved	X
Bit 12	R	Reserved	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	Unused	X

Reserved

These bits are used only for PMC test purposes. They are not used in normal operating mode.

Register 0055H: RXSDQ FIFO SOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	Reserved	X
Bit 12	R	Reserved	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	Reserved	X

Reserved

These bits are used only for PMC test purposes. They are not used in normal operating mode.

Register 0058H: RXSDQ FIFO Indirect Address

This is an indirect register that is used to specify the address of the FIFO that the user is setting up or reading the setup for. FIFOs need to be configured according to a set of rules defined in Sections 14.13 and 14.14. This register is the common address used for the four registers including this one: RXSDQ FIFO Indirect Configuration, RXSDQ FIFO Indirect Buffer Available and Data Available Thresholds, and RXSDQ FIFO Indirect Cells and Packets Count. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information. Note that this read and write-back procedure must be performed for each of the above registers, even if its contents are not changing.

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	0
Bit 12	R	EMPTY	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

PHYID[5:0]

This is a 6-bit number that is used to describe the current FIFO being addressed by the rest of the FIFO setup registers – the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count. The range of FIFO numbers that can be used is 0 to 2FH. The PHYID[5:0] value is equivalent to the Channel Number assigned by the RCAS-12 blocks (see Section 12.5).

EMPTY

This read-only bit indicates if the **requested FIFO** is empty. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty.

FLUSH

This is a write-only bit used to discard all the current data in a specified FIFO. This should typically be used if a non-empty FIFO needs to be reconfigured. If this bit is manually set, it must also be manually cleared before enabling the specified FIFO. Note that this bit can only be set or cleared when RWB = 0 and PHYID is used to select the correct PHY since it is an indirect access bit.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers FIFO Indirect Configuration, FIFO Indirect Buffer Available Threshold, FIFO Indirect Data Available Threshold, and FIFO Indirect Cells and Packets Count. When this bit is set to 0, the user is writing the configuration of a FIFO. The RXSDQ latches in the data in the FIFO Indirect Configuration, FIFO Indirect Buffer Available Threshold, FIFO Indirect Data Available Threshold, and FIFO Indirect Cells and Packets Count registers.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the information for the FIFO is now available in the FIFO Indirect Configuration, FIFO Indirect Buffer Available Threshold, FIFO Indirect Data Available Threshold, and FIFO Indirect Cells and Packets Count registers.

Register 0059H: RXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	0
Bit 5		Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

BLOCK_PTR[4:0]

This is a 5-bit number that is calculated and programmed by the user based on the number of PHYs, the size of each FIFO, and total number of FIFOs required by the system. The rules governing this calculation are set in Sections 14.13 and 14.14.

FIFO_BS[1:0]

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY. The values to be programmed for each of these sizes are given in Table 54.

FIFO_NUMBER[5:0]

This is a 6-bit internal FIFO number that is used to associate a given PHY ID with a FIFO. This number can be in one of 4 ranges, and is unique for each PHY. The rules governing this calculation are set in Sections 14.13 and 14.14.

POS_SEL

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs. Note that a packet FIFO can process ATM cell traffic, but without enforcing cell size. When POS_SEL=0, there are 5 dead cycles between cell transfers, resulting in a 98.2% bandwidth for a 100 MHz clock (102 MHz clock is sufficient for 100% bandwidth). When POS_SEL=1, there are only 2 dead cycles between transfers, so full ATM bandwidth is possible with a 91 MHz clock. Thus, it is recommended that POS_SEL be set to logic 0 only for UL3 applications.

ENABLE

This bit enables individual FIFOs. Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but continues to assert Data Available internally until it is drained completely. In order to reconfigure FIFOs during operation, they need to be disabled first.

Register 005AH: RXSDQ FIFO Indirect Data Available Threshold

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register is used to set the Data Available Threshold for each of the FIFOs. This threshold is explained in Section **14.16**. The FIFOs need not be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again.

Reserved

The Reserved bits should be set to their default values for proper operation.

DT[7:0]

These bits specify the Data Available threshold for the FIFO selected by the FIFO Indirect Address register PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is DT[7:0] +1 = 16. This number should be a standard fraction of the FIFO size in blocks. In the case of UL3 ATM FIFOs, this number must be set to a value of DT[7:0] = 3 (ATM cells are 4 Blocks long).

For PL3 interfaces, RVAL will be asserted for the channel (PHYID[5:0]) when the FIFO depth is equal to or greater than DT[7:0] + 1 or when an EOP is in the FIFO.

For UL3 ATM interfaces, RCA will be asserted for the channel (PHYID[5:0]) when the FIFO depth is equal to or greater than one cell (DT[7:0] + 1 = 4 blocks = 1 cell).

See the bit description for BURST_SIZE (register 0043H) and Section 14.16 for more details on programming the DT settings.

Register 005BH: RXSDQ FIFO Indirect Cell and Packet Count

This register is used to read the 4-bit non-saturating FIFO counters for the enabled FIFOs, which count the number of ATM cells or packets accepted by the FIFO. The counts are latched when the register 0000H of the S/UNI-MACH48 is written to. These counters are then reset, and the latched values can be read individually through this register.

The counters provided by the RXSDQ are purely for diagnostic purposes. They should be ignored in normal operations.

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

COUNT[3:0]

These read-only bits hold the last sampled count for the FIFO requested for in FIFO Indirect Address register PHYID[5:0] bits. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over.

Register 005CH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[15]	X
Bit 14	R	ACOUNT[14]	X
Bit 13	R	ACOUNT[13]	X
Bit 12	R	ACOUNT[12]	X
Bit 11	R	ACOUNT[11]	X
Bit 10	R	ACOUNT[10]	X
Bit 9	R	ACOUNT[9]	X
Bit 8	R	ACOUNT[8]	X
Bit 7	R	ACOUNT[7]	X
Bit 6	R	ACOUNT[6]	X
Bit 5	R	ACOUNT[5]	X
Bit 4	R	ACOUNT[4]	X
Bit 3	R	ACOUNT[3]	X
Bit 2	R	ACOUNT[2]	X
Bit 1	R	ACOUNT[1]	X
Bit 0	R	ACOUNT[0]	X

Register 005DH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[31]	X
Bit 14	R	ACOUNT[30]	X
Bit 13	R	ACOUNT[29]	X
Bit 12	R	ACOUNT[28]	X
Bit 11	R	ACOUNT[27]	X
Bit 10	R	ACOUNT[26]	X
Bit 9	R	ACOUNT[25]	X
Bit 8	R	ACOUNT[24]	X
Bit 7	R	ACOUNT[23]	X
Bit 6	R	ACOUNT[22]	X
Bit 5	R	ACOUNT[21]	X
Bit 4	R	ACOUNT[20]	X
Bit 3	R	ACOUNT[19]	X
Bit 2	R	ACOUNT[18]	X
Bit 1	R	ACOUNT[17]	X
Bit 0	R	ACOUNT[16]	X

ACOUNT[31:0]

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the RXSDQ. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over and starts counting again from 0.

Register 005EH: RXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the RXSDQ due to FIFO overflows. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over and starts counting again from 0.

Register 0060H: TXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	TXSDQTIP	X
Bit 0	R/W	SDQRST	1

SDQRST

This bit is used to reset the TXSDQ. The TXSDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

TXSDQTIP

The TXSDQTIP bit indicates that the TXSDQ counters are in the process of being transferred to their holding registers. A transfer is initialized by writing to the S/UNI-MACH48 Global Performance Monitor Update register (0000H). TXSDQTIP is logic 1 while a transfer is in progress. It returns to logic 0 when the transfer is completed.

Register 0061H: TXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	SOPE	0
Bit 1	R/W	EOPE	0
Bit 0	R/W	OFLE	0

OFLE

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

OFLE

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

EOPE

When this bit is set to 1, bad EOP signals cause the INTB output to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

SOPE

When this bit is set to 1, bad SOP signals cause the INTB output to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

Reserved

This bit should be set to logic 0 for proper operation.

Register 0063H: TXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	OFLI	X

OFLI

This bit is set when any of the configured FIFOs overflows. The FIFO number that caused this interrupt is available in OFL_FIFO[5:0]. This bit is cleared when read by the user. This overflow indication can be set by each byte of a cell or packet that is being written into a full FIFO, so multiple interrupts can be generated for the same cell or packet if the interrupt indication is read too quickly.

OFL_FIFO[5:0]

These bits are used to indicate the FIFO number which overflowed and set the OFLI indication. These bits are valid only when OFLI is logic 1. If multiple FIFOs overflow before this interrupt is serviced, OFL_FIFO[5:0] will indicate the FIFO that first overflowed.

Register 0064H: TXSDQ FIFO EOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	EOP_FIFO[5]	X
Bit 12	R	EOP_FIFO[4]	X
Bit 11	R	EOP_FIFO[3]	X
Bit 10	R	EOP_FIFO[2]	X
Bit 9	R	EOP_FIFO[1]	X
Bit 8	R	EOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	EOPI	X

EOPI

This bit is set when two EOPs arrive consecutively on the same FIFO without being separated by a SOP. The FIFO number that caused the interrupt is available in EOP_FIFO[5:0]. This bit is cleared when read by the user.

EOP_FIFO[5:0]

These bits are used to indicate the FIFO which observed a bad EOP sequence and set the EOPI indication. These bits are valid only when EOPI is logic 1. If multiple bad EOP sequences occur before this interrupt is serviced, EOP_FIFO[5:0] will indicate the FIFO that first observed the bad EOP sequence.

Register 0065H: TXSDQ FIFO SOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	SOP_FIFO[5]	X
Bit 12	R	SOP_FIFO[4]	X
Bit 11	R	SOP_FIFO[3]	X
Bit 10	R	SOP_FIFO[2]	X
Bit 9	R	SOP_FIFO[1]	X
Bit 8	R	SOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	SOPI	X

SOPI

This bit is set when two SOPs arrive consecutively on the same FIFO without being separated by a EOP. The FIFO number that caused the interrupt is available in SOP_FIFO[5:0]. This bit is cleared when read by the user.

SOP_FIFO[5:0]

These bits are used to indicate the FIFO which observed a bad SOP sequence and set the SOPI indication. These bits are valid only when SOPI is logic 1. If multiple bad SOP sequences occur before this interrupt is serviced, SOP_FIFO[5:0] will indicate the FIFO that first observed the bad SOP sequence.

Register 0068H: TXSDQ FIFO Indirect Address

This is an indirect register that is used to specify the address of the FIFO that the user is setting up or reading the setup for. FIFOs need to be configured according to a set of rules defined in Sections 14.13 and 14.14. This register is the common address used for the four registers including this one: TXSDQ FIFO Indirect Configuration, TXSDQ FIFO Indirect Buffer Available and Data Available Thresholds, and TXSDQ FIFO Indirect Cells and Packets Count. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information. Note that this read and write-back procedure must be performed for each of the above configuration registers, even if its contents are not changing.

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	0
Bit 12	R	EMPTY	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

PHYID[5:0]

This is a 6-bit number that is used to describe the current FIFO being addressed by the rest of the FIFO setup registers – the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count. The range of FIFO numbers that can be used is 0 to 2FH. The PHYID[5:0] value is equivalent to the Channel Number assigned by the TCAS-12 blocks (see Section 12.6).

EMPTY

This read-only bit indicates if the **requested FIFO** is empty. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty.

FLUSH

This is a write-only bit used to discard all the current data in a specified FIFO. This should typically be used if a non-empty FIFO needs to be reconfigured. If this bit is manually set, it must also be manually cleared before enabling the specified FIFO. Note that this bit can only be set or cleared when RWB = 0 and PHYID is used to select the correct PHY since it is an indirect access bit.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count. When this bit is set to 0, the user is writing the configuration of a FIFO. The TXSDQ latches in the data in the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count registers.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the information for the FIFO is now available in the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count registers.

Register 0069H: TXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	0
Bit 5		Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

BLOCK_PTR[4:0]

This is a 5-bit number that is calculated and programmed by the user based on the number of PHYs, the size of each FIFO, and total number of FIFOs required by the system. The rules governing this calculation are set in Sections 14.13and 14.14.

FIFO_BS[1:0]

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY. The values to be programmed for each of these sizes are given in Table 54.

FIFO_NUMBER[5:0]

This is a 6-bit internal FIFO number that is used to associate a given PHY ID with a FIFO. This number can be in one of 4 ranges, and is unique for each PHY. The rules governing this calculation are set in Sections 14.13 and 14.14.

POS_SEL

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs

ENABLE

This bit enables individual FIFOs. Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but continues to assert Data Available internally until it is drained completely. In order to reconfigure FIFOs during operation, they need to be disabled first.

Register 006AH: TXSDQ FIFO Indirect Data and Buffer Available Thresholds

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	BT[4]	0
Bit 3	R/W	BT[3]	0
Bit 2	R/W	BT[2]	0
Bit 1	R/W	BT[1]	1
Bit 0	R/W	BT[0]	1

This register is used to set the Data and Buffer Available Thresholds for each of the FIFOs.

The Buffer Available Threshold is explained in Section **14.15**. The FIFOs need not be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again.

The Data Available threshold is explained in Section **14.16**. The FIFOs need not be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again.

BT[4:0]

These bits specify the Buffer Available threshold for the FIFO specified in PHYID[5:0] bits in the FIFO Indirect Address register. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to BT[4:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is BT[4:0] +1 = 32. This number should be a standard fraction of the FIFO size in blocks. In the case of UL3 ATM FIFOs, this number must be set to a value of BT[4:0] = 3 since ATM cells are 4 blocks in size. PL3 FIFOs may follow the guidelines described in section 14.16.

DT[7:0]

These bits specify the Data Available threshold for the FIFO selected by the FIFO Indirect Address register PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is DT[7:0] +1 = 192. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number must be set to a value of DT[7:0] = 3 (ATM cells are 4 Blocks long).

The DT[7:0] threshold sets the level at which the cell/packet processors (TCFP or TTDP) blocks can begin transmission of a cell or packet. Once transmission of a cell or packet begins, it cannot be stopped so this threshold should be set to a value which guarantees that the Utopia/POS-PHY interface can write to the FIFO in due time to prevent FIFO underruns. For packet data, it is recommended that DT[7:0] be set to a larger value about equal to 1/2 or 2/3 the size of the FIFO.

Register 006BH: TXSDQ FIFO Indirect Cells and Packets Count

This register is used to read the 4-bit non-saturating FIFO counters for the enabled FIFOs, which count the number of ATM cells or packets accepted by the FIFO. The counts are latched when the register 0000H of the S/UNI-MACH48 is written to. These counters are then reset, and the latched values can be read individually through this register.

The counters provided by the TXSDQ are purely for diagnostic purposes. They should be ignored in normal operations.

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

COUNT[3:0]

These read-only bits hold the last sampled count for the FIFO requested for in FIFO Indirect Address register PHYID[5:0] bits. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over.

Register 006CH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[15]	X
Bit 14	R	ACOUNT[14]	X
Bit 13	R	ACOUNT[13]	X
Bit 12	R	ACOUNT[12]	X
Bit 11	R	ACOUNT[11]	X
Bit 10	R	ACOUNT[10]	X
Bit 9	R	ACOUNT[9]	X
Bit 8	R	ACOUNT[8]	X
Bit 7	R	ACOUNT[7]	X
Bit 6	R	ACOUNT[6]	X
Bit 5	R	ACOUNT[5]	X
Bit 4	R	ACOUNT[4]	X
Bit 3	R	ACOUNT[3]	X
Bit 2	R	ACOUNT[2]	X
Bit 1	R	ACOUNT[1]	X
Bit 0	R	ACOUNT[0]	X

Register 006DH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[31]	X
Bit 14	R	ACOUNT[30]	X
Bit 13	R	ACOUNT[29]	X
Bit 12	R	ACOUNT[28]	X
Bit 11	R	ACOUNT[27]	X
Bit 10	R	ACOUNT[26]	X
Bit 9	R	ACOUNT[25]	X
Bit 8	R	ACOUNT[24]	X
Bit 7	R	ACOUNT[23]	X
Bit 6	R	ACOUNT[22]	X
Bit 5	R	ACOUNT[21]	X
Bit 4	R	ACOUNT[20]	X
Bit 3	R	ACOUNT[19]	X
Bit 2	R	ACOUNT[18]	X
Bit 1	R	ACOUNT[17]	X
Bit 0	R	ACOUNT[16]	X

ACOUNT[31:0]

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the TXSDQ. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over and starts counting again from 0.

Register 006EH: TXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the TXSDQ due to FIFO overflows. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over and starts counting again from 0.

12.1 RCFP Register Summary

There are 4 RCFP blocks in the S/UNI-MACH48 device. Their base addresses (RCFP_BASE) are: 0070H, 0080H, 0090H, and 00A0H. The RCFP is the receive Cell/Packet processor for STS-12c and STS-48c channels.

Each RCFP block is dedicated to a range of timeslots (system side) and channel numbers (system side) for STS-12c and STS-48c data streams.

The RCFP block residing in the least significant RCFP_BASE address location is dedicated to all the timeslots shown in Table 53 and to the first row of timeslots in STS-48c/STM-16c mode (RX48c = 1) and in Table 52 when not in STS-48c/STM-16c mode (RX48C = 0). This RCFP block is also dedicated to channel 0.

The RCFP block residing in the 2nd least significant RCFP_BASE address location is dedicated to the second row of the timeslot map in Table 52 and to the channel number 12. This RCFP block is not used when in STS-48c/STM-16c mode (RX48C = 1).

The RCFP block residing in the 3rd least significant RCFP_BASE address location is dedicated to the third row of the timeslot map in Table 52 and to the channel number 24. This RCFP block is not used when in STS-48c/STM-16c mode (RX48C = 1).

The RCFP block residing in the most significant RCFP_BASE address location is dedicated to the bottom row of the timeslot map in Table 52 and to the channel number 36. This RCFP block is not used when in STS-48c/STM-16c mode (RX48C = 1).

Register RCFP_BASE + 0H: RCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	POS_SEL	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	STRIP_SEL	0
Bit 7	R/W	DELINDIS	0
Bit 6	R/W	IDLEPASS	0
Bit 5	R/W	CRCPASS	0
Bit 4	R/W	CRC_SEL[1]	1
Bit 3	R/W	CRC_SEL[0]	1
Bit 2	R/W	RXOTYPB	0
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the RCFP. When PROV is logic 0, the RCFP ATM and packet processors are disabled and will not transfer any valid data to the Receive FIFO interface. When PROV is logic 1, the RCFP ATM or packet processor is enabled and will process data presented to it and transfer data to the Receive FIFO (RXSDQ).

DESCRMBL

The DESCRMBL bit controls the descrambling of the packet or ATM cell payload with the polynomial $x^{43} + 1$. When DESCRMBL is set to logic 0, frame or cell payload descrambling is disabled. When DESCRMBL is set to logic 1, payload descrambling is enabled.

RXOTYPB

The RXOTYPB bit determines if an incoming alarm signal (from IPAIS[x] if RHPP_EN=0, or if path AIS or loss-of-pointer is detected by the RHPP if RHPP_EN=1) will stop a packet by simply asserting EOP, (RXOTYPB set to logic 1), or by asserting both EOP and ERR, (RXOTYPB set to logic 0). When RXOTYPB is set to logic 1, premature termination of the packet will result in that packet failing a FCS check.

This bit is only valid when in POS mode. In ATM mode the RCFP will finish processing any cell in progress and then stop until the alarm signal is cleared.

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, after byte destuffing and descrambling.

Table 14 Functionality of the CRC_SEL[1 0] Register Bits

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS verification
01	Reserved	Reserved
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

CRCPASS

The CRCPASS bit controls the dropping of cells and packets based on the detection of a CRC error. When in ATM mode and when CRCPASS is a logic 0, cells containing an HCS error are dropped.

When CRCPASS is logic 1, cells are passed to the external FIFO interface regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine will never lose cell delineation.

Regardless of the programming of this bit, ATM cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the DELINDIS bit in this register is set to logic 1.

When in POS mode and CRCPASS is logic 1, then packets with FCS errors are not marked as such and are passed to the external FIFO interface as if no FCS error occurred. When CRCPASS is logic 0, then packets with FCS errors are marked with ERR.

IDLEPASS

The IDLEPASS bit controls the function of the ATM Idle Cell filter. It is only valid when in ATM mode. When IDLEPASS is written with logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is enabled, the Idle Cell Header Pattern and Mask register bits are ignored. The default state of this bit and the bits in the RCFP Idle Cell Header and Mask Register enable the dropping of Idle cells.

DELINDIS

The DELINDIS bit can be used to disable HDLC flag alignment and byte de-stuffing. DELINDIS is only valid in POS mode with a POS-PHY Level 3 Interface.

This bit should only be set when Transparent Data Mode is desired. In this mode, data is passed directly from the TelecomBus payload to the POS-PHY Level 3 Bus without flag delineation, byte de-stuffing or CRC checking. Use of Transparent mode requires the use of 64 byte packets, and the CRC_SEL bits must be set to “00”. Note: If byte counting is desired, RBY_MODE must also be set to a logic 1.

STRIP_SEL

The frame check sequence stripping bit (STRIP_SEL) selects the CRC stripping mode of the RCFP. When STRIP_SEL is logic 1, CRC stripping is enabled. When STRIP_SEL is logic 0, CRC stripping is disabled. Note that CRC_SEL[1:0] must not equal "00", (no CRC) for stripping to be enabled. When stripping is enabled the received packet FCS or ATM cell HCS byte(s) are not passed to the RXSDQ FIFO. When STRIP is disabled the received packet FCS are transferred over the FIFO interface. When DELINDIS is enabled, packets and cells are not delineated therefore the value of STRIP_SEL is ignored. **The STRIP_SEL bit must be set to logic 1 if working in ATM mode.**

INVERT

The data inversion bit (INVERT) configures the processor to logically invert the incoming stream before processing it. When INVERT is set to logic 1, the stream is logically inverted before processing. When INVERT is set to logic 0, the stream is not inverted before processing.

POS_SEL

The Packet Over SONET (POS_SEL) bit selects the data type mode of the RCFP. When POS_SEL is logic 1, POS mode is selected. When POS_SEL is logic 0, ATM mode is selected.

Reserved

All Reserved bits must be set to their default values for proper operation.

Register RCFP_BASE + 1H: RCFP Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	OOFV	X
Bit 8	R	LOFV	X
Bit 7	R/W	MINLE	0
Bit 6	R/W	MAXLE	0
Bit 5	R/W	ABRTE	0
Bit 4	R/W	XFERE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	CRCE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOFE	0

LOFE

The LOFE bit enables the generation of an interrupt due to a change in the ATM LCD state. When LOFE is set to logic 1, the interrupt is enabled.

OOFE

The OOFE bit enables the generation of an interrupt due to a change in ATM cell delineation state or packet Idle state. When OOFE is set to logic 1, the interrupt is enabled.

CRCE

The CRCE bit enables the generation of an interrupt due to the detection of an ATM HCS or packet FCS error. When CRCE is set to logic 1, the interrupt is enabled.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RCFP performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set to logic 1, the interrupt is enabled.

LOFV

The LOFV bit gives the ATM Loss of Cell Delineation state. When LOFV is logic 1, an out of cell delineation (LOF) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LOFV is logic 0, the RCFP has been in cell delineation for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[10:0] register bits in the RCFP LCD Count Threshold register.

OOFV

The OOFV bit indicates the ATM cell delineation or packet out of frame alignment state. When OOFV is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries or the packet processor is in Idle state. When OOFV is logic 0, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO or the packet processor is not in Idle state.

Register RCFP_BASE + 2H: RCFP Interrupt Indication and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	MINLI	X
Bit 6	R	MAXLI	X
Bit 5	R	ABRTI	X
Bit 4	R	XFERI	X
Bit 3	R	Reserved	X
Bit 2	R	CRCI	X
Bit 1	R	OOFI	X
Bit 0	R	LOFI	X

LOFI

The LOFI bit is set to logic 1 when there is a change in the loss of cell delineation (LCD) state. The current value of the LCD state is available through the LOFV bit in the RCFP Interrupt Enable register. This bit is set to logic 0 immediately after a read to this register. This interrupt can be masked using LOFE.

OOFI

The OOFI bit is set to logic 1 when the RCFP ATM cell processor enters or exits the SYNC state or the packet processor enters or exits the frame alignment state. The OOFI bit is set to logic 0 immediately after a read to this register. This interrupt can be masked using OOFE.

CRCI

The CRCI bit is set to logic 1 when an ATM HCS or packet FCS error is detected. This bit is set to logic 0 immediately after a read to this register. This interrupt can be masked using CRCE.

Reserved

This bit is not used.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. Logic 1 in this bit position indicates that the RCFP performance monitor counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by a rising edge on the LCLK input. XFERI is set to logic 0 after this register is read. This interrupt can be masked using XFERE.

ABRTI

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE. ABRTI is set to logic 0 after this register is read.

MAXLI

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE. MAXLI is set to logic 0 after this register is read.

MINLI

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. This interrupt can be masked using MINLE. MINLI is set to logic 0 after this register is read.

Register RCFP_BASE + 3H: RCFP Minimum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	0
Bit 10	R/W	MINPL[2]	1
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RBY_MODE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits should be set to their default values for proper operation.

RBY_MODE

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[39:0] counters work. When RBY_MODE is logic 0, RBY_IC[39:0] will count all bytes in received packets (including FCS and Abort bytes) after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[39:0] will count all bytes in received packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid when working in POS mode. Note that in transparent mode (DELINDIS=1), RBY_MODE must be set to logic 1.

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame after destuffing but including the FCS. The default minimum packet length is 4 octets. Values smaller than 4 should not be used.

Register RCFP_BASE + 4H: RCFP Maximum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

MAXPL[16:1]

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum packet length. MAXPL[0] is automatically set to logic 0. Packets larger than this length are marked with an error. This Maximum Packet Length defaults to 1.5 Kbytes. The packet length used here is defined as the number of bytes encapsulated into the POS frame excluding byte stuffing but including the FCS. The default maximum packet length is 1536 octets. The maximum packet length allowed is 128 Kbytes. MAXPL[16:0] should not be set higher than 0x1FFFA or lower than 0x00006 to guarantee correct behaviour.

Register RCFP_BASE + 5H: RCFP LCD Count Threshold

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0]. Note that this value forms a lower bound for the assertion of LCD. In the presence of random data, false headers could be discovered, which would reset the counter and delay the declaration of LCD.

The default value of LCD[10:0] is 360, which translates to the following:

Table 15 Average STS-x cell period versus LCD integration period

Format	Average Cell Period	Default LCD Integration Period
STS-48c	176.9 ns	63.8 μs
STS-12c	707.5 ns	254.7 μs

Register RCFP_BASE + 6H: RCFP Idle Cell Header and Mask

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[3]	0
Bit 10	R/W	PTI[2]	0
Bit 9	R/W	PTI[1]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to this register to select the bits included in the cell filter. Logic 1 in this bit position enables the CLP bit in the pattern register to be compared. Logic 0 causes the masking of the CLP bit. The default enables the register bit comparison.

MPTI[3:0]

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. Logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. Logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bit. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

Note that an all-zeros pattern must be present in the VPI and VCI fields of the Idle cell.

Register RCFP_BASE + 7H: RCFP Receive Byte/Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RBY_IC[15]	X
Bit 14	R	RBY_IC[14]	X
Bit 13	R	RBY_IC[13]	X
Bit 12	R	RBY_IC[12]	X
Bit 11	R	RBY_IC[11]	X
Bit 10	R	RBY_IC[10]	X
Bit 9	R	RBY_IC[9]	X
Bit 8	R	RBY_IC[8]	X
Bit 7	R	RBY_IC[7]	X
Bit 6	R	RBY_IC[6]	X
Bit 5	R	RBY_IC[5]	X
Bit 4	R	RBY_IC[4]	X
Bit 3	R	RBY_IC[3]	X
Bit 2	R	RBY_IC[2]	X
Bit 1	R	RBY_IC[1]	X
Bit 0	R	RBY_IC[0]	X

Register RCFP_BASE + 8H: RCFP Receive Byte/Idle Cell Counter

Bit	Type	Function	Default
Bit 15	R	RBY_IC[31]	X
Bit 14	R	RBY_IC[30]	X
Bit 13	R	RBY_IC[29]	X
Bit 12	R	RBY_IC[28]	X
Bit 11	R	RBY_IC[27]	X
Bit 10	R	RBY_IC[26]	X
Bit 9	R	RBY_IC[25]	X
Bit 8	R	RBY_IC[24]	X
Bit 7	R	RBY_IC[23]	X
Bit 6	R	RBY_IC[22]	X
Bit 5	R	RBY_IC[21]	X
Bit 4	R	RBY_IC[20]	X
Bit 3	R	RBY_IC[19]	X
Bit 2	R	RBY_IC[18]	X
Bit 1	R	RBY_IC[17]	X
Bit 0	R	RBY_IC[16]	X

Register RCFP_BASE + 9H: RCFP Receive Byte/Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	RBY_IC[39]	X
Bit 6	R	RBY_IC[38]	X
Bit 5	R	RBY_IC[37]	X
Bit 4	R	RBY_IC[36]	X
Bit 3	R	RBY_IC[35]	X
Bit 2	R	RBY_IC[34]	X
Bit 1	R	RBY_IC[33]	X
Bit 0	R	RBY_IC[32]	X

RBY_IC[39:0]

When POS mode is selected, the RBY_IC[39:0] bits indicate the number of bytes received within POS frames during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes in the count is controlled by the RBY_MODE register bit. HDLC flags are not counted.

When ATM mode is selected, the RBY_IC[39:0] bits indicate the number of Idle cells received and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

Register RCFP_BASE + AH: RCFP Packet/Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[15]	X
Bit 14	R	RP_RC[14]	X
Bit 13	R	RP_RC[13]	X
Bit 12	R	RP_RC[12]	X
Bit 11	R	RP_RC[11]	X
Bit 10	R	RP_RC[10]	X
Bit 9	R	RP_RC[9]	X
Bit 8	R	RP_RC[8]	X
Bit 7	R	RP_RC[7]	X
Bit 6	R	RP_RC[6]	X
Bit 5	R	RP_RC[5]	X
Bit 4	R	RP_RC[4]	X
Bit 3	R	RP_RC[3]	X
Bit 2	R	RP_RC[2]	X
Bit 1	R	RP_RC[1]	X
Bit 0	R	RP_RC[0]	X

Register RCFP_BASE + BH: RCFP Receive Packet/ATM Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[31]	X
Bit 14	R	RP_RC[30]	X
Bit 13	R	RP_RC[29]	X
Bit 12	R	RP_RC[28]	X
Bit 11	R	RP_RC[27]	X
Bit 10	R	RP_RC[26]	X
Bit 9	R	RP_RC[25]	X
Bit 8	R	RP_RC[24]	X
Bit 7	R	RP_RC[23]	X
Bit 6	R	RP_RC[22]	X
Bit 5	R	RP_RC[21]	X
Bit 4	R	RP_RC[20]	X
Bit 3	R	RP_RC[19]	X
Bit 2	R	RP_RC[18]	X
Bit 1	R	RP_RC[17]	X
Bit 0	R	RBY_IC[16]	X

RP_RC[31:0]

When POS mode is selected, the RP_RC[31:0] bits indicate the number of received good packets passed to the FIFO interface during the last accumulation interval.

When ATM mode is selected, the RP_RC[31:0] bits indicate the number of received ATM cells and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

Register RCFP_BASE + CH: RCFP Receive Erred FCS/HCS Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]	X
Bit 14	R	EFCS[14]	X
Bit 13	R	EFCS[13]	X
Bit 12	R	EFCS[12]	X
Bit 11	R	EFCS[11]	X
Bit 10	R	EFCS[10]	X
Bit 9	R	EFCS[9]	X
Bit 8	R	EFCS[8]	X
Bit 7	R	EFCS[7]/HCS[7]	X
Bit 6	R	EFCS[6]/HCS[6]	X
Bit 5	R	EFCS[5]/HCS[5]	X
Bit 4	R	EFCS[4]/HCS[4]	X
Bit 3	R	EFCS[3]/HCS[3]	X
Bit 2	R	EFCS[2]/HCS[2]	X
Bit 1	R	EFCS[1]/HCS[1]	X
Bit 0	R	EFCS[0]/HCS[0]	X

EFCS[15:0]

When POS mode is selected, the EFCS[15:0] bits indicate the number of received FCS errors during the last accumulation interval.

HCS[7:0]

When ATM mode is selected, the HCS[7:0] bits indicate the number of HCS errors received in the last accumulation interval. Note that the behavior of this counter differs from that of the RTDP, in that all 7 HCS errors that cause the loss of cell delineation are counted.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

Register RCFP_BASE + DH: RCFP Receive Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	RABR[15]	X
Bit 14	R	RABR[14]	X
Bit 13	R	RABR[13]	X
Bit 12	R	RABR[12]	X
Bit 11	R	RABR[11]	X
Bit 10	R	RABR[10]	X
Bit 9	R	RABR[9]	X
Bit 8	R	RABR[8]	X
Bit 7	R	RABR[7]	X
Bit 6	R	RABR[6]	X
Bit 5	R	RABR[5]	X
Bit 4	R	RABR[4]	X
Bit 3	R	RABR[3]	X
Bit 2	R	RABR[2]	X
Bit 1	R	RABR[1]	X
Bit 0	R	RABR[0]	X

RABR[15:0]

When POS mode is selected, the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

Register RCFP_BASE + EH: RCFP Receive Minimum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

RMINL[15:0]

When POS mode is selected, the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected. Note that all minimum packet violations are counted in this register. This behavior differs from that of the RTDP.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

Register RCFP_BASE + FH: RCFP Receive Maximum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

RMAXL[15:0]

When POS mode is selected, the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

12.2 TCFP Register Summary

There are 4 TCFP blocks in the S/UNI-MACH48 device. Their base addresses (TCFP_BASE) are: 00B0H, 00C0H, 00D0H, and 00E0H. The TCFP is the transmit Cell/Packet processor for STS-12c and STS-48c channels.

Each TCFP block is dedicated to a range of timeslots (system side) and channel numbers (system side) for STS-12c and STS-48c data streams.

The TCFP block residing in the least significant TCFP_BASE address location is dedicated to all the timeslots shown in Table 53 and the first row of timeslots in STS-48c/STM-16c mode (TX48c = 1) and in Table 52 when not in STS-48c/STM-16c mode (TX48C = 0). The TS0 corresponds to the timeslot at the left side of each row. This TCFP block is dedicated to channel 0.

The TCFP block residing in the 2nd least significant TCFP_BASE address location is dedicated to the second row of the timeslot map in Table 52 and to the channel number 12. This TCFP block is not used when in STS-48c/STM-16c mode (TX48C = 1).

The TCFP block residing in the 3rd least significant TCFP_BASE address location is dedicated to the third row of the timeslot map in Table 52 and to the channel number 24. This TCFP block is not used when in STS-48c/STM-16c mode (TX48C = 1).

The TCFP block residing in the most significant TCFP_BASE address location is dedicated to the bottom row of the timeslot map in Table 52 and to the channel number 36. This TCFP block is not used when in STS-48c/STM-16c mode (TX48C = 1).

Register TCFP_BASE + 0H: TCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	FIFO_ERRE	0
Bit 14	R/W	FIFO_UDRE	0
Bit 13	R/W	XFERE	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	DELINDIS	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	POS_SEL	0
Bit 7	R/W	CRC_SEL[1]	1
Bit 6	R/W	CRC_SEL[0]	1
Bit 5	R/W	FLAG[3]	0
Bit 4	R/W	FLAG[2]	0
Bit 3	R/W	FLAG[1]	0
Bit 2	R/W	FLAG[0]	0
Bit 1	R/W	SCRMBL	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the TCFP. When PROV is logic 0, the TCFP ATM and packet processors are disabled and will not request data from the TXSDQ FIFO interface and will respond to data requests with all 1's data. When PROV is logic 1, the TCFP ATM or packet processor is enabled and will respond to data requests with valid data after requesting and processing data from the TXSDQ FIFO interface.

SCRMBL

The SCRMBL bit controls the scrambling of the packet data stream or ATM cell payload. When SCRMBL is a logic 1, scrambling is enabled. When SCRMBL is a logic 0, scrambling is disabled.

FLAG[3:0]

The flag insertion control (FLAG[3:0]) configures the minimum number of flag bytes the packet processor inserts between packets. The minimum number of flags (01111110) inserted between packets is shown in the table below. FLAG[3:0] are used only in POS mode.

Table 16 Selection of the number of FLAG Bytes

FLAG[3:0]	Minimum Number of FLAG Bytes
0000	1 flag
0001	2 flags
0010	4 flags
0011	8 flags
0100	16 flags
0101	32 flags
0110	64 flags
0111	128 flags
1000	256 flags
1001	512 flags
1010	1024 flags
1011	2048 flags
1100	4096 flags
1101	8192 flags
1110	16384 flags
1111	32768 flags

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, before byte stuffing and scrambling.

Table 17 CRC Mode Selection

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS inserted
01	Reserved	No FCS inserted
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

POS_SEL

The POS_SEL bit enables the POS HDLC frame processing mode. When POS_SEL is set to logic 1, POS processing will occur. When POS_SEL is set to logic 0, ATM mode is selected.

Reserved

The Reserved bits should be set to logic 0 for proper operation.DELINDIS

The DELINDIS bit can be used to disable HDLC flag alignment and byte stuffing. All payload data written to the POS-PHY Level 3 interface is passed directly to the TelecomBus Interface. DELINDIS is only valid in POS mode.

This bit should only be set when Transparent Data Mode is desired. In this mode, data is passed directly from the POS-PHY Level 3 Bus to the TelecomBus payload without flag insertion, byte stuffing or CRC generation. Use of Transparent mode requires the use of 64 byte packets, and the FIFO must not be allowed to under-run since no flags are available to fill excess bandwidth. In addition, the CRC_SEL bits must be set to "00".

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the transmitted packet/cell counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

FIFO_UDRE

The FIFO_UDRE bit enables the generation of an interrupt due to a FIFO underrun. When FIFO_UDRE is set to logic 1, the interrupt is enabled the signal INT will be set to logic 1 whenever FIFO_UNRI is set to logic 1.

FIFO_ERRE

The FIFO_ERRE bit enables the generation of an interrupt due to a FIFO error. When FIFO_ERRE is set to logic 1, the interrupt is enabled and the signal INT will be set to logic 1 whenever FIFO_ERRI is set to logic 1.

Register TCFP_BASE + 1H: TCFP Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	FIFO_ERRI	0
Bit 14	R	FIFO_UDRI	0
Bit 13	R	XFERI	0
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the transmitted cell/packet counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the TCFP counter register locations, or initiating a global performance monitor update by writing to register 0000H. XFERI is set to logic 0 when this register is read.

FIFO_UDRI

The FIFO_UDRI bit is logic 1 when an attempt is made to read from the FIFO while it is empty. This is considered a system error.

This bit is set to logic 0 immediately after a read to this register.

FIFO_ERRI

This bit is set to one when an error is detected on the read side of the FIFO. This error can be caused by an abnormal sequence of TSOP and TEOP signals or the assertion of FIFO_ERR. This assertion can normally be caused by a previous FIFO overrun condition or a user asserted error from the POS-PHY L3 interface.

This bit is set to logic 0 immediately after a read to this register.

Register TCFP_BASE + 2H: TCFP Idle/Unassigned ATM Cell Header

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]

The PAYLD[7:0] (Idle Cell Payload) value reflects the payload bytes which will be inserted into the ATM Idle cell generated by the TCFP.

CLP

The CLP (Cell Loss Priority) bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

PTI[2:0]

The PTI[2:0] (Payload Type) bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

GFC[3:0]

The GFC[3:0] (Generic Flow Control) bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode. The all zeros pattern is transmitted in the VCI and VPI fields of the idle/unassigned cell.

Register TCFP_BASE + 3H: TCFP Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	DCRC[7]	0
Bit 14	R/W	DCRC[6]	0
Bit 13	R/W	DCRC[5]	0
Bit 12	R/W	DCRC[4]	0
Bit 11	R/W	DCRC[3]	0
Bit 10	R/W	DCRC[2]	0
Bit 9	R/W	DCRC[1]	0
Bit 8	R/W	DCRC[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TX_BYTE_MODE	0
Bit 4	R/W	XOFF	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved

The Reserved bits should be set to their default values for proper operation.

INVERT

The data inversion bit (INVERT) configures the ATM or packet processor to logically invert the outgoing data stream. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0.

XOFF

The XOFF serves as a transmission enable bit. When XOFF is set to logic 0, ATM cells or packets are transmitted normally. When XOFF is set to logic 1, the cell or packet currently being transmitted is completed and then transmission is suspended. When XOFF is set to logic 1, the TCFP will stop requesting data from the TXSDQ and ATM Idle cells or HDLC flags will be sent on the TCFP egress interface. Note that while XOFF is set to logic 1, byte and packet counters may reflect bytes held in the TCFP's internal FIFO that have not yet been transmitted

TX_BYTE_MODE

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[39:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS and Abort bytes) before the byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS, Abort, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in POS mode.

DCRC[7:0]

The diagnostic CRC word (DCRC[7:0]) configures the ATM or packet processor to logically invert bits in the inserted CRC on the outgoing data stream for diagnostic purposes. When any bit in DCRC[7:0] is set to logic 1, the corresponding bit in the FCS value inserted by the POS processor or the HCS value inserted by the ATM processor is logically inverted. DCRC[7:0] is ignored when no FCS is inserted. Each DCRC[x] bit will cause a bit error in each byte of the 2 byte or 4 byte FCS.

Register TCFP_BASE + 4H: TCFP Transmit Cell/Packet Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[15]	X
Bit 14	R	TX_CELL[14]	X
Bit 13	R	TX_CELL[13]	X
Bit 12	R	TX_CELL[12]	X
Bit 11	R	TX_CELL[11]	X
Bit 10	R	TX_CELL[10]	X
Bit 9	R	TX_CELL[9]	X
Bit 8	R	TX_CELL[8]	X
Bit 7	R	TX_CELL[7]	X
Bit 6	R	TX_CELL[6]	X
Bit 5	R	TX_CELL[5]	X
Bit 4	R	TX_CELL[4]	X
Bit 3	R	TX_CELL[3]	X
Bit 2	R	TX_CELL[2]	X
Bit 1	R	TX_CELL[1]	X
Bit 0	R	TX_CELL[0]	X

Register TCFP_BASE + 5H: TCFP Transmit Cell/Packet Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[31]	X
Bit 14	R	TX_CELL[30]	X
Bit 13	R	TX_CELL[29]	X
Bit 12	R	TX_CELL[28]	X
Bit 11	R	TX_CELL[27]	X
Bit 10	R	TX_CELL[26]	X
Bit 9	R	TX_CELL[25]	X
Bit 8	R	TX_CELL[24]	X
Bit 7	R	TX_CELL[23]	X
Bit 6	R	TX_CELL[22]	X
Bit 5	R	TX_CELL[21]	X
Bit 4	R	TX_CELL[20]	X
Bit 3	R	TX_CELL[19]	X
Bit 2	R	TX_CELL[18]	X
Bit 1	R	TX_CELL[17]	X
Bit 0	R	TX_CELL[16]	X

TX_CELL[31:0]

The TX_CELL[31:0] bits indicate the number of cells or **non-aborted** packets transmitted to the TCFP egress stream during the last accumulation interval. ATM Idle cells, HDLC flags, and HDLC Abort bytes inserted into the transmission stream are not counted.

A write to any one of the TCFP counter registers loads all the corresponding TCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

Register TCFP_BASE + 6H: TCFP Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_BYTE[15]	X
Bit 14	R	TX_ BYTE [14]	X
Bit 13	R	TX_ BYTE [13]	X
Bit 12	R	TX_ BYTE [12]	X
Bit 11	R	TX_ BYTE [11]	X
Bit 10	R	TX_ BYTE [10]	X
Bit 9	R	TX_ BYTE [9]	X
Bit 8	R	TX_ BYTE [8]	X
Bit 7	R	TX_ BYTE [7]	X
Bit 6	R	TX_ BYTE [6]	X
Bit 5	R	TX_ BYTE [5]	X
Bit 4	R	TX_ BYTE [4]	X
Bit 3	R	TX_ BYTE [3]	X
Bit 2	R	TX_ BYTE [2]	X
Bit 1	R	TX_ BYTE [1]	X
Bit 0	R	TX_ BYTE [0]	X

Register TCFP_BASE + 7H: TCFP Transmit Byte Counter

Bit	Type	Function	Default
Bit 15	R	TX_ BYTE [31]	X
Bit 14	R	TX_ BYTE [30]	X
Bit 13	R	TX_ BYTE [29]	X
Bit 12	R	TX_ BYTE [28]	X
Bit 11	R	TX_ BYTE [27]	X
Bit 10	R	TX_ BYTE [26]	X
Bit 9	R	TX_ BYTE [25]	X
Bit 8	R	TX_ BYTE [24]	X
Bit 7	R	TX_ BYTE [23]	X
Bit 6	R	TX_ BYTE [22]	X
Bit 5	R	TX_ BYTE [21]	X
Bit 4	R	TX_ BYTE [20]	X
Bit 3	R	TX_ BYTE [19]	X
Bit 2	R	TX_ BYTE [18]	X
Bit 1	R	TX_ BYTE [17]	X
Bit 0	R	TX_ BYTE [16]	X

Register TCFP_BASE + 8H: TCFP Transmit Byte Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	TX_ BYTE [39]	X
Bit 6	R	TX_ BYTE [38]	X
Bit 5	R	TX_ BYTE [37]	X
Bit 4	R	TX_ BYTE [36]	X
Bit 3	R	TX_ BYTE [35]	X
Bit 2	R	TX_ BYTE [34]	X
Bit 1	R	TX_ BYTE [33]	X
Bit 0	R	TX_ BYTE [32]	X

Register TCFP_BASE + 9H: TCFP Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	TX_ABT[15]	X
Bit 14	R	TX_ABT[14]	X
Bit 13	R	TX_ABT[13]	X
Bit 12	R	TX_ABT[12]	X
Bit 11	R	TX_ABT[11]	X
Bit 10	R	TX_ABT[10]	X
Bit 9	R	TX_ABT[9]	X
Bit 8	R	TX_ABT[8]	X
Bit 7	R	TX_ABT[7]	X
Bit 6	R	TX_ABT[6]	X
Bit 5	R	TX_ABT[5]	X
Bit 4	R	TX_ABT[4]	X
Bit 3	R	TX_ABT[3]	X
Bit 2	R	TX_ABT[2]	X
Bit 1	R	TX_ABT[1]	X
Bit 0	R	TX_ABT[0]	X

TX_ABT[15:0]

The TX_ ABT[15:0] bits indicate the number aborted packets transmitted to the TCFP egress stream during the last accumulation interval. These counters are only valid when processing packets.

A write to any one of the TCFP counter registers loads all the corresponding TCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48.

12.3 RTDP Register Summary

There are 4 RTDP blocks in the S/UNI-MACH48 device. Their base addresses (RTDP_BASE) are: 00F0H, 0110H, 0130H, and 0150H. The RTDP is the receive Cell/Packet processor for STS-3c and lower rate channels.

Each RTDP block is dedicated to a range of timeslots (system side) and channel numbers (system side) and are only used for STS-3c/STM-1, STS-1/STM-0, and DS3 data streams.

The RTDP block residing in the least significant RTDP_BASE address location is dedicated to the first row of the timeslot maps shown in Table 52. The TS0 corresponds to the timeslot at the left side of each row. This RTDP block is also dedicated to the least significant channel numbers (0 – 11).

The RTDP block residing in the 2nd least significant RTDP_BASE address location is dedicated to the second row of the timeslot maps in Table 52 and to the channel numbers (12-23).

The RTDP block residing in the 3rd least significant RTDP_BASE address location is dedicated to the third row of the timeslot maps in Table 52 and to the channel numbers (24-35).

The RTDP block residing in the most significant RTDP_BASE address location is dedicated to the bottom row of the timeslot maps in Table 52 and to the channel numbers (36-47).

Register RTDP_BASE + 0H: RTDP Indirect Channel Select

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	CHAN[3]	0
Bit 2	R/W	CHAN[2]	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

CHAN[3:0]

The indirect channel number bits (CHAN[3:0]) indicate the channel to be updated or queried in the indirect access.

Reserved

The Reserved bit should be set to its default value for proper operation.

RWB

The read/write bar (RWB) bit selects between an update operation (write) or a query operation (read). Writing a logic 0 to RWB triggers the update operation of the channel specified by CHAN[3:0] with the information in the RTDP Indirect registers. Writing a logic 1 to RWB triggers a query of the channel specified by CHAN[3:0] and the information is placed in all of the RTDP Indirect Registers.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is logic 1 when a write to the Indirect Channel Select register triggers an indirect access and will stay logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in all the Indirect Data registers or to determine when a new indirect write operation may commence. (Note – BUSY is also logic 1 after reset while the channel provision RAM is being initialized and is cleared when the RAM has completed initialization and the RTDP is ready to accept an indirect access operation to the RAM.)

Register RTDP_BASE + 1H: RTDP Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	HCSDQDB	0
Bit 11	R/W	DS3_DSTF_NCD	0
Bit 10	R/W	POS_SEL	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	STRIP_SEL	0
Bit 7	R/W	DELINDIS	0
Bit 6	R/W	IDLEPASS	0
Bit 5	R/W	CRCPASS	0
Bit 4	R/W	CRC_SEL[1]	1
Bit 3	R/W	CRC_SEL[0]	1
Bit 2	R/W	RXOTYP	0
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

The Indirect Configuration Register is provided at RTDP address 1. This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

PROV

The processor provision bit (PROV) configures the RTDP to process ATM cells and packets as configured. When PROV is logic 1, the selected channel's processor is enabled. When PROV is logic 0, the selected channel's processor is disabled.

DESCRMBL

The DESCRMBL bit controls the descrambling of the packet or ATM cell payload with the polynomial $x^{43} + 1$. When DESCRMBL is set to logic 0, frame or cell payload descrambling is disabled. When DESCRMBL is set to logic 1, payload descrambling is enabled.

RXOTYP

The RXOTYP determines if an incoming alarm signal (from IPAIS[x] if RHPP_EN=0 or if path AIS or loss-of-pointer is detected by the RHPP if RHPP_EN=1), DS3 out of frame, or PLCP out of frame will stop a packet by simply asserting EOP or by asserting EOP and ERR. When RXOTYP is set to logic zero, the abort sequence is inserted generating a user abort error. When the RXOTYP is set to logic one, the frame processor performs a simple flag insertion and thus the packet will be flagged as an FCS error.

This bit is only valid when processing packets. When processing ATM cells, the RTDP will finish processing any cell in progress and then stop until the alarm is cleared.

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, after bit/byte destuffing and descrambling.

Table 18 Functionality of the CRC_SEL[1 0] Register Bits

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS verification
01	Reserved	Reserved
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

CRCPASS

The CRCPASS bit controls the dropping of cells and packets based on the detection of a CRC error.

When processing ATM cells and when CRCPASS is a logic 0, cells containing an HCS error are dropped. When CRCPASS is a logic 1, cells are passed to the external FIFO interface regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine will never lose cell delineation.

When processing packets and when CRCPASS is logic 1, then packets with FCS errors are not marked as such and are passed to the external FIFO interface as if no FCS error occurred. When CRCPASS is logic 0, then packets with FCS errors are marked using ERR.

Note that ATM idle cells which contain HCS errors will cause the state machine to change state regardless of the setting of the IDLEPASS register bit.

Regardless of the programming of this bit, ATM cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the DELINDIS bit in this register is set to logic 1.

IDLEPASS

The IDLEPASS bit controls the function of the ATM Idle Cell filter. It is only valid when processing ATM cells. When IDLEPASS is written with a logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic 1, the Idle Cell Header Pattern and Mask register bits are ignored. The default state of this bit and the bits in the RTDP Idle Cell Header and Mask Register enable the dropping of idle cells.

DELINDIS

The DELINDIS bit can be used to disable all HDLC flag alignment. All payload data read by the RTDP is passed to the FIFO interface without the requirement of having to find packet delineation first. DELINDIS is only valid in POS mode.

This bit should only be set when Transparent Data Mode is desired. In this mode, data is passed directly from the TelecomBus payload to the POS-PHY Level 3 Bus without flag delineation, byte or bit de-stuffing or CRC checking. Use of Transparent mode requires the use of 64 byte packets, and the CRC_SEL bits must be set to “00”.

STRIP_SEL

The indirect frame check sequence stripping bit (STRIP_SEL) configures the RTDP to remove the CRC from the outgoing packet. When STRIP_SEL is logic 1 and CRC_SEL[1:0] is not equal to "00" (no CRC), the received packet FCS byte(s) or ATM cell HCS byte(s) are not transferred over the FIFO interface. When STRIP_SEL is set to logic 0, the received packet FCS are transferred over the FIFO interface. **The STRIP_SEL bit must be set to logic 1 if working in ATM mode.**

INVERT

The data inversion bit (INVERT) configures the processor to logically invert the incoming stream before processing it. When INVERT is set to logic 1, the stream is logically inverted before processing. When INVERT is set to logic 0, the stream is not inverted before processing.

POS_SEL

The ATM/POS selection bit (POS_SEL) configures the RTDP for operation in ATM or packet mode. When POS_SEL is logic 1, then packet mode is selected. When POS_SEL is logic 0, then ATM mode is selected.

DS3_DSTF_NCD

The DS3 Bit-Destuff/Nibble Cell Delineation (DS3_DSTF_NCD) selection configures the RTDP for bit-stuffed HDLC or nibble-aligned cell delineation for DS3 mode. When DS3_DSTF_NCD is logic 1 and POS_SEL is logic 1, the bit-stuffed HDLC operation is enabled. When DS3_DSTF_NCD is logic 1 and POS_SEL is logic 0, overhead nibble aligned DS3 delineation is performed (for ATM DS3 direct mapped applications). If DS3_DSTF_NCD is logic 0, byte-stuffed HDLC and byte-aligned cell delineation is performed.

HCSDQDB

The HCSDQDB bit enables HCS checking for DQDB type cells. When HCSDQDB is a logic 0, the first 4 header bytes are used in the HCS validation calculation. When HCSDQDB is a logic 1, only 3 of the header octets (octets 2, 3 and 4) are used for HCS validation. This bit is also used to modify the idle cell detection circuitry to check for DQDB idle cells. The header bytes for a DQDB idle cell are:

0xxxxxxxx 00000000 00000000 00000000.

The HCSDQDB bit is only valid if POS_SEL is logic 0 and CRC_SEL[1:0] is ‘b10 or ‘b11.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Register RTDP_BASE + 2H: RTDP Indirect Minimum Packet Length and Bit Order

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	0
Bit 10	R/W	MINPL[2]	1
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	BIT_ABRTE	0
Bit 3	R/W	RBY_MODE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	SBSD	0

The Indirect Minimum Packet Length and Bit Order Register is provided at RTDP address 2. This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

SBSD

The Swap Byte Stuffed Data is used to control the bit order of the data between the descrambling and the destuffing operations, thus controlling the sense that the bits were received on the line. When set to a logic zero, the bytes pass through unchanged (the most significant bit of the byte was received first). When set to a logic one, the bit ordering must be reversed (the least significant bit of the byte was received first). This bit is only valid when operating in packet mode. This should be set to logic 1 for bit synchronous HDLC and logic 0 for byte synchronous PPP.

Reserved

The Reserved bits should be set to their default value for proper operation.

RBY_MODE

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[39:0] counters work. When RBY_MODE is logic 0, RBY_IC[31:0] will count all bytes in received packets (including FCS and Abort bytes) after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[31:0] will count all bytes in received packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid when working in byte-stuffed POS mode. RBY_MODE must be set to logic 0 for bit-stuffed HDLC mode and is invalid for the ATM mode.

BIT_ABRTE

The Bit Abort Sequence Abort Enable (BIT_ABRTE) is used to enable counts of errors caused by a one byte packet consisting only of an bit-stuffed abort sequence (at least seven ones) when in bit de-stuffed packet mode. When BIT_ABRTE = 0, a flag followed by an abort sequence will generate a set of error conditions which will be counted as erred FCS, Min Packet length and Aborted packet counters. When BIT_ABRTE = 1, the same sequence will not cause the error counters to increment. When the all-ones sequence is being used as idle space between packets, enabling this bit prevents spurious error counts from being generated. Note that this bit does not block associated error interrupts (MINLI, UCRCI, ABRTI) which should be disabled on a channel by channel basis when all-ones sequences are used as idle.

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the frame after destuffing but including the FCS. The default minimum packet length is 4 octets. Values smaller than 4 should not be used.

Register RTDP_BASE + 3H: RTDP Indirect Maximum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

The Indirect Maximum Packet Length Register is provided at RTDP address 3. This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

MAXPL[16:0]

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum packet length. MAXPL[0] is set equal to 0. Packets larger than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame after destuffing but including the FCS bytes. The default maximum packet length is 1536 octets.

Register RTDP_BASE + 4H: RTDP Indirect LCD Count Threshold

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

The Indirect LCD Count Threshold Register is provided at RTDP address 4. This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to the following:

Format	Average Cell Period	Default LCD Integration Period
STS-3c	2.83 μs	1018.8 μs
STS-1/STM-0	8.76 μs	3.16 ms
DS3 ATM direct mapped	9.59 μs	3.45 ms
DS3 PLCP mapped	10.42 μs	3.75 ms

Register RTDP_BASE + 5H: RTDP Indirect Idle Cell Header and Mask

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[3]	0
Bit 10	R/W	PTI[2]	0
Bit 9	R/W	PTI[1]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

The Indirect Idle Cell Header and Mask Register is provided at RTDP address 5. This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to this register to select the bits included in the cell filter. A logic 1 in this bit position enables the CLP bit in the pattern register to be compared. A logic zero causes the masking of the CLP bit.

MPTI[3:0]

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the Configuration Register must be set to logic zero to enable dropping of cells matching this pattern.

Register RTDP_BASE + 6H: RTDP Indirect Receive Byte/Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RBY_IC[15]	X
Bit 14	R	RBY_IC[14]	X
Bit 13	R	RBY_IC[13]	X
Bit 12	R	RBY_IC[12]	X
Bit 11	R	RBY_IC[11]	X
Bit 10	R	RBY_IC[10]	X
Bit 9	R	RBY_IC[9]	X
Bit 8	R	RBY_IC[8]	X
Bit 7	R	RBY_IC[7]	X
Bit 6	R	RBY_IC[6]	X
Bit 5	R	RBY_IC[5]	X
Bit 4	R	RBY_IC[4]	X
Bit 3	R	RBY_IC[3]	X
Bit 2	R	RBY_IC[2]	X
Bit 1	R	RBY_IC[1]	X
Bit 0	R	RBY_IC[0]	X

Register RTDP_BASE + 7H: RTDP Indirect Receive Byte/Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	RBY_IC[31]	X
Bit 14	R	RBY_IC[30]	X
Bit 13	R	RBY_IC[29]	X
Bit 12	R	RBY_IC[28]	X
Bit 11	R	RBY_IC[27]	X
Bit 10	R	RBY_IC[26]	X
Bit 9	R	RBY_IC[25]	X
Bit 8	R	RBY_IC[24]	X
Bit 7	R	RBY_IC[23]	X
Bit 6	R	RBY_IC[22]	X
Bit 5	R	RBY_IC[21]	X
Bit 4	R	RBY_IC[20]	X
Bit 3	R	RBY_IC[19]	X
Bit 2	R	RBY_IC[18]	X
Bit 1	R	RBY_IC[17]	X
Bit 0	R	RBY_IC[16]	X

RBY_IC[31:0]

When packet mode is selected, the RBY_IC[31:0] bits indicate the number of bytes received within frames during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes in the count is controlled by the RBY_MODE register bit. HDLC flags are not counted.

When ATM mode is selected, the RBY_IC[31:0] bits indicate the number of Idle cells received and passed to the FIFO interface in the last accumulation interval.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS will be updated.

Register RTDP_BASE + 8H: RTDP Indirect Packet/Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[15]	X
Bit 14	R	RP_RC[14]	X
Bit 13	R	RP_RC[13]	X
Bit 12	R	RP_RC[12]	X
Bit 11	R	RP_RC[11]	X
Bit 10	R	RP_RC[10]	X
Bit 9	R	RP_RC[9]	X
Bit 8	R	RP_RC[8]	X
Bit 7	R	RP_RC[7]	X
Bit 6	R	RP_RC[6]	X
Bit 5	R	RP_RC[5]	X
Bit 4	R	RP_RC[4]	X
Bit 3	R	RP_RC[3]	X
Bit 2	R	RP_RC[2]	X
Bit 1	R	RP_RC[1]	X
Bit 0	R	RP_RC[0]	X

Register RTDP_BASE + 9H: RTDP Indirect Receive Packet/ATM Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[31]	X
Bit 14	R	RP_RC[30]	X
Bit 13	R	RP_RC[29]	X
Bit 12	R	RP_RC[28]	X
Bit 11	R	RP_RC[27]	X
Bit 10	R	RP_RC[26]	X
Bit 9	R	RP_RC[25]	X
Bit 8	R	RP_RC[24]	X
Bit 7	R	RP_RC[23]	X
Bit 6	R	RP_RC[22]	X
Bit 5	R	RP_RC[21]	X
Bit 4	R	RP_RC[20]	X
Bit 3	R	RP_RC[19]	X
Bit 2	R	RP_RC[18]	X
Bit 1	R	RP_RC[17]	X
Bit 0	R	RBY_IC[16]	X

RP_RC[31:0]

When packet mode is selected, the RP_RC[31:0] bits indicate the number of received good packets received passed to the FIFO interface during the last accumulation interval.

When ATM mode is selected, the RP_RC[31:0] bits indicate the number of received ATM cells received and passed to the FIFO interface in the last accumulation interval.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS will be updated.

Register RTDP_BASE + AH: RTDP Indirect Receive Erred FCS/HCS Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]	X
Bit 14	R	EFCS[14]	X
Bit 13	R	EFCS[13]	X
Bit 12	R	EFCS[12]	X
Bit 11	R	EFCS[11]	X
Bit 10	R	EFCS[10]	X
Bit 9	R	EFCS[9]	X
Bit 8	R	EFCS[8]	X
Bit 7	R	EFCS[7]/HCS[7]	X
Bit 6	R	EFCS[6]/HCS[6]	X
Bit 5	R	EFCS[5]/HCS[5]	X
Bit 4	R	EFCS[4]/HCS[4]	X
Bit 3	R	EFCS[3]/HCS[3]	X
Bit 2	R	EFCS[2]/HCS[2]	X
Bit 1	R	EFCS[1]/HCS[1]	X
Bit 0	R	EFCS[0]/HCS[0]	X

EFCS[15:0]

When packet mode is selected, the EFCS[15:0] bits indicate the number of received FCS errors during the last accumulation interval.

HCS[7:0]

When ATM mode is selected, the HCS[7:0] bits indicate the number of HCS errors received in the last accumulation interval. Note that the last HCS error that causes the cell processor to enter the HUNT state will not be reflected in the count. This differs from the operation of the RCFP.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS will be updated.

Register RTDP_BASE + BH: RTDP Indirect Receive Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	RABR[15]	X
Bit 14	R	RABR[14]	X
Bit 13	R	RABR[13]	X
Bit 12	R	RABR[12]	X
Bit 11	R	RABR[11]	X
Bit 10	R	RABR[10]	X
Bit 9	R	RABR[9]	X
Bit 8	R	RABR[8]	X
Bit 7	R	RABR[7]	X
Bit 6	R	RABR[6]	X
Bit 5	R	RABR[5]	X
Bit 4	R	RABR[4]	X
Bit 3	R	RABR[3]	X
Bit 2	R	RABR[2]	X
Bit 1	R	RABR[1]	X
Bit 0	R	RABR[0]	X

RABR[15:0]

When packet mode is selected, the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS will be updated.

Register RTDP_BASE + CH: RTDP Indirect Receive Minimum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

The Indirect Receive Minimum Length Packet Error Counter Register is provided at RTDP address C. This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

RMINL[15:0]

When packet mode is selected, the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected. Note that malformed packets smaller than 4 bytes will not be counted in this register.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS will be updated.

Register RTDP_BASE + DH: RTDP Indirect Receive Maximum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

The Indirect Receive Maximum Length Packet Error Counter Register is provided at RTDP address D. This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

RMAXL[15:0]

When packet mode is selected, the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS will be updated.

Register RTDP_BASE + 10H + *n*: RTDP Interrupt Enable (*n* = 0 to 5)

Bit	Type	Function	Default
Bit 15	R/W	XFERE	0
Bit 14	R/W	MINLE_***2n+1***	0
Bit 13	R/W	MAXLE_***2n+1***	0
Bit 12	R/W	ABRTE_***2n+1***	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	CRCE_***2n+1***	0
Bit 9	R/W	OOFE_***2n+1***	0
Bit 8	R/W	LOFE_***2n+1***	0
Bit 7		Unused	X
Bit 6	R/W	MINLE_***2n***	0
Bit 5	R/W	MAXLE_***2n***	0
Bit 4	R/W	ABRTE_***2n***	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	CRCE_***2n***	0
Bit 1	R/W	OOFE_***2n***	0
Bit 0	R/W	LOFE_***2n***	0

RTDP registers 10H-15H contain the Interrupt Enable bits for the 12 channels. The channel mapping for these registers is as follows:

n	RTDP Register	Channel Number for 2n	Channel Number for 2n+1
0	10H	0	1
1	11H	2	3
2	12H	4	5
3	13H	6	7
4	14H	8	9
5	15H	10	11

LOFE

The LOFE bit enables the generation of an interrupt due to a change in the ATM LCD state. When LOFE is set to logic 1, the interrupt is enabled.

OOFE

The OOFE bit enables the generation of an interrupt due to a change in ATM cell delineation state or packet alignment state. When OOFE is set to logic 1, the interrupt is enabled.

CRCE

The CRCE bit enables the generation of an interrupt due to the detection of an ATM HCS or packet FCS error. When CRCE is set to logic 1, the interrupt is enabled.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set to logic 1, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RTDP performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled. XFERE is only available at register 10H.

Register RTDP_BASE + 16H + *n*: RTDP Interrupt Indication (*n* = 0 to 5)

Bit	Type	Function	Default
Bit 15		XFERI	X
Bit 14	R	MINLI_***2n+1***	X
Bit 13	R	MAXLI_***2n+1***	X
Bit 12	R	ABRTI_***2n+1***	X
Bit 11	R	Reserved	X
Bit 10	R	CRCI_***2n+1***	X
Bit 9	R	OOFI_***2n+1***	X
Bit 8	R	LOFI_***2n+1***	X
Bit 7		Unused	X
Bit 6	R	MINLI_***2n***	X
Bit 5	R	MAXLI_***2n***	X
Bit 4	R	ABRTI_***2n***	X
Bit 3	R	Reserved	X
Bit 2	R	CRCI_***2n***	X
Bit 1	R	OOFI_***2n***	X
Bit 0	R	LOFI_***2n***	X

RTDP registers 16H-1BH contain the Interrupt Indication bits for the 12 channels. The channel mapping for these registers is as follows:

n	RTDP Register	Channel Number for 2n	Channel Number for 2n+1
0	16H	0	1
1	17H	2	3
2	18H	4	5
3	19H	6	7
4	1H	8	9
5	1BH	10	11

LOFI

The LOFI bit is logic 1 when there is a change in the loss of cell delineation (LCD) state for the channel. The current value of the LCD is available in the LOFV bits in the RTDP LOF Status register. This bit is reset immediately after a read to this register.

OOFI

The OOFI bit is logic 1 when the RTDP ATM cell processor for the channel enters or exits the SYNC state or the packet processor finds a new flag alignment. The current value of the out-of-delineation state is available in the OOFV bits in the RTDP OOF Status register. The OOFI bit is reset immediately after a read to this register.

CRCI

The CRCI bit is logic 1 when an ATM HCS or packet FCS error is detected on the channel. This bit is reset immediately after a read to this register.

Reserved:

The Reserved bit is unused.

ABRTI

The ABRTI bit indicates bit enables the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE for the channel. ABRTI is cleared to logic 0 after this register is read.

MAXLI

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE for the channel. MAXLI is cleared to logic 0 after this register is read.

MINLI

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. This interrupt can be masked using MINLE for the channel. MINLI is cleared to logic 0 after this register is read. Note that although packets smaller than 4 bytes will not increment the RMINL counter, they will cause the MINLI interrupt.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred on the channel. A logic 1 in this bit position indicates that the RTDP performance monitor counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by writing to register 0000H for global performance monitor update. XFERI is set to logic 0 after this register is read. XFERI is only available at register 16H.

Register RTDP_BASE + 1CH: RTDP OOF Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	OOFV_11	X
Bit 10	R	OOFV_10	X
Bit 9	R	OOFV_9	X
Bit 8	R	OOFV_8	X
Bit 7	R	OOFV_7	X
Bit 6	R	OOFV_6	X
Bit 5	R	OOFV_5	X
Bit 4	R	OOFV_4	X
Bit 3	R	OOFV_3	X
Bit 2	R	OOFV_2	X
Bit 1	R	OOFV_1	X
Bit 0	R	OOFV_0	X

OOFV_***x***

The OOFV_***x*** bit indicates the ATM cell delineation or packet Idle state for channel ***x***. When OOFV_***x*** is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries or the packet processor has not found a flag alignment. When OOFV_***x*** is logic 0, the cell delineation state machine is in the 'SYNC' state or the packet processor is frame aligned.

Register RTDP_BASE + 1DH: RTDP LOF Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	LOFV_11	X
Bit 10	R	LOFV_10	X
Bit 9	R	LOFV_9	X
Bit 8	R	LOFV_8	X
Bit 7	R	LOFV_7	X
Bit 6	R	LOFV_6	X
Bit 5	R	LOFV_5	X
Bit 4	R	LOFV_4	X
Bit 3	R	LOFV_3	X
Bit 2	R	LOFV_2	X
Bit 1	R	LOFV_1	X
Bit 0	R	LOFV_0	X

LOFV_***x***

The LOFV_***x*** bit gives the ATM Loss of Cell Delineation state for channel ***x***. When LOF is logic 1, an out of cell delineation (OOF) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LOFV_***x*** is logic 0, the RTDP has been in cell delineation for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[10:0] register bits in the RTDP LCD Count Threshold register.

When in bit-stuffed HDLC mode, LOFV_***x*** shows the Idle status of the channel. If LOFV_***x*** is logic 1, then the channel is currently in Idle state.

12.4 TTDP Register Summary

There are 4 TTDP blocks in the S/UNI-MACH48 device. Their base addresses (TTDP_BASE) are: 0170H, 0180H, 0190H, and 01A0H. The TTDP is the transmit Cell/Packet processor for STS-3c and lower rate channels.

Each TTDP block is dedicated to a range of timeslots (system side) and channel numbers (system side) and are only used for STS-3c/STM-1, STS-1/STM-0, and DS3 data streams.

The TTDP block residing in the least significant TTDP_BASE address location is dedicated to the first row of the timeslot maps shown in Table 52. The TS0 corresponds to the timeslot at the left side of each row. This TTDP block is also dedicated to the least significant channel numbers (0 – 11).

The TTDP block residing in the 2nd least significant TTDP_BASE address location is dedicated to the second row of the timeslot maps in Table 52 and to the channel numbers (12-23).

The TTDP block residing in the 3rd least significant TTDP_BASE address location is dedicated to the third row of the timeslot maps in Table 52 and to the channel numbers (24-35).

The TTDP block residing in the most significant TTDP_BASE address location is dedicated to the bottom row of the timeslot maps in Table 52 and to the channel numbers (36-47).

Register TTDP_BASE + 0H: TTDP Indirect Channel Select

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	CHAN[3]	0
Bit 2	R/W	CHAN[2]	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

The Indirect Channel Address Register is provided at TTDP address 0. Note that when configuring a channel in the TTDP, that channel must be unprovisioned in the downstream TCAS12 or the configuration write may not be properly executed.

CHAN[3:0]

The indirect channel number bits (CHAN[3:0]) indicate the channel to be updated or queried in the indirect access.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

RWB

The read/write bar (RWB) bit selects between an update operation (write) and a query operation (read). Writing logic 0 to RWB triggers the update operation of the channel specified by CHAN[3:0] with the information in TTDP Registers 1, 2, and 3. Writing a logic 1 to RWB triggers a query of the channel specified by CHAN[3:0] and the information is placed in all of the Indirect Registers.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is logic 1 when a write to the Indirect Channel Select register triggers an indirect access and will stay logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in all the Indirect Data registers or to determine when a new indirect write operation may commence. (Note – BUSY is also logic 1 after reset while the channel provision RAM is being initialized and is cleared when the RAM has completed initialization and the TTDP is ready to accept an indirect access operation to the RAM.)

Register TTDP_BASE + 1H: TTDP Indirect Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	DELINDIS	0
Bit 11	R/W	HCSDQDB	0
Bit 10	R/W	BIT_STUFF	0
Bit 9	R/W	POS_SEL	0
Bit 8	R/W	CRC_SEL[1]	1
Bit 7	R/W	CRC_SEL[0]	1
Bit 6	R/W	FLAG[3]	0
Bit 5	R/W	FLAG[2]	0
Bit 4	R/W	FLAG[1]	0
Bit 3	R/W	FLAG[0]	0
Bit 2	R/W	SCRMBL	1
Bit 1	R/W	IDLE	0
Bit 0	R/W	PROV	0

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

PROV

The processor provision bit (PROV) is used to enable the TTDP. When PROV is logic 0, the TTDP ATM and POS processors are disabled and will not request data from the FIFO interface and will respond to data requests with idle data (all 1's). When PROV is logic 1, the TCFP ATM or POS processor is enabled and will respond to data requests with valid data after requesting and processing data from the TXSDQ FIFO interface.

IDLE

The inter-frame time fill bit (IDLE) configures the packet processor to use flag bytes or HDLC idle as the inter-frame time fill between packets. When IDLE is set to logic 0, the packet processor uses flag bytes as the inter-frame time fill. When IDLE is set to logic 1, the packet processor uses HDLC idle (all one's byte with no byte or bit stuffing pattern) as the inter-frame time fill. IDLE is only valid when POS_SEL is set to logic 1.

SCRMBL

The scramble enable bit (SCRMBL) controls the scrambling of the packet data stream or ATM cell payload. When SCRMBL is set to logic 1, scrambling is enabled. When SCRMBL is set to logic 0, scrambling is disabled.

FLAG[3:0]

The flag insertion control (FLAG[3:0]) configures the minimum number of flags or idle bytes the packet processor inserts between packets. The minimum number of flags (01111110) or bytes of idle (11111111) between two flags inserted between packets is shown in the table below. Idle bytes are inserted between flags only if the IDLE bit is set to logic 1. FLAG[3:0] are valid only when POS_SEL is set to logic 1.

Table 19 Selection of the number of Flag Bytes

FLAG[3:0]	Minimum Number of Flag/Idle Bytes
0000	1 flag/0 bytes of idle
0001	2 flags/0 bytes of idle
0010	4 flags/2 bytes of idle
0011	8 flags/6 bytes of idle
0100	16 flags/14 bytes of idle
0101	32 flags/30 bytes of idle
0110	64 flags/62 bytes of idle
0111	128 flags/126 bytes of idle
1000	256 flag/254 bytes of idle
1001	512 flags/510 bytes of idle
1010	1024 flags/1022 bytes of idle
1011	2048 flags/2046 bytes of idle
1100	4096 flags/4094 bytes of idle
1101	8192 flags/8190 bytes of idle
1110	16384 flags/16382 bytes of idle
1111	32768 flags/32766 bytes of idle

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, when HCSDQDB is logic 0, the CRC is calculated over the first four ATM header octets, and when HCSDQDB is logic 1, the CRC is calculated over octets 2, 3, and 4. For packet applications, the CRC is calculated over the whole packet data, before byte stuffing and scrambling.

Table 20 CRC Mode Selection

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS inserted
01	Reserved	No FCS inserted
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

POS_SEL

The ATM/POS selection bit (POS_SEL) configures the TTDP for operation in ATM or POS mode. When POS_SEL is logic 1, then POS mode is selected. When POS_SEL is logic 0, then ATM mode is selected.

BIT_STUFF

The HDLC bit-stuff selection (BIT_STUFF) configures the TTDP for bit-stuffed HDLC. When BIT_STUFF is logic 1, the TTDP performs bit-stuffed HDLC. When BIT_STUFF is logic 0, the TTDP performs byte-stuffed HDLC. Bit-stuffed HDLC is intended for use with DS3 based HDLC. BIT_STUFF is only valid when POS_SEL is logic 1.

HCSDQDB

The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets, 2, 3, and 4 are included in the HCS calculation as required by IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are included in the HCS calculation as required by the ATM Forum UNI specification and ITU-T Recommendation I.432.

DELINDIS

The DELINDIS bit controls the disabling of bit/byte stuffing and flag insertion. When a logic 1 is written to DELINDIS, flags are not inserted unless a FIFO underrun occurs, and data is not stuffed. When a logic 0 is written to DELINDIS, packets are delimited by flags, and stuffed according to the IDLE, FLAG, and BIT_STUFF configuration bits. CRC insertion and scrambling are not affected by DELINDIS. DELINDIS is only valid when POS_SEL is logic 1. This bit should only be set when Transparent Mode operation is desired. In Transparent Mode, data must be written to the POS-PHY Level 3 Bus in 64 byte blocks, and the FIFO must not be allowed to underflow. In addition for Transparent Mode, the CRC_SEL bits should be set to “00” to disable CRC generation.

Reserved

The Reserved register bits must be set to logic 0 for proper operation.

Register TTDP_BASE + 2H: TTDP Indirect Idle/Unassigned ATM Cell Header

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

The Indirect Idle/Unassigned ATM Cell Header Register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

PAYLD[7:0]

The PAYLD[7:0] (Idle Cell Payload) value reflects the payload bytes which will be inserted into the ATM Idle cell generated by the TTDP.

CLP

The Cell Loss Priority bit (CLP) contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TTDP detects that no outstanding cells are available from the external FIFO and data is requested on the TTDP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

PTI[2:0]

The Payload Type bits (PTI[2:0]) contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TTDP detects that no outstanding cells are available for transmission. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

GFC[3:0]

The Generic Flow Control bits (GFC[3:0]) contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TTDP detects that no outstanding cells are available from the external FIFO for transmission. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode. The all zeros pattern is transmitted in the VCI and VPI fields of the idle/unassigned cell.

Register TTDP_BASE + 3H: TTDP Indirect Diagnostics

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	TX_BYTE_MODE	0
Bit 5	R/W	Reserved	X
Bit 4	R/W	DCRC	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	SBSD	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

Reserved

The Reserved bits must be set to their default value for proper operation. Set the unknown Reserved bit (bit 5) to '0'.

SBSD

The Swap Byte Stuffed Data bit (SBSD) is used to control the bit order of the data between the stuffing and the scrambling operations, thus controlling the sense that the bits will be sent on the line. When set to a logic zero, the bytes pass through unchanged (the most significant bit of the byte is transmitted first). When set to a logic one, the bit ordering is reversed (the least significant bit of the byte is transmitted first). This bit is only valid when operating in packet mode. It should be set to logic 0 for PPP POS mode and logic 1 for bit-stuffed DS3 HDLC mode.

INVERT

The data inversion bit (INVERT) configures the ATM or packet processor to logically invert the outgoing data stream from the TTDP. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0.

DCRC

The diagnostic CRC bit (DCRC) configures the ATM or packet processor to err the CRC on the outgoing data stream for diagnostic purposes. When DCRC is set to logic 1, the FCS value inserted by the POS/HDLC processor or the HCS value inserted by the ATM processor is logically XORed with CRC_XOR[7:0]. The inserted FCS or HCS is not logically XORed when DCRC is set to logic 0. DCRC is ignored when PROV is logic 0.

TX_BYTE_MODE

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[31:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[31:0] will count all bytes in transmitted packets (including FCS and Abort bytes) before the bit/byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[31:0] will count all bytes in transmitted packets (including FCS, Abort, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in byte-stuffed POS mode. In bit-stuffed HDLC mode, TX_BYTE_MODE must be set to logic 0. TX_BYTE[31:0] is not used in ATM mode.

Register TTDP_BASE + 4H: TTDP Indirect Transmit Cell/Packet Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[15]	X
Bit 14	R	TX_CELL[14]	X
Bit 13	R	TX_CELL[13]	X
Bit 12	R	TX_CELL[12]	X
Bit 11	R	TX_CELL[11]	X
Bit 10	R	TX_CELL[10]	X
Bit 9	R	TX_CELL[9]	X
Bit 8	R	TX_CELL[8]	X
Bit 7	R	TX_CELL[7]	X
Bit 6	R	TX_CELL[6]	X
Bit 5	R	TX_CELL[5]	X
Bit 4	R	TX_CELL[4]	X
Bit 3	R	TX_CELL[3]	X
Bit 2	R	TX_CELL[2]	X
Bit 1	R	TX_CELL[1]	X
Bit 0	R	TX_CELL[0]	X

Register TTDP_BASE + 5H: TTDP Indirect Transmit Cell/Packet Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[31]	X
Bit 14	R	TX_CELL[30]	X
Bit 13	R	TX_CELL[29]	X
Bit 12	R	TX_CELL[28]	X
Bit 11	R	TX_CELL[27]	X
Bit 10	R	TX_CELL[26]	X
Bit 9	R	TX_CELL[25]	X
Bit 8	R	TX_CELL[24]	X
Bit 7	R	TX_CELL[23]	X
Bit 6	R	TX_CELL[22]	X
Bit 5	R	TX_CELL[21]	X
Bit 4	R	TX_CELL[20]	X
Bit 3	R	TX_CELL[19]	X
Bit 2	R	TX_CELL[18]	X
Bit 1	R	TX_CELL[17]	X
Bit 0	R	TX_CELL[16]	X

TX_CELL[31:0]

The transmit cell/packet count bits (TX_CELL[31:0]) indicate the number of cells or **non-aborted** packets transmitted during the last accumulation interval. ATM Idle cells, HDLC flags, and HDLC Idle bytes inserted into the transmission stream are not counted.

A direct write to any one of the TTDP counter registers loads all the corresponding TTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the TTDP and TCAS will be updated.

Register TTDP_BASE + 6H: TTDP Indirect Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_BYTE[15]	X
Bit 14	R	TX_ BYTE [14]	X
Bit 13	R	TX_ BYTE [13]	X
Bit 12	R	TX_ BYTE [12]	X
Bit 11	R	TX_ BYTE [11]	X
Bit 10	R	TX_ BYTE [10]	X
Bit 9	R	TX_ BYTE [9]	X
Bit 8	R	TX_ BYTE [8]	X
Bit 7	R	TX_ BYTE [7]	X
Bit 6	R	TX_ BYTE [6]	X
Bit 5	R	TX_ BYTE [5]	X
Bit 4	R	TX_ BYTE [4]	X
Bit 3	R	TX_ BYTE [3]	X
Bit 2	R	TX_ BYTE [2]	X
Bit 1	R	TX_ BYTE [1]	X
Bit 0	R	TX_ BYTE [0]	X

Register TTDP_BASE + 7H: TTDP Indirect Transmit Byte Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_ BYTE [31]	X
Bit 14	R	TX_ BYTE [30]	X
Bit 13	R	TX_ BYTE [29]	X
Bit 12	R	TX_ BYTE [28]	X
Bit 11	R	TX_ BYTE [27]	X
Bit 10	R	TX_ BYTE [26]	X
Bit 9	R	TX_ BYTE [25]	X
Bit 8	R	TX_ BYTE [24]	X
Bit 7	R	TX_ BYTE [23]	X
Bit 6	R	TX_ BYTE [22]	X
Bit 5	R	TX_ BYTE [21]	X
Bit 4	R	TX_ BYTE [20]	X
Bit 3	R	TX_ BYTE [19]	X
Bit 2	R	TX_ BYTE [18]	X
Bit 1	R	TX_ BYTE [17]	X
Bit 0	R	TX_ BYTE [16]	X

TX_BYTE[31:0]

The TX_ BYTE[31:0] bits indicate the number of bytes in packets transmitted to the TTDP egress stream during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes is controlled by the TX_BYTE_MODE register bit. HDLC flags and Idle characters are not counted. The TX_BYTE[31:0] counters are only valid when processing packets.

A direct write to any one of the TTDP counter registers loads all the corresponding TTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the TTDP and TCAS will be updated.

Register TTDP_BASE + 8H: TTDP Indirect Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	TX_ABT[15]	X
Bit 14	R	TX_ABT[14]	X
Bit 13	R	TX_ABT[13]	X
Bit 12	R	TX_ABT[12]	X
Bit 11	R	TX_ABT[11]	X
Bit 10	R	TX_ABT[10]	X
Bit 9	R	TX_ABT[9]	X
Bit 8	R	TX_ABT[8]	X
Bit 7	R	TX_ABT[7]	X
Bit 6	R	TX_ABT[6]	X
Bit 5	R	TX_ABT[5]	X
Bit 4	R	TX_ABT[4]	X
Bit 3	R	TX_ABT[3]	X
Bit 2	R	TX_ABT[2]	X
Bit 1	R	TX_ABT[1]	X
Bit 0	R	TX_ABT[0]	X

TX_ABT[15:0]

The transmit aborted packet count bits (TX_ ABT[15:0]) indicate the number aborted packets transmitted to the TTDP egress stream during the last accumulation interval. These counters are only valid when packet mode is selected.

A direct write to any one of the TTDP counter registers loads all the corresponding TTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0000H can be written to initiate a global performance counter update across the S/UNI-MACH48. Note that only counters for channels that are provisioned and enabled in the TTDP and TCAS will be updated.

Register TTDP_BASE + 9H: TTDP CRC Error Mask

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	CRC_XOR[7]	0
Bit 6	R/W	CRC_XOR[6]	0
Bit 5	R/W	CRC_XOR[5]	0
Bit 4	R/W	CRC_XOR[4]	0
Bit 3	R/W	CRC_XOR[3]	0
Bit 2	R/W	CRC_XOR[2]	0
Bit 1	R/W	CRC_XOR[1]	0
Bit 0	R/W	CRC_XOR[0]	0

CRC_XOR[7:0]

The error mask CRC XOR bits (CRC_XOR[7:0]) is used in conjunction with DCRC to generate CRC errors. When DCRC is set to logic 1, the FCS byte values inserted by the POS/HDLC processor or the HCS value inserted by the ATM processor is logically XORed with CRC_XOR[7:0]. The inserted FCS or HCS is not logically XORed when DCRC is set to logic 0. DCRC is ignored when PROV is logic 0.

Register TTDP_BASE + AH: TTDP Interrupt Enable 1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R/W	XFERE	0
Bit 11	R/W	FIFO_ERRE_11	0
Bit 10	R/W	FIFO_ERRE_10	0
Bit 9	R/W	FIFO_ERRE_9	0
Bit 8	R/W	FIFO_ERRE_8	0
Bit 7	R/W	FIFO_ERRE_7	0
Bit 6	R/W	FIFO_ERRE_6	0
Bit 5	R/W	FIFO_ERRE_5	0
Bit 4	R/W	FIFO_ERRE_4	0
Bit 3	R/W	FIFO_ERRE_3	0
Bit 2	R/W	FIFO_ERRE_2	0
Bit 1	R/W	FIFO_ERRE_1	0
Bit 0	R/W	FIFO_ERRE_0	0

FIFO_ERRE_**x**

The FIFO error interrupt enable bit (FIFO_ERRE_**x**) enables the generation of a hardware interrupt due to a FIFO error condition (TERR is asserted at the POS-PHY L3 interface or SOP and EOP are at unexpected locations) for channel **x**H. When FIFO_ERRE_**x** is set to logic one, the interrupt is enabled and causes FIFO_ERRI_**x** and the output INTB to be asserted. When set to logic zero, FIFO_ERRI_**x** will be asserted but not INTB.

XFERE

The transfer interrupt enable bit (XFERE) enables the generation of a hardware interrupt when an accumulation interval is completed and new values are stored in the transmitted packet/cell counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled and causes XFERI and the output INTB to be asserted. When XFERE is set to logic 0, XFERI will be asserted, but not INTB. XFERI is the transfer interrupt associated with all provisioned channels.

Register TTDP_BASE + BH: TTDP Interrupt Enable 2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	FIFO_UDRE_11	0
Bit 10	R/W	FIFO_UDRE_10	0
Bit 9	R/W	FIFO_UDRE_9	0
Bit 8	R/W	FIFO_UDRE_8	0
Bit 7	R/W	FIFO_UDRE_7	0
Bit 6	R/W	FIFO_UDRE_6	0
Bit 5	R/W	FIFO_UDRE_5	0
Bit 4	R/W	FIFO_UDRE_4	0
Bit 3	R/W	FIFO_UDRE_3	0
Bit 2	R/W	FIFO_UDRE_2	0
Bit 1	R/W	FIFO_UDRE_1	0
Bit 0	R/W	FIFO_UDRE_0	0

FIFO_UDRE_**x**

The FIFO underrun interrupt enable bit (FIFO_UDRE_**x**) enables the generation of an interrupt due to a FIFO underrun for channel **x**H. When FIFO_UDRE_**x** is set to logic 1, the interrupt is enabled and causes FIFO_UDRI_**x** and the output INTB to be asserted. When FIFO_UDRE is set to logic 0, FIFO_UDRI_**x** will be asserted but not INTB.

Register TTDP_BASE + CH: TTDP Interrupt 1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	XFERI	X
Bit 11	R	FIFO_ERRI_11	X
Bit 10	R	FIFO_ERRI_10	X
Bit 9	R	FIFO_ERRI_9	X
Bit 8	R	FIFO_ERRI_8	X
Bit 7	R	FIFO_ERRI_7	X
Bit 6	R	FIFO_ERRI_6	X
Bit 5	R	FIFO_ERRI_5	X
Bit 4	R	FIFO_ERRI_4	X
Bit 3	R	FIFO_ERRI_3	X
Bit 2	R	FIFO_ERRI_2	X
Bit 1	R	FIFO_ERRI_1	X
Bit 0	R	FIFO_ERRI_0	X

FIFO_ERRI_**x**

The FIFO error interrupt bit (FIFO_ERRI_**x**) bit is set to one when an ERROR is detected on the read side of the FIFO for channel **x**H. An abnormal sequence of TSOP and TEOP signals or the assertion of TERR from the POS-PHY interface can cause this error. This can normally be caused by a previous FIFO overrun condition. This bit is cleared to logic 0 immediately after a read to this register

XFERI

The transfer counter complete interrupt bit (XFERI) indicates that a transfer of accumulated counter data has occurred for all provisioned channels. A logic 1 in this bit position indicates that the transmitted cell/packet counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or writing to register 0000H for a global performance monitor update. XFERI is cleared to logic 0 when this register is read.

Register TTDP_BASE + DH: TTDP Interrupt 2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	FIFO_UDRI_11	X
Bit 10	R	FIFO_UDRI_10	X
Bit 9	R	FIFO_UDRI_9	X
Bit 8	R	FIFO_UDRI_8	X
Bit 7	R	FIFO_UDRI_7	X
Bit 6	R	FIFO_UDRI_6	X
Bit 5	R	FIFO_UDRI_5	X
Bit 4	R	FIFO_UDRI_4	X
Bit 3	R	FIFO_UDRI_3	X
Bit 2	R	FIFO_UDRI_2	X
Bit 1	R	FIFO_UDRI_1	X
Bit 0	R	FIFO_UDRI_0	X

FIFO_UDRI_**x**

The FIFO underrun interrupt bit (FIFO_UDRI_**x**) bit is logic 1 when an attempt is made to read from the TXSDQ FIFO while it is empty for channel **x**H. This is considered a system error. This bit is cleared to logic 0 immediately after a read to this register.

Register TTDP_BASE + EH: TTDP Transmit Off

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	XOFF_11	X
Bit 10	R/W	XOFF _10	X
Bit 9	R/W	XOFF _9	X
Bit 8	R/W	XOFF _8	X
Bit 7	R/W	XOFF _7	X
Bit 6	R/W	XOFF _6	X
Bit 5	R/W	XOFF _5	X
Bit 4	R/W	XOFF _4	X
Bit 3	R/W	XOFF _3	X
Bit 2	R/W	XOFF _2	X
Bit 1	R/W	XOFF _1	X
Bit 0	R/W	XOFF _0	X

XOFF_**x**

The transmission off bit (XOFF_**x**) serves as a transmission enable bit for channel **x**. When channel x is provisioned and XOFF_**x** is set to logic 0, ATM cells or packets are transmitted normally. When channel **x** is provisioned and XOFF_**x** is set to logic 1, the cell or packet being transmitted is completed and then transmission is suspended. When XOFF_**x** is asserted, the TTDP will not request data from the external FIFO. ATM Idle cells or POS flags will be sent on the TTDP egress interface.

12.5 RCAS12 Register Summary

There are 4 RCAS12 blocks in the S/UNI-MACH48 device. Their base addresses (RCAS12_BASE) are: 01B0H, 01C0H, 01D0H, and 01E0H. The RCAS12 is used to map channel numbers from the STS-1 timeslots into Utopia/POS interface (RADR[5:0] values).

Each RCAS-12 block is dedicated to a range of timeslots (system side) and channel numbers (system side) for STS-12c and STS-48c data streams.

The RCAS-12 block residing in the least significant RCAS12_BASE address location is dedicated to all the timeslots shown in Table 53 and the first row of timeslots in STS-48c/STM-16c mode (RX48C = 1) and in Table 52 when not in STS-48c/STM-16c mode (RX48C = 0). The TS0 corresponds to the timeslot at the left side of each row.

The RCAS-12 block residing in the 2nd least significant RCAS12_BASE address location is dedicated to the second row of the timeslot map in Table 52 and to the channel number 12 when RX48C = 0. When RX48C = 1, all timeslots should be provisioned and enabled for channel 0.

The RCAS-12 block residing in the 3rd least significant RCAS12_BASE address location is dedicated to the third row of the timeslot map in Table 52 and to the channel number 24 when RX48C = 0. When RX48C = 1, all timeslots should be provisioned and enabled for channel 0.

The RCAS-12 block residing in the most significant RCAS12_BASE address location is dedicated to the bottom row of the timeslot map in Table 52 and to the channel number 36 when RX48C = 0. When RX48C = 1, all timeslots should be provisioned and enabled for channel 0.

Register RCAS12_BASE + 0H: RCAS12 Channel Disable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R/W	Reserved	0
Bit 11	R/W	CH11_DIS	1
Bit 10	R/W	CH10_DIS	1
Bit 9	R/W	CH9_DIS	1
Bit 8	R/W	CH8_DIS	1
Bit 7	R/W	CH7_DIS	1
Bit 6	R/W	CH6_DIS	1
Bit 5	R/W	CH5_DIS	1
Bit 4	R/W	CH4_DIS	1
Bit 3	R/W	CH3_DIS	1
Bit 2	R/W	CH2_DIS	1
Bit 1	R/W	CH1_DIS	1
Bit 0	R/W	CH0_DIS	1

CH***x***_DIS

The Channel ***x*** disable bit (CH***x***_DIS) controls the squelching of data directed to Channel ***x***. When CH***x***_DIS is logic 1, the RCAS-12 will disable transfer of any data to Channel ***x***. When CH***x***_DIS is logic 0, data is transferred to Channel ***x*** normally.

Register RCAS12_BASE + 1H: RCAS12 Channel Loopback Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R/W	OC12C_LBEN	0
Bit 11	R/W	CH11_ LBEN	0
Bit 10	R/W	CH10_ LBEN	0
Bit 9	R/W	CH9_ LBEN	0
Bit 8	R/W	CH8_ LBEN	0
Bit 7	R/W	CH7_ LBEN	0
Bit 6	R/W	CH6_ LBEN	0
Bit 5	R/W	CH5_ LBEN	0
Bit 4	R/W	CH4_ LBEN	0
Bit 3	R/W	CH3_ LBEN	0
Bit 2	R/W	CH2_ LBEN	0
Bit 1	R/W	CH1_ LBEN	0
Bit 0	R/W	CH0_LBEN	0

CH***x***_LBEN

The Channel ***x*** diagnostic loopback enable bit (CH***x***_LBEN) is used to enable a diagnostic loopback from the transmit Channel ***x*** data stream to the receive Channel ***x*** data stream. When CH***x***_LBEN is logic 1, the receive data directed to Channel ***x*** is to be over-written by data retrieved from the loopback FIFO of Channel ***x***. When CH***x***_LBEN is logic 0, the loopback is disabled.

OC12C_LBEN

The OC12C_LBEN bit should be set to logic 1 (along with the corresponding CH**x**_LBEN bit) for per-channel diagnostic loopback when the RCAS12 is processing one STS-12c channel. It should be set to logic 0 if the RCAS12 is not enabled for per-channel diagnostic loopback with an STS-12c channel.

Register RCAS12_BASE + 2H + *x*: RCAS12 Timeslot *x* Configuration (*x* = 0H to BH)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	TS***x***_MODE[2]	0
Bit 6	R/W	TS***x***_MODE[1]	0
Bit 5	R/W	TS***x***_MODE[0]	0
Bit 4	R/W	TS***x***_PROV	0
Bit 3	R/W	TS***x***_CHAN[3]	0
Bit 2	R/W	TS***x***_CHAN[2]	0
Bit 1	R/W	TS***x***_CHAN[1]	0
Bit 0	R/W	TS***x***_CHAN[0]	0

TSx_CHAN[3:0]

The TS***x***_CHAN[3:0] bits give the channel number to which the input data stream in timeslot ***x*** is directed to.

TSx_PROV

The TS***x***_PROV bit provisions and unprovisions the timeslot. When TS***x***_PROV is logic 1, the receive data stream on timeslot ***x*** is processed as part of the channel as indicated by TS***x***_CHAN[3:0]. When TS***x***_PROV is logic 0, the receive data stream on timeslot ***x*** does not belong to any channel and is ignored.

TS***x***_MODE[2:0]

The TS***x***_MODE[2:0] bits identify the type of traffic carried on timeslot ***x***. All timeslots associated with a concatenated payload channel must be set up appropriately as shown in Table 21.

Table 21 RCAS12 Timeslot Mode Selection

TS***x***_MODE[2:0]	Line Traffic Type
000	STS-12c/STM-4c
001	STS-3c/STM-1

TS*x*_MODE[2:0]	Line Traffic Type
010	STS-1/STM-0
011	DS3 HDLC
100	DS3 Direct Mapped ATM
101	DS3 PLCP ATM
110	Reserved
111	Reserved

12.6 TCAS12 Register Summary

There are 4 TCAS12 blocks in the S/UNI-MACH48 device. Their base addresses (TCAS12_BASE) are: 01F0H, 0200H, 0210H, and 0220H. The TCAS12 is used to map channel numbers from the Utopia/POS interface (TADR[5:0] values) into STS-1 timeslots.

Each TCAS-12 block is dedicated to a range of timeslots (system side) and channel numbers (system side) for STS-12c and STS-48c data streams.

The TCAS-12 block residing in the least significant TCAS12_BASE address location is dedicated to all the timeslots shown in Table 53 and the first row of timeslots in STS-48c/STM-16c mode (TX48C = 1) and in Table 52 when not in STS-48c/STM-16c mode (TX48C = 0). The TS0 corresponds to the timeslot at the left side of each row.

The TCAS-12 block residing in the 2nd least significant TCAS12_BASE address location is dedicated to the second row of the timeslot map in Table 52 and to the channel number 12 when TX48C = 0. When TX48C = 1, all timeslots should be provisioned and enabled for channel 0.

The TCAS-12 block residing in the 3rd least significant TCAS12_BASE address location is dedicated to the third row of the timeslot map in Table 52 and to the channel number 24 when TX48C = 0. When TX48C = 1, all timeslots should be provisioned and enabled for channel 0.

The TCAS-12 block residing in the most significant TCAS12_BASE address location is dedicated to the bottom row of the timeslot map in Table 52 and to the channel number 36 when TX48C = 0. When TX48C = 1, all timeslots should be provisioned and enabled for channel 0.

Register TCAS12_BASE + 0H: TCAS12 Channel Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	CH11_DIS	1
Bit 10	R/W	CH10_DIS	1
Bit 9	R/W	CH9_DIS	1
Bit 8	R/W	CH8_DIS	1
Bit 7	R/W	CH7_DIS	1
Bit 6	R/W	CH6_DIS	1
Bit 5	R/W	CH5_DIS	1
Bit 4	R/W	CH4_DIS	1
Bit 3	R/W	CH3_DIS	1
Bit 2	R/W	CH2_DIS	1
Bit 1	R/W	CH1_DIS	1
Bit 0	R/W	CH0_DIS	1

CH***x***_DIS

The Channel ***x*** disable bit (CH***x***_DIS) disables Channel ***x***. When CH***x***_DIS is logic 1, the TCAS-12 will cease requesting data from the upstream block and FDATA[7:0] is inserted onto the timeslot. When CH***x***_DIS is logic 0, the TCAS-12 will request data from the upstream block for Channel ***x*** normally.

Register TCAS12_BASE + 1H: TCAS12 OALARM Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	CH11_OALARM	0
Bit 10	R/W	CH10_OALARM	0
Bit 9	R/W	CH9_OALARM	0
Bit 8	R/W	CH8_OALARM	0
Bit 7	R/W	CH7_OALARM	0
Bit 6	R/W	CH6_OALARM	0
Bit 5	R/W	CH5_OALARM	0
Bit 4	R/W	CH4_OALARM	0
Bit 3	R/W	CH3_OALARM	0
Bit 2	R/W	CH2_OALARM	0
Bit 1	R/W	CH1_OALARM	0
Bit 0	R/W	CH0_OALARM	0

CH***x***_OALARM

The Channel ***x*** output alarm bit (CH***x***_OALARM) is used to assert the OALARM output of the S/UNI-MACH48. When set to logic 1, the corresponding OALARM[x] signal will be asserted during the timeslots associated with the channel. When set to logic 0, the corresponding OALARM[x] signal will not be asserted during the timeslots associated with the channel.

Register TCAS12_BASE + 2 + *x*: TCAS12 Timeslot *x* Configuration (*x* = 0H to BH)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	LOCK0	0
Bit 7	R/W	TS***x*** _MODE[2]	0
Bit 6	R/W	TS***x*** _MODE[1]	0
Bit 5	R/W	TS***x*** _MODE[0]	0
Bit 4	R/W	TS***x*** _PROV	0
Bit 3	R/W	TS***x*** _CHAN[3]	0
Bit 2	R/W	TS***x*** _CHAN[2]	0
Bit 1	R/W	TS***x*** _CHAN[1]	0
Bit 0	R/W	TS***x*** _CHAN[0]	0

TS***x***_CHAN[3:0]

The TS***x***_CHAN[3:0] bits give the channel number from which the data stream in timeslot ***x*** is taken from.

TS***x***_PROV

The TS***x***_PROV bit provisions and unprovisions the timeslot. When TS***x***_PROV is logic 1, data to timeslot ***x*** is processed as part of the channel as indicated by TS***x***_CHAN[3:0]. When TS***x***_PROV is logic 0, the data transmitted on timeslot ***x*** is taken from the TCAS-12's FDATA[7:0] register bit settings instead of from the upstream block.

TS***x***_MODE[2:0]

The TS***x***_MODE[2:0] bits identify the type of traffic carried on timeslot ***x***. All timeslots associated with a concatenated payload channel must be set up appropriately as shown in Table 22.

Table 22 TCAS12 Timeslot Mode Selection

TS*x*_MODE[2:0]	Line Traffic Type
000	STS-12c/STM-4c
001	STS-3c/STM-1
010	STS-1/STM-0
011	DS3 HDLC
100	DS3 Direct Mapped ATM
101	DS3 PLCP ATM
110	Reserved
111	Reserved

LOCK0

The LOCK0 bit controls the payload offset of the outgoing data stream in the locked mode. When LOCK0 is set to logic 1, the J1 byte in the outgoing data stream is forced to the byte immediately following the H3 bytes (pointer offset = 0). When LOCK0 is logic 0, the J1 byte is forced to the byte immediately following the J0 byte (pointer offset = 522). For either setting of LOCK0, the outgoing H1 and H2 bytes will be valid.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Register TCAS12_BASE + EH: TCAS12 Idle Timeslot Fill Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	FDATA[7]	1
Bit 6	R/W	FDATA[6]	1
Bit 5	R/W	FDATA[5]	1
Bit 4	R/W	FDATA[4]	1
Bit 3	R/W	FDATA[3]	1
Bit 2	R/W	FDATA[2]	1
Bit 1	R/W	FDATA[1]	1
Bit 0	R/W	FDATA[0]	1

This register contains the data to be written to disabled timeslots.

FDATA[7:0]

The fill data bits (FDATA[7:0]) are transmitted during unprovisioned timeslots (TS***x***_PROV) or timeslots connected to disabled channels (CH***x***_DIS). or serial links.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

12.7 DS3 Register Summary

There are 48 identical Functional Partitions of DS3 blocks. Each DS3 block contains a SPLR, PLCP PMON, DS3 FRMR, RBOC, RDLC, DS3 PMON, D3MD, SPLT, DS3 TRAN, XBOC, TDPR, and D3MA. These blocks perform PLCP framing, PLCP performance monitor counting, DS3 framing, Bit Oriented Code detection, DS3 Facility Data Link extraction, DS3 performance monitor counting, STS-1 to DS3 demapping, PLCP transmission, DS3 transmission, Bit Oriented Code transmission, DS3 Facility Data Link insertion, and DS3 to STS-1 mapping respectively.

The DS3 blocks have base addresses (DS3_BASE) of:

Table 23 DS3 Base Address Assignment

Timeslot Location	DS3_BASE
S1,1 S2,1 S3,1 S4,1 S1,2 S2,2 S3,2 S4,2 S1,3 S2,3 S3,3 S4,3	0230H, 0290H, 02F0H, 0350H, 03B0H, 0410H, 0470H, 04D0H, 0530H, 0590H, 05F0H, 0650H
S5,1 S6,1 S7,1 S8,1 S5,2 S6,2 S7,2 S8,2 S5,3 S6,3 S7,3 S8,3	06B0H, 0710H, 0770H, 07D0H, 0830H, 0890H, 08F0H, 0950H, 09B0H, 0A10H, 0A70H, 0AD0H
S9,1 S10,1 S11,1 S12,1 S9,2 S10,2 S11,2 S12,2 S9,3 S10,3 S11,3 S12,3	0B30H, 0B90H, 0BF0H, 0C50H, 0CB0H, 0D10H, 0D70H, 0DD0H, 0E30H, 0E90H, 0EF0H, 0F50H
S13,1 S14,1 S15,1 S16,1 S13,2 S14,2 S15,2 S16,2 S13,3 S14,3 S15,3 S16,3	0FB0H, 1010H, 1070H, 10D0H, 1130H, 1190H, 11F0H, 1250H, 12B0H, 1310H, 1370H, 13D0H

There is only a single DS3 PRBS generation/detection block, the PRGD, so it is not part of any DS3 block. It starts at address 1500H.

Each DS3 block is dedicated to a range of timeslots (line side) and channel numbers (system side).

The DS3 block residing in the 12 least significant DS3_BASE address locations are dedicated to the first row of the timeslot maps shown in Table 52. The DS3 block residing in the least significant DS3_BASE address is dedicated to the leftmost timeslot. It can be allocated to any of the least significant channel numbers (0 – 11).

The DS3 block residing in the most significant DS3_BASE address locations are dedicated to the bottom row of the timeslot maps shown in Table 52. The DS3 block residing in the most significant DS3_BASE address is dedicated to the rightmost timeslot. It can be allocated to any of the most significant channel numbers (36 – 47). The operation is identical for the other DS3_BASE address locations.

Register DS3_BASE + 0H: SPLR Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REFRAME	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	Reserved	0

Reserved

The Reserved bit must be set to logic 0 for proper operation.

PLCPEN

The PLCPEN bit enables PLCP framing. When a logic 1 is written to PLCPEN, PLCP framing is enabled. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLR block are disabled.

REFRAME

The REFRAME bit is used to trigger reframing. When a logic 1 is written to REFRAME, the S/UNI-MACH48 is forced out of PLCP frame and a new search for frame alignment is initiated. Note that only a logic 0 to logic 1 transition of the REFRAME bit triggers reframing; multiple write operations are required to ensure such a transition.

FORM[1:0]

The FORM[1:0] bits select the PLCP frame format as shown below.

Table 24 SPLR FORM[1 0] Configurations

FORM[1]	FORM[0]	PLCP Framing Format
0	0	DS3
0	1	Reserved
1	0	Reserved
1	1	Reserved

Register DS3_BASE + 1H: SPLR Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	FEBEE	0
Bit 5	R/W	COLSSE	0
Bit 4	R/W	BIPEE	0
Bit 3	R/W	FEE	0
Bit 2	R/W	YELE	0
Bit 1	R/W	LOFE	X
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit enables interrupt generation when a PLCP out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

LOFE

The LOFE bit enables interrupt generation when a PLCP loss of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

YELE

The YELE bit enables interrupt generation when a PLCP yellow alarm defect is declared or removed. The interrupt is enabled when a logic 1 is written.

FEE

The FEE bit enables interrupt generation when the SPLR detects a PLCP framing octet error. The interrupt is enabled when a logic 1 is written.

BIPEE

The BIPEE bit enables interrupt generation when the SPLR detects a PLCP bit interleaved parity error. The interrupt is enabled when a logic 1 is written.

COLSSE

The COLSSE bit enables interrupt generation when the SPLR detects a change of PLCP link status. The interrupt is enabled when a logic 1 is written.

FEBEE

The FEBEE bit enables interrupt generation when the SPLR detects a PLCP far end block error. The interrupt is enabled when a logic 1 is written.

Register DS3_BASE + 2H: SPLR Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	FEBEI	X
Bit 5	R	COLSSI	X
Bit 4	R	BIPEI	X
Bit 3	R	FEI	X
Bit 2	R	YELI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI

The OOFI bit is set to logic 1 when a PLCP out of frame defect is detected or removed. The OOF defect state is contained in the SPLR Status Register. The OOFI bit position is set to logic 0 when this register is read.

LOFI

The LOFI bit is set to logic 1 when a PLCP loss of frame defect is detected or removed. The LOF defect state is contained in the SPLR Status Register. The LOFI bit position is set to logic 0 when this register is read.

YELI

The YELI bit is set to logic 1 when a PLCP yellow alarm defect is detected or removed. The yellow alarm defect state is contained in the SPLR Status Register. The YELI bit position is set to logic 0 when this register is read.

FEI

The FEI bit is set to logic 1 when a PLCP framing octet error is detected. A framing octet error is generated when one or more errors are detected in the framing alignment octets (A1, and A2), or the path overhead identification octets. The FEI bit position is set to logic 0 when this register is read.

BIPEI

The BIPEI bit is set to logic 1 when a PLCP bit interleaved parity (BIP) error is detected. BIP errors are detected using the B1 byte in the PLCP path overhead. The BIPEI bit position is set to logic 0 when this register is read.

COLSSI

The COLSSI bit is set to logic 1 when a PLCP change of link status signal code is detected. The link status signal code is contained in the path status octet (G1). Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. A change of link status event occurs when two consecutive and identical link status codes are received that differ from the current code. The COLSSI bit position is set to logic 0 when this register is read.

FEBEI

The FEBEI bit is set to logic 1 when a PLCP far end block error (FEBE) is detected. FEBE errors are indicated in the PLCP path status octet (G1). The FEBEI bit position is set to logic 0 when this register is read.

Register DS3_BASE + 3H: SPLR Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	LSS[2]	X
Bit 5	R	LSS[1]	X
Bit 4	R	LSS[0]	X
Bit 3		Unused	X
Bit 2	R	YELV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV

The OOFV bit indicates the current PLCP out of frame defect state. When an error is detected in both the A1 and A2 octets or when an error is detected in two consecutive path overhead identifier octets, OOFV is set to logic 1. When the SPLR has found two valid, consecutive sets of A1 and A2 octets with two valid and sequential path overhead identifier octets, the OOFV bit is set to logic 0.

LOFV

The LOFV bit indicates the current PLCP loss of frame defect state. The loss of frame defect state is an integrated version of the out of frame defect state. The declaration/removal times for the loss of frame defect state is summarized in the table below:

Table 25 PLCP LOF Declaration/Removal Times

PLCP Format	Declaration (ms)	Removal (ms)
DS3	1	12

If the OOF defect state is transient, the LOF counter is decremented at a rate 1/12 (DS3 PLCP) of the incrementing rate.

YELV

The YELV bit indicates the current PLCP yellow alarm defect state. YELV is set to a logic 1 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 1. YELV is set to a logic 0 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 0.

LSS[2:0]

The LSS[2:0] bits contain the current link status signal code. Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. LSS[2:0] is updated when two consecutive and identical link status signal codes are received.

Register DS3_BASE + 4H: SPLT Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	M1TYPE	0
Bit 4	R/W	M2TYPE	0
Bit 3	R/W	FIXSTUFF	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	EXT	0

EXT

The EXT bit must be set to logic 0 for proper operation.

PLCPEN

The PLCPEN bit enables PLCP frame insertion. When a logic 1 is written to PLCPEN, DS3 PLCP framing is inserted. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLT block are disabled.

FIXSTUFF

The FIXSTUFF bit controls the transmit PLCP frame octet/nibble stuffing used for DS3 PLCP frame formats. When a logic 0 is written to FIXSTUFF, stuffing is determined by the REF8K input. When a logic 1 is written to FIXSTUFF and the DS3 PLCP frame format is enabled, a nibble is stuffed into the 13 nibble trailer twice every three stuff opportunities (i.e. 13, 14, 14 nibbles). This stuff ratio provides for a nominal PLCP frame rate of 125.0002366 µs (an error of 1.9 ppm).

M2TYPE

The M2TYPE bit selects the type of code transmitted in the M2 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M2TYPE, the fixed pattern type 0 code is transmitted in the M2 octet. When a logic 1 is written to M2TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M2 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

M1TYPE

The M1TYPE bit selects the type of code transmitted in the M1 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M1TYPE, the fixed pattern type 0 code is transmitted in the M1 octet. When a logic 1 is written to M1TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M1 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

FORM[1:0]

When PLCPEN = 0, the FORM[1:0] bits select the ATM direct-mapped transmission frame format as shown below. When PLCPEN = 1, the FORM[1:0] bits select the transmission and PLCP frame format as shown below.

Table 26 SPLT FORM[1 0] Configurations

FORM[1]	FORM[0]	PLCP or ATM Direct-mapped Framing Format / Cell Alignment
0	0	DS3 / nibble
0	1	Reserved
1	0	Reserved
1	1	Reserved

Register DS3_BASE + 5H: SPLT Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	SRCF1	0
Bit 4	R/W	SRCB1	0
Bit 3	R/W	SRCG1	0
Bit 2	R/W	SRCM1	0
Bit 1	R/W	SRCM2	0
Bit 0	R/W	SRCC1	0

SRCC1

The SRCC1 bit value selects the source for the C1 octet. If SRCC1 is logic 0, the C1 bit position is derived internally as specified by the FIXSTUFF bit in the SPLT Configuration Register. If SRCC1 is logic 1, the C1 bit position is set to logic 0.

SRCM2

The SRCM2 bit value selects the source for the M2 octet. If SRCM2 is logic 0, the M2 bit position is derived internally as specified by the M2TYPE bit in the SPLT Configuration Register. If SRCM2 is logic 1, the M2 octet is set to logic 0 (as required by the ATM Forum User Network Interface specification).

SRCM1

The SRCM1 bit value selects the source for the M1 octet. If SRCM1 is logic 0, the M1 bit position is derived internally as specified by the M1TYPE bit in the SPLT Configuration Register. If SRCM1 is logic 1, the M1 octet is set to logic 0 (as required by the ATM Forum User Network Interface specification).

SRCG1

The SRCG1 bit value selects the source for the G1 octet. If SRCG1 is logic 0, the G1 bit position is derived internally as required. If SRCG1 is logic 1, the G1 byte is set to logic 0.

SRCB1

The SRCB1 bit selects the source for the B1 octet. If SRCB1 is logic 0, the internally calculated bit interleaved parity value is inserted in the B1 byte. If SRCB1 is logic 0, the B1 byte is set to logic 0.

SRCF1

The SRCF1 bit value selects the source for the F1 octet. If SRCF1 is logic 0, the F1 bit position is determined by the SPLT F1 Octet Register. If SRCF1 is logic 1, the F1 byte is set to logic 0.

Reserved

The Reserved bit must be programmed to logic 0 for proper operation.

Register DS3_BASE + 6H: SPLT Diagnostics and G1 Octet

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	DPFRM	0
Bit 6	R/W	DAFRM	0
Bit 5	R/W	DB1	0
Bit 4	R/W	DFEBE	0
Bit 3	R/W	YEL	0
Bit 2	R/W	LSS[2]	0
Bit 1	R/W	LSS[1]	0
Bit 0	R/W	LSS[0]	0

LSS[2:0]

The LSS[2:0] bits control the value inserted in the link status signal code bit positions of the path status octet (G1). These bits should be written with logic 0 when implementing an ATM Forum UNI-compliant DS3 interface.

YEL

The YEL bit controls the yellow signal bit position in the path status octet (G1). When a logic 1 is written to YEL, the PLCP yellow alarm signal is transmitted.

DFEBE

The DFEBE bit controls the insertion of far end block errors in the PLCP frame. When DFEBE is written with a logic 1, a single FEBE is inserted each PLCP frame. When DFEBE is written with a logic 0, FEBEs are indicated based on receive PLCP bit interleaved parity errors.

DB1

The DB1 bit controls the insertion of bit interleaved parity (BIP) errors in the PLCP frame. When DB1 is written with a logic 1, a single BIP error is inserted in each PLCP frame. When DB1 is written with a logic 0, the bit interleaved parity is calculated and inserted normally.

DAFRM

The DAFRM bit controls the insertion of frame alignment pattern errors. When DAFRM is written with a logic 1, a single bit error is inserted in each A1 octet, and in each A2 octet. When DAFRM is written with a logic 0, the frame alignment pattern octets are inserted normally.

DPFRM

The DPFRM bit controls the insertion of parity errors in the path overhead identification (POHID) octets. When DPFRM is written with a logic 1, a parity error is inserted in each POHID octet. When DPFRM is written with a logic 0, the POHID octets are inserted normally.

Register DS3_BASE + 7H: SPLT F1 Octet

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	F1[7]	0
Bit 6	R/W	F1[6]	0
Bit 5	R/W	F1[5]	0
Bit 4	R/W	F1[4]	0
Bit 3	R/W	F1[3]	0
Bit 2	R/W	F1[2]	0
Bit 1	R/W	F1[1]	0
Bit 0	R/W	F1[0]	0

F1[7:0]

The F1[7:0] bits contain the value inserted in the path user channel octet (F1). F1[7] is the most significant bit, and is transmitted first. F1[0] is the least significant bit and is the last bit transmitted in the octet.

Register DS3_BASE + 8H: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M308	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE

The CBE bit enables the DS3 C-bit parity application. When a logic 1 is written to CBE, C-bit parity mode is enabled. While the C-bit parity application is enabled, C-bit parity error events, far end block errors are accumulated. **The CBE bit must be set to logic 1 for normal operation**.

AISC

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR

The REFR bit initiates a DS3 reframe. When a logic 1 is written to REFR, the DS3 FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI

The UNI bit must be written to logic 1 for proper DS3 operation.

M3O8

The M3O8 bit controls the DS3 out of frame decision criteria. When a logic 1 is written to M3O8, DS3 out of frame is declared when 3 of 8 framing bits (F-bits) are in error. When a logic 0 is written to M3O8, the 3 of 16 framing bits in error criteria is used, as recommended in ANSI T1.107

MBDIS

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT

The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register DS3_BASE + 9H: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bit must be set to logic 0 for proper operation.

OOFE

The OOFE bit enables interrupt generation when a DS3 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

IDLE

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

FERFE

The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

CBITE

The CBITE bit enables interrupt generation when the DS3 FRMR detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic 1 is written.

REDE

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is logic 0 when the state of the RED indication changes.

COFAE

The COFAE bit enables interrupt generation when the DS3 FRMR detects a DS3 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Register DS3_BASE + 9H: DS3 FRMR Additional Configuration Register (ACE=1)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bit must be set to logic 0 for proper operation.

AISONES

The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:

Table 27 DS3 FRMR AIS Configurations

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern in the payload, C-bits all logic 0, and X-bits=1. This can be detected by setting both AISPAT and AISC high, and declaring AIS only when AISV=1 and FERFV=0 (Register x33H).
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register DS3_BASE + AH: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0		Unused	X

OOFI

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI

The AISI bit is set to logic 1 when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

IDLI

The IDLI bit is set to logic 1 when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic 0 when this register is read.

FERFI

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

CBITI

The CBITI bit is set to logic 1 when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic 0 when this register is read.

REDI

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Register DS3_BASE + BH: DS3 FRMR Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0		Unused	X

OOFV

The OOFV bit indicates the current DS3 out of frame defect state. When the DS3 FRMR has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the DS3 FRMR has found frame alignment, the OOFV bit is set to logic 0.

AISV

The AISV bit indicates the alarm indication signal state. When the DS3 FRMR detects the AIS maintenance signal, AISV is set to logic 1.

IDLV

The IDLV bit indicates the IDLE signal state. When the DS3 FRMR detects the IDLE maintenance signal, IDLV is set to logic 1.

FERFV

The FERFV bit indicates the current far end receive failure defect state. When the DS3 FRMR detects an M-frame with the X1 and X2 bits both set to zero, FERFV is set to logic 1. When the DS3 FRMR detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic 0.

CBITV

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic 1 (indicating the presence of the C-bit parity application) when the AIC bit is logic 1 for 63 consecutive M-frames. CBITV is set to logic 0 (indicating the presence of the M23 or SYNTRAN applications) when AIC is logic 0 for 2 or more M-frames in the last 15.

REDV

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR frame alignment acquisition circuitry has been out of frame for 2.23ms (or for 13.5ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23ms (or 13.5ms if FDET=0).

ACE

The ACE bit selects the Additional Configuration Register. This register is located at address DS3_BASE + 9H, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at address DS3_BASE + 9H.

Register DS3_BASE + CH: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	CBIT	0

CBIT

The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic 1, C-bit parity is enabled, and the DS3 TRAN modifies the C-bits as required to include the path maintenance data link, the FEAC channel, the far end block error indication, and the path parity. **The CBIT bit must be written wth logic 1 for normal operation**.

Reserved

The reserved bits must be programmed to logic 0 for proper operation.

FERF

The FERF bit enables insertion of the far end receive failure maintenance signal in the DS3 stream. When FERF is written with a logic 1, the X1 and X2 overhead bit positions are set to logic 0. When FERF is written with a logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.

IDL

The IDL bit enables insertion of the idle maintenance signal in the DS3 stream. When IDL is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1100.... The DS3 overhead bit insertion (X, P, M F, and C) continues normally. When IDL is written with a logic 0, the idle signal is not inserted.

AIS

The AIS bit enables insertion of the AIS maintenance signal in the DS3 stream. When AIS is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1010.... The DS3 overhead bit insertion (X, P, M and F) continues normally. The values inserted in the C-bits during AIS transmission are controlled by the CBTRAN bit in this register. When AIS is written with a logic 0, the AIS signal is not inserted.

CBTRAN

The CBTRAN bit controls the C-bit values during AIS transmission. When CBTRAN is written with a logic 0, the C-bits are overwritten with zeros during AIS transmission as specified in ANSI T1.107. When CBTRAN is written with a logic 1, C-bit insertion continues normally (as controlled by the CBIT bit in this register) during AIS transmission.

Register DS3_BASE + DH: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	X
Bit 1	R/W	DPERR	X
Bit 0	R/W	DFEBE	0

DFEBE

The DFEBE bit controls the insertion of far end block errors in the DS3 stream. When DFEBE is written with a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0. When DFEBE is written with a logic 0, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR

The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic 1, the P-bits are inverted before insertion. When DPERR is written with a logic 0, the parity is calculated and inserted normally.

DCPERR

The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic 1 and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic 0, the path parity is calculated and inserted normally.

DMERR

The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic 1, the M-bits are inverted before insertion. When DMERR is written with a logic 0, the M-bits are inserted normally.

DFERR

The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic 1, the F-bits are inverted before insertion. When DFERR is written with a logic 0, the F-bits are inserted normally.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

Register DS3_BASE + 10H: RDLC Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN

The EN bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled. When RDLC is disabled, the RDLC FIFO buffer and interrupts are all cleared. When RDLC is enabled, it will immediately begin looking for flags.

TR

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic 0.

MM

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when performing the address comparison.

MEN

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the RDLC FIFO.

Reserved

This register bit should be set to logic 0 for proper operation.

Register DS3_BASE + 11H: RDLC Interrupt Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. The value of INTC[6:0] = ‘b0000000 sets the interrupt FIFO fill level to 128.

INTE

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC will not assert INTB.

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register DS3_BASE + 12H: RDLC Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/40th that of the SYSCLK.

INTR

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control Register is set to logic 1, a RDLC interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

1. The number of bytes specified in the RDLC Interrupt Control register have been received on the data link and written into the FIFO

2. RDLC FIFO buffer overrun has been detected

3. The last byte of a packet has been written into the RDLC FIFO

4. The last byte of an aborted packet has been written into the RDLC FIFO

5. Transition of receiving all ones to receiving flags has been detected.

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in the following table:

Table 28 RDLC PBS[2 0] Data Status

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC Status Register is read.

COLS

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register DS3_BASE + 13H: RDLC Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than $1/40^{th}$ that of SYSCLK.

RD[7:0]

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status Register is read.

Register DS3_BASE + 14H: RDLC Primary Address Match

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register DS3_BASE + 15H: RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Register DS3_BASE + 18H: TDPR Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/32nd that of SYSCLK.

EN

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN bit is set to logic 0, the TDPR is disabled and an all 1's Idle sequence is transmitted on the datalink.

Reserved

The Reserved bits should be set to their default values for proper operation.

ABT

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the TDPR FIFO is transmitted. The TDPR FIFO is then reset. All data in the TDPR FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

EOM

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared upon a write to the TDPR Transmit Data register.

FIFOCLR

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHARE

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, then separate closing and opening flags are inserted between successive frames.

Register DS3_BASE + 19H: TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

Register DS3_BASE + 1AH: TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

Register DS3_BASE + 1BH: TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE

The LFILLE enables a transition to logic 1 on LFILLI to generate an interrupt on INTB. If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB. If LFILLE is a logic 0, a transition to logic 1 on LFILLI will not generate an interrupt on INTB.

UDRE

The UDRE enables a transition to logic 1 on UDRI to generate an interrupt on INTB. If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB. If UDRE is a logic 0, a transition to logic 1 on UDRI will not generate an interrupt on INTB.

OVRE

The OVRE enables a transition to logic 1 on OVRI to generate an interrupt on INTB. If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB. If OVRE is a logic 0, a transition to logic 1 on OVRI will not generate an interrupt on INTB.

FULLE

The FULLE enables a transition to logic 1 on FULLI to generate an interrupt on INTB. If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB. If FULLE is a logic 0, a transition to logic 1 on FULLI will not generate an interrupt on INTB.

Reserved

This bit should be set to logic 0 for proper operation.

Register DS3_BASE + 1CH: TDPR Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4		Unused	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/32nd that of SYSCLK.

LFILLI

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

BLFILL

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register DS3_BASE + 1DH: TDPR Transmit Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/32nd that of SYSCLK.

TD[7:0]

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Register DS3_BASE + 20H: RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE

The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic 1 is written to FEACE, the interrupt generation is enabled.

AVC

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic 0 is written to AVC, a FEAC code is validated when 8 out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received code do not match the validated code.

When a logic 1 is written to AVC, a FEAC code is validated when 4 out of the last 5 received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic 1 is written to IDLE, the interrupt generation is enabled.

Register DS3_BASE + 21H: RBOC Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]

The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all ones ("111111") when no code has been validated.

FEACI

The FEACI bit is set to logic 1 when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic 0 when this register is read.

IDLI

The IDLI bit is set to logic 1 when a validated FEAC code is removed. The FEAC[5:0] bits are set to all ones when the code is removed. The IDLI bit position is set to logic 0 when this register is read.

Register DS3_BASE + 24H: XBOC Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	BOCSMPI	X
Bit 6	R/W	BOCSMPE	0
Bit 5	R	RDY	X
Bit 4		Unused	X
Bit 3	R/W	RPT[3]	0
Bit 2	R/W	RPT[2]	0
Bit 1	R/W	RPT[1]	0
Bit 0	R/W	RPT[0]	0

RPT[3:0]

These bits contain the 4 bit repeat count (N-1) used to determine the number (N) of consecutive, identical, 16-bit bit oriented code patterns to be transmitted before sampling the XBOC BOC register again. In the event that the BOC code value does not change, the same bit oriented code pattern will be repeated continuously. The RPT[3:0] bits can be changed at any time, and are sampled at the same time as the XBOC BOC register. To change the BOC code at the end of each repetition, the RPT[3:0] and BC[5:0] values should be updated and stable within N*16 - 3 BOC code bit periods of the BOCSMPI transitioning to logic 1 while RDY is logic 1, where N is the number of times the BOC code is to be repeated.

RDY

The RDY bit is set to logic 1 when the BOC Code Register and RPT[3:0] are sampled by the XBOC, indicating that the XBOC is ready to be up updated with a new BOC. Whenever BC[5:0] is updated, the RDY bit goes low, indicating that the new BOC has not yet been accepted by the XBOC state machine.

BOCSMPE

Setting BOCSMPE to logic 1 enables a hardware interrupt to be generated on INTB when BOCSMPI transitions to logic 1.

BOCSMPI

The BOCSMPI bit is set to logic 1 when the BOC Code Register and RPT[3:0] are sampled by the XBOC, indicating that the BOC code register is ready to be updated with a new value. Whenever the BOC Control Register is read, the BOCSMPI bit is cleared.

Register DS3_BASE + 25H: XBOC Bit Oriented Code

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BC[5]	1
Bit 4	R/W	BC[4]	1
Bit 3	R/W	BC[3]	1
Bit 2	R/W	BC[2]	1
Bit 1	R/W	BC[1]	1
Bit 0	R/W	BC[0]	1

BC[5:0]

These bits are the 6-bit BOC to be transmitted. Setting all of the BC[5:0] bits to logic 1 disables BOC transmission and an all 1's signal is transmitted on the DS3 FEAC bits. To change the BOC code at the end of each repetition, the RPT[3:0] and BC[5:0] values should be updated and stable within N*16 - 3 BOC code bit periods of the BOCSMPI transitioning to logic 1 while RDY is logic 1, where N is the number of times the BOC code is to be repeated.

Register DS3_BASE + 31H: DS3 PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR

The OVR bit indicates the overrun status of the PMON holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR

The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE

The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register DS3_BASE + 36H: DS3 PMON Framing Bit Error Event Count (LSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[1]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register DS3_BASE + 37H: DS3 PMON Framing Bit Error Event Count (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]

FERR[9:0] represents the number of DS3 F-bit and M-bit errors that have been detected since the last time the framing error counter was polled.

The counter (and all other counters in the DS3 PMON) is polled by writing to any of the PMON register addresses (DS3_BASE + 0x34H to DS3_BASE + 0x3FH) or to the S/UNI-MACH48 Global Monitor Update register (0000H). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes approximately 255 DS3 clock cycles which are generated from demapping from an STS-1 timeslot.

This counter is paused when the corresponding framer has lost frame alignment.

Register DS3_BASE + 3AH: DS3 PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register DS3_BASE + 3BH: DS3 PMON Parity Error Event Count (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]

PERR[15:0] represents the number of DS3 P-bit errors that have been detected since the last time the parity error counter was polled.

The counter (and all other counters in the DS3 PMON) is polled by writing to any of the PMON register addresses (DS3_BASE + 0x34H to DS3_BASE + 0x3FH) or to the S/UNI-MACH48 Global Monitor Update register (0000H). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes approximately 255 DS3 clock cycles which are generated from demapping from an STS-1 timeslot.

This counter is paused when the corresponding framer has lost frame alignment.

Register DS3_BASE + 3CH: DS3 PMON Path Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register DS3_BASE + 3DH: DS3 PMON Path Parity Error Event Count (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

CPERR[13:0]

CPERR[13:0] represents the number of DS3 path parity errors that have been detected since the last time the DS3 path parity error counter was polled.

The counter (and all other counters in the DS3 PMON) is polled by writing to any of the PMON register addresses (DS3_BASE + 0x34H to DS3_BASE + 0x3FH) or to the S/UNI-MACH48 Global Monitor Update register (0000H). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes approximately 255 DS3 clock cycles which are generated from demapping from an STS-1 timeslot.

This counter is paused when the corresponding framer has lost frame alignment.

Register DS3_BASE + 3EH: DS3 PMON FEBE Event Count (LSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register DS3_BASE + 3FH: DS3 PMON FEBE Event Count (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[13:0]

FEBE[13:0] represents the number of DS3 far end block errors that have been detected since the last time the FEBE error counter was polled.

The counter (and all other counters in the DS3 PMON) is polled by writing to any of the PMON register addresses (DS3_BASE + 0x34H to DS3_BASE + 0x3FH) or to the S/UNI-MACH48 Global Monitor Update register (0000H). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes approximately 255 DS3 clock cycles which are generated from demapping from an STS-1 timeslot.

This counter is paused when the corresponding framer has lost frame alignment.

Register DS3_BASE + 41H: PLCP PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR

The OVR bit indicates the overrun status of the PLCP PMON holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR

The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE

The INTE bit enables the generation of an interrupt when the PLCP PMON counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register DS3_BASE + 48H: PLCP PMON FEBE Count (LSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[1]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register DS3_BASE + 49H: PLCP PMON FEBE Count (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FEBE[15]	X
Bit 6	R	FEBE[14]	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[15:0]

FEBE[15:0] represents the number of PLCP far end block errors (FEBE) that have been detected since the last time this FEBE error counter was polled.

The counter (and all other counters in the PLCP PMON) is polled by writing to any of the PMON register addresses (DS3_BASE + 0x44H to DS3_BASE + 0x4FH) or to the S/UNI-MACH48 Global Monitor Update register (0000H). Such a write transfers the internally accumulated count to the FEBE Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes approximately 95 DS3 clock cycles (1.5µs) which are generated from demapping from an STS-1 timeslot.

FEBE errors are not accumulated when the SPLR has declared a PLCP out of frame defect state.

Register DS3_BASE + 4AH: PLCP PMON B1 Error Count LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	B1E[7]	X
Bit 6	R	B1E[6]	X
Bit 5	R	B1E[5]	X
Bit 4	R	B1E[4]	X
Bit 3	R	B1E[3]	X
Bit 2	R	B1E[2]	X
Bit 1	R	B1E[1]	X
Bit 0	R	B1E[0]	X

Register DS3_BASE + 4BH: PLCP PMON B1 Error Count (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	B1E[15]	X
Bit 6	R	B1E[14]	X
Bit 5	R	B1E[13]	X
Bit 4	R	B1E[12]	X
Bit 3	R	B1E[11]	X
Bit 2	R	B1E[10]	X
Bit 1	R	B1E[9]	X
Bit 0	R	B1E[8]	X

B1E[15:0]

B1E[15:0] represents the number of PLCP bit interleaved parity (BIP) errors that have been detected since the last time the B1 error counter was polled.

The counter (and all other counters in the PLCP PMON) is polled by writing to any of the PMON register addresses (DS3_BASE + 0x44H to DS3_BASE + 0x4FH) or to the S/UNI-MACH48 Global Monitor Update register (0000H). Such a write transfers the internally accumulated count to the FEBE Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes approximately 95 DS3 clock cycles (1.5µs) which are generated from demapping from an STS-1 timeslot.

B1E errors are not accumulated when the SPLR has declared a PLCP out of frame defect state.

Register DS3_BASE + 4CH: PLCP PMON Framing Error Event Count LSB

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register DS3_BASE + 4DH: PLCP PMON Framing Error Event Count (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FE[13]	X
Bit 4	R	FE[12]	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[13:0]

FE[13:0] represents the number of PLCP framing pattern octet errors and path overhead identification octet errors that have been detected since the last time the framing error event counter was polled.

The counter (and all other counters in the PLCP PMON) is polled by writing to any of the PMON register addresses (DS3_BASE + 0x44H to DS3_BASE + 0x4FH) or to the S/UNI-MACH48 Global Monitor Update register (0000H). Such a write transfers the internally accumulated count to the FEBE Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes approximately 95 DS3 clock cycles (1.5µs) which are generated from demapping from an STS-1 timeslot.

FE errors are not accumulated when the SPLR has declared a PLCP out of frame defect state.

Register DS3_BASE + 50H: D3MD Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	AISGEN	0

AISGEN

The active high DS3 Alarm Indication Signal enable bit (AISGEN) configures the D3MD to generate a DS3 AIS signal. Any data on the STS-1 SPE is lost due to the assertion of AISGEN. AISGEN is valid only in DS3 mode.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

Register DS3_BASE + 51H: D3MD Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	X
Bit 0	R	UFLI	X

UFLI

When logic 1, this bit indicates that an underflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

OFLI

When logic 1, this bit indicates that an overflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

The OFLI and UFLI bits and the interrupt are cleared when this register is read by the microprocessor interface.

Register DS3_BASE + 52H: D3MD Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

UFLIEN

When set to logic 1, UFLIEN enables generation of an interrupt if an elastic store underflow condition occurs (UFLI=’1’).

OFLIEN

When set to logic 1, OFLIEN bit enables generation of an interrupt if an elastic store overflow condition occurs (OFLI=’1’).

Register DS3_BASE + 54H: D3MA Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RBSO	0
Bit 0	R/W	AISGEN	0

AISGEN

The active high DS3 Alarm Indication Signal enable bit (AISGEN) configures the D3MA to generate a DS3 AIS signal. Any data on the STS-1 SPE is lost due to the assertion of AISGEN. AISGEN is valid only in DS3 mode.

RBSO

When RBSO is logic 1, the R bits of the DS3 mapping are set to logic 1's. If RBSO bit is Logic 0, the R bits are set to logic 0's.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

Register DS3_BASE + 55H: D3MA Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	X
Bit 0	R	UFLI	X

UFLI

When logic 1, this bit indicates that an underflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

OFLI

When logic 1, this bit indicates that an overflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

The OFLI and UFLI bits and the interrupt are cleared when this register is read by the microprocessor interface.

Register DS3_BASE + 56H: D3MA Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

UFLIEN

When set to logic 1, UFLIEN enables generation of an interrupt if an elastic store underflow condition occurs (UFLI=’1’).

OFLIEN

When set to logic 1, OFLIEN bit enables generation of an interrupt if an elastic store overflow condition occurs (OFLI=’1’).

12.8 SIRP Register Summary

There are 4 SIRP blocks in the S/UNI-MACH48 device. Their base addresses (SIRP_BASE) are: 14C0H, 14D0H, 14E0H, and 14F0H. The SIRP maps REI and RDI signals from the G1 byte of the receive SONET Path Overhead into the transmit SONET Path Overhead.

Each SIRP block is dedicated to a range of timeslots. These timeslots are on the system side of the TSI blocks (IWTI, IPTI, OWTI, and OPTI).

For the monitor side, the SIRP block residing in the least significant SIRP_BASE address location is dedicated to the first row of the system-side timeslot maps shown in Table 52 and Table 53. The TS0 corresponds to the system-side timeslot at the left side of each row.

For the insertion side, the SIRP block residing in the least significant SIRP_BASE address location is dedicated to the first row of the system-side timeslot maps shown in Table 52 and Table 53. The TS0 corresponds to the system-side timeslot at the left side of each row.

The SIRP block residing in the 2nd least significant SIRP _BASE address location is dedicated to the second row of the system-side timeslot maps. The SIRP block residing in the 3rd least significant SIRP _BASE address location is dedicated to the third row of the system-side timeslot maps. The SIRP block residing in the most significant SIRP _BASE address location is dedicated to the bottom row of the system-side timeslot maps.

When in STS-48c/STM-16c mode, only the SIRP residing at address 14C0H is used.

Register SIRP_BASE + *x*: SIRP Timeslot *x* Configuration Register (*x* = 00H to 0BH)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	TS***x***_RDI[1]	0
Bit 10	R/W	TS***x***_RDI[0]	0
Bit 9	R/W	TS***x***_REI[3]	0
Bit 8	R/W	TS***x***_REI[2]	0
Bit 7	R/W	TS***x***_REI[1]	0
Bit 6	R/W	TS***x***_REI[0]	0
Bit 5	R/W	Ts***x***_FORCE_LCD	0
Bit 4	R/W	TS***x***_RDI20F	0
Bit 3	R/W	TS***x***_ERDI	0
Bit 2	R/W	TS***x***_RMODE[1]	1
Bit 1	R/W	TS***x***_RMODE[0]	1
Bit 0	R/W	TS***x***_PROV	0

TS***x***_PROV

When TS***x***_PROV is logic 0, automatic remote alarm reporting is disabled for the data stream on timeslot ***x***. When TS***x***_PROV is logic 1, automatic remote alarm reporting is enabled for the data stream on timeslot ***x***.

Note that the TS***x***_PROV bit must be set to logic 1 if timeslot ***x*** is the first timeslot of an STS-n channel, or the J1 will not propagate to the TelecomBus port. In this case, if the user still desires to disable remote alarm reporting, all other bits in this register should be set to logic 0.

TS***x***_RMODE[1:0]

The TS***x***_RMODE[1:0] bits identify the mode of reporting STS Path Remote Defect Indications (RDI) for each timeslot ***x*** as shown in Table 29.

Table 29 SIRP RDI and REI Reporting Modes

TS*x*_RMODE[1:0]	Error Reporting Mode
00	Register Mode: Source REI[3:0] and RDI[1:0] from internal registers TS*x*_REI[3:0] and TS*x*_RDI[1:0] respectively. The remote alarm port and LCD indications (which map to a specified 2 bit programmable RDI code) are ignored.
01	Remote Alarm Input Only Mode: Source REI[3:0] and RDI[1:0] entirely from remote alarm port.
10	Remote Alarm Input with Loss of ATM Cell Delineation Input Mode: Source REI[3:0] from remote alarm port and RDI[1:0] from LCD indications with a specified 2 bit RDI code. When LCD condition is not present, source RDI[1:0] from remote alarm port.
11	Normal Error Reporting Mode: Source REI[3:0] from remote alarm port. LCD indications with a specified 2-bit RDI code is compared to incoming RDI[1:0] from remote alarm port. Higher priority RDI takes precedence.

TS*x*_ERDI

The TS*x*_ERDI bit selects between normal and extended RDI encoding on timeslot *x*. When TS*x*_ERDI is logic 1, extended RDI is selected. The RDI output is treated as a 2-bit codepoint. When TS*x*_ERDI is logic 0, normal RDI is selected. These selections are summarized in Table 30.

Table 30 SIRP RDI Settings

TS*x*_ERDI = 1	TS*x*_RDI[1:0]	ERDI Interpretation	G1 bits 5,6,7 (GR-253-CORE)
	00	No RDI-P defect	001
	01	ERDI-P payload defect	010
	10	ERDI-P server defect	101
	11	ERDI-P connectivity defect	110
TS*x*_ERDI = 0	00	No RDI-P defect	0xx
	01	No RDI-P defect	0xx
	10	RDI-P defect	1xx
	11	RDI-P defect	1xx

TS*x*_RDI20F

The TS*x*_RDI20F bits specify the configuration of RDI maintenance duration. The standard required duration is 10 frames. The GR-253 objective duration is 20 frames. The two options are specified by the TS*x*_RDI20F bit are selected as shown in Table 31.

Table 31 SIRP RDI Maintenance

TS*x*_RDI20F	Configuration
0	A particular RDI value for will be maintained for the required 10 frames before changing to a lower priority RDI code.

1	A particular RDI value for will be maintained for the GR-253 objective 20 frames before changing to a lower priority RDI code.

TS***x***_FORCE_LCD

The TS***x***_FORCE_LCD bit is used to force a Loss of ATM Cell Delineation (LCD) event on a specified timeslot ***x***. A logic OR operation is performed on the LCD indication and matching TS***x***_FORCE_LCD bit. When TS***x***_FORCE_LCD is logic 1, an LCD event is assumed and RDI[1:0] is sourced entirely from a specified 2 bit RDI code (LCD[1:0]) for timeslot ***x***. The TS***x***_FORCE_LCD bit is ignored when TS***x***_RMODE[1:0] = b'00 and b'01.

TS***x***_REI[3:0]

The TS***x***_REI[3:0] bits are used to manually transmit an STS path Remote Error Indication (REI) when both TS***x***_RMODE[1:0] register bits are logic 0. If TS***x***_REI[3:0] is set to a value other than 0, then that value will be transmitted at the next opportunity. After the transmission is completed, TS***x***_REI[3:0] is reset to the value 0. When TSx_RMODE[1:0] register bits are not set low, the TSx_REI[3:0] bits are ignored.

TS***x***_RDI[1:0]

The TS***x***_RDI[1:0] bits control the value of the RDI output of the data stream selected when both TS***x***_RMODE[1:0] register bits are logic 0. When extended RDI is enabled (TS***x***_ERDI logic 1), the RDI output is controlled directly by TS***x***_RDI [1:0] register bits when either register bit is logic 1. The RDI output reflects the remote alarm status (if TS***x***_PROV = 1) when both TS***x***_RDI[1:0] register bits are logic 0. When extended RDI is disabled (TS***x***_ERDI logic 0), and the RDI[0] register bit is logic 1, the RDI output is forced logic 1 regardless of the remote alarm status. When RDI[0] is logic 0, the RDI output reflects the remote alarm status. When both TS***x***_RMODE[1:0] register bits are not logic 0, the TS***x***_RDI[1:0] bits are ignored.

Register SIRP_BASE + 0CH: SIRP Configuration Register

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RDIPRIHI[1]	0
Bit 4	R/W	RDIPRIHI[0]	0
Bit 3	R/W	RDIPRIMID[1]	0
Bit 2	R/W	RDIPRIMID[0]	0
Bit 1	R/W	LCD[1]	1
Bit 0	R/W	LCD[0]	0

LCD[1:0]

The LCD[1:0] bits represent the 2 bit programmable RDI code generated when a Loss of ATM Cell Delineation (LCD) event is detected. **Note:** LCD[1:0] correspond to G1 bits 5, 6 described in GR-253-CORE respectively and will need to be set to the value ‘b01 to correspond to GR-253-CORE’s LCD triggered ERDI-P Payload defect indication.

RDIPRIHI[1:0]

The RDIPRIHI[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the highest priority code. High priority codes will replace low priority codes at the next G1 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed. **Note:** When the MACH48 is used with PMC-Sierra’s Spectra devices, RDIPRIHI should be set to ‘b10 to avoid conflicts with downstream priority schemes. This setting complies with GR-253.

RDIPRIMID[1:0]

The RDIPRIMID[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the second highest priority code. These bits combined with the RDIPRIHI bits allow almost any priority scheme to be specified. The bits are interpreted as shown in Table 32. **Note:** When the MACH48 is used with PMC-Sierra’s Spectra devices, RDIPRIMID should be set to ‘b11 to avoid conflicts with downstream priority schemes. This setting complies with GR-253.

Table 32 SIRP RDI Priority Schemes

RDIPRIHI[1:0]	RDIPRIMID[1:0]	Priority of Codes (3 = highest)	
		Code	Priority
11	01	11	3
		01	2
		10	1
		00	0
11	10	11	3
		10	2
		01	1
		00	0
10	**11**	**10**	**3**
		11	**2**
		01	**1**
		00	**0**
10	01	10	3
		01	2
		11	1
		00	0
01	11	01	3
		11	2
		10	1
		00	0
01	10	01	3
		10	2
		11	1
		00	0
00	00	11	1
		10	1
		01	1
		00	0
other codes	other codes	Reserved	

Note: When RDIPRIHI[1:0] and RDIPRIMID[1:0] are both equal to b'00, all RDI codes have equal priority except RDI[1:0] = b'00 which always has lowest priority.

Register 1500H: PRGD Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

MANSYNC

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

AUTOSYNC

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 6 or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTO SYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

RINV

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted.

TINV

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted

PS

The PS bit selects the generated pattern. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated.

The PS bit must be programmed to the desired setting before programming any other PRGD registers, or the transmitted pattern may be corrupted. Any time the setting of the PS bit is changed, the rest of the PRGD registers should be reprogrammed.

QRSS

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDATO stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PDR[1:0]

The PDR[1:0] bits select the content of the four pattern detector registers (at addresses 150CH to 150FH) to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in Table 33.

Table 33 PRGD Pattern Detector Register Configuration

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	BitCount	Bit Count (MSB)

Register 1501H: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

OVR

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

XFERI

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the S/UNI-MACH48 Identify, and Global Performance Update register (0000H). XFERI is set to logic 0 when this register is read.

BEI

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

SYNCI

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, then the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

SYNCI

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, then the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

SYNCV

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 6 or more bit errors in a 64 bit period window).

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

BEE

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

SYNCE

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

Register 1502H: PRGD Length

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 1503H: PRGD Tap

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 1504H: PRGD Error Insertion Register

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EIR[2:0]

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in Table 34.

Table 34 PRGD Generated Bit Error Rate Configurations

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

EVENT

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

Register 1508H: PRGD Pattern Insertion #1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 1509H: PRGD Pattern Insertion #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 150AH: PRGD Pattern Insertion #3

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[10]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 150BH: PRGD Pattern Insertion #4

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written.

Register 150CH: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PD[7]	X
Bit 6	R	PD[6]	X
Bit 5	R	PD[5]	X
Bit 4	R	PD[4]	X
Bit 3	R	PD[3]	X
Bit 2	R	PD[2]	X
Bit 1	R	PD[1]	X
Bit 0	R	PD[0]	X

Register 150DH: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PD[15]	X
Bit 6	R	PD[14]	X
Bit 5	R	PD[13]	X
Bit 4	R	PD[12]	X
Bit 3	R	PD[11]	X
Bit 2	R	PD[10]	X
Bit 1	R	PD[9]	X
Bit 0	R	PD[8]	X

Register 150EH: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PD[23]	X
Bit 6	R	PD[22]	X
Bit 5	R	PD[21]	X
Bit 4	R	PD[20]	X
Bit 3	R	PD[19]	X
Bit 2	R	PD[18]	X
Bit 1	R	PD[17]	X
Bit 0	R	PD[16]	X

Register 150FH: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PD[31]	X
Bit 6	R	PD[30]	X
Bit 5	R	PD[29]	X
Bit 4	R	PD[28]	X
Bit 3	R	PD[27]	X
Bit 2	R	PD[26]	X
Bit 1	R	PD[25]	X
Bit 0	R	PD[24]	X

PD[31:0]

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0}. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

12.9 PRGM Register Summary

There are 8 PRGM blocks in the S/UNI-MACH48 device. Their base addresses (PRGM_BASE) are: 1510H, 1520H, 1530H, 1540H, 1550H, 1560H, 1570H, and 1580H. The PRGM blocks are used for PRBS generation and monitoring on STS-1, STS-3c, STS-12c and STS-48c channels.

Each PRGM block is dedicated to a range of system-side timeslots of either a working or a protection link.

PRGM_BASE	Reference Links (If no timeslot swapping is performed at the IPTI, IWTI, OPTI, and OWTI)	Notes
1510H	OD[1][7:0] when SER_EN = 0. RPWRK[1]/RNWRK[1], TPWRK[1]/TNWRK[1] when SER_EN = 1.	Must be configured to be the "master" PRGM for STS-48c/STM-16c mode.
1520H	OD[2][7:0] when SER_EN = 0. RPWRK[2]/RNWRK[2], TPWRK[2]/TNWRK[2] when SER_EN = 1.	Must be configured to be a "slave" PRGM for STS-48c/STM-16c mode.
1530H	OD[3][7:0] when SER_EN = 0. RPWRK[3]/RNWRK[3], TPWRK[3]/TNWRK[3] when SER_EN = 1.	Must be configured to be a "slave" PRGM for STS-48c/STM-16c mode.
1540H	OD[4][7:0] when SER_EN = 0. RPWRK[4]/RNWRK[4], TPWRK[4]/TNWRK[4] when SER_EN = 1.	Must be configured to be a "slave" PRGM for STS-48c/STM-16c mode.
1550H	RPPROT[1]/RNPROT[1], TPPROT[1]/TNPROT[1] when SER_EN = 1.	Must be configured to be the "master" PRGM for STS-48c/STM-16c mode.
1560H	RPPROT[2]/RNPROT[2], TPPROT[2]/TNPROT[2] when SER_EN = 1.	Must be configured to be a "slave" PRGM for STS-48c/STM-16c mode.
1570H	RPPROT[3]/RNPROT[3], TPPROT[3]/TNPROT[3] when SER_EN = 1.	Must be configured to be a "slave" PRGM for STS-48c/STM-16c mode.
1580H	RPPROT[4]/RNPROT[4], TPPROT[4]/TNPROT[4] when SER_EN = 1.	Must be configured to be a "slave" PRGM for STS-48c/STM-16c mode.

For the monitor side, the PRGM block residing in the least significant PRGM _BASE address location is dedicated to the first row of the system timeslot maps shown in Table 52. The timeslot 0 (TSLOT[3:0] = 0) corresponds to the system timeslot at the left side of each row.

For the generator side, the PRGM block residing in the least significant PRGM _BASE address location is dedicated to the first row of the system timeslot maps shown in Table 52. The timeslot 0 (TSLOT[3:0] = 0) corresponds to the system timeslot at the left side of each row.

The PRGM block residing in the 2nd least significant PRGM _BASE address location is dedicated to the second row of the system timeslot map.

The PRGM block residing in the 3rd least significant PRGM _BASE address location is dedicated to the third row of the system timeslot map.

The PRGM block residing in the most significant PRGM _BASE address location is dedicated to the bottom row of the system timeslot map.

Register PRGM_BASE + 00H: PRGM Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	TSLOT[3]	0
Bit 2	R/W	TSLOT[2]	0
Bit 1	R/W	TSLOT[1]	0
Bit 0	R/W	TSLOT[0]	0

TSLOT[3:0]

The TSLOT[3:0] bits select which timeslot division is accessed by the current indirect transfer.

Table 35 PRGM Timeslot Selection

TSLOT[3:0]	Timeslot #
0000	Invalid STS-1 path
0001-1100	STS-1 path #0 to STS-1 path #11
1101-1111	Invalid STS-1 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is accessed by the current indirect transfer.

Six pages are defined for the monitor (IADDR[3] = ‘0’) as shown in Table 36: the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

Table 36 PRGM Monitor RAM Pages

IADDR[3:0]	RAM page
0000	Timeslot Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page
0011	B1/E1 value page
0100	Monitor error count page
0101	Received B1 and E1

Four pages are defined for the generator (IADDR [3] = '1') as shown in Table 37: the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

Table 37 PRGM Generator RAM Pages

IADDR[3:0]	RAM page
1000	Timeslot Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	B1/E1 value page

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register PRGM_BASE + 01H : PRGM Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfered to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

PRGM Indirect Register 0H: Monitor Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	AMODE	0
Bit 0	R/W	MON_ENA	0

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the timeslot specified in the TSLOT[3:0] of PRGM register 0H (PRGM Indirect Addressing). If MON_ENA is set to '1', a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is logic 0, the data at the input of the monitor is ignored.

AMODE

If the AMODE is high, the monitor is in Autonomous mode, and the start of the incoming SONET/SDH SPE is always place next to the H3 byte (zero offset), so the J1 pulses indications from the TelecomBus is ignored. When AMODE is low, the SONET/SDH frame is received on the TelecomBus.

AMODE can be used in MST applications where the J1 pulses are not given by the TelecomBus. The upstream device sourcing the PRBS data must align its SPE with zero offset so the PRGM can align to it. This is required because in MST mode (see Section 14.3), the S/UNI-MACH48's pointer processor (RHPP) sits downstream of the PRGM and thus cannot provide the J1 alignment.

INV_PRBS

Sets the monitor to invert the PRBS before comparing it to the internally generated payload. When logic 1, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

Sets the monitor to re-initialize the PRBS sequence. When logic 1, the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. In master/slave configuration, to re-initialize the PRBS, RESYNC has to be logic 1 in the master PRGM only. RESYNC is self-clearing.

B1E1_ENA

When logic 1, this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to the complement of the same value. When B1E1_ENA is logic 1, the B1 and E1 bytes are monitored.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When logic 0, the payload contains PRBS bytes, and when logic 1, a sequential pattern is monitored.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

PRGM Indirect Register 1H: Monitor PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR state of the timeslot (TSLOT[3:0]) specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

PRGM Indirect Register 2H: Monitor PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRBS[7:0]

The PRBS[7:0] register, are the 6 LSBs of the LFSR state of the timeslot (TSLOT[3:0]) specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

PRGM Indirect Register 3H: Monitor B1/E1 Value Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

B1[7:0]

When enabled, the monitoring of the B1byte in the incoming SONET/SDH frame is a simple comparison to the value in the B1[7:0] register. The same value is used for the monitoring of the E1 byte except its complement is used.

PRGM Indirect Register 4H: Monitor Error Count Page

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

ERR_CNT[15:0]

The ERR_CNT[15:0] registers, is the number of error in the PRBS bytes detected during the monitoring. Errors are accumulated only when the monitor is in the synchronized state. Even if there are multiple errors within one PRBS byte, only one error is counted. The transfer of an individual PRGM's error counters to their holding registers is trigger by a write to the PRGM Performance Counters Transfer Trigger register (PRGM_BASE + 0CH). The PRGM's counters will also be updated by writing to register 0000H which initiates a chip-wide global performance monitor update. The error counters will not wrap around after reaching FFFFH. It will saturate to this value.

Note that the 3 errors that cause the PRGM to lose synchronization may in fact be counted as 3, 4, or 5 errors.

PRGM Indirect Register 5H: Monitor Received B1/E1 Bytes Page

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular timeslot (TSLOT[3:0]). Every time a B1 byte is received, it is copied in this register.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular timeslot (TSLOT[3:0]). Every time a E1 byte is received, it is copied in this register.

PRGM Indirect Register 8H: Generator Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	PRBS_ENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ _PRBSB	0
Bit 4	R/W	B1E1_ENA	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	X
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

INV_PRBS

Sets the generator to invert the PRBS before inserting it in the payload. When logic 1, the PRBS bytes will be inverted, else they will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When logic 1, the MSB of the next byte will be inverted, inducing a single bit error. The register clear itself when the operation is complete. A read operation will always result in a logic ‘0’.

B1E1_ENA

This bit enables the replacement of the B1 byte in the SONET/SDH frame, by a programmable value. The E1 byte is replaced by the complement of the same value. When B1E1_ENA is logic 1, the B1 and E1 bytes are replaced in the frame, else they go through the PRGM unaltered.

SEQ _PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When logic 0, the payload is filled with PRBS bytes, and when logic 1, a sequential pattern is inserted.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

PRBS_ENA

This bit specifies if PRBS is to be generated and replace the data. If PRBS_ENA is logic 1, patterns are generated and replace the original data stream, else no pattern is generated and the unmodified data is output.

Reserved

The Reserved bit should be programmed to logic 0 for proper operation.

PRGM Indirect Register 9H: Generator PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR state of the timeslot (TSLOT[3:0]) specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

PRGM Indirect Register AH: Generator PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRBS[6:0]

The PRBS[6:0] register, are the 7 LSBs of the LFSR state of the timeslot (TSLOT[3:0]) specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

PRGM Indirect Register BH: Generator B1/E1 Value Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

B1[7:0]

When enabled, the value in this register is inserted in the B1byte position in the outgoing SONET/SDH frame. The complement of this value is also inserted at the E1 byte position.

Register PRGM_BASE + 02H: PRGM Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	GEN_MSSLEN[2]	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

GEN_STS3C[0]

The STS-3c payload configuration (GEN_STS3C[0]) bit selects the payload configuration. When GEN_STS3C[0] is set to logic 1, the timeslots #0, #4 and #8 are part of a STS-3c payload. When GEN_STS3C[0] is set to logic 0, the timeslots are STS-1 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[0] register bit.

GEN_STS3C[1]

The STS-3c payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1 timeslots #1, #5 and #9 are part of a STS-3c payload. When GEN_STS3C[1] is set to logic 0, the timeslots are STS-1 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[1] register bit.

GEN_STS3C[2]

The STS-3c payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1 timeslots #2, #6 and #10 are part of a STS-3c payload. When GEN_STS3C[2] is set to logic 0, the timeslots are STS-1 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[2] register bit.

GEN_STS3C[4]

The STS-3c payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1 timeslots #3, #7 and #11 are part of a STS-3c payload. When GEN_STS3C[3] is set to logic 0, the timeslots are STS-1 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[3] register bit.

GEN_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's generator as shown in Table 38.

Table 38 PRGM Generator Master/Slave Configuration

GEN_MSSLEN[2:0]	Configuration
000	ms/sl configuration disable (STS-12c/STM-4c and below)
001	Reserved2 PRGMs (STS-24/STM-8)
010	Reserved
011	ms/sl configuration enable 4 PRGMs (STS-48c/STM-16c)
100	Reserved
101 - 111	Invalid configuration

GEN_MSSLEN[2:0] is ignored when the register GEN_STS12C is logic 0.

GEN_STS12C

The STS-12c payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the timeslots #0 to #11 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[3:0] register bit. The GEN_STS12C register bit has precedence over the GEN_STS3C[3:0] register bit.

GEN_STS12CSL

The slave STS-12c payload configuration (GEN_STS12CSL) bit selects the slave payload configuration. When GEN_STS12CSL is set to logic 1, the timeslots #0 to #11 are part of a slave payload. When GEN_STS12CSL is set to logic 0, the timeslots #0 to # 11 are part of a concatenate master payload. When GEN_STS12C is set to logic 0, the GEN_STS12CSL register bit has no effect.

GEN_STS12CSL is ignored when GEN_MSSLEN[2:0] is "000".

Register PRGM_BASE + 03H: PRGM Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	MON_MSSLEN[2]	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

MON_STS3C[0]

The STS-3c payload configuration (MON_STS3C[0]) bit selects the payload configuration. When MON_STS3C[0] is set to logic 1, the STS-1/STM-0 timeslots #0, #4 and #8 are part of a STS-3c payload. When MON_STS3C[0] is set to logic 0, the timeslots are STS-1 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[0] register bit.

MON_STS3C[1]

The STS-3c payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 timeslots #1, #5 and #9 are part of a STS-3c payload. When MON_STS3C[1] is set to logic 0, the timeslots are STS-1 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[1] register bit.

MON_STS3C[2]

The STS-3c payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 timeslots #2, #6 and #10 are part of a MON_STS-3c payload. When MON_STS3C[2] is set to logic 0, the timeslots are STS-1 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[2] register bit.

MON_STS3C[4]

The STS-3c payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 timeslots #3, #7 and #11 are part of a STS-3c payload. When MON_STS3C[3] is set to logic 0, the timeslots are STS-1 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[3] register bit.

MON_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's monitor.

Table 39 PRGM Monitor Master/Slave Configuration

MON_MSSLEN[2:0]	Configuration
000	Ms/sl configuration disable (STS-12c/STM-4c and below)
001	Reserved
010	Reserved
011	ms/sl configuration enable 4 PRGMs (STS-48/STM-16)
100	Reserved
101 - 111	Invalid configuration

MON_MSSLEN[2:0] is ignored when the register MON_STS12C is logic 0.

MON_STS12C

The STS-12c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #0 to #11 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 timeslots are defined with the MON_STS3C[3:0] register bit. The MON_STS12C register bit has precedence over the MON_STS3C[3:0] register bit.

MON_STS12CSL

The slave STS-12c payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the timeslots #0 to #11 are part of a slave payload. When MON_STS12CSL is set to logic 0, the timeslots #0 to # 11 are part of a concatenate master payload. When MON_STS12C is set to logic 0, the MON_STS12CSL register bit has no effect.

MON_STS12CSL is ignored when MON_MSSLEN[2:0] is "000".

Register PRGM_BASE + 04H: PRGM Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register, is the status of the interrupt generated by each of the 12 STS-1 timeslots when an error has been detected. The MON**x**_ERRI is logic 1 when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 timeslot **x**. This bit is independent of MON**x**_ERRE, and is cleared after it's been read.

Register PRGM_BASE + 05H: PRGM Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register, enables the interrupt for each of the 12 STS-1 timeslots. When MON**x**_ERRE is set to logic 1, the Byte Error Interrupt can generate an external interrupt on INTB. When MON**x**_ERRE is set to logic 0, the Byte Error Interrupt will not generate an external interrupt on INTB.

Register PRGM_BASE + 06H: PRGM Monitor B1/E1 Bytes Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_B1E1I	X
Bit 10	R	MON11_B1E1I	X
Bit 9	R	MON10_B1E1I	X
Bit 8	R	MON9_B1E1I	X
Bit 7	R	MON8_B1E1I	X
Bit 6	R	MON7_B1E1I	X
Bit 5	R	MON6_B1E1I	X
Bit 4	R	MON5_B1E1I	X
Bit 3	R	MON4_B1E1I	X
Bit 2	R	MON3_B1E1I	X
Bit 1	R	MON2_B1E1I	X
Bit 0	R	MON1_B1E1I	X

MON**x**_B1E1I

The Monitor B1/E1Bytes Interrupt Status register, is the status of the interrupt generated by each of the 12 STS-1 timeslots when a change in the status of the comparison has been detected on the B1/E1 bytes. The MON**x**_B1E1I is logic 1 when the monitor is in the synchronized state and when the status change is detected on either the B1 or E1 bytes in the STS-1 path **x**. For example, if a mismatch is detected and the previous comparison was a match, the MON**x**_B1E1I will be logic 1. But if a mismatch is detected and the previous comparison was a mismatch, the MON**x**_B1E1I will keep its previous value. This bit is independent of MON**x**_B1E1E, and is cleared after it's been read.

Register PRGM_BASE + 07H: Monitor B1/E1 Bytes Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_B1E1E	0
Bit 10	R/W	MON11_ B1E1E	0
Bit 9	R/W	MON10_ B1E1E	0
Bit 8	R/W	MON9_ B1E1E	0
Bit 7	R/W	MON8_ B1E1E	0
Bit 6	R/W	MON7_ B1E1E	0
Bit 5	R/W	MON6_ B1E1E	0
Bit 4	R/W	MON5_ B1E1E	0
Bit 3	R/W	MON4_ B1E1E	0
Bit 2	R/W	MON3_ B1E1E	0
Bit 1	R/W	MON2_ B1E1E	0
Bit 0	R/W	MON1_ B1E1E	0

MON**x**_B1E1E

The Monitor B1/E1 Bytes Interrupt Enable register, enables the interrupt for each of the 12 STS-1 timeslots. When MON**x**_B1E1E is logic 1, the B1/E1Bytes event is allowed to generate an external interrupt on INTB.

Register PRGM_BASE + 09H: PRGM Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register, is logic 1 when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 timeslot goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set to logic 1. For concatenated payloads, only the STS-1 path state machine that first detects the change in Synchronization Status in this PRBS monitor will set MON**x**_SYNCI to logic 1. This bit is independent of MON**x**_SYNCE, and is cleared after it's been read. Note that the PRGM will synchronize on an all zeroes or all ones pattern. To verify that a valid PRBS pattern is the signal the PRGM is locked to, check the PRBS[22:0] bits in the PRGM Monitor PRBS Accumulator Page. If the bits are not all zeroes or all ones, then the synchronization is due to locking on a valid PRBS pattern.

Register PRGM_BASE + 0AH: PRGM Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register, allows each individual STS-1 timeslot to generate an external interrupt on INTB. When MON**x**_SYNCE is logic 1, whenever a change occurs in the synchronization state of the monitor in STS-1 timeslot **x**, generates an interrupt on INTB.

Register PRGM_BASE + 0BH: PRGM Monitor Synchronization Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

MON**x**_SYNCV

The Monitor Synchronization Status register, reflects the state of the monitor's state machine. When MON**x**_SYNCV is logic 0, the monitor lost synchronization for the timeslot **x**. When MON**x**_SYNCV is logic 1, the monitor is in synchronization for the timeslot **x**. The Synchronization Status is only valid when the corresponding monitor is enabled. Note that the PRGM will synchronize on an all zeroes or all ones pattern. To verify that a valid PRBS pattern is the signal the PRGM is locked to, check the PRBS[22:0] bits in the PRGM Monitor PRBS Accumulator Page. If the bits are not all zeroes or all ones, then the synchronization is due to locking on a valid PRBS pattern.

Register PRGM_BASE + 0CH: PRGM Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	PRGM_TIP	X

The Performance Counters Transfer Trigger register is provided at PRGM read address 0Ch.

A write in this register will trigger the transfer of the error counters of the corresponding PRGM block to its holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the PRGM_TIP bit is set to logic 1. When the holding registers contain the value of the error counters, PRGM_TIP returns to logic 0.

PRGM_TIP

The PRGM Transfer In Progress bit reflects the state of the counter transfers. When PRGM_TIP is high, an error counter transfer has been initiated but the counters are not transferred in the holding register yet. When PRGM_TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be polled after an error counters transfer request, to determine if the counters are ready to be read.

12.10 RHPP Register Summary

There are 4 RHPP blocks in the S/UNI-MACH48 device. Their base addresses (RHPP_BASE) are: 1600H, 1680H, 1700H, and 1780H. The RHPP performs H1/H2 pointer interpretation to find the J1 byte locations in the receive direction.

Each RHPP block is dedicated to a range of timeslots (system side).

The RHPP block residing in the least significant RHPP_BASE address location is dedicated to all the timeslots shown in Table 53 and to the first row of timeslots in STS-48c/STM-16c mode (RX48c = 1) and in Table 52 when not in STS-48c/STM-16c mode (RX48C = 0).

The RHPP block residing in the 2nd least significant RHPP_BASE address location is dedicated to the second row of the timeslot map in Table 52 and to the channel number 12. This RHPP block is not used when in STS-48c/STM-16c mode (RX48C = 1).

The RHPP block residing in the 3rd least significant RHPP_BASE address location is dedicated to the third row of the timeslot map in Table 52 and to the channel number 24. This RHPP block is not used when in STS-48c/STM-16c mode (RX48C = 1).

The RHPP block residing in the most significant RHPP_BASE address location is dedicated to the bottom row of the timeslot map in Table 52 and to the channel number 36. This RHPP block is not used when in STS-48c/STM-16c mode (RX48C = 1).

Register RHPP_BASE + 00H: RHPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	ADDR[3]	0
Bit 8	R/W	ADDR[2]	0
Bit 7	R/W	ADDR[1]	0
Bit 6	R/W	ADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	TSLOT[3]	0
Bit 2	R/W	TSLOT[2]	0
Bit 1	R/W	TSLOT[1]	0
Bit 0	R/W	TSLOT[0]	0

TSLOT[3:0]

The STS-1/STM-0 system side timeslot (TSLOT[3:0]) bits select which STS-1/STM-0 timeslot is accessed by the current indirect transfer.

TSLOT[3:0]	Timeslot #
0000	Invalid path
0001-1100	Path #0 to Path #11
1101-1111	Invalid path

ADDR[2:0]

The address location (ADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address ADDR[3:0]	Indirect Data Register
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value
0011	Reserved
0100	Reserved
0101	Pointer Interpreter status

Indirect Address ADDR[3:0]	Indirect Data Register
0110	Reserved
0111	Reserved
1000	Negative Justification Event Count
1001	Positive Justification Event Count
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the RHPP Indirect Data Registers.

Register RHPP_BASE + 01H: RHPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the RHPP Indirect Address Register.

DATA[15:0] has a different meaning depending on which indirect address is accessed.

RHPP Indirect Register 00H: Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0	R/W	Reserved	0

The Pointer Interpreter Configuration Indirect Register is provided at RHPP r/w indirect address 00H.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The "justification more than 3 frames ago enable" (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + ss. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + ss + offset value in the range 0 to 782 (764 in TU-3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

Reserved

The Reserved bits must be programmed to 0 for proper operation.

RHPP Indirect Register 01H: Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The Pointer Interpreter Configuration Indirect Register is provided at RHPP r/w indirect address 01H.

Reserved

The Reserved bits must be programmed to 0 for proper operation.

RHPP Indirect Register 02H: Pointer Value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12		Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value Indirect Register is provided at RHPP r/w address 02H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS pointer being process by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV [2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

RHPP Indirect Register 05H: Pointer Interpreter status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	NDF	0
Bit 5	R	ILLPTR	0
Bit 4	R	INVNDF	0
Bit 3	R	DISCOPA	0
Bit 2	R	CONCAT	0
Bit 1	R	ILLJREQ	0
Bit 0	R	NEWPTR	0

The Pointer Interpreter Status Indirect Register is provided at RHPP r/w indirect address 05H.

NEWPTR

The new pointer (NEWPTR) signal is logic 1 when an incoming pointer satisfying the new_point indication is received.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is logic 1 when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

CONCAT

The CONCAT bit is logic 1 if the H1 and H2 pointer bytes received match the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is logic 1 when there is a pointer adjustment due to receiving a pointer repeated three times.

INVNDF

The invalid new data flag (INVNDF) signal is logic 1 when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is logic 1 when the pointer received is out of the range. Legal values are from 0 to 782.

NDF

The new data flag (NDF) signal is logic 1 when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

RHPP Indirect Register 07H: RHPP Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

The Path REI Error Counter Indirect Register is provided at RHPP r/w indirect address 07H.

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register (RHPP_BASE + 03H). or by a write to the Global Performance Monitor Update (0000H). The TIP bit in the Global Performance Monitor Update (0000H) indicates the transfer status.

Register RHPP_BASE + 02H: RHPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at RHPP r/w address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #0, #4 and #8 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When the STS-1/STM-0 paths #0, #4 and #8 are configured as part of an STS-12c or STS-48c in the S/UNI-MACH48 Receive Timeslot Configuration registers, the STS3C[1] register bit is ignored.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When the STS-1/STM-0 paths #1, #5 and #9 are configured as part of an STS-12c or STS-48c in the S/UNI-MACH48 Receive Timeslot Configuration registers, the STS3C[1] register bit is ignored.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When the STS-1/STM-0 paths #2, #6 and #10 are configured as part of an STS-12c or STS-48c in the S/UNI-MACH48 Receive Timeslot Configuration registers, the STS3C[1] register bit is ignored.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When the STS-1/STM-0 paths #3, #7 and #11 are configured as part of an STS-12c or STS-48c in the S/UNI-MACH48 Receive Timeslot Configuration registers, the STS3C[1] register bit is ignored.

Reserved

The Reserved bits must be programmed to logic 0 for proper operation.

Register RHPP_BASE + 03H: RHPP Counters update

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The RHPP Path Interrupt Status Register is provided at RHPP read address 04H. Any write to the RHPP Counters Update Register (provided at RHPP address 03H) will trigger the transfer of all RHPP counter values to their holding registers. It is equivalent at the TSB level to a write to the Global Performance Monitor Update register (0000H). The TIP bit in the Global Performance Monitor Update (0000H) indicates the transfer status.

Register RHPP_BASE + 04H: RHPP Path Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	P_INT[11]	X
Bit 10	R	P_INT[10]	X
Bit 9	R	P_INT[9]	X
Bit 8	R	P_INT[8]	X
Bit 7	R	P_INT[7]	X
Bit 6	R	P_INT[6]	X
Bit 5	R	P_INT[5]	X
Bit 4	R	P_INT[4]	X
Bit 3	R	P_INT[3]	X
Bit 2	R	P_INT[2]	X
Bit 1	R	P_INT[1]	X
Bit 0	R	P_INT[0]	X

The RHPP Path Interrupt Status Register is provided at RHPP read address 04H.

P_INT[11:0]

The Path Interrupt Status bit (P_INT[11:0]) tells which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts, it is simply added to reduce the average number of accesses required to service interrupts.

Register RHPP_BASE + 05H: RHPP Pointer Concatenation Processing Disable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	PTRCDIS[11]	0
Bit 10	R/W	PTRCDIS[10]	0
Bit 9	R/W	PTRCDIS[9]	0
Bit 8	R/W	PTRCDIS[8]	0
Bit 7	R/W	PTRCDIS[7]	0
Bit 6	R/W	PTRCDIS[6]	0
Bit 5	R/W	PTRCDIS[5]	0
Bit 4	R/W	PTRCDIS[4]	0
Bit 3	R/W	PTRCDIS[3]	0
Bit 2	R/W	PTRCDIS[2]	0
Bit 1	R/W	PTRCDIS[1]	0
Bit 0	R/W	PTRCDIS[0]	0

The Pointer Concatenation processing Disable Register is provided at RHPP r/w address 05H.

PTRCDIS[11:0]

The concatenation pointer processing disable (PTRCDIS[11:0]) bits disable the path concatenation pointer processor from blocking data flow. When PTRCDIS[n] is set to logic 1, detection of a LOPC-P or AISC-P condition will not cause the RTDP/RCFP to stop processing data. When PTRCDIS[n] is set to logic 0, detection of a LOPC-P, or AISC-P condition will cause the RTDP/RCFP to stop processing data. Note that this bit has no effect on interrupts, and concatenation based interrupts will still be reported unless disabled individually.

Register RHPP_BASE + 08H + 8*x*: RHPP Pointer Interpreter Status (*x* = 0 to BH)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	X
Bit 0		Unused	X

The Pointer Interpreter Status Register is provided at RHPP r/w address 08H + 8***x*** where 0H ≤ x ≤ BH.

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP state. PLOPV is set to logic 0 when the state machine is not in the LOP state. While any of PLOPV, PAISV, PLOPCV or PAISCV is logic 1, the appropriate CHx_DIS bit in the RCAS should be set to 1 to disable data processing on the invalid data stream unless an upstream device has already disabled the payload by writing all ‘1’s to the SPE.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state. While any of PLOPV, PAISV, PLOPCV or PAISCV is logic 1, the appropriate CHx_DIS bit in the RCAS should be set to 1 to disable data processing on the invalid data stream unless an upstream device has already disabled the payload by writing all ‘1’s to the SPE.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC state. PLOPCV is set to logic 0 when the state machine is not in the LOPC state. While any of PLOPV, PAISV, PLOPCV or PAISCV is logic 1, the appropriate CHx_DIS bit in the RCAS should be set to 1 to disable data processing on the invalid data stream unless an upstream device has already disabled the payload by writing all '1's to the SPE.

PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the AIS state. While any of PLOPV, PAISV, PLOPCV or PAISCV is logic 1, the appropriate CHx_DIS bit in the RCAS should be set to 1 to disable data processing on the invalid data stream unless an upstream device has already disabled the payload by writing all '1's to the SPE.

Register RHPP_BASE + 09H + 8*x*: RHPP Pointer Interpreter Interrupt Enable (*x* = 0 to BH)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	X
Bit 0	R/W	PTRJEE	0

The Pointer Interpreter Interrupt Enable Register is provided at RHPP r/w address 09H + 8***x*** where 0H ≤ x ≤ BH.

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the event activation of the hardware interrupt (INTB) output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt (INTB) output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt (INTB) output.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the hardware (INTB) output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt (INTB) output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt (INTB) output.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt (INTB) output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt (INTB) output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt (INTB) output.

PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt (INTB) output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt (INTB) output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt (INTB) output.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt (INTB) output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt (INTB) output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt (INTB) output.

Register RHPP_BASE + 0AH + 8*x*: RHPP Pointer Interpreter Interrupt Status (*x* = 0 to BH)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

The Pointer Interpreter Interrupt Status Register is provided at RHPP r/w address 0AH + 8***x*** where 0H ≤ x ≤ BH.

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared when this register is read.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared when this register is read.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP state or exit from the LOP state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read. When the PLOPI interrupt is asserted, and if an upstream device is not disabling the payload by writing all '1's to the SPE, the user should disable or enable data processing by setting or clearing the appropriate CH*x*_DIS bit in the RCAS, depending on the value of PLOPV.

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared when this register is read. When the PAISI interrupt is asserted, and if an upstream device is not disabling the payload by writing all '1's to the SPE, the user should disable or enable data processing by setting or clearing the appropriate CH*x*_DIS bit in the RCAS, depending on the value of PAISV.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC state or exit from the LOPC state). The interrupt status bit is independent of the interrupt enable bit. PLOPCI is cleared to logic 0 when this register is read. When the PLOPCI interrupt is asserted, and if an upstream device is not disabling the payload by writing all '1's to the SPE, the user should disable or enable data processing by setting or clearing the appropriate CH*x*_DIS bit in the RCAS, depending on the value of PLOPCV.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. PAISCI is cleared when this register is read. When the PAISCI interrupt is asserted, and if an upstream device is not disabling the payload by writing all '1's to the SPE, the user should disable or enable data processing by setting or clearing the appropriate CH*x*_DIS bit in the RCAS, depending on the value of PAISCV.

12.11 STSI (IWTI, IPTI, OWTI, OPTI) Register Summary

There are 4 STSI blocks in the S/UNI-MACH48 device. The STSI blocks map the arbitrarily ordered STS-1 timeslots on the TelecomBus to the legal timeslot groupings reqired by the S/UNI-MACH48 for STS-1, STS-3c, STS-12c or STS-48c channels. Their parameters are as follows:

TSI Block Name	STSI Base Address	Ingress Data Stream Source	Egress Data Stream Destination
IWTI	1800H	Incoming parallel TelecomBus interface when SER_EN = 0. RPWRK[4:1] and RNWRK[4:1] when SER_EN = 1.	System side timeslots when RWSEL pin = 1 and register bit RWSEL_EN = 1. SER_PRT_SEL register bits select whether Rx system-side timeslots come from the IWTI or IPTI when SER_EN = 1 and RWSEL_EN = 0.
IPTI	1808H	RPPROT[4:1] and RNPROT[4:1] when SER_EN = 1.	System side timeslots when RWSEL pin = 0 and register bit RWSEL_EN = 1.
OWTI	1810H	System side data stream.	Outgoing parallel TelecomBus interface when SER_EN = 0. TPWRK[4:1] and TNWRK[4:1] when SER_EN = 1.
OPTI	1818H	System side data stream.	TPPROT[4:1] and TNPROT[4:1] when SER_EN = 1.

Register STSI_BASE + 00H: STSI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	0
Bit 10	R/W	PAGE	0
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TSOUT[3]	0
Bit 6	R/W	TSOUT[2]	0
Bit 5	R/W	TSOUT[1]	0
Bit 4	R/W	TSOUT[0]	0
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

This register provides the data stream number, the time-slot number and the control page select used to access the control pages. Writing to this register triggers an indirect register access.

DOUTSEL[1:0]

The Data Output Select (DOUTSEL[1:0]) bits select which output data stream is accessed by the current indirect transfer.

DOUTSEL[1:0]	DOUT
00	OD[1][7:0] for OWTI, SER_EN = 0 TPWRK/TNWRK[1] for OWTI, SER_EN = 1 TPPROT/TNPROT[1] for OPTI, SER_EN = 1 Data sourced to first row of system timeslots for IWTI and IPTI (see Table 52 and Table 53)
01	OD[2]]7:0] for OWTI, SER_EN = 0 TPWRK/TNWRK[2] for OWTI, SER_EN = 1 TPPROT/TNPROT[2] for OPTI, SER_EN = 1 Data sourced to second row of system timeslots for IWTI and IPTI (see Table 52 and Table 53)

DOUTSEL[1:0]	DOUT
10	OD[3][7:0] for OWTI, SER_EN = 0 TPWRK/TNWRK[3] for OWTI, SER_EN = 1 TPPROT/TNPROT[3] for OPTI, SER_EN = 1 Data sourced to third row of system timeslots for IWTI and IPTI (see Table 52 and Table 53)
11	OD[4][7:0] for OWTI, SER_EN = 0 TPWRK/TNWRK[4] for OWTI, SER_EN = 1 TPPROT/TNPROT[4] for OPTI, SER_EN = 1 Data sourced to fourth row of system timeslots for IWTI and IPTI (see Table 52 and Table 53)

TSOUT[3:0]

The indirect STS-1/STM-0 output time slot (TSOUT[3:0]) bits indicate the STS-1/STM-0 output time slot accessed in the current indirect access. Time slots #0 to #2 are valid in STS-3/STM-1 mode. Time slots #0 to #11 are valid in STS-12/STM-4 mode.

TSOUT[3:0]	STS-1/STM-0 Time Slot #
0000	Invalid time slot
0001-1100	Time slot #0 to time slot #11
1101-1111	Invalid time slot

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the STSI Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the STSI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the Indirect Data Register or when another write access can be initiated.

Register STSI_BASE + 01H: STSI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	SER_PRT_SEL / Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	TSIN[3]	0
Bit 6	R/W	TSIN[2]	0
Bit 5	R/W	TSIN[1]	0
Bit 4	R/W	TSIN[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DINSEL[1]	0
Bit 0	R/W	DINSEL[0]	0

This register contains the data read from the control pages after an indirect read operation or the to be data written to the control pages in an indirect write operation.

DINSEL[1:0]

The Data Input Select (DINSEL[1:0]) bits report the data stream number read after an indirect read operation has completed. The data stream number to be written to the control pages must be set up in this register before triggering a write. DINSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation.

DINSEL[1:0]	Data Stream
00	ID[1][7:0] for IWTI, SER_EN = 0 RPWRK/RNWRK[1] for IWTI, SER_EN = 1 RPPROT/RNPROT[1] for IPTI, SER_EN = 1 Data sourced from first row of system timeslots for OWTI and OPTI (see Table 52 and Table 53).
01	ID[2][7:0] for IWTI, SER_EN = 0 RPWRK/RNWRK[2] for IWTI, SER_EN = 1 RPPROT/RNPROT[2] for IPTI, SER_EN = 1 Data sourced from second row of system timeslots for OWTI and OPTI (see Table 52 and Table 53).
10	ID[3][7:0]] for IWTI, SER_EN = 0 RPWRK/RNWRK[3] for IWTI, SER_EN = 1

DINSEL[1:0]	Data Stream
	RPPROT/RNPROT[3] for IPTI, SER_EN = 1 Data sourced from third row of system timeslots for OWTI and OPTI (see Table 52 and Table 53).
11	ID[4][7:0]] for IWTI, SER_EN = 0 RPWRK/RNWRK[4] for IWTI, SER_EN = 1 RPPROT/RNPROT[4] for IPTI, SER_EN = 1 Data sourced from fourth row of system timeslots for OWTI and OPTI (see Table 52 and Table 53).

TSIN[3:0]

The STS-1/STM-0 Input Time Slot (TSIN[3:0]) bits report the time-slot number (mod 12) read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. TSIN[3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Time slots #0 to #2 are valid in STS-3/STM-1 mode. Time slots #0 to #11 are valid in STS-12/STM-4 mode.

TSIN[3:0]	STS-1/STM-0 Time Slot #
0000	Invalid time slot
0001-1100	Time slot #0 to time slot #11
1101-1111	Invalid time slot

SER_PRT_SEL

The SER_PRT_SEL is only available in the IWTI block. It is Reserved in the IPTI, OWTI, and OPTI blocks.

This bit selects whether the system side timeslot (selected by TSOUT[3:0] and DOUTSEL[1:0] in the IWTI Indirect Address register) directed to the core of the S/UNI-MACH48 is sourced by the IWTI or the IPTI outputs. This allows STS-1 timeslots from the working and protection receive serial TelecomBus links to be intermixed.

When SER_PRT_SEL is logic 1, the IPTI data is inserted. When SER_PRT_SEL is logic 0, the IWTI is inserted. The SER_PRT_SEL only has effect when the serial TelecomBus mode is enabled (SER_EN input pin is logic 1) and the global work/protect link selection is disabled (RWSEL_EN is logic 0). The SER_PRT_SEL function will change the receive stream muxing immediately. Reserved:

The Reserved bits must be set to logic 0 for proper operation.

Register STSI_BASE + 02H: STSI Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	PSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

COAPE

The change of active page interrupt enable (COAPE) bit enables/disables the change of active page hardware interrupt on INTB. When the COAPE bit is set to logic 1, an interrupt is generated when the active page changes from page 0 to page 1 or from page 1 to page 0. These interrupts are masked when COAPE is set to logic 0.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering of the J0/Z0 bytes. This configuration bit only has an effect when the STSI is in the dynamic switching mode – if the STSI is in any of the static switching modes then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not reordered by the muxing block. When this bit is set to logic 1, normal reordering of the J0/Z0 bytes is enabled.

PSEL

The page select (PSEL) bit is used in the selection of the current active. This bit is logically XORed with the value of the ICMP (for IWTI and IPTI) and OCMP (for OWTI and OPTI) signal to determine which control page is currently active.

ACTIVE

The active page indication (ACTIVE) bit indicates which control page is currently active. When this bit is logic 0 then page 0 is controlling the dynamic mux. When this bit is logic 1 then page 1 is controlling the dynamic mux.

Register STSI_BASE + 03H: STSI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COAPI	X

COAPI

The change of active page interrupt statue bit (COAPI) reports the status of the change of active page interrupt. COAPI is set to logic 1 when the active control page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register. COAPI remains valid when the interrupt is not enabled (COAPE set to logic 0) and may be polled to detect change of active control page events.

12.12 R8TD Register Summary

There are 8 R8TD blocks in the S/UNI-MACH48 device. They are only active when the line side LVDS serial interface is enabled (SER_EN is logic 1). The R8TD decodes the 8B/10B serial TelecomBus, and alligns the four data-links for processing by the S/UNI-MACH48.

There is one R8TD for each LVDS link. They are mapped as follows:

TSI Block Name	R8TD Base Address	Ingress Link
R8TD#1	1820H	RPWRK[1] RNWRK[1]
R8TD#2	1828H	RPWRK[2] RNWRK[2]
R8TD#3	1830H	RPWRK[3] RNWRK[3]
R8TD#4	1838H	RPWRK[4] RNWRK[4]
R8TD#5	1840H	RPPROT[1] RNPROT[1]
R8TD#6	1848H	RPPROT[2] RNPROT[2]
R8TD#7	1850H	RPPROT[3] RNPROT[3]
R8TD#8	1858H	RPPROT[4] RNPROT[4]

Register R8TD_BASE + 00H: R8TD Control and Status

Bit	Type	Function	Default
Bit 15	R/W	DLBEN	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	SETLCV	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the R8TD.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is logic 1 when the character alignment block is in the out-of-character-alignment state. OCAV is logic 0 when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is logic 1 when the frame alignment block is in the out-of-frame-alignment state. OFAV is logic 0 when the frame alignment block is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is logic 1, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is logic 0.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is logic 1, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is logic 0.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is logic 1, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is logic 0.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is logic 1, and interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUEO is logic 0.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is logic 1 to force high-order AIS signals in the R8TD egress data stream if the R8TD is in the out-of-frame-alignment state. The R8TD egress data stream is left unaffected in the out-of-frame alignment state when the OFFAIS is logic 0.

SETLCV

The SETLCV bit is used to introduce line code violations in the receive data stream. When logic 1, SETLCV will induce a large number of LCVs on the data stream. When logic 0, SETLCV will not alter the incoming data stream. This feature can be used to cause excessive LCVs which in turn will force the R8TD to search for a new character alignment.

DLBEN

The diagnostic loopback enable bit (DLBEN) controls diagnostic loopback operation. When DLBEN is logic 1, serial TelecomBus diagnostic loopback is enabled. When DLBEN is logic 0, serial TelecomBus diagnostic loopback is disabled. The loopback involves the complementary R8TD and T8TE blocks. For example, the T8TE which sources TPWRK/TNWRK[1] will be diagnostically looped back to the R8TD which sinks RPWRK/RNWRK[1]. Note that when DLBEN is logic 1 on any link, all LVDS links from the same working/protection group must have DLBEN logic 1.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register R8TD_BASE + 01H: R8TD Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due to change of character alignment events and detection of line code violations.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is logic 1 when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is logic 1 when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

LCVI:

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is logic 1 when a line code violation event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is logic 1 when this event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events.

Register R8TD_BASE + 02H: R8TD Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

This register reports the number of line code violations in the previous accumulation period.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV registers are polled by writing to this register or to register 0000H, the S/UNI-MACH48 Global Performance Monitor Update. This action transfers the internally accumulated error count to the LCV registers within 5 SYSCLK cycles (approx 65ns) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register R8TD_BASE + 03H: R8TD Analog Control 1

Bit	Type	Function	Default
Bit 15	R/W	DRU_ATMSB	1
Bit 14	R/W	RX_ATMSB	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	RX_LBSEL	0
Bit 10	R/W	A_RSTB	1
Bit 9	R/W	DRU_RX_TIN[3]	0
Bit 8	R/W	DRU_RX_TIN[2]	0
Bit 7	R/W	DRU_RX_TIN[1]	0
Bit 6	R/W	DRU_RX_TIN[0]	0
Bit 5	R/W	DRU_CTRL[3]	0
Bit 4	R/W	DRU_CTRL[2]	0
Bit 3	R/W	DRU_CTRL[1]	0
Bit 2	R/W	DRU_CTRL[0]	0
Bit 1	R/W	DRU_IDDQ	0
Bit 0		Unused	X

This register controls the analog wrapper signals.

DRU_ATMSB

The DRU_ATMSB bit controls the DRU analog wrapper signal, DRU_ATMSB. When DRU_ATMSB is logic 0 analog test mode is enabled and DRU_RX_TIN[3:0] selects the analog test to be performed in the DRU. This bit is used for PMC internal test purposes and must be set to logic 1 for normal operation.

RX_ATMSB

The RX_ATMSB bit controls the RXLV analog wrapper signal, RX_ATMSB. When RX_ATMSB is logic 0 analog test mode is enabled and DRU_RX_TIN[3:0] selects the analog test to be performed in the RXLV. This bit is used for PMC internal test purposes and must be set to logic 1 for normal operation.

DRU_ENB

The DRU_ENB bit controls the DRU analog wrapper signal, DRU_ENB. When DRU_ENB is logic 0 the DRU circuit is enabled for normal operation.

RX_ENB

The RX_ENB bit controls the RXLV analog wrapper signal, RX_ENB. When RX_ENB is logic 0 the RXLV circuit is enabled for normal operation.

RX_LBSEL

The RX_LBSEL bit controls the RXLV analog wrapper signal, RX_LBSEL. When RX_LBSEL is logic 1 diagnostic RX-TX loopback is enabled for RXLV. **RX_LBSEL is set to logic 1 for normal operation.**

A_RSTB

The A_RSTB bit is used as a soft-reset for the DRU analog block. The DRU block is reset when A_RSTB is logic 0.

DRU_RX_TIN[3:0]

The DRU_RX_TIN[3:0] bits control the DRU and RXLV analog wrapper signal, DRU_RX_TIN[3:0]. The DRU_RX_TIN[3:0] bus is used to select analog test modes. These bits are not used in normal operation.

DRU_CTRL[3:0]

The DRU_CTRL[3:0] bits control the DRU analog wrapper signals, DRU_CTRL[3:0]. **The DRU_CTRL[3:0] bits must be programmed to 'b1101 for proper operation.**

Register R8TD_BASE + 04H: R8TD Analog Control 2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	DRU_DTBRD[3]	X
Bit 8	R	DRU_DTBRD[2]	X
Bit 7	R	DRU_DTBRD[1]	X
Bit 6	R	DRU_DTBRD[0]	X
Bit 5	R/W	DRU_DTBWR[3]	0
Bit 4	R/W	DRU_DTBWR[2]	0
Bit 3	R/W	DRU_DTBWR[1]	0
Bit 2	R/W	DRU_DTBWR[0]	0
Bit 1	R/W	RX_CTRL[1]	0
Bit 0	R/W	RX_CTRL[0]	0

These registers control the analog wrapper signals. They are not used for normal operation.

RX_CTRL[1:0]

The RX_CTRL[1:0] bits control the RXLV analog wrapper signals, RX_CTRL[1:0]. The RX_CTRL[1:0] bus is used for PMC internal testing and should be driven to logic 0 for normal operation.

DRU_DTBWR[3:0]

The DRU digital test bus write signal bits (DRU_DTBWR[3:0]),control the DRU analog wrapper signal, DRU_DTB. These values are used to drive values on the DTB bus. These register bits are used for PMC internal testing and should be left at logic 0 for normal operation.

DRU_DTBRD[3:0]

The DRU digital test bus read signal bits (DRU_DTB_OUT[3:0]) are used to read values from the DRU analog block signal, DRU_DTB. These register bits are used for PMC internal testing and are not used for normal operation.

Register R8TD_BASE + 05H: R8TD Analog Control 3

Bit	Type	Function	Default
Bit 15	R/W	DRU_SCAN_IN[3]/DRU_SCAN_OUT[3]	X
Bit 14	R/W	DRU_SCAN_IN[2]/DRU_SCAN_OUT[2]	X
Bit 13	R/W	DRU_SCAN_IN[1]/DRU_SCAN_OUT[1]	X
Bit 12	R/W	DRU_SCAN_IN[0]/DRU_SCAN_OUT[0]	X
Bit 11	R/W	DRU_SCAN_EN1	0
Bit 10	R/W	DRU_SCAN_EN2	0
Bit 9	R/W	DRU_CLK_EN1	0
Bit 8	R/W	DRU_CLK_EN2	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register controls the DRU and RXLV analog blocks for PMC internal testing. They are not used for normal operation.

DRU_SCAN_IN[3:0]

The DRU_SCAN_IN[3:0] bits (accessed during a write) control the analog wrapper signals, DRU_SCAN_IN[3:0].

DRU_SCAN_OUT[3:0]

The DRU_SCAN_OUT[3:0] bits (accessed during a read) control read the analog wrapper signals, DRU_SCAN_OUT[3:0].

DRU_SCAN_EN1

The DRU_SCAN_EN1, control the analog wrapper signal, DRU_SCAN_EN1.

DRU_SCAN_EN2

The DRU_SCAN_EN2, control the analog wrapper signal, DRU_SCAN_EN2.

DRU_CLK_EN1

The DRU_CLK_EN1, control the analog wrapper signal, DRU_CLK_EN1.

DRU_CLK_EN2

The DRU_CLK_EN2, control the analog wrapper signal, DRU_CLK_EN2.

12.13 T8TE Register Summary

There are 8 T8TE blocks in the S/UNI-MACH48 device. They are only active when the line side LVDS serial interface is enabled (SER_EN is logic 1). The T8TE encodes the 8B/10B serial TelecomBus.

There is one T8TE for each LVDS link. They are mapped as follows:

TSI Block Name	T8TE Base Address	Egress Link
T8TE#1	1860H	TPWRK[1] TNWRK[1]
T8TE #2	1868H	TPWRK[2] TNWRK[2]
T8TE #3	1870H	TPWRK[3] TNWRK[3]
T8TE #4	1878H	TPWRK[4] TNWRK[4]
T8TE #5	1880H	TPPROT[1] TNPROT[1]
T8TE #6	1888H	TPPROT[2] TNPROT[2]
T8TE #7	1890H	TPPROT[3] TNPROT[3]
T8TE #8	1898H	TPPROT[4] TNPROT[4]

Register T8TE_BASE + 00H: T8TE Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	LLBEN	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the T8TE.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the outgoing data stream. When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that TelecomBus control characters are not affected by the DLCV bit but are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic 1 is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic 0 when read. **CENTER must be set for all active T8TE instances after the CSU is locked to insure that skew between different transmit serial streams is minimal.**

LLBEN

The line loopback enable bit (LLBEN) controls line loopback operation. When LLBEN is logic 1, serial line loopback is enabled. When LLBEN is logic 0, line loopback is disabled.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is logic 1, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the output data stream. When TPINS is logic 0, no test patterns are generated.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Register T8TE_BASE + 01H: T8TE Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when the T8TE Interrupt status register is read. This bit does not cause a hardware interrupt on INTB, but it may be polled to check for errors.

Register T8TE_BASE + 02H: T8TE TelecomBus Mode #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE7[1]	0
Bit 14	R/W	TMODE7[0]	0
Bit 13	R/W	TMODE6[1]	0
Bit 12	R/W	TMODE6[0]	0
Bit 11	R/W	TMODE5[1]	0
Bit 10	R/W	TMODE5[0]	0
Bit 9	R/W	TMODE4[1]	0
Bit 8	R/W	TMODE4[0]	0
Bit 7	R/W	TMODE3[1]	0
Bit 6	R/W	TMODE3[0]	0
Bit 5	R/W	TMODE2[1]	0
Bit 4	R/W	TMODE2[0]	0
Bit 3	R/W	TMODE1[1]	0
Bit 2	R/W	TMODE1[0]	0
Bit 1	R/W	TMODE0[1]	0
Bit 0	R/W	TMODE0[0]	0

Register T8TE_BASE + 03H: T8TE TelecomBus Mode #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE11[1]	0
Bit 6	R/W	TMODE11[0]	0
Bit 5	R/W	TMODE10[1]	0
Bit 4	R/W	TMODE10[0]	0
Bit 3	R/W	TMODE9[1]	0
Bit 2	R/W	TMODE9[0]	0
Bit 1	R/W	TMODE8[1]	0
Bit 0	R/W	TMODE8[0]	0

T8TE Registers 02H and 03H store 12 STS-1's TelecomBus mode settings.

TMODE0[1:0]-TMODE11[1:0]

The TelecomBus mode registers (TMODE0[1:0]-TMODE11[1:0]) contain TelecomBus mode settings for each STS-1 timeslot in the STS-12 stream. Each STS-1 stream can work in MST, or HPT mode (see Section 14.3 for description of MST and HPT modes). The setting stored in TMODE**x**[1:0] (**x** can be 0-11) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters. Table 40 shows the configurations of each STS-1 stream.

Table 40 TelecomBus Mode

TMODEx[1:0]	Functional Description
00	MST Mode
01	HPT Mode
10	Reserved
11	Reserved

Register T8TE_BASE + 04H: T8TE Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

TP[9:0]

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the outgoing data stream for jitter test purpose. When the TPINS bit is logic 1, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the output data stream.

Register T8TE_BASE + 05H: T8TE Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	IDDQ	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	ATIN[3]	0
Bit 5	R/W	ATIN[2]	0
Bit 4	R/W	ATIN[1]	0
Bit 3	R/W	ATIN[0]	0
Bit 2	R/W	TXLV_ATMSB	1
Bit 1	R/W	PISO_ATMSB	1
Bit 0	R/W	ARSTB	1

These registers control analog blocks.

ARSTB

The analog reset bit (ARSTB) controls the TXLV and PISO operation. When ARSTB is logic 0, the TXLV and PISO are reset. This bit must be set to logic 1 for normal operation.

PISO_ATMSB

The PISO analog test mode select bit (PISO_ATMSB) controls the PISO test operation. PISO_ATMSB drives the output PISO_ATMSB pin low to enable test mode in the PISO. This bit is used for PMC internal test purposes and must be set to logic 1 for normal operation.

TXLV_ATMSB

The TXLV analog test mode select bit (TXLV_ATMSB) controls the TXLV test operation. TXLV_ATMSB drives the output TXLV_ATMSB pin low to enable test mode in the TXLV block. This bit is used for PMC internal test purposes and must be set to logic 1 for normal operation.

ATIN[3:0]

The analog test control inputs (ATIN[3:0]) control the PISO and TXLV test circuitry. These bits are used for PMC internal test purposes and are not used for normal operation.

PISO_ENB

The PISO enable bit (PISO_ENB) controls the PISO operation. When set to logic 1, PISO_ENB disables the PISO. When set to logic 0, PISO_ENB enables the PISO.

TXLV_ENB

The TXLV enable bit (TXLV_ENB) controls the TXLV operation. When set to logic 1, TXLV_ENB disables the TXLV. When set to logic 0, TXLV_ENB enables the TXLV.

IDDQ

The IDDQ controls the PISO operation. When IDDQ is set high, IDDQ test of the PISOis enabled. For normal operation IDDQ should be set to logic 0.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Register T8TE_BASE + 06H: T8TE DTB Bus

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	DTBO[3]	0
Bit 6	R/W	DTBO[2]	0
Bit 5	R/W	DTBO[1]	0
Bit 4	R/W	DTBO[0]	0
Bit 3	R	DTBI[3]	X
Bit 2	R	DTBI[2]	X
Bit 1	R	DTBI[1]	X
Bit 0	R	DTBI[0]	X

These registers control digital test bus for PISO and TXLV. They are not used for normal operation and should be left at their default values.

DTBO[3:0]

The analog wrapper digital test bus output bits (DTB_OUT[3:0]) are used to drive values on the digital test bus (DTB[3:0]). These bits are not used in normal operation.

DTBI[3:0]

The analog wrapper digital test bus input bits (DTB_IN[3:0]) are used to read values from the digital test bus (DTB[3:0]). Thee bits are not used in normal operation.

12.14 DLL Register Summary

The registers listed here are not to be used for any normal mode operation. They allow diagnostics for manufacturing procedures. There are 3 DLL blocks in the S/UNI-MACH48 device. The DLL's are used to meet timing requirements of device outputs. **No configuration of the DLL blocks is necessary for normal operation**.

DLL Clock	Base Address
RFCLK	18A0H
TFCLK	18A4H
SYSCLK	18A8H

Register DLL_BASE + 0H: DLL Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits should be set to logic 0 for proper operation.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is logic 1, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is logic 0, changes in the ERROR and ERR status do not generate an interrupt.

Register DLL_BASE + 01H: DLL Clock Vernier Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits should be set to logic 0 for proper operation. For normal operation, these bits should be left at logic zero.

Register DLL_BASE + 02H: DLL Clock Delay Tap Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Reserved

The Reserved bits serve no normal mode function.

Register DLL_BASE + 03H: DLL Clock Control Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	X
Bit 0	R	RUN	X

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of REFCLK and the rising edge of CLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1. The RUN register bit is cleared only by a system reset or a software reset (writing to DLL register 2).

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is logic 1. When ERROR is logic 1, the DLL cannot generate a DLLCLK phase which causes the rising edge of REFCLK to be aligned to the rising edge of CLK. ERROR is logic 0, when the DLL captures lock again.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. If the ERRORE interrupt enable is logic 1, the INTB output is also asserted when ERRORI asserts.

Reserved

The Reserved bits are not used in normal operations.

Register 18ACH: CSTR Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

Except for the CSU_ENB register bit, the other register bits are used for manufacturing test purposes only. They are not required for normal operations.

Reserved

The Reserved bits should be set to their default values for normal operation.

CSU_RSTB

The CSU_RSTB signal is a software reset signal that forces the CSU into a reset.

CSU_ENB

The CSU enable control signal (CSU_ENB) bit forces the CSU into low power configuration. The CSU is disabled when CSU_ENB is logic 1. The CSU is enabled when CSU_ENB is logic 0. This bit must be set to logic 0 for normal operation.

Register 18ADH: CSTR Interrupt Enable and CSU Lock Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1	R	CSU_LOCKV	X
Bit 0	R/W	CSU_LOCKE	0

CSU_LOCKE

The CSU lock interrupt enable bit (CSU_LOCKE) enables the assertion of a hardware interrupt on INTB when the CSU lock status changes. When CSU_LOCKE is logic 1, the hardware interrupt is enabled. When CSU_LOCKE is logic 0, the hardware interrupt is disabled.

CSU_LOCKV

The CSU lock status (CSU_LOCKV) indicates the current state of the CSU. When CSU_LOCKV is logic 1, the CSU has locked on to the SYSCLK reference and is operating normally. When CSU_LOCKV is logic 0, the CSU has not locked onto the SYSCLK reference and is not in normal operating mode.

Register 18AEH: CSTR CSU Lock Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1		Unused	X
Bit 0	R	CSU_LOCKI	X

CSU_LOCKI

The CSU lock interrupt indication bit (CSU_LOCKI) reports changes in the CSU lock status. CSU_LOCKI is logic 1 when the CSU transitions to or out of lock state. CSU_LOCKI is cleared when this register is read.

12.15 Dropped Cell/Packet Counter Summary

The registers listed here can be used to determine on a per-channel basis how many cells or packets are being dropped due to FIFO overflows.

Register 1900H + *x*: S/UNI-MACH48 Channel #*x* Dropped Cell/Packet Counter

Bit	Type	Function	Default
Bit 15	R	DROPCNT*x*[15]	X
Bit 14	R	DROPCNT*x*[14]	X
Bit 13	R	DROPCNT*x*[13]	X
Bit 12	R	DROPCNT*x*[12]	X
Bit 11	R	DROPCNT*x*[11]	X
Bit 10	R	DROPCNT*x*[10]	X
Bit 9	R	DROPCNT*x*[9]	X
Bit 8	R	DROPCNT*x*[8]	X
Bit 7	R	DROPCNT*x*[7]	X
Bit 6	R	DROPCNT*x*[6]	X
Bit 5	R	DROPCNT*x*[5]	X
Bit 4	R	DROPCNT*x*[4]	X
Bit 3	R	DROPCNT*x*[3]	X
Bit 1	R	DROPCNT*x*[2]	X
Bit 1	R	DROPCNT*x*[1]	X
Bit 0	R	DROPCNT*x*[0]	X

DROPCNT*x*[15:0]

The Channel *X* Dropped Cell/Packet Counter gives the number of cells or packets that were dropped due to FIFO overflows in the last accumulation interval for channel *X* (*X* = 0, 1 … 47 decimal or 0, 1 … 2F hex). An accumulation interval is initialized by writing to the S/UNI-MACH48 Global Performance Monitor Update register (0000H) or to any Dropped Cell/Packet Counter register (1900H – 192FH).

Register 1930H: S/UNI-MACH48 Drop Counter Interrupt Enable #1

Bit	Type	Function	Default
Bit 15	R/W	DROP_EN[15]	0
Bit 14	R/W	DROP_EN[14]	0
Bit 13	R/W	DROP_EN[13]	0
Bit 12	R/W	DROP_EN[12]	0
Bit 11	R/W	DROP_EN[11]	0
Bit 10	R/W	DROP_EN[10]	0
Bit 9	R/W	DROP_EN[9]	0
Bit 8	R/W	DROP_EN[8]	0
Bit 7	R/W	DROP_EN[7]	0
Bit 6	R/W	DROP_EN[6]	0
Bit 5	R/W	DROP_EN[5]	0
Bit 4	R/W	DROP_EN[4]	0
Bit 3	R/W	DROP_EN[3]	0
Bit 1	R/W	DROP_EN[2]	0
Bit 1	R/W	DROP_EN[1]	0
Bit 0	R/W	DROP_EN[0]	0

Register 1931H: S/UNI-MACH48 Drop Counter Interrupt Enable #2

Bit	Type	Function	Default
Bit 15	R/W	DROP_EN[31]	0
Bit 14	R/W	DROP_EN[30]	0
Bit 13	R/W	DROP_EN[29]	0
Bit 12	R/W	DROP_EN[28]	0
Bit 11	R/W	DROP_EN[27]	0
Bit 10	R/W	DROP_EN[26]	0
Bit 9	R/W	DROP_EN[25]	0
Bit 8	R/W	DROP_EN[24]	0
Bit 7	R/W	DROP_EN[23]	0
Bit 6	R/W	DROP_EN[22]	0
Bit 5	R/W	DROP_EN[21]	0
Bit 4	R/W	DROP_EN[20]	0
Bit 3	R/W	DROP_EN[19]	0
Bit 1	R/W	DROP_EN[18]	0
Bit 1	R/W	DROP_EN[17]	0
Bit 0	R/W	DROP_EN[16]	0

Register 1932H: S/UNI-MACH48 Drop Counter Interrupt Enable #3

Bit	Type	Function	Default
Bit 15	R/W	DROP_EN[47]	0
Bit 14	R/W	DROP_EN[46]	0
Bit 13	R/W	DROP_EN[45]	0
Bit 12	R/W	DROP_EN[44]	0
Bit 11	R/W	DROP_EN[43]	0
Bit 10	R/W	DROP_EN[42]	0
Bit 9	R/W	DROP_EN[41]	0
Bit 8	R/W	DROP_EN[40]	0
Bit 7	R/W	DROP_EN[39]	0
Bit 6	R/W	DROP_EN[38]	0
Bit 5	R/W	DROP_EN[37]	0
Bit 4	R/W	DROP_EN[36]	0
Bit 3	R/W	DROP_EN[35]	0
Bit 1	R/W	DROP_EN[34]	0
Bit 1	R/W	DROP_EN[33]	0
Bit 0	R/W	DROP_EN[32]	0

DROP_EN[47:0]

The Channel *X* Dropped Cell/Packet Interrupt Enable bit (DROP_EN[*x*]) enables the generation of an interrupt due to a cell or packet being dropped due to the FIFO for channel *X* overflowing. When DROP_EN[*x*] is set to logic 1, the interrupt is enabled.

Register 1933H: S/UNI-MACH48 Drop Counter Interrupt #1

Bit	Type	Function	Default
Bit 15	R	DROPI [15]	X
Bit 14	R	DROPI[14]	X
Bit 13	R	DROPI[13]	X
Bit 12	R	DROPI[12]	X
Bit 11	R	DROPI[11]	X
Bit 10	R	DROPI[10]	X
Bit 9	R	DROPI[9]	X
Bit 8	R	DROPI[8]	X
Bit 7	R	DROPI[7]	X
Bit 6	R	DROPI[6]	X
Bit 5	R	DROPI[5]	X
Bit 4	R	DROPI[4]	X
Bit 3	R	DROPI[3]	X
Bit 1	R	DROPI[2]	X
Bit 1	R	DROPI[1]	X
Bit 0	R	DROPI[0]	X

Register 1934H: S/UNI-MACH48 Drop Counter Interrupt #2

Bit	Type	Function	Default
Bit 15	R	DROPI[31]	X
Bit 14	R	DROPI[30]	X
Bit 13	R	DROPI[29]	X
Bit 12	R	DROPI[28]	X
Bit 11	R	DROPI[27]	X
Bit 10	R	DROPI[26]	X
Bit 9	R	DROPI[25]	X
Bit 8	R	DROPI[24]	X
Bit 7	R	DROPI[23]	X
Bit 6	R	DROPI[22]	X
Bit 5	R	DROPI[21]	X
Bit 4	R	DROPI[20]	X
Bit 3	R	DROPI[19]	X
Bit 1	R	DROPI[18]	X
Bit 1	R	DROPI[17]	X
Bit 0	R	DROPI[16]	X

Register 1935H: S/UNI-MACH48 Drop Counter Interrupt #3

Bit	Type	Function	Default
Bit 15	R	DROPI[47]	X
Bit 14	R	DROPI[46]	X
Bit 13	R	DROPI[45]	X
Bit 12	R	DROPI[44]	X
Bit 11	R	DROPI[43]	X
Bit 10	R	DROPI[42]	X
Bit 9	R	DROPI[41]	X
Bit 8	R	DROPI[40]	X
Bit 7	R	DROPI[39]	X
Bit 6	R	DROPI[38]	X
Bit 5	R	DROPI[37]	X
Bit 4	R	DROPI[36]	X
Bit 3	R	DROPI[35]	X
Bit 1	R	DROPI[34]	X
Bit 1	R	DROPI[33]	X
Bit 0	R	DROPI[32]	X

DROPI[47:0]

When the Channel *X* Dropped Cell/Packet Interrupt bit (DROPI[*x*]) is high, it indicates that a cell or packet was dropped due to the FIFO for channel *X* overflowing. These bits are cleared when each register is read. When DROP_EN[*x*] is set to logic 1, a system interrupt is generated. When DROP_EN[*x*] is set to logic 0, no system interrupt is generated, but these bits may still be polled for status information.

13 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-MACH48. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[13]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-MACH48 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-MACH48 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 41 Test Mode Register Memory Map

Address	Register
0000H-1FFFH	Normal Mode Registers
2000	Master Test Register
2001	Test Mode Address Force Enable
2002	Test Mode Address Force Value
2003	Analog Block Test
2004-3FFF	Reserved For Test

13.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 2000H: S/UNI-MACH48 Master Test

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	W	BYPASS	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	Reserved	0
Bit 2	W	Reserved	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-MACH48 test features. All bits, except PMCTST, PMCATST and BYPASS are reset to zero by a reset of the S/UNI-MACH48 using the RSTB input. PMCTST, PMCATST, and BYPASS are reset when CSB is logic 1. PMCTST, PMCATST and BYPASS can also be reset by writing a logic 0 to the corresponding register bit.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-MACH48 . While the HIZIO bit is a logic one, all output pins of the S/UNI-MACH48 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

PMCTST

The PMCTST bit is used to configure the S/UNI-MACH48 for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-MACH48 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors, and all analog blocks are forced into IDDQ mode. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST

The PMCATST bit is used to configure the analog portion of the S/UNI-MACH48 for PMC's manufacturing tests. The PMCATST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

BYPASS

The BYPASS bit forces the clock recovery and clock synthesis units into a reset, and permits the input data and clock to feed directly into the serial-to-parallel converter. BYPASS is available for PMC manufacturing test purposes only.

Register 2001H: S/UNI-MACH48 Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	TM_A_EN[12]	X
Bit 10	R/W	TM_A_EN[11]	X
Bit 9	R/W	TM_A_EN[10]	X
Bit 8	R/W	TM_A_EN[9]	X
Bit 7	R/W	TM_A_EN[8]	X
Bit 6	R/W	TM_A_EN[7]	X
Bit 5	R/W	TM_A_EN[6]	X
Bit 4	R/W	TM_A_EN[5]	X
Bit 3	R/W	TM_A_EN[4]	X
Bit 1	R/W	TM_A_EN[3]	X
Bit 1	R/W	TM_A_EN[2]	X
Bit 0	R/W	TM_A_EN[1]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A_EN[12:1]

When TM_A_EN[X] is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[X] register bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A_EN[12:2] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2002H: S/UNI-MACH48 Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	TM_A[12]	X
Bit 10	R/W	TM_A[11]	X
Bit 9	R/W	TM_A[10]	X
Bit 8	R/W	TM_A[9]	X
Bit 7	R/W	TM_A[8]	X
Bit 6	R/W	TM_A[7]	X
Bit 5	R/W	TM_A[6]	X
Bit 4	R/W	TM_A[5]	X
Bit 3	R/W	TM_A[4]	X
Bit 1	R/W	TM_A[3]	X
Bit 1	R/W	TM_A[2]	X
Bit 0	R/W	TM_A[1]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A[12:1]

When TM_A_EN[X] is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[X] bit replaces the input pin A[X]. The TM_A[X] bits are not cleared on reset.

Register 2003H: S/UNI-MACH48 Top Level Test Register

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	CLOCKTST	X
Bit 0	R/W	FORCECOUNT	X

This register is used to enable test mode in the analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

FORCECOUNT

When FORCECOUNT and PMCTST are logic 1, the counter that generates the 8kHz clock that clocks the LOF integrator are forced to the value 4 sysclk cycles before the 8kHz clock pulse. This bit allows the LOF integrator to be tested in a reasonable time-frame.

CLOCKTST

When CLOCKTST and PMCTST are logic 1, the VCLK clock muxes are forced into normal operation so that the 52 MHz and 19 MHz generated clocks are testable.

Reserved

The reserved bits should be set to logic 0 for normal tests. They have no affect on the operation of the device when PMCTST is logic 0.

13.2 JTAG Test Port

The S/UNI-MACH48 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 42 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 43 Identification Register

Length	32 bits
Version Number	2H
Part Number	7390H
Manufacturer's Identification Code	0CDH
Device Identification	273900CDH

Table 44 Boundary Scan Register

Length - 386 bits

Pin/Enable	Register Bit	Cell Type	Device ID	Pin/Enable	Register Bit	Cell Type	Device ID
OEB_RDAT[31]	385	OUT_CELL	L	OD_3[5]	192	OUT_CELL	-
RDAT[31]	384	OUT_CELL	L	OEB_OD_3[0]	191	OUT_CELL	-
OEB_RDAT[29]	383	OUT_CELL	H	OD_3[0]	190	OUT_CELL	-
RDAT[29]	382	OUT_CELL	L	OEB_OPL[3]	189	OUT_CELL	-
OEB_RDAT[30]	381	OUT_CELL	L	OPL[3]	188	OUT_CELL	-
RDAT[30]	380	OUT_CELL	H	OEB_OD_3[1]	187	OUT_CELL	-
OEB_RDAT[28]	379	OUT_CELL	H	OD_3[1]	186	OUT_CELL	-
RDAT[28]	378	OUT_CELL	H	OEB_OD_3[2]	185	OUT_CELL	-
OEB_RDAT[27]	377	OUT_CELL	L	OD_3[2]	184	OUT_CELL	-
RDAT[27]	376	OUT_CELL	L	IPAIS[2]	183	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device ID	Pin/Enable	Register Bit	Cell Type	Device ID
OEB_RDAT[26]	375	OUT_CELL	H	OEB_OJ0J1[3]	182	OUT_CELL	-
RDAT[26]	374	OUT_CELL	H	OJ0J1[3]	181	OUT_CELL	-
OEB_RDAT[25]	373	OUT_CELL	H	ID_2[6]	180	IN_CELL	-
RDAT[25]	372	OUT_CELL	L	ID_2[7]	179	IN_CELL	-
OEB_RDAT[23]	371	OUT_CELL	L	IDP[2]	178	IN_CELL	-
RDAT[23]	370	OUT_CELL	H	ID_2[4]	177	IN_CELL	-
OEB_RDAT[24]	369	OUT_CELL	L	ID_2[5]	176	IN_CELL	-
RDAT[24]	368	OUT_CELL	L	ID_2[3]	175	IN_CELL	-
OEB_RDAT[22]	367	OUT_CELL	L	ID_2[1]	174	IN_CELL	-
RDAT[22]	366	OUT_CELL	L	ID_2[2]	173	IN_CELL	-
OEB_RDAT[21]	365	OUT_CELL	L	IJ0J1[2]	172	IN_CELL	-
RDAT[21]	364	OUT_CELL	L	OEB_OALARM[2]	171	OUT_CELL	-
OEB_RDAT[20]	363	OUT_CELL	L	OALARM[2]	170	OUT_CELL	-
RDAT[20]	362	OUT_CELL	L	IPL[2]	169	IN_CELL	-
OEB_RDAT[19]	361	OUT_CELL	H	ID_2[0]	168	IN_CELL	-
RDAT[19]	360	OUT_CELL	H	OEB_OD_2[7]	167	OUT_CELL	-
OEB_RDAT[18]	359	OUT_CELL	L	OD_2[7]	166	OUT_CELL	-
RDAT[18]	358	OUT_CELL	L	OEB_ODP[2]	165	OUT_CELL	-
OEB_RDAT[17]	357	OUT_CELL	H	ODP[2]	164	OUT_CELL	-
RDAT[17]	356	OUT_CELL	H	OEB_OD_2[4]	163	OUT_CELL	-
OEB_RDAT[16]	355	OUT_CELL	L	OD_2[4]	162	OUT_CELL	-
RDAT[16]	354	OUT_CELL	H	OEB_OD_2[3]	161	OUT_CELL	-
OEB_RDAT[15]	353	OUT_CELL	-	OD_2[3]	160	OUT_CELL	-
RDAT[15]	352	OUT_CELL	-	OEB_OD_2[5]	159	OUT_CELL	-
OEB_RDAT[14]	351	OUT_CELL	-	OD_2[5]	158	OUT_CELL	-
RDAT[14]	350	OUT_CELL	-	OEB_OD_2[6]	157	OUT_CELL	-
OEB_RDAT[12]	349	OUT_CELL	-	OD_2[6]	156	OUT_CELL	-
RDAT[12]	348	OUT_CELL	-	OEB_OD_2[0]	155	OUT_CELL	-
OEB_RDAT[13]	347	OUT_CELL	-	OD_2[0]	154	OUT_CELL	-
RDAT[13]	346	OUT_CELL	-	OEB_OD_2[1]	153	OUT_CELL	-
OEB_RDAT[11]	345	OUT_CELL	-	OD_2[1]	152	OUT_CELL	-
RDAT[11]	344	OUT_CELL	-	OEB_OD_2[2]	151	OUT_CELL	-
OEB_RDAT[10]	343	OUT_CELL	-	OD_2[2]	150	OUT_CELL	-
RDAT[10]	342	OUT_CELL	-	OEB_OJ0J1[2]	149	OUT_CELL	-
OEB_RDAT[9]	341	OUT_CELL	-	OJ0J1[2]	148	OUT_CELL	-
RDAT[9]	340	OUT_CELL	-	OEB_OPL[2]	147	OUT_CELL	-
OEB_RDAT[8]	339	OUT_CELL	-	OPL[2]	146	OUT_CELL	-
RDAT[8]	338	OUT_CELL	-	IDP[1]	145	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device ID	Pin/Enable	Register Bit	Cell Type	Device ID
OEB_RDAT[6]	337	OUT_CELL	-	IPAIS[1]	144	IN_CELL	-
RDAT[6]	336	OUT_CELL	-	ID_1[4]	143	IN_CELL	-
OEB_RDAT[7]	335	OUT_CELL	-	ID_1[5]	142	IN_CELL	-
RDAT[7]	334	OUT_CELL	-	ID_1[7]	141	IN_CELL	-
OEB_RDAT[5]	333	OUT_CELL	-	ID_1[6]	140	IN_CELL	-
RDAT[5]	332	OUT_CELL	-	ID_1[2]	139	IN_CELL	-
OEB_RDAT[4]	331	OUT_CELL	-	ID_1[3]	138	IN_CELL	-
RDAT[4]	330	OUT_CELL	-	IPL[1]	137	IN_CELL	-
OEB_RDAT[3]	329	OUT_CELL	-	ID_1[0]	136	IN_CELL	-
RDAT[3]	328	OUT_CELL	-	ID_1[1]	135	IN_CELL	-
OEB_RDAT[2]	327	OUT_CELL	-	OEB_OALARM[1]	134	OUT_CELL	-
RDAT[2]	326	OUT_CELL	-	OALARM[1]	133	OUT_CELL	-
OEB_RDAT[1]	325	OUT_CELL	-	IJ0J1[1]	132	IN_CELL	-
RDAT[1]	324	OUT_CELL	-	OEB_OD_1[5]	131	OUT_CELL	-
OEB_RDAT[0]	323	OUT_CELL	-	OD_1[5]	130	OUT_CELL	-
RDAT[0]	322	OUT_CELL	-	OEB_OD_1[6]	129	OUT_CELL	-
OEB_RPRTY	321	OUT_CELL	-	OD_1[6]	128	OUT_CELL	-
RPRTY	320	OUT_CELL	-	OEB_ODP[1]	127	OUT_CELL	-
OEB_RSOC_RSOP	319	OUT_CELL	-	ODP[1]	126	OUT_CELL	-
RSOC_RSOP	318	OUT_CELL	-	OEB_OD_1[7]	125	OUT_CELL	-
OEB_REOP	317	OUT_CELL	-	OD_1[7]	124	OUT_CELL	-
REOP	316	OUT_CELL	-	OEB_OD_1[3]	123	OUT_CELL	-
OEB_RSX	315	OUT_CELL	-	OD_1[3]	122	OUT_CELL	-
RSX	314	OUT_CELL	-	OEB_OD_1[4]	121	OUT_CELL	-
OEB_RERR	313	OUT_CELL	-	OD_1[4]	120	OUT_CELL	-
RERR	312	OUT_CELL	-	OEB_OD_1[0]	119	OUT_CELL	-
OEB_RMOD[1]	311	OUT_CELL	-	OD_1[0]	118	OUT_CELL	-
RMOD[1]	310	OUT_CELL	-	OEB_OD_1[1]	117	OUT_CELL	-
OEB_RMOD[0]	309	OUT_CELL	-	OD_1[1]	116	OUT_CELL	-
RMOD[0]	308	OUT_CELL	-	OEB_OD_1[2]	115	OUT_CELL	-
RADR[4]	307	IN_CELL	-	OD_1[2]	114	OUT_CELL	-
RADR[3]	306	IN_CELL	-	OEB_OJ0J1[1]	113	OUT_CELL	-
RADR[5]	305	IN_CELL	-	OJ0J1[1]	112	OUT_CELL	-
OEB_RCA_RVAL	304	OUT_CELL	-	OEB_OPL[1]	111	OUT_CELL	-
RCA_RVAL	303	OUT_CELL	-	OPL[1]	110	OUT_CELL	-
RADR[1]	302	IN_CELL	-	OEB_D[15]	109	OUT_CELL	-
RADR[2]	301	IN_CELL	-	D[15]	108	IO_CELL	-

Pin/Enable	Register Bit	Cell Type	Device ID	Pin/Enable	Register Bit	Cell Type	Device ID
RENB	300	IN_CELL	-	OEB_D[14]	107	OUT_CELL	-
RFCLK	299	IN_CELL	-	D[14]	106	IO_CELL	-
RADR[0]	298	IN_CELL	-	OEB_D[13]	105	OUT_CELL	-
OEB_ROHCH[5]	297	OUT_CELL	-	D[13]	104	IO_CELL	-
ROHCH[5]	296	OUT_CELL	-	OEB_D[12]	103	OUT_CELL	-
OEB_ROHCH[4]	295	OUT_CELL	-	D[12]	102	IO_CELL	-
ROHCH[4]	294	OUT_CELL	-	OEB_D[11]	101	OUT_CELL	-
OEB_ROHCH[2]	293	OUT_CELL	-	D[11]	100	IO_CELL	-
ROHCH[2]	292	OUT_CELL	-	OEB_D[10]	99	OUT_CELL	-
OEB_ROHCH[3]	291	OUT_CELL	-	D[10]	98	IO_CELL	-
ROHCH[3]	290	OUT_CELL	-	OEB_D[9]	97	OUT_CELL	-
OEB_ROHCH[0]	289	OUT_CELL	-	D[9]	96	IO_CELL	-
ROHCH[0]	288	OUT_CELL	-	OEB_D[8]	95	OUT_CELL	-
OEB_ROHVAL	287	OUT_CELL	-	D[8]	94	IO_CELL	-
ROHVAL	286	OUT_CELL	-	OEB_D[7]	93	OUT_CELL	-
OEB_ROHCH[1]	285	OUT_CELL	-	D[7]	92	IO_CELL	-
ROHCH[1]	284	OUT_CELL	-	OEB_D[6]	91	OUT_CELL	-
OEB_ROH	283	OUT_CELL	-	D[6]	90	IO_CELL	-
ROH	282	OUT_CELL	-	OEB_D[5]	89	OUT_CELL	-
OEB_ROHFP	281	OUT_CELL	-	D[5]	88	IO_CELL	-
ROHFP	280	OUT_CELL	-	OEB_D[4]	87	OUT_CELL	-
OEB_TOHCH[3]	279	OUT_CELL	-	D[4]	86	IO_CELL	-
TOHCH[3]	278	OUT_CELL	-	OEB_D[3]	85	OUT_CELL	-
OEB_TOHCH[2]	277	OUT_CELL	-	D[3]	84	IO_CELL	-
TOHCH[2]	276	OUT_CELL	-	OEB_D[2]	83	OUT_CELL	-
OEB_TOHCH[4]	275	OUT_CELL	-	D[2]	82	IO_CELL	-
TOHCH[4]	274	OUT_CELL	-	OEB_D[1]	81	OUT_CELL	-
OEB_TOHCH[5]	273	OUT_CELL	-	D[1]	80	IO_CELL	-
TOHCH[5]	272	OUT_CELL	-	OEB_D[0]	79	OUT_CELL	-
OEB_TOHVAL	271	OUT_CELL	-	D[0]	78	IO_CELL	-
TOHVAL	270	OUT_CELL	-	A[13]	77	IN_CELL	-
OEB_TOHCH[0]	269	OUT_CELL	-	A[11]	76	IN_CELL	-
TOHCH[0]	268	OUT_CELL	-	A[12]	75	IN_CELL	-
OEB_TOHCH[1]	267	OUT_CELL	-	A[10]	74	IN_CELL	-
TOHCH[1]	266	OUT_CELL	-	A[9]	73	IN_CELL	-
TOH	265	IN_CELL	-	A[8]	72	IN_CELL	-
TOHINS	264	IN_CELL	-	A[7]	71	IN_CELL	-
OEB_TOHFP	263	OUT_CELL	-	A[6]	70	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device ID	Pin/Enable	Register Bit	Cell Type	Device ID
TOHFP	262	OUT_CELL	-	A[5]	69	IN_CELL	-
OCMP	261	IN_CELL	-	A[4]	68	IN_CELL	-
ICMP	260	IN_CELL	-	A[3]	67	IN_CELL	-
RWSEL	259	IN_CELL	-	A[2]	66	IN_CELL	-
OEB_TJ0FP	258	OUT_CELL	-	A[1]	65	IN_CELL	-
TJ0FP	257	OUT_CELL	-	CSB	64	IN_CELL	-
SYSCLK	256	IN_CELL	-	A[0]	63	IN_CELL	-
OJ0REF	255	IN_CELL	-	ALE	62	IN_CELL	-
RJ0FP	254	IN_CELL	-	RDB	61	IN_CELL	-
IPAIS[4]	253	IN_CELL	-	WRB	60	IN_CELL	-
IDP[4]	252	IN_CELL	-	RSTB	59	IN_CELL	-
ID_4[7]	251	IN_CELL	-	OEB_INTB	58	OUT_CELL	-
ID_4[6]	250	IN_CELL	-	INTB	57	OUT_CELL	-
ID_4[5]	249	IN_CELL	-	POS_UL3B	56	IN_CELL	-
ID_4[4]	248	IN_CELL	-	OEB_RPOHFP	55	OUT_CELL	-
ID_4[3]	247	IN_CELL	-	RPOHFP	54	OUT_CELL	-
ID_4[2]	246	IN_CELL	-	REF8K	53	IN_CELL	-
ID_4[1]	245	IN_CELL	-	DS3TICLK	52	IN_CELL	-
IPL[4]	244	IN_CELL	-	TDAT[30]	51	IN_CELL	-
ID_4[0]	243	IN_CELL	-	TDAT[31]	50	IN_CELL	-
IJ0J1[4]	242	IN_CELL	-	SER_EN	49	IN_CELL	-
OEB_OALARM[4]	241	OUT_CELL	-	TDAT[28]	48	IN_CELL	-
OALARM[4]	240	OUT_CELL	-	TDAT[29]	47	IN_CELL	-
OEB_ODP[4]	239	OUT_CELL	-	TDAT[25]	46	IN_CELL	-
ODP[4]	238	OUT_CELL	-	TDAT[24]	45	IN_CELL	-
OEB_OD_4[7]	237	OUT_CELL	-	TDAT[26]	44	IN_CELL	-
OD_4[7]	236	OUT_CELL	-	TDAT[27]	43	IN_CELL	-
OEB_OD_4[6]	235	OUT_CELL	-	TDAT[21]	42	IN_CELL	-
OD_4[6]	234	OUT_CELL	-	TDAT[22]	41	IN_CELL	-
OEB_OD_4[5]	233	OUT_CELL	-	TDAT[23]	40	IN_CELL	-
OD_4[5]	232	OUT_CELL	-	TDAT[18]	39	IN_CELL	-
OEB_OD_4[4]	231	OUT_CELL	-	TDAT[19]	38	IN_CELL	-
OD_4[4]	230	OUT_CELL	-	TDAT[20]	37	IN_CELL	-
OEB_OD_4[3]	229	OUT_CELL	-	TDAT[16]	36	IN_CELL	-
OD_4[3]	228	OUT_CELL	-	TDAT[17]	35	IN_CELL	-
OEB_OD_4[1]	227	OUT_CELL	-	TDAT[13]	34	IN_CELL	-
OD_4[1]	226	OUT_CELL	-	TDAT[12]	33	IN_CELL	-
OEB_OD_4[2]	225	OUT_CELL	-	TDAT[14]	32	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device ID	Pin/Enable	Register Bit	Cell Type	Device ID
OD_4[2]	224	OUT_CELL	-	TDAT[15]	31	IN_CELL	-
OEB_OD_4[0]	223	OUT_CELL	-	TDAT[9]	30	IN_CELL	-
OD_4[0]	222	OUT_CELL	-	TDAT[10]	29	IN_CELL	-
OEB_OPL[4]	221	OUT_CELL	-	TDAT[11]	28	IN_CELL	-
OPL[4]	220	OUT_CELL	-	TDAT[6]	27	IN_CELL	-
IPAIS[3]	219	IN_CELL	-	TDAT[7]	26	IN_CELL	-
OEB_OJ0J1[4]	218	OUT_CELL	-	TDAT[8]	25	IN_CELL	-
OJ0J1[4]	217	OUT_CELL	-	TDAT[4]	24	IN_CELL	-
IDP[3]	216	IN_CELL	-	TDAT[5]	23	IN_CELL	-
ID_3[7]	215	IN_CELL	-	TDAT[1]	22	IN_CELL	-
ID_3[5]	214	IN_CELL	-	TDAT[0]	21	IN_CELL	-
ID_3[6]	213	IN_CELL	-	TDAT[2]	20	IN_CELL	-
ID_3[2]	212	IN_CELL	-	TDAT[3]	19	IN_CELL	-
ID_3[3]	211	IN_CELL	-	TSOC_TSOP	18	IN_CELL	-
ID_3[4]	210	IN_CELL	-	TEOP	17	IN_CELL	-
IPL[3]	209	IN_CELL	-	TPRTY	16	IN_CELL	-
ID_3[0]	208	IN_CELL	-	TMOD[1]	15	IN_CELL	-
ID_3[1]	207	IN_CELL	-	TMOD[0]	14	IN_CELL	-
OEB_OALARM[3]	206	OUT_CELL	-	TERR	13	IN_CELL	-
OALARM[3]	205	OUT_CELL	-	TSX	12	IN_CELL	-
IJ0J1[3]	204	IN_CELL	-	TADR[5]	11	IN_CELL	-
OEB_OD_3[6]	203	OUT_CELL	-	TADR[4]	10	IN_CELL	-
OD_3[6]	202	OUT_CELL	-	OEB_STPA	9	OUT_CELL	-
OEB_OD_3[7]	201	OUT_CELL	-	STPA	8	OUT_CELL	-
OD_3[7]	200	OUT_CELL	-	OEB_TCA_PTPA	7	OUT_CELL	-
OEB_ODP[3]	199	OUT_CELL	-	TCA_PTPA	6	OUT_CELL	-
ODP[3]	198	OUT_CELL	-	TADR[1]	5	IN_CELL	-
OEB_OD_3[3]	197	OUT_CELL	-	TADR[0]	4	IN_CELL	-
OD_3[3]	196	OUT_CELL	-	TADR[2]	3	IN_CELL	-
OEB_OD_3[4]	195	OUT_CELL	-	TADR[3]	2	IN_CELL	-
OD_3[4]	194	OUT_CELL	-	TENB	1	IN_CELL	-
OEB_OD_3[5]	193	OUT_CELL	-	TFCLK	0	IN_CELL	-

Notes:

1. When set high, INTB will be set to high impedance.
2. Each output cell has its own output enable (OEB*)
3. OEB_RDAT[31] is the first bit in the boundary scan chain, and TFCLK is the first bit out of the boundary scan chain.

13.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 12 Input Observation Cell (IN_CELL)

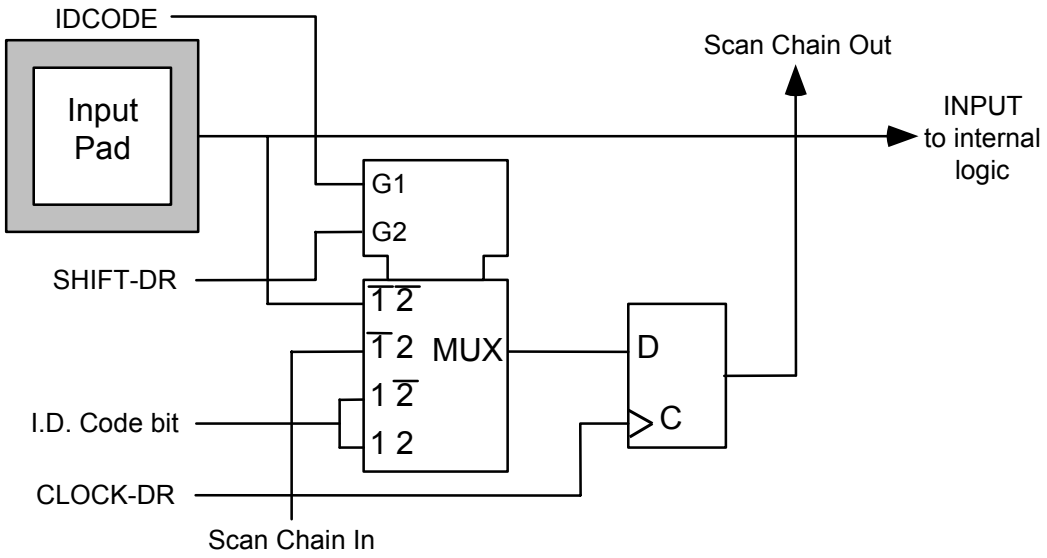


Figure 13 Output Cell (OUT_CELL)

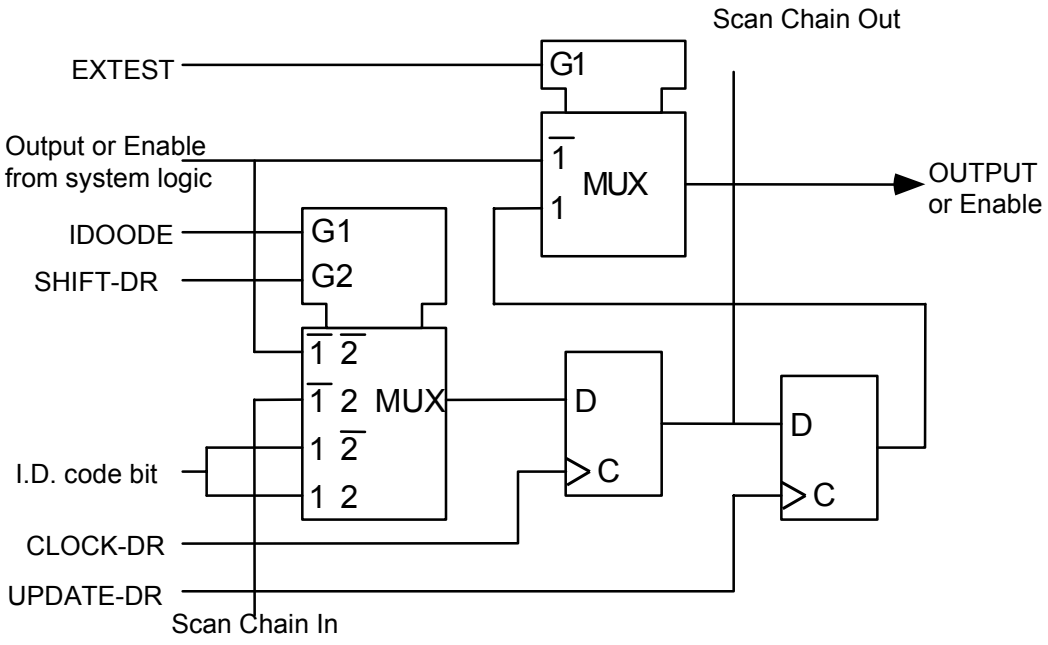


Figure 14 Bidirectional Cell (IO_CELL)

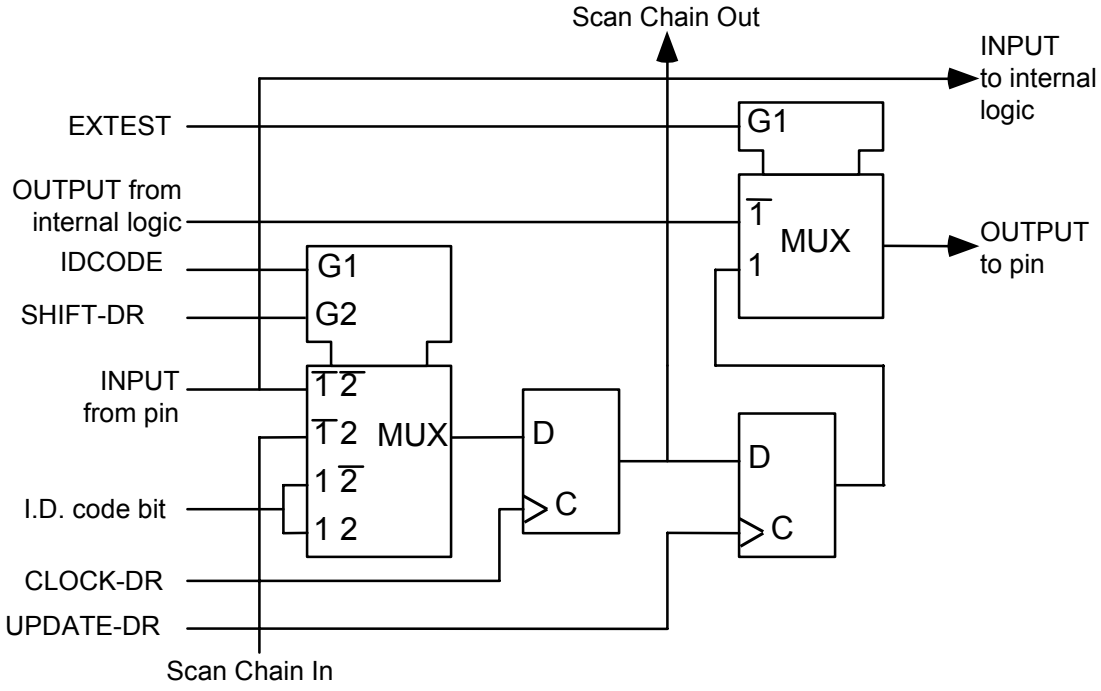
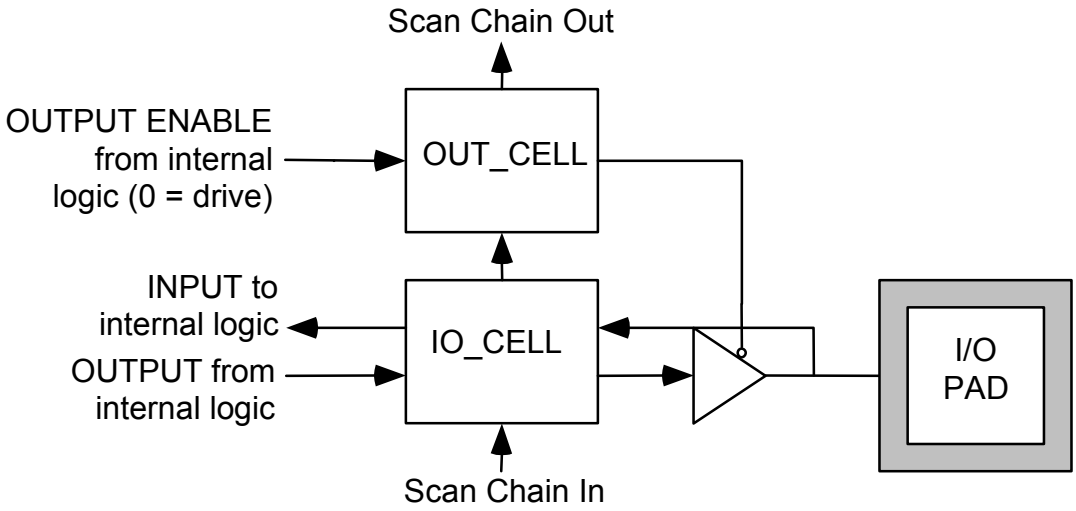


Figure 15 Layout of Output Enable and Bidirectional Cells



14 Operation

14.1 S/UNI-MACH48 Conceptual Regions

The S/UNI-MACH48 can conceptually be split into 3 regions: line side timeslots, system side timeslots, and system side channels. Each region has its data streams segregated differently and has a transmit half and a receive half.

In the Rx-Line-Side and Tx-Line-Side Timeslots regions, the data stream is formed from an aggregation of STS-1/STM-0s, STS-3c/STM-1s, STS-12c/STM-4cs, or a single STS-48c/STM-16c. Timeslots correspond to SONET/SDH timeslots. The timeslots which form each concatenated payload can be organized in any manner.

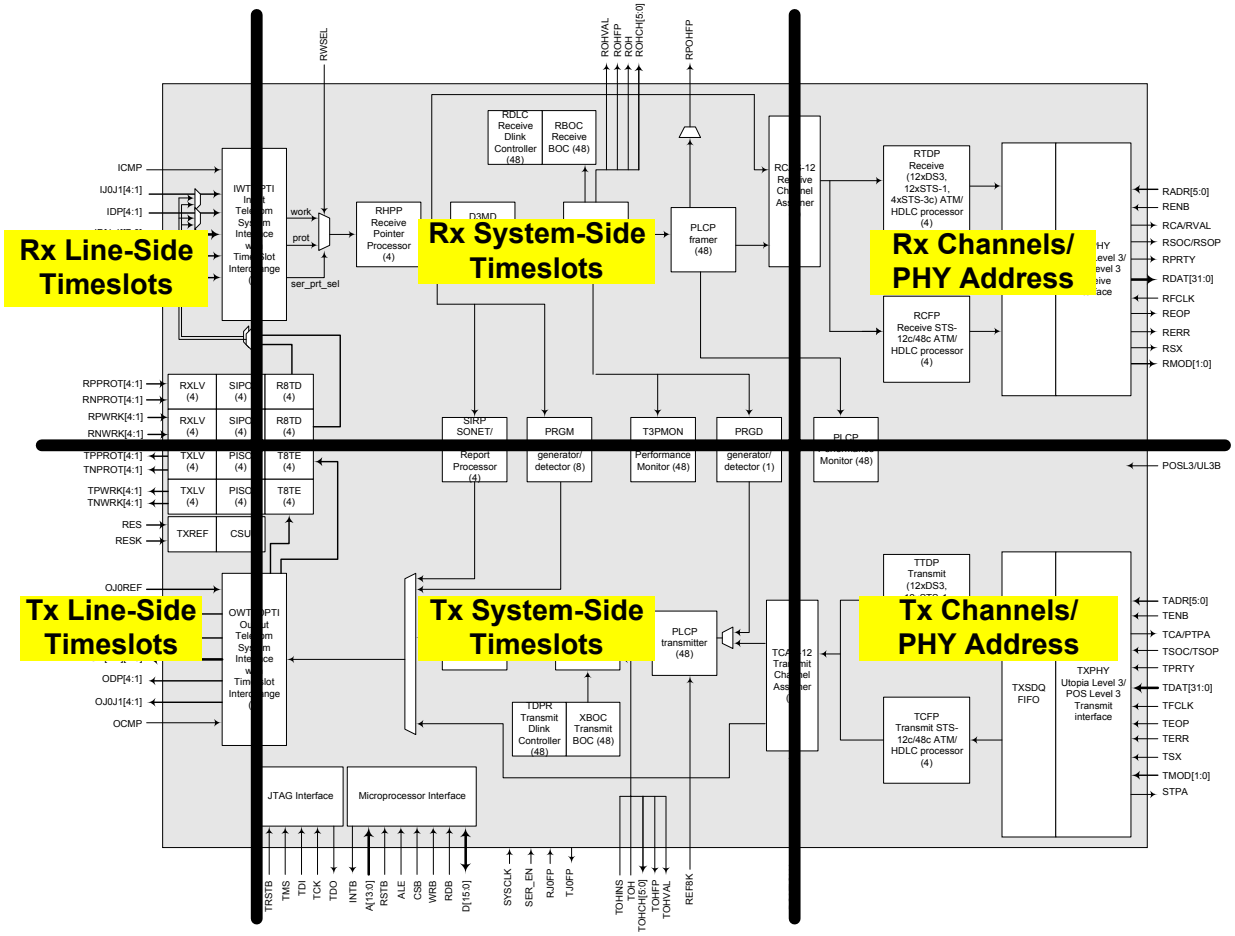
In the Rx-System-Side and Tx-System-Side Timeslots regions, the timeslots also correspond to SONET/SDH timeslots. However, the timeslots which form each concatenated payload in this region must be organized into the formats shown in Table 52 and Table 53. To fully utilize the features of the S/UNI-MACH48, it is recommended to organize the timeslots so they are symmetrical on the Receive (Rx) and Transmit (Tx) sides. Symmetrical organization allows automatic alarm reaction such as sending of DS3 FERFS upon detection of DS3 FEBE, LCD, OOF, RED, and AIS, RDI transmission upon LCD indications, and loopback of SONET/SDH RDI and REI values. Symmetrical organization also allows per-channel loopback of ATM/POS/HDLC data from the system Utopia L3 and POS-PHY L3 interfaces.

Translation from the Rx-Line-Side region to the Rx-System-Side region is done in the IWTI and IPTI blocks. Translation from the Tx-System-Side to the Tx-Line-Side region is done in the OWTI and OPTI blocks.

In the Rx Channels/PHY Address and Tx Channels/PHY Address regions, the data is organized in terms of channels. Channels are also known as PHY Addresses. The Channel/PHY Address value is equivalent to the value of RADR[5:0] and TADR[5:0] on the Utopia L3 interface or the PHY address presented on TDAT[5:0] (when TSX = 1),and RDAT[5:0] (when RSX = 1) on the POS-PHY L3 interface.

Translation from the Rx-System-Side region to the Rx Channel/PHY Address region is done in the RCAS12 blocks. Translation from the Tx Channel/PHY Address to the Tx-System-Side region is done in the TCAS12 blocks.

Figure 16 S/UNI-MACH48 Conceptual Regions



14.2 Serial TelecomBus (LVDS) Operation

14.2.1 Character Alignment

The character alignment sub-block locates character boundaries in the incoming Serial TelecomBus 8B/10B data stream. The framer logic may be in one of two states, SYNC state and HUNT state. It uses the 8B/10B control character (K28.5) which encodes the SONET/SDH J0 byte to locate character boundaries and to enter the SYNC state. It monitors the receive data stream for line code violations (LCV). An LCV is declared when the running disparity of the receive data is not consistent with the previous character or the data is not one of the characters defined in IEEE std. 802.3. Excessive LCVs are used to transition the framer logic to the HUNT state.

Normal operation occurs when the character alignment sub-block is in the SYNC state. 8B/10B characters are extracted from the FIFO using the character alignment of the K28.5 character that caused entry to the SYNC state. Mimic K28.5 characters at other alignments are ignored. The receive data is constantly monitored for line code violations. If 5 or more LCVs are detected in a window of 15 characters, the character alignment sub-block transitions to the HUNT state. It will search all possible alignments in the receive data for the K28.5 character. In the mean time, the original character alignment is maintained until a K28.5 character is found. At that point, the character alignment is moved to this new location and the sub-block transitions to the SYNC state.

14.2.2 Frame Alignment

The frame alignment sub-block monitors the data read from the FIFO buffer sub-block for the J0 byte. When the frame counter sub-block indicates the J0 byte position, a J0 character is expected to be read from the FIFO. If a J0 byte is read out of the FIFO at other byte positions, a J0 byte error counter is incremented. When the counter reaches a count of 3, the frame alignment sub-block transitions to HUNT state. The next time a J0 character is read from the FIFO, the associated read address is latched and the sub-block transitions back to the SYNC state. The J0 byte error counter is cleared when a J0 byte is read from the FIFO at the expected position.

14.2.3 Character Decode

The following tables show the extended 8B/10B maps used by the S/UNI-MACH48. The extended character set allows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. The table is divided into two sections, one for each software configurable mode of operation.

Table 45 Serial TelecomBus 8B/10B Control Character Decoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	IJ0J1=’b1, IPL = ‘b0 Transport frame alignment
K.28.4-	001111 0010	-	IPAIS=’b1’ High-order path AIS
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	IPL = ‘b0, High-order path H3 byte, no negative justification event
K28.0+	-	110000 1011	IPL = ‘b0 High-order path PSI byte, positive justification event
K28.6	001111 0110	110000 1001	IJ1=’b1’, IPL = ‘b1 High-order path frame alignment

14.2.4 Character Encode

The character encode sub-block encodes the TelecomBus control characters into an extended set of 8B/10B TelecomBus control signals. The table is divided into two sections, one for each mode of operation in the 8B/10B encoder in an external device upstream of the S/UNI-MACH48.

Table 46 Serial TelecomBus 8B/10B Control Character Encoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	OJ0='b1' Transport frame alignment OD[7:0] = 'h01
K.28.4-	001111 0010	-	OALARM='b1' High-order path alarm (set using the CHx_OALARM (x = 0, 1, …11) register bits in the TCAS12 blocks)
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	OPL = 'b0, High-order path H3 byte, no negative justification event OD[7:0] = 'h00
K28.0+	-	110000 1011	OPL = 'b0 High-order path PSO byte, positive justification event OD[7:0] = 'h00
K28.6	001111 0110	110000 1001	OJ1='b1' High-order path frame alignment OD[7:0] = 'h00

14.3 TelecomBus MST and HPT Modes

The S/UNI-MACH48 can be made to operate in either Multiplex Section Termination (MST) or High Order Path Termination (HPT) mode.

MST mode is used for systems where each device (like the PM5315 Spectra-2488, PM5313 Spectra-622, PM5317 Spectra 4x155, or the S/UNI-MACH48) have J1 pointer interpretors so only the J0 frame indicator is required.

HPT mode is used for systems which have devices that do not have J1 pointer interpretors so J1 indications are required on the TelecomBus interfaces.

The parallel TelecomBus inherently supplies both MST and HPT signals. The serial TelecomBus needs to be configured for MST or HPT modes. In MST mode, the J1 character is not overwritten by special 8B/10B characters. In HPT mode, it is specially marked to indicate the J1 location.

On the S/UNI-MACH48 receive interface, MST mode can be activated by setting the RHPP_EN register bit to logic 1 in the S/UNI-MACH48 Master Reset, Configuration, and Global Digital Loopback register. HPT mode is actived by setting the RHPP_EN register bit to logic 0.

On the S/UNI-MACH48 transmit interface, MST mode is activated for timeslot ***x*** by setting the TMODE***x***[1:0] bits to logic ‘b00 in the T8TE TelecomBus Mode #1 and T8TE TelecomBus Mode #2 registers. HPT mode is activated by setting TMODE***x***[1:0] to logic ‘b01. Note that regardless of the MST/HPT setting in the transmit direction, valid H1/H2 bytes (J1 Pointer) are always output on the TelecomBus, so a downstream device may operate in MST mode.

14.4 DS3 PLCP Frame Format

The S/UNI-MACH48 provides support for DS3 PLCP frame formats. The structure of this format is illustrated in Figure 17.

Figure 17 DS3 PLCP Frame Format

<table>
<tr><td>A1</td><td>A2</td><td>P11</td><td>Z6</td><td>ATM Cell</td><td rowspan="12">PLCP Frame
Rate 125 µs</td></tr>
<tr><td>A1</td><td>A2</td><td>P10</td><td>Z5</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P9</td><td>Z4</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P8</td><td>Z3</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P7</td><td>Z2</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P6</td><td>Z1</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P5</td><td>F1</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P4</td><td>B1</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P3</td><td>G1</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P2</td><td>M2</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P1</td><td>M1</td><td>ATM Cell</td></tr>
<tr><td>A1</td><td>A2</td><td>P0</td><td>C1</td><td>ATM Cell</td><td>Trailer</td></tr>
<tr><td colspan="3">Framing (3 octets)</td><td>POH</td><td>53 octets</td><td>13 or 14 nibbles</td></tr>
</table>

The DS3 PLCP frame provides the transmission of 12 ATM cells every 125 µs. The PLCP frame is nibble aligned to the overhead bits in the DS3 frame; however, there is no relationship between the start of the PLCP frame and the start of the DS3 M-frame. A trailer is inserted at the end of each PLCP frame. The number of nibbles inserted (13 or 14) is varied continuously such that the resulting PLCP frame rate can be locked to an 8 kHz reference.

Table 47 PLCP Overhead Processing

Overhead Field	Transmit Operation	Receive Operation
A1, A2: Frame Alignment Pattern	Inserts the PLCP frame alignment pattern (F628H)	Searches the receive stream for the PLCP frame alignment pattern. When the pattern has been detected for two consecutive rows, along with two valid, and sequential path overhead identifier octets, the S/UNI-MACH48 declares in-frame. Note that the ATM cell boundaries are implicitly known when the PLCP frame is located, thus cell delineation is accomplished by locating the PLCP frame. When errors are detected in both octets in a single row, or when errors are detected in two consecutive path overhead identifier octets, the S/UNI-MACH48 declares an out-of-frame defect. The loss-of-frame defect is an integrated version of the out-of-frame defect state.
PO-P11: Path Overhead Identifier	Inserts the path overhead identifier codes in accordance with the PLCP frame alignment. See Table 48.	Identifies the PLCP path overhead bytes by monitoring the sequence of the POI bytes.
Z1-Z6: Growth:	These octets are unused and are programmed with all zeros.	These octets are ignored.
F1: User Channel	This octet is unused and the value inserted in this octet is controlled by an internal register.	This octet is ignored.
B1: Bit Interleaved Parity	This octet contains an 8-bit interleaved parity (BIP) calculated across the entire PLCP frame (excluding the A1, A, Pn octets and the trailer). The B1 value is calculated based on even parity and the value inserted in the current frame is the BIP result calculated for the previous frame.	The bit interleaved parity is calculated for the current frame and stored. The B1 octet contained in the subsequent frame is extracted and compared against the calculated value. Differences between the two values provide an indication of the end-to-end bit error rate. These differences are accumulated in a counter in the PLCP PMON block.
G1: Path Status	The first four bit positions provide a PLCP far end block error function and indicates the number of B1 errors detected at the near end. The FEBE field has nine legal values (0000b-1000b) indicating between zero and eight B1 errors. The fifth bit position is used to transmit PLCP yellow alarm. The last three bit positions provide the link status signal used in IEEE-802.6 DQDB implementations. Yellow alarm and link status signal insertion is controlled by the internal registers.	The G1 byte provides the PLCP FEBE function and is accumulated in an a counter in the PLCP PMON block. PLCP yellow alarm is detected or removed when the yellow bit is set to logic one or zero for ten consecutive frames. The yellow alarm state and the link status signal state are contained in the SPLR Status register.

Overhead Field	Transmit Operation	Receive Operation
M1, M2: Control Information	These octets carry the DQDB layer management information. Internal register controls the nominal value inserted in these octets. These octets are unused in ATM Forum T3 UNI 3.0 specification.	These octets are ignored.
C1: Cycle/Stuff Counter	The coding of this octet depends on the PLCP frame format. This octet indicates the number of stuff nibbles (13 or 14) at the end of each PLCP frame. The C1 value is varied in a three frame cycle where the first frame always contains 13 stuff nibbles, the second frame always contains 14 nibbles, and the third frame contains 13 or 14 nibbles. The stuffing may be varied by a nibble so that the PLCP frame rate can be locked to an external 8 kHz timing reference from REF8K, a loop-timed 8 kHz reference, or fixed stuffing via the FIXSTUFF bit in the SPLT Configuration Register. See Table 49.	Interprets the trailer length according to the selected PLCP frame format and the received C1 code.

Table 48 PLCP Path Overhead Identifier Codes

POI	POI Code (Hex)
P11	2C
P10	29
P9	25
P8	20
P7	1C
P6	19
P5	15
P4	10
P3	0D
P2	08
P1	04
P0	01

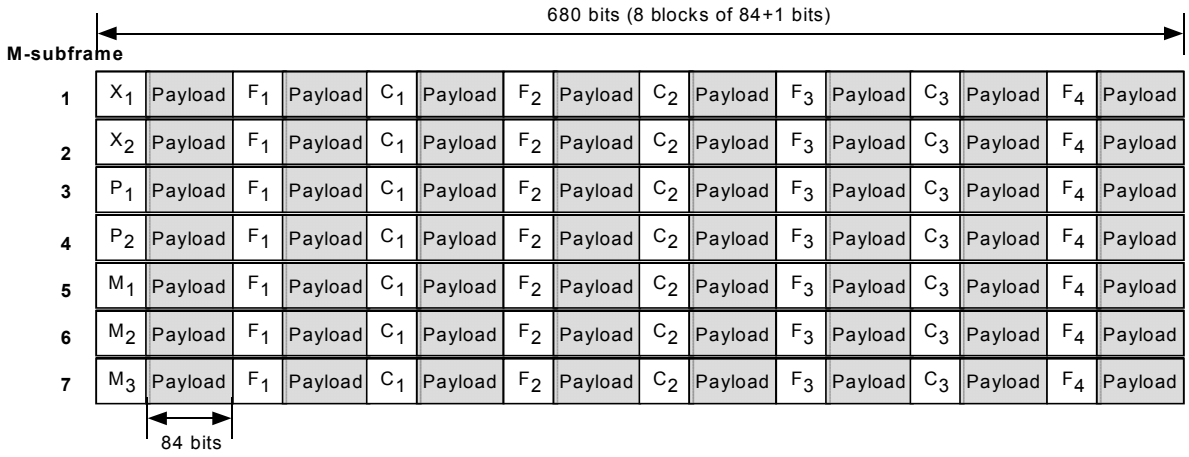
Table 49 DS3 PLCP Trailer Length

C1(Hex)	Frame/Trailer Length
FF	1 (13 Nibbles)
00	2 (14 Nibbles)
66	3 (13 Nibbles)
99	3 (14 Nibbles)

14.5 DS3 Frame Format

The S/UNI-MACH48 supports C-bit parity DS3 framing format which is mapped into or demapped from an STS-1 SPE as shown in Table 1. This format can be extended to support direct mapping of ATM cells, PLCP mapping of ATM cells, and direct mapping of HDLC. An overview of the DS3 frame format is shown in Figure 18.

Figure 18 DS3 Frame Structure



While in-frame, the DS3 receiver continuously checks for M-bit or F-bit framing bit errors, and P-bit parity errors. When C-bit parity mode is selected, both C-bit parity errors and far end block errors are accumulated.

When the C-bit parity framing format is detected, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. HDLC messages in the Path Maintenance Data Link are received by an internal data link receiver.

The DS3 transmitter allows for the insertion of the overhead bits into a DS3 bit stream. Status signals such as far end receive failure (FERF), the alarm indication signal (AIS) and the idle signal can be inserted when the transmission of these signals is enabled

The processing of the overhead bits in the DS3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH, TOHINS, TOHFP, TOHVAL, and TOHCHAN[5:0]. In the receive direction, most of the overhead bits our brought out serially on the ROH data stream.

Table 50 DS3 Frame Overhead Operation

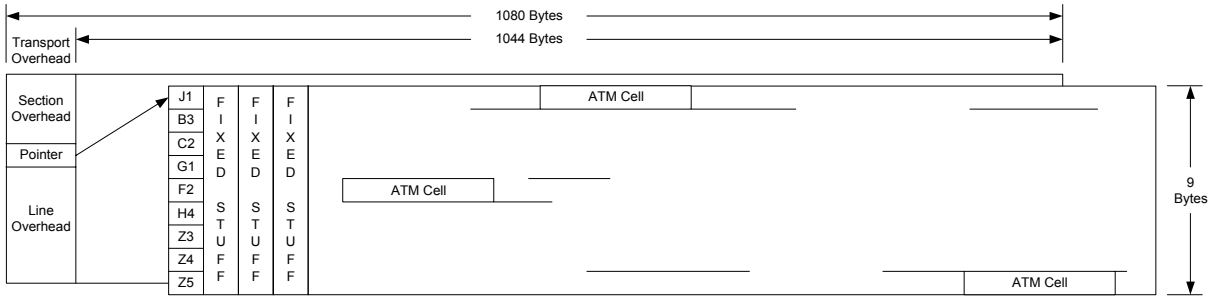
Control Bit	Transmit Operation	Receive Operation
Xx: X-Bit Channel	Inserts the FERF signal on the X-bits.	Monitors and detects changes in the state of the FERF signal on the X-bits.
Px: P-Bit Channel	Calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.	Calculates the parity for the received payload. Errors are accumulated in internal registers.
Mx: M-Frame Alignment Signal	Generates the M-frame alignment signal (M1=0, M2=1, M3=0).	Finds the M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Fx: M-subframe Alignment Signal	Generates the M-subframe signal (F1=1, F2=0, F3=0, F4=1).	Finds M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Cx: C-Bit Channels	C-bit Parity Operation: The C-bit Parity ID bit is forced to logic 1. The second C-bit in M-subframe 1 is set to logic 1. The third C-bit in M-subframe 1 provides a far-end alarm and control (FEAC) signal. The FEAC channel is sourced by the XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. The 3 C-bits in M-subframe 5 contain the 28.2 Kbit/s path maintenance datalink. The remaining C-bits are unused and set to logic 1.	C-bit Parity Operation: The FEAC channel on the third C-bit in M-subframe 1 is detected by the RBOC block. Path parity errors and FEBEs on the C-bits in M-subframes 3 and 4 are accumulated in counters. The path maintenance datalink signal is extracted by the receive HDLC controller.

14.6 SONET/SDH Frame Mappings

14.6.1 ATM Mapping

The S/UNI-MACH48 processes the ATM cell mapping for STS-1/STM-0, STS-3c/STM-1, STS-12c/STM-4c, and STS-48c/STM-16c. In Figure 19, the STS-12c/STM-4c mapping is shown. In this mapping, three stuff columns are included in the SPE. No other options are provided.

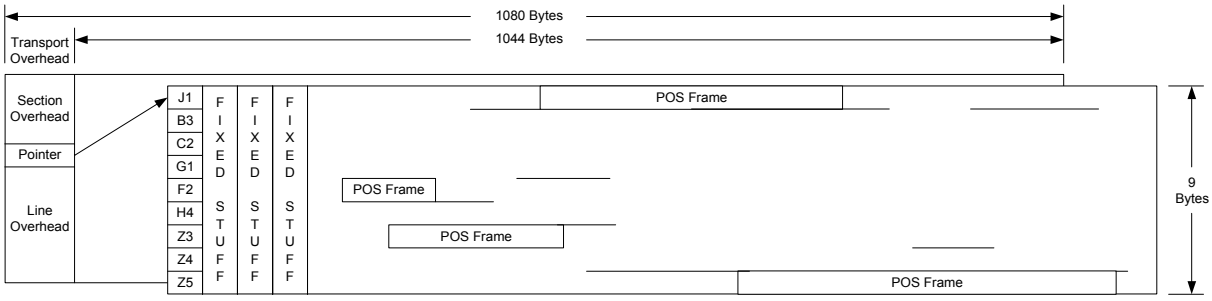
Figure 19 ATM Mapping into a STS-12c/STM-4c SPE



14.6.2 Packet over SONET Mapping

The S/UNI-MACH48 processes the Packet over SONET mapping for STS-1/STM-0, STS-3c/STM-1, STS-12c/STM-4c, and STS-48c/STM-16c. In Figure 20, the STS-12c/STM-4c mapping is shown. Three stuff columns are included in the SPE.

Figure 20 POS Mapping into a STS-12c/STM-4c SPE



14.6.3 Transport and Path Overhead Bytes Used by the S/UNI-MACH48

The S/UNI-MACH48 processes a subset of the complete transport overhead present in an SONET stream. The S/UNI-MACH48 uses but does not process the J0, J1, or G1 bytes. The H1 and H2 bytes are used when the RHPP is enabled and are set to the value 0 in the transmit direction.

Transport Overhead Bytes

J0: The J0 byte is currently defined as the STS-48/STM-16 section trace byte for SONET/SDH. Its location is communicated in the TelecomBus control signals.

H1, H2: When the RHPP is enabled, the H1 and H2 pointer values locate the path overhead column in the SONET/SDH frame.

In the transmit direction, the H1 and H2 pointer values reflect the setting of the LOCK0 bit in the TCAS12. In the receive direction, the RHPP uses the pointer to locate the J1 byte position(s). Path AIS is detected by the RHPP.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction when the RHPP is not used as stuff actions are inherently communicated in the TelecomBus control signals. When the RHPP is enabled, the H3 byte will contain payload during negative stuff events.

Path Overhead Bytes

J1: The Path Trace byte is used as an indication of the start position of an SPE. Its location is communicated in the TelecomBus control signals.

G1: The path status byte provides a path FEBE function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

In the transmit direction, the S/UNI-MACH48 provides register bits to control the path RDI (bit 5) and auxiliary path RDI (bit 6) states. For path FEBE, the number of B3 errors detected in the previous interval is inserted either automatically or using a register. This path FEBE code has 9 legal values, namely 0 to 8 errors.

In the receive direction, a legal path FEBE value is accumulated in the path FEBE event counter. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers.

14.7 ATM Cell Data Structure

ATM cells may be passed to/from the S/UNI-MACH48 using a 52 byte cell structure on a 32-bit UTOPIA level 3 compliant interface.

Figure 21 shows the default ATM cell format for the S/UNI-MACH48 at the UTOPIA Level 3 interface. It is the 13x32-bit word structure with no HCS or UDF bytes.

Bit 31 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first four header octets).

Figure 21 A 52 Byte ATM Data Structure

	Bit 31 Bit 16		Bit 15 Bit 0	
Word 1	H1	H2	H3	H4
Word 2	Payload 1	Payload 2	Payload 3	Payload 4
Word 3	Payload 5	Payload 6	Payload 7	Payload 8
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
Word 12	Payload 41	Payload 42	Payload 43	Payload 44
Word 13	Payload 45	Payload 46	Payload 47	Payload 48

14.8 POS/HDLC Data Structure

Packets may be passed to/from the S/UNI-MACH48 using a 32-bit POS-PHY Level 3 compliant interface.

The 32-bit POS-PHY Level 3 data structure is shown in Figure 22. The packet length of 63 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable. Octets are written in the same order they are to be transmitted or they were received on the SONET line. All words are composed of four octets, except the last word of a packet which can have one, two, three, or four octets. If the Transmit Packet Processor (TCFP or TTDP) is configured to not insert the FCS field, then these bytes should be included with the packet passed through the POS-PHY L3 interface. Similarly, if the Receive Packet Processor (RCFP or RTDP) is configured to not strip the FCS field, then these bytes will be included at the end of the packet.

Figure 22 A 63 Byte Packet Data Structure

	Bit 31	Bit 16	Bit 15	Bit 0
Word 1	Byte 1/SOP	Byte 2	Byte 3	Byte 4
Word 2	Byte 5	Byte 6	Byte 7	Byte 8
Word 3	Byte 9	Byte 10	Byte 11	Byte 12
. . .	. . .	. . .	. . .	. . .
Word 15	Byte 57	Byte 58	Byte 59	Byte 60
Word 16	Byte 61	Byte 62	Byte 63/EOP	Unused

Both the start of the packet and the end of the packet must be identified by the TSOP/RSOP and TEOP/REOP signals. When the first section of a packet is transferred over the interface, the TSOP/RSOP signals will be high for Byte 1 of the packet only. The TMOD[1:0] pins will indicate how many bytes of the final word are valid.

Bits 31 to 24 form the first transmitted byte and bit 31 can be configured to be the bit which is transmitted first. This is the desired set-up for byte-synchronous POS. Bit 24 can also be configured to be the first transmitted bit of this byte. This is the desired set-up for bit-synchronous HDLC.

14.8.1 Limitation When Using Externally Generated FCS in STS-48c Mode

When the S/UNI-MACH48 is set up in STS-48c POS mode (TX48C is logic 1) and FCS bytes are passed through the transmit POS-PHY L3 interface, the overall throughput is reduced. The maximum bandwidth throughput will be reduced by a maximum of 2 bytes per packet. The overall effect will depend on the length of the packets + FCS bytes being transferred through the POS-PHY L3 interface. If the packet + FCS length is evenly divisible by 4 bytes, no bandwidth is lost for that packet.

14.8.2 Limitations on Small Packets

The S/UNI-MACH48 cannot handle packet payloads (excluding FCS) which are smaller than 4 bytes.

In the receive direction, the RCFP and RTDP should be programmed such that the minimum packet size is at least 4 bytes + FCS. Packet payloads of size 3 bytes or less are tagged by the RCFP and RTDP packet processors and marked as minimum length violations. For configurations where the FCS is passed through the PL3 bus, the FCS byte count should be treated as payload bytes for these minimum packet size calculations.

In the transmit direction, the minimum packet payload size permitted is 4 bytes. The exception to this is when the packet is aborted by use of the TERR pin. Aborted packets can be less than the 4 byte minimum. The S/UNI-MACH48 will extend these packets to 4 bytes before tagging with the appropriate abort sequence.

14.9 Setting up Timeslot Assignments in the IWTI, IPTI, OWTI, and OPTI

The STSI blocks in the S/UNI-MACH48 (IWTI, IPTI, OWTI, and OPTI) can be used to rearrange system side and line side SONET/SDH timeslots. Each block buffers 48 timeslots and rearranges them as desired before outputting them. The STSI blocks allow user configuration of timeslot mappings, basic bypass of timeslots, and predefined mappings for standard TelecomBus interfaces.

14.9.1 Standard Line-Side Timeslot Map

The standard Line-side Timeslot Map at the S/UNI-MACH48 interface is shown in Table 51. The timeslots on the left side of Table 51 are presented on ID[x] or OD[x] (or RPWRK[x]/RNWRK[x], RPPROT[x]/RNPROT[x], TPWRK[x]/TNWRK[x], and TPPROT[x]/TNPROT[x] link if SER_EN = 1) before the timeslots on the right. The following discussion references ID[x][7:0] and OD[x][7:0], but can also apply to the serial TelecomBus links.

Payload bytes from the SONET/SDH stream are labeled by Sx,y. Within Sx,y, the STS-3/STM-1 number is given by ‘x’ and the column number within the STS-3/STM-1 is given by ‘y’. With such a mapping, an STS-12c/STM-4c data stream will be transferred across one complete ID[x][7:0] or OD[x][7:0] bus.

Table 51 Standard Line-Side Timeslot Map

	Line-Side Timeslots											
ID[1][7:0] OD[1][7:0]	S1,1	S2,1	S3,1	S4,1	S1,2	S2,2	S3,2	S4,2	S1,3	S2,3	S3,3	S4,3
ID[2][7:0] OD[2][7:0]	S5,1	S6,1	S7,1	S8,1	S5,2	S6,2	S7,2	S8,2	S5,3	S6,3	S7,3	S8,3
ID[3][7:0] OD[3][7:0]	S9,1	S10,1	S11,1	S12,1	S9,2	S10,2	S11,2	S12,2	S9,3	S10,3	S11,3	S12,3
ID[4][7:0] OD[4][7:0]	S13,1	S14,1	S15,1	S16,1	S13,2	S14,2	S15,2	S16,2	S13,3	S14,3	S15,3	S16,3

14.9.2 Required System-Side Timeslot Map for Sub-STS-48c/STM-16c Data Streams

The required system-side Timeslot Map inside the S/UNI-MACH48 interface is shown in Table 52 for sub-STS-48c/STM-16c data stream. The timeslots on the left side of Table 52 precede the timeslots on the right.

Payload bytes from the SONET/SDH stream are labeled by Sx,y. Within Sx,y, the STS-3/STM-1 number is given by ‘x’ and the column number within the STS-3/STM-1 is given by ‘y’.

With such a mapping, an STS-12c/STM-4c data stream will occupy one complete stream. STS-3c/STM-1 data streams within each STS-12/STM-4 data stream must be allocated to a set of Sx,1 and Sx,2 and Sx,3 timeslots shown in Table 52. STS-1/STM-0 data streams (and those containing mapped DS3s) can belong in any non-STS-12c/STM-4c or non-STS-3c/STM-1 timeslot.

Note that the timeslot assignment locations between Table 51 and Table 52 are identical. Thus, if no movement of any channels is required for sub-STS-48c/STM-16c mode (TX48C = 0 and RX48C = 0), the IPTI_MODE[1:0], IWTI_MODE[1:0], OPTI_MODE[1:0], and OWTI_MODE[1:0] bits in the S/UNI-MACH48 Miscellaneous register can be programmed to bypass mode (‘b01).

Table 52 Required System-Side Timeslot Map (TX48C = 0, RX48C = 0)

	System-Side Timeslots											
Stream 0	S1,1	S2,1	S3,1	S4,1	S1,2	S2,2	S3,2	S4,2	S1,3	S2,3	S3,3	S4,3
Stream 1	S5,1	S6,1	S7,1	S8,1	S5,2	S6,2	S7,2	S8,2	S5,3	S6,3	S7,3	S8,3
Stream 2	S9,1	S10,1	S11,1	S12,1	S9,2	S10,2	S11,2	S12,2	S9,3	S10,3	S11,3	S12,3
Stream 3	S13,1	S14,1	S15,1	S16,1	S13,2	S14,2	S15,2	S16,2	S13,3	S14,3	S15,3	S16,3

14.9.3 Required System-Side Timeslot Map for STS-48c/STM-16c Data Streams

The required system-side Timeslot Map inside the S/UNI-MACH48 interface is shown in Table 53 for an STS-48c/STM-16c data stream. The timeslots on the left side of Table 53 precede the timeslots on the right.

Payload bytes from the SONET/SDH stream are labeled by Sx,y. Within Sx,y, the STS-3/STM-1 number is given by ‘x’ and the column number within the STS-3/STM-1 is given by ‘y’. This gives a common reference to the line-side timeslot map given by Table 51.

Streams 0 to 3 now no longer represent separate STS-12/STM-4 data streams. Instead, they combine to form a single stream which is 4 times as wide as the STS-12/STM-4 streams shown in Table 52.

Mapping from the standard line-side timeslot mapping shown in Table 51 to the STS-48c/STM-16c system-side timeslot mapping shown in Table 53 can be done by setting the IPTI_MODE[1:0] and IWTI_MODE[1:0] bits to ‘b10 and the OPTI_MODE[1:0] and OWTI_MODE[1:0] bits to ‘b11in the S/UNI-MACH48 Miscellaneous register.

Table 53 Required System-Side Timeslot Map (TX48C = 1, RX48C = 1)

	System-Side Timeslots											
Stream 0	S1,1	S5,1	S9,1	S13,1	S1,2	S5,2	S9,2	S13,2	S1,3	S5,3	S9,3	S13,3
Stream 1	S2,1	S6,1	S10,1	S14,1	S2,2	S6,2	S10,2	S14,2	S2,3	S6,3	S10,3	S14,3
Stream 2	S3,1	S7,1	S11,1	S15,1	S3,2	S7,2	S11,2	S15,2	S3,3	S7,3	S11,3	S15,3
Stream 3	S4,1	S8,1	S12,1	S16,1	S4,2	S8,2	S12,2	S16,2	S4,3	S8,3	S12,3	S16,3

14.9.4 Custom Timeslot Mappings and Movement of Timeslots Associated With a Channel

If the IPTI_MODE[1:0], IWTI_MODE[1:0], OPTI_MODE[1:0], or OWTI_MODE[1:0] bits are set to ‘b00, then the corresponding STSI block will be set for customer timeslot mapping. This permits the user to swap the position of STS-1/STM-0, STS-3c/STM-1, and STS-12c/STM-4c channels or interface with non-standard line-side timeslot maps.

The channels must still fit into the required system-side timeslot map in a manner which is required by a channel of such a rate. For example, an STS-3c channel which occupied line-side timeslots S1,1 and S1,2 and S1,3 in Table 51 can be moved to system-side timeslots S7,1 and S7,2 and S7,3 in Table 52. The analogous mapping can be done from the system-side timeslots to the line-side timeslots.

The following procedure shows how the IWTI block can be programmed perform such a remapping of timeslots. Page 0 of the IWTI block is configured in the example.

1. Set IWTI_MODE[1:0] equal to ‘b00.

2. For the IWTI, the base address STSI_BASE is 1800H.

3. Read BUSY in the STSI Indirect Address register at STSI_BASE + 00H. If it is logic 0, proceed to step 4. Otherwise, poll BUSY until it is logic 0.

4. Write 0010H to the STSI Indirect Data register at STSI_BASE + 01H to set TSIN[3:0] to 1 and DINSEL[1:0] to 0. This selects the ID[1][7:0] and line-side timeslot S1,1 as the input bus and timeslot respectively.

5. Write 0031H to the STSI Indirect Address register at STSI_BASE + 00H to set TSOUT[3:0] to 3 and DOUTSEL[1:0] to 1. This selects the position S7,1 on the output stream and system-side timeslot in the page 0 mapping of the IWTI.

6. Read BUSY in the STSI Indirect Address register at STSI_BASE + 00H. If it is logic 0, proceed to step 7. Otherwise, poll BUSY until it is logic 0.

7. Write 0050H to the STSI Indirect Data register at STSI_BASE + 01H to set TSIN[3:0] to 5 and DINSEL[1:0] to 0. This selects the ID[1][7:0] and line-side timeslot S1,2 as the input bus and timeslot respectively.

8. Write 0071H to the STSI Indirect Address register at STSI_BASE + 00H to set TSOUT[3:0] to 7 and DOUTSEL[1:0] to 1. This selects the position S7,2 on the output stream and system-side timeslot in the page 0 mapping of the IWTI.

9. Read BUSY in the STSI Indirect Address register at STSI_BASE + 00H. If it is logic 0, proceed to step 10. Otherwise, poll BUSY until it is logic 0.

10. Write 0090H to the STSI Indirect Data register at STSI_BASE + 01H to set TSIN[3:0] to 9 and DINSEL[1:0] to 0. This selects the ID[1][7:0] and line-side timeslot S1,3 as the input bus and timeslot respectively.

11. Write 00B1H to the STSI Indirect Address register at STSI_BASE + 00H to set TSOUT[3:0] to BH and DOUTSEL[1:0] to 1. This selects the position S7,3 on the output stream and system-side timeslot in the page 0 mapping of the IWTI.

12. Go back to step 1 if you want to configure more timeslot mappings.

14.9.5 Active and Standby Pages in the STSI Blocks

The STSI blocks contain 2 pages of configurations: an active page, and an inactive page. Selection of the page in use in the IWTI and IPTI is done by the ICMP input signal. Selection of the page in use in the OWTI and OPTI is done by the OCMP input signal.

The existence of an active page and an inactive page allows the user to set-up an alternate timeslot mapping on multiple devices or multiple STSI blocks before performing a global switch to the new mapping. The swapping of the page in use is done at transport frame boundaries. The ICMP and OCMP are sampled at the J0 locations defined by RJ0FP and OJ0REF are logic 1 respectively.

14.10 Using RWSEL and SER_PRT_SEL

The RWSEL and SER_PRT_SEL signals are used to select how the working and protection incoming serial TelecomBus signals (RPWRK[4:1]/RNWRK[4:1] and RPPROT[4:1]/RNPROT[4:1]) are inserted into the data stream going to the S/UNI-MACH48 core. These functions are only valid when the serial TelecomBus interface is selected (SER_EN input signal is logic 1).

The RWSEL input pin is used to perform a global switch between the working and protection data streams. It is only active when the RWSEL_EN register bit in the S/UNI-MACH48 Configuration and Diagnostic register is set to logic 1. When RWSEL is logic 1, the working data stream is selected to be routed to the core of the S/UNI-MACH48 device. The protection data streams will only go as far as their corresponding PRGM blocks so that PRBS pattern detection can be used to verify the link integrity. When RWSEL is logic 0, the protection data streams will be routed to the core of the S/UNI-MACH48 device. The working data streams will only go as far as their corresponding PRGM blocks so that the link integrity can be verified.

The RWSEL is sampled and the switch between the working and protection links occurs at transport frame boundaries as shown in Section 15.5.

The SER_PRT_SEL register bits in the IWTI Indirect Data Register is used when RWSEL_EN is set to logic 0 and when not working in STS-48c mode.

SER_PRT_SEL allows selection of data from the working and protection serial TelecomBus links on a per-STS-1 timeslot granularity to be routed to the S/UNI-MACH48 core. When SER_PRT_SEL is logic 1, the system-side timeslot (see Table 52 and Table 53) associated with the TSOUT[3:0] and DOUTSEL[1:0] bits in the IWTI Indirect Address register will come from a protection link (RPPROT[x]/RNPROT[x]) via the IPTI block. When SER_PRT_SEL is logic 0, the associated system-side timeslot will come from a working link (RPWRK[x]/RNWRK[x]) via the IWTI block.

SER_PRT_SEL changes take place immediately. It does not wait for transport frame boundaries.

14.11 Setting up Channels for Different Link Rates

The S/UNI-MACH48 can process ATM, POS, and HDLC traffic for DS3, STS-1/STM-0, STS-3c/STM-1, STS-12c/STM-4c, and STS-48c/STM-16c traffic rates. To take advantage of all the automated features in the S/UNI-MACH48, the system side timeslots should be configured symmetrically between the transmit and receive paths. If required, the STSI blocks, IWTI, IPTI, OWTI, and OPTI can be used to rearrange line side timeslots to appropriate system side timeslots on an STS-1/STM-0 basis.

System side timeslots and system side channel numbers are integrally linked. The timeslots referred to are those on the system side of the IWTI, IPTI, OWTI, and OPTI blocks and are those which are directly processed by the RCAS12, TCAS12, TCFP, RCFP, RTDP, TTDP, SIRP, PRGM, and all the DS3 blocks.

Timeslot locations are illustrated in Table 52 and Table 53. Refer to Sections 12.5 and 12.6 for information on how RCAS-12 and TCAS-12 timeslots are linked to those shown in Table 52 and Table 53.

- STS-48c/STM-16c traffic occupies all the line side timeslots, system-side timeslots, and channel number 0 on the system side.

- STS-12c/STM-4c traffic occupies 12 line-side timeslots and 12 system-side timeslots which are part of the same TelecomBus set. A set starts at timeslots S1,1, S5,1, S9,1 or S13,1 as shown in Table 52 and Table 53. Valid sets are labeled in Table 7 and Table 9. The set starting at system-side timeslot S1,1 must be allocated to channel number 0. Likewise, the set starting at system-side timeslot S5,1 must be allocated to channel number 12. The set starting at system-side timeslot S9,1 must be allocated to channel number 24 and the set starting at system-side timeslot S13,1 must be allocated to channel number 36.

- STS-3c/STM-1 traffic occupies 3 line-side timeslots and 3 system-side timeslots which are spaced 4 apart as shown in Table 51 and Table 52. Valid sets are labeled in Table 7 and Table 9. The set residing in the same stream as system-side timeslot S1,1 must be allocated to a channel number between 0 and 11. Likewise, a set residing in the same stream as system-side timeslot S5,1 must be allocated to a channel number between 12 and 23. A set residing in the same steam as system-side timeslot S9,1 must be allocated to a channel number between 24 and 35 and a set residing in the same stream as system-side timeslot S13,1 must be allocated to a channel number between 36 and 47.

- STS-1/STM-0 and DS3 traffic can reside at any line or system timeslot not occupied by a concatenated payload. The STS-1/STM-0/DS3 may be allocated to one of 12 available channel numbers. For example, an STS-1/STM-0/DS3 set residing in the same stream as system-side timeslot S1,1 must be allocated to a channel number between 0 and 11. Likewise, a set residing in the same stream as system-side timeslot S5,1 must be allocated to a channel number between 12 and 23. A set residing in the same steam as system-side timeslot S9,1 must be allocated to a channel number between 24 and 35 and a set residing in the same stream as system-side timeslot S13,1 must be allocated to a channel number between 36 and 47.

14.11.1 Example Set-up:

The following is an example configuration for an STS-3c/STM-1 bidirectional channel residing at line-side timeslots S4,1, S4,2, and S4,3 and system-side timeslots S4,1, S4,2, and S4,3 and channel/PHY address 3.

1. Set RS4_1[1:0], RS4_2[1:0], and RS4_3[1:0] register bits in the S/UNI-MACH48 Receive Timeslot Configuration registers (0002H – 0007H) to ‘b01 for STS-3c.

2. Set TS4_1[1:0], TS4_2[1:0], and TS4_3[1:0] register bits in the S/UNI-MACH48 Transmit Timeslot Configuration registers (0008H – 000DH) to ‘b01 for STS-3c.

3. Set up the RXSDQ and TXSDQ as follows for PHYID = 3:
    - Assuming timeslots S1,1, S2,1, and S3,1 consist of STS-1 data streams with FIFO sizes of 16 Blocks, BLOCK_PTR[4:0] for the channel in question can be calculated to be 06H, FIFO_NUMBER[5:0] is set to 3, and FIFO_BS[1:0] is set to 0x2 (see Section 14.13).
    - Set POS_SEL to logic 1 for POS/HDLC traffic or 0 for ATM traffic.
    - Set TXSDQ BT[4:0] and DT[7:0] to 0x3 for an ATM channel. Otherwise set them according to the constraints described in Sections 14.15 and 14.16.
    - Set RXSDQ DT[7:0] to 0x3 for an ATM channel. Otherwise set them according to the constraints described in Section 14.16.

4. Configure the RXPHY as follows:
    - If using the POS-PHY L3 interface, set the CALENDAR_LENGTH[6:0] value to 2FH to allow 48 calendar entries.
    - If using the POS-PHY L3 interface, for CALENDAR_ADDR[6:0] values of 03H, 13H, and 23H, set CALENDAR_DATA[5:0] equal to 03H. This allows the S/UNI-MACH48 polling mechanisms to poll channel number 3 three times out of 48. The sequence is spread out evenly amongst the 48 calendar sequences.
    - Set ODDPARITY to configure the parity to be generated.
    - Set BURST_SIZE[3:0] for PHY_ADDR[5:0] = 0x3 (see Section 14.16). If an ATM PHY, set BURST_SIZE[3:0] to the value 0x3.

5. Configure the TXPHY as follows:

- Set ODDPARITY to configure the parity to be generated.
- Set PARERREN to select if parity errors are to cause packets to be aborted.

6. Configure the RTDP at RTDP_BASE = 00F0H as follows for CHAN[3:0] = 3:
   - Set the POS_SEL to 1 if processing POS. Set to logic 0 for ATM.
   - Set CRC_SEL[1:0] for desired CRC type.
7. Configure the TTDP at TTDP_BASE = 0170H as follows for CHAN[3:0] = 3:
   - Set the POS_SEL to 1 if processing POS. Set to logic 0 for ATM.
   - Set CRC_SEL[1:0] for desired CRC type.
8. Configure the RCAS12 at RCAS12_BASE = 01B0H for Timeslots ***x*** = 3, 7, and 11 as follows:
   - Set TS***x***_CHAN[3:0] = 3.
   - Set TSx_MODE[2:0] = ‘b001.
   - Set TS***x***_PROV = 1.
9. Configure the TCAS12 at TCAS12_BASE = 01F0H for Timeslots ***x*** = 3, 7, and 11 as follows:
   - Set TS***x***_CHAN[3:0] = 3.
   - Set TSx_MODE[2:0] = ‘b001.
   - Set TS***x***_PROV = 1.
10. Configure the SIRP at SIRP_BASE = 14C0H for Timeslots ***x*** = 3 as follows:
    - Set PROV = 1.
    - Set TS3_RMODE[1:0], TS3_RDI20F, and TS3_ERDI to the desired alarm reporting mode.
    - Set the RDIPRIHI[1:0] and RDIPRIMID[1:0] and LCD[1:0] bits for the desired alarm reporting mode.
11. Set SDQRST = 0 in RXSDQ and TXSDQ.
12. Set ENABLE = 1 in RXSDQ and TXSDQ for PHY_ID = 3. Ensure all other information for the indirect write to PHY_ID = 3 is unchanged from the previous SDQ configs.
13. Set RTDP (at RTDP_BASE = 01B0H, channel number 3) PROV = 1.
14. Set TTDP (at TTDP_BASE = 01F0H, channel number 3) PROV = 1.
15. Set TCAS12 (at TCAS_BASE = 01F0H) CH3_DIS = 0.
16. Set TXPHY TXPRST = 0.
17. Set RXPHY RXPRST = 0.

18. Set RCAS12 (at RCAS12_BASE = 01B0H) CH3_DIS = 0.

14.12 Dynamically Reprovisioning Channels to Different Rates

The S/UNI-MACH48 allows dynamic modification of channel rates without affecting other channels. For instance, a single STS-3c/STM-1 channel can be broken up into 3 separate STS-1/STM-0 channels. The following are the steps required:

1. Find the system side timeslots associated with the channel to be modified.

2. If the dynamic modification involves a data-rate of STS-3c or below, disable any independent software process that might update counters in the S/UNI-MACH48.

3. In the RCAS12 and TCAS12 blocks, set CH***x***_DIS to logic 1 for the affected channels.

4. In the RCAS12, TCAS12, and SIRP blocks, set TS***x***_PROV to logic 0 for the affected system timeslots.

5. Reconfigure the affected RS***x_y***[1:0] register bits in the S/UNI-MACH48 Receive Timeslot Configuration registers (0002H – 0007H).

6. Reconfigure the affected TS***x_y***[1:0] register bits in the S/UNI-MACH48 Transmit Timeslot Configuration registers (0008H – 000DH).

7. Reset the PROV bits in the affected channels in the TCFP, TTDP, RCFP, and RTDP blocks.

8. Reconfigure the RXSDQ and TXSDQ as described in Section 14.14. Use the FLUSH bit for the affected FIFO_PTR addresses to clear the FIFOs. Make sure EMPTY = 1 for each affected FIFO_PTR then write 0 to FLUSH for each affected FIFO_PTR.

9. Reconfigure the RXPHY's calendar to match the new channel rates. See Section 14.17.

10. Reconfigure the RCAS12, TCAS12, and SIRP blocks so the timeslots involved in the modified channel correspond to the proper channel rate using the TS***x***_MODE and TS***x***_CHAN bits. Set the TS***x***_PROV bits for these timeslots. Leave the CH***x***_DIS bits asserted for the new channel(s).

11. Reconfigure the TCFP, TTDP, RCFP, and RTDP for the new channel. Set the PROV bits for the new channel(s).

12. Clear the CH***x***_DIS bits associated with the new channel(s) to enable the new channel(s).

13. Re-enable any suspended software processes that update counters in the S/UNI-MACH48.

14.13 RXSDQ and TXSDQ FIFO Size Configuration

The SDQ supports 3 different FIFO sizes – 16 Blocks (equal to 4 ATM Cells or 256 bytes), 48 Blocks (equal to 12 ATM Cells or 768 bytes), and 192 Blocks (equal to 48 ATM Cells or 3072 bytes). Table 54 shows the recommended FIFO sizes for different data rates.

Table 54 Suggested FIFO Buffer Sizes

FIFO_BS[1:0]	FIFO Size (Blocks)	FIFO Size (Cells)	Suggested BW
00	Reserved	Reserved	Reserved
01	16	4	DS3/STS-1
10	48	12	STS-3c
11	192	48	STS-12c/48c

There are 768 Blocks (192 ATM Cells or 12288 bytes) of total storage that can be carved up into a maximum of 48 FIFOs of the sizes mentioned above. The storage is organized in 4 banks of 192 Blocks each. Block numbers 0 to 191 (000H to 0BFH) are in Bank 0, 192 to 383 (0C0H to 17FH) are in Bank 1, 384 to 575 (180H to 23FH) are in Bank 2, and 576 to 767 (240H to 2FFH) are in Bank 3.

In order to configure the SDQ, the user must first determine the size of each FIFO in Blocks, and sum them. The total number of Blocks must be less than 768. The minimum FIFO size is 16 Blocks or 4 Cells. An additional restriction in the SDQ is that each of the four Banks of the SDQ cannot contain more than 12 FIFOs of any size. Thus, if a user has configured 12 FIFOs of 8 Blocks each in Bank 0, then although only 96 of the possible 192 Blocks are used, no more can be configured in this Bank.

The user then needs to program three things for a given FIFO PHYID (channel) –

The physical FIFO Number – the user can set up the FIFO in any one of the four available Banks. The value of the FIFO_NUMBER[5:0] register bits (as specified in the FIFO Indirect Configuration Register) must be set to correspond to the channel number (or equivalently, the PHY number) as shown in Table 55.

Table 55 SDQ FIFO_NUMBER Configuration

Bank	UL3/PL3 Channel #	FIFO_NUMBER[5:0]
0	0 to 11	0 to 11 (0x00 to 0x0B)
1	12 to 23	16 to 27 (0x10 to 0x1B)
2	24 to 35	32 to 43 (0x20 to 0x2B)
3	36 to 47	48 to 59 (0x30 to 0x3B)

Note that the FIFO_NUMBER value must be set to correspond explicitly to the UL3/PL3 Channel #. For instance, for UL3/PL3 Channel #11, the FIFO_NUMBER must be set to the value 11 (0x0B). For UL3/PL3 Channel #36, FIFO_NUMBER must be set to the value 48 (0x30). For UL3/PL3 Channel #25, FIFO_NUMBER must be set to the value 33 (0x21), and so on for all the other UL3/PL3 Channel numbers.

The Block Pointer – this is calculated using the starting Block number, which should be an integral multiple of the FIFO size. Since there are 192 Blocks in a Bank, the starting Block number is actually an 8 bit number. However, since the smallest FIFO is a multiple of 8 Blocks, only the upper 5 are significant – these 5 bits are called the Block Pointer. The Block Pointer is specified in the FIFO Indirect Configuration register in the BLOCK_PTR[4:0] field.

The FIFO Size – this is a 2 bit number that specifies one of 3 possible sizes for the FIFO. Refer to Table 54 for the values used to specify the FIFO sizes, and a guide to sizing the FIFO based on the bandwidth of the associated PHY. It is up to the discretion of the user to apply this guide to each specific case. This number is specified in the FIFO Indirect Configuration register in the FIFO_BS[1:0] field.

A FIFO occupies the number of Blocks specified by it's size starting at the Block Pointer. The user must not configure the Block pointers such that two FIFOs overlap. The user can, however, have gaps between consecutive Blocks, which can potentially be filled by expanding one or the other Block. However, since only 3 FIFO sizes are valid, the user cannot arbitrarily expand a FIFO. Care must be taken to ensure that when expanding from one size to the next, the FIFOs do not overlap. Refer to Section 14.14 for a guide to expanding and contracting configured Blocks in the SDQ.

The following table illustrates the configuration for a typical case. This case involves 3 PHYs that have a bandwidth of STS-12, and are allocated 192 Block FIFOs each. There is one STS-3c PHY configured, using a 48 Block FIFO, 6 STS-1 FIFOs each with a 16 Block FIFO, and 3 DS3 PHYs, each with 16 Block FIFOs. Bank 0, Bank 1 and Bank 3 have one FIFO each, while Bank 2 has 10 FIFOs. The sum of all the Blocks used in this example is 768 which is the maximum number of Blocks available. The rest of the configuration is according to the table.

Table 56 SDQ Configuration Example

UL3/PL3 Channel #	PHYID [5:0]	BW	Size (Blocks/ Cells)	FIFO_BS [1:0]	Bank	FIFO_ NUMBER [5:0]	Starting Block	BLOCK_ PTR[4:0]
0	0x00	STS-12c	192/48	'b11	0	0x00	0x0	0x0
12	0x0C	STS-12c	192/48	'b11	1	0x10	0x0	0x0
24	0x18	STS-3	48/12	'b10	2	0x20	0x0	0x0
25	0x19	STS-1	16/4	'b01	2	0x21	0x30	0x6
26	0x1A	STS-1	16/4	'b01	2	0x22	0x40	0x8
27	0x1B	STS-1	16/4	'b01	2	0x23	0x50	0xA
28	0x1C	STS-1	16/4	'b01	2	0x24	0x60	0xC
29	0x1D	STS-1	16/4	'b01	2	0x25	0x70	0xE
30	0x1E	STS-1	16/4	'b01	2	0x26	0x80	0x10
31	0x1F	DS3	16/4	'b01	2	0x27	0x90	0x12
32	0x20	DS3	16/4	'b01	2	0x28	0xA0	0x14
33	0x21	DS3	16/4	'b01	2	0x29	0xB0	0x16
36	0x24	STS-3c	16/4	'b01	3	0x30	0x0	0x0

UL3/PL3 Channel #	PHYID [5:0]	BW	Size (Blocks/ Cells)	FIFO_BS [1:0]	Bank	FIFO_ NUMBER [5:0]	Starting Block	BLOCK_ PTR[4:0]
37	0x25	STS-3c	16/4	‘b01	3	0x31	0x10	0x2
38	0x26	STS-3c	16/4	‘b01	3	0x32	0x20	0x4
39	0x27	STS-3c	16/4	‘b01	3	0x33	0x30	0x6

Note that this configuration leaves some spare capacity in Bank 3. Each bank has the capacity to handle 12 FIFOs of 16 blocks each. In the example, only 16 FIFOs have been assigned and they take up a sum of 640 blocks. This is because four STS-3c FIFOs have been configured to hold only 16 blocks each instead of 48. Because of the way their BLOCK_PTR[4:0] have been set the FIFO corresponding to Channel #39 can expand it’s FIFO sizes to be 48 blocks without affecting other FIFOs. However, channels 36-38 cannot expand without moving the other channels to make room for the larger FIFO. See Section 14.14 for details on SDQ dynamic reconfiguration.

When configuring/modifying SDQ for a PHY ID, the FIFO# should be set accordingly. Different PHY IDs cannot have the same FIFO# otherwise, the configuration of the other PHY will be overwritten.

The SDQ cannot detect errors due to user misconfiguration. If the user sets up FIFOs that overlap each other, or do not start at a Block number that is an integral multiple of the size of the FIFO, the results will be unpredictable.

14.14 RXSDQ and TXSDQ Dynamic Reconfiguration

Each PHY connected to a FIFO can have a depth of 16, 48 or 192 Blocks. The SDQ allows the reconfiguration of these PHY to different sizes (for example: the aggregation of four adjacent 12 Block FIFOs into one 48 Block FIFO) without dropping any cells or packets in FIFOs belonging to other PHYs. In order to perform a reconfiguration, the FIFOs being reconfigured should first be disabled (ENABLE = 0) using the FIFO Indirect Configuration register. When disabled, the FIFO will cease to accept any new data, but will continue to drain all existing blocks to the read interface. The user should manually empty the FIFO (by writing a 1 to the FLUSH bit in the FIFO Indirect Address register). Once all the FIFOs that need to be reconfigured are empty, the user must manually clear the FLUSH bit, then write the new configuration by recalculating the FIFO_NUMBER[5:0] and BLOCK_PTR[4:0] bits, changing the FIFO_BS[1:0] bits, and finally in a separate indirect write, setting the appropriate ENABLE bit. This procedure ensures that the FIFOs not being reconfigured are not affected in any way, and allows the ones being reconfigured to not drop any pre-existing data.

As indicated, the user can only aggregate adjacent FIFOs. However, any individual FIFO can be expanded as long as there is no overlap between FIFOs due to this expansion. The user can reduce a FIFO’s size at any time as this will not cause an overlap.

Care should be taken to insure that the ENABLE bit is not set until all other configuration changes have already been written into the FIFO by applying the following procedure:

1. Set indirect data values with ENABLE = 0

2. Write desired indirect address with FLUSH = 1
3. Wait until EMPTY is polled as 1
4. Set indirect data values
5. Write indirect address with FLUSH = 0
6. When ready, set indirect data values with ENABLE = 1
7. Write desired indirect address

For step 4, the user must read all indirect data values for the desired PHY and write them back modifying only the ENABLE bit by setting it to logic 1. Note that this procedure of reading all indirect data values and writing all indirect data values for each indirect write performed is required to maintain the desired configuration for the SDQ FIFOs.

14.15 TXSDQ Buffer Available Operation

For each of the FIFOs configured in the TXSDQ, a Buffer Available (BA[p]) bit indicates whether or not the FIFO p can accept more data. The BA[p] status is given (BA[p] = 1) when the TXSDQ can accommodate at least another injection of BT[4:0] + 1 blocks into its FIFO p. When the number of blocks available in FIFO p is less than (BT[4:0] + 1), then BA[p] is deasserted (BA[p] = 0). At this point, no more new data can be accepted, but the current transaction completes (if BT[p] is not set at the maximum for FIFO p). Eventually, when some of the data in FIFO p is drained by the read interface, the available FIFO space will equal or exceed BT[4:0] + 1. BA[p] is asserted when this condition is reached. The BA[p] state is reflected by the TCA and STPA and PTPA output signals on the Utopia L3 and POS-PHY L3 interfaces when PHY p is selected and/or polled.

In setting the TXSDQ buffer available threshold BT[4:0], the maximum data burst size from the upstream device must be taken into account. Section 15.8.2 describes how to program BT[4:0] to keep the upstream device from overflowing the TXSDQ FIFO. In general, the following formula applies:

(BT[4:0] + 1) ≥ max burst size from upstream device + system application margin

The values of BT[4:0] and DT[7:0] in the TXSDQ Indirect Data and Buffer Available Thresholds register must be set so that:

(DT[7:0] + 1) + (BT[4:0] + 1) ≤ FIFO size

The FIFO size is set using the FIFO_BS[1:0] register bits in the TXSDQ FIFO Indirect Configuration register and DT[7:0] is the TXSDQ is set in the TXSDQ Indirect Data and Buffer Available Thresholds register. This constraint keeps the FIFO from entering a state where the TXSDQ cannot sustain a new burst from the upstream device and the downstream TCFP or TTDP block does not have enough data to initiate a transfer.

For ATM FIFOs, BT[4:0] and DT[7:0] must be set equal to the value 3. This sets the threshold to be 4 blocks which is the space occupied by an ATM cell. The upstream device should also set its maximum burst size to be equal to one ATM cell. Note that for ATM FIFO's with a POS-PHY bus, if the TPAHOLD bit = 1, BT[4:0] should be set to 7 as described in Section 15.8.2.

The TXSDQ and RXSDQ FIFOs are divided up into blocks of 16 bytes each which is the smallest granularity of the FIFO. Note two packets cannot occupy the same FIFO Block. A 17 byte packet will occupy two full blocks, though the second block will be mostly empty, and wasted space. This needs to be considered when attempting to predict the available space in the buffer, and this is the reason why bandwidth tends to be lower for packet sizes that are slightly larger than an integral number of bytes.

14.16 RXSDQ and TXSDQ Data Available and Burst-Size Operation

In the RXSDQ and TXSDQ blocks, each FIFO indicates whether or not data is available for reading by asserting the Data Available line (DA[p] for FIFO p). The DA[p] line is asserted by the RXSDQ or TXSDQ under two conditions:

- If the queue depth of FIFO p is greater than a user configured Data Available Threshold (DT[p]), i.e. if there is more data than specified by the threshold.
- If at least one EOP is stored in the FIFO, i.e. the tail end of at least one packet is available in the threshold.

The DA[p] line gets de-asserted when the data in the FIFO falls below the threshold and there are no EOPs in the FIFO. For the RXSDQ, the DA[p] state is reflected by the RCA output signal on the Utopia L3 interface. When using the POS-PHY L3 interface, the RXPHY polls the DA[p] signals using its Calendar Sequence to determine if there is any data in the PHY to output.

For the RXSDQ, the BURST_SIZE[3:0] setting in the RXPHY Indirect Burst Size register is closely tied to the DT[7:0] setting in the RXSDQ FIFO Indirect Data Available Threshold register. BURST_SIZE[3:0] must be set to a value less than or equal to (DT[7:0]). This will prevent the RXPHY from initiating a burst until there is sufficient data in the RXSDQ.

For transfer of ATM cells, the BURST_SIZE[3:0] and DT[7:0] must both be set to the value 3. This makes the threshold equal to 4 blocks which will contain one ATM cell.

It is also important to note that larger burst sizes may cause the FIFOs in the RXSDQ to reach higher fill levels because more time is needed per PHY to complete a burst. Also, since a burst is terminated when an EOP signal is detected, small packets will cause their associated PHY to be penalized in net throughput across the POS-PHY L3 interface. To maximize fairness, it is recommended to keep the burst size fairly small – on the order of 4 blocks (BURST_SIZE[3:0] = 0x3).

In the TXSDQ, once the DA[p] signal indicates that enough data is in the TXSDQ to begin a cell or packet transfer, the downstream TTDP or TCFP blocks will begin pulling data from the corresponding FIFO. It will continue pulling regardless of the DA[p] state until the cell or packet is complete. At this time, it will start the next cell or packet transfer from the TXSDQ only after the DA[p] signal is again asserted.

The value of DT[7:0] in the TXSDQ Indirect Data and Buffer Available Thresholds register must be set so that:

(DT[7:0] + 1) + (BT[4:0] + 1) ≤ FIFO size

The FIFO size is set using the FIFO_BS[1:0] register bits in the TXSDQ FIFO Indirect Configuration register and BT[4:0] is set in the TXSDQ FIFO Indirect Data and Buffer Available Thresholds register. This constraint keeps the FIFO from entering a state where the TXSDQ cannot sustain a new burst from the upstream device and the downstream TCFP or TTDP block does not have enough data to initiate a transfer.

For packet data streams, it is recommended that DT[7:0] be set to a value close to half or 2/3 of the size of the FIFO. For ATM cell streams, DT[7:0] must be set to the value 0x3.

14.17 RXPHY POS-PHY L3 Servicing

In POS-PHY Level 3, the RXPHY controls the flow of data across the interface to the Link Layer device and additionally decides which PHY channel has the privilege to use the bus. The block will read the channel calendar registers and select a FIFO p that has Data Available (DA[p]) signals asserted. The method of selection is programmed by the user. Servicing is proportional to the number of occurrences a PHY number is entered in the calendar register (see RXPHY Calendar Indirect Address Data register). Once a PHY channel is selected, the POS block controls the RSX signal and passes REOP, RSOP and RVAL signals from the RXSDQ to the POS-PHY L3 interface. Additionally, it accepts RENB from the Link Layer device and passes it on to the RXSDQ block. The control of transfer size and pause between transfers is accomplished with the use of an internal version of the RENB signal and the BURST_SIZE and RSXPAUSE registers. The burst size is programmable on a per PHY basis.

14.17.1 RXPHY POS-PHY L3 Servicing Algorithm

The calendar servicing algorithm makes choices for service according to the user programmable calendar entered in the RXPHY Calendar Indirect Address Data register.

Table 57 RXPHY Calendar Example

Servicing ptr →

RXSDQ Packet available assertion DA[p]	PHY enable	CALENDAR ADDR	CALENDAR DATA
1	1	0	PHYIDx
0	0	1	PHYIDy
1	1	2	PHYIDz
..	..	..	..
..	..	..	..
0	1	127	PHYIDz

The calendar algorithm is implemented by using a pointer called the servicing pointer. The servicing pointer moves down the calendar, and the first positive packet available assertion the pointer encounters will be the PHYID selected for transfer on the next subsequent opportunity. It is recommended that repeated entries in the calendar be spread in a uniform manner in the calendar. This will help maximize the chances of selection in a proportional manner. The servicing algorithm remembers all assertions for packet available made in the past and advances the servicing pointer through the responses without regard to the age of the response. This algorithm provides flexibility in servicing without starvation so long as the number of entries in the calendar for a PHY are proportional to the bandwidth of that PHY.

The table above is an example showing the Calendar with the data available response (DA[p]) from the RXSDQ. In this example, the entire 128 entries are used and PHYIDx and PHYIDz are enabled and PHYIDy is not enabled. The servicing pointer traverses the entries that responded with a positive data available DA[p] assertion. In this example, the selection would be to choose PHYIDx first and then choose PHYIDz.

The number of Calendar entries in one cycle is programmable with a maximum value of 128.

For most applications using the S/UNI-MACH48, it is recommended that the calendar length be set to 48 and each STS-1 granule be distributed evenly across the calendar ordering. This will simplify the procedure needed to create concatenated channels or disperse a concatenated channel into individual channels. If dynamic reprovisioning may be required, we recommend that the calendar be programmed as in Table 58.

Table 58 RXPHY Calendar Recommended Setup

Calendar Entry	STS-1 ch#	STS-3c ch#	STS-12c ch#	Calendar Entry	STS-1 ch#	STS-3c ch#	STS-12c ch#
0	0	0	0	24	28	24	0
1	1	1	12	25	29	25	12
2	2	2	24	26	30	26	24
3	3	3	36	27	31	27	36
4	12	12	0	28	40	36	0
5	13	13	12	29	41	37	12
6	14	14	24	30	42	38	24
7	15	15	36	31	43	39	36
8	24	24	0	32	8	0	0
9	25	25	12	33	9	1	12
10	26	26	24	34	10	2	24
11	27	27	36	35	11	3	36
12	36	36	0	36	20	12	0
13	37	37	12	37	21	13	12
14	38	38	24	38	22	14	24
15	39	39	36	39	23	15	36
16	4	0	0	40	32	24	0

Calendar Entry	STS-1 ch#	STS-3c ch#	STS-12c ch#	Calendar Entry	STS-1 ch#	STS-3c ch#	STS-12c ch#
17	5	1	12	41	33	25	12
18	6	2	24	42	34	26	24
19	7	3	36	43	35	27	36
20	16	12	0	44	44	36	0
21	17	13	12	45	45	37	12
22	18	14	24	46	46	38	24
23	19	15	36	47	47	39	36

For instance, if an STS-3c channel occupied entries 0, 16, and 32 in the calendar, it can be broken up into 3 STS-1 channels by simply overwriting those 3 calendar entries with new PHY channel numbers.

If 3 STS-1 channels are to be combined into an STS-3c channel, the 3 calendar entires can simply be written with the STS-3c channel number and the calendar will be reprovisioned with each channel receiving the appropriate service bandwidth.

Note that when reconfiguring the calendar, the affected calendar entries must be unprovisioned in its upstream blocks first (RXSDQ, RTDP, RCFP, RCAS blocks) to ensure that they are not being serviced while the reconfiguration is taking place. Unprovisioning the channels will make it so the calendar algorithm sees no data available from those channels.

14.18 Setting ATM Mode of Operation over Utopia L3 or POS-PHY L3

ATM is the default operation mode for the S/UNI-MACH48. The following sequence of operation should be used to prepare a channel(s) for ATM operation without affecting other channels.

1. Input pin POSL3/UL3B must be tied to logic 1 to enable mixed-ATM/POS operation or to logic 0 for pure ATM operation with Utopia Level 3 interface. The POS-PHY L3 interface must be used for dual-mode operation. This must be set at power-up.

2. Unprovision (disable) all line-side timeslots and system side channels which are to be changed. This is to be done in the TCAS12, RCAS12, TCFP, RCFP, TTDP, RTDP, RXSDQ, and TXSDQ blocks. The FIFOs of the corresponding channels will be reset and emptied when they are unprovisioned.

3. Leave the TXSDQ and RXSDQ BT[4:0] and DT[7:0] values equal to their default values of 3 respectively. See Sections 14.15 and 14.16 for details.

4. Set the POS_SEL register bits in the TCFP, RCFP, TTDP and RTDP blocks to logic 0 for the desired ATM channels. Optionally set the POS_SEL register bits RXSDQ and TXSDQ blocks to 0 for the desired ATM channels if runt cell detection is required at the expense of reduced bandwidth. The RXSDQ and TXSDQ will still process cells correctly, though without the size checking if configured for POS traffic.

5. Optionally, reset the performance monitoring counters in all blocks by writing to the S/UNI-MACH48 Global Performance Monitor Update register. TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

14.18.1 Transmit UL3 Interface Misalignment Recovery

For both single-PHY and multi-PHY transfers on the Transmit UL3 interface, cell alignment is done on 1-to-0 transition of TENB. That is, TSOC is expected on the same cycle where TENB has just transitioned to logic 0. Thus, if the upstream device has misalignment between its TENB and TSOC, the S/UNI-MACH48 will align its cells to the TENB and may give error indications on its RUNTCELLI (TXPHY Interrupt Status register, 0049H) and/or SOPI interrupt (TXSDQ SOP Error Port and Interrupt Indication, 0065H). Once the upstream device has realigned its signals, the S/UNI-MACH48 will realign on the next 1-to-0 transition of TENB.

14.18.2 Receive UL3 Interface Misalignment Recovery

For both single-PHY and multi-PHY transfers on the Receive UL3 interface, cell transfer is aligned to the RENB signal. Once asserted to logic 0, RENB must not deassert until cycle P11 of a cell. The S/UNI-MACH48 will not respond to early deassertions of RENB and will continue transfer of the cell in progress.

To realign the S/UNI-MACH48 to the downstream device, the RENB must remain deasserted for more than 13 clock cycles. This will guarantee that the S/UNI-MACH48 has completed transfer of any cell and is ready to reselect a new PHY via RENB.

This means that for a single-PHY application, RENB cannot be tied low with the downstream device expecting to align using the RSOC output of the S/UNI-MACH48.

14.19 Setting Packet Mode of Operation Over POS-PHY L3

The following sequence of operation should be used to prepare a particular channel(s) for Packet operation without affecting other channels.

1. Input pin POSL3/UL3B must be tied to logic 1 to enable the POS-PHY L3 system interface at power-up.

2. Unprovision (disable) all line-side timeslots and system side channels which are to be changed. This is to be done in the TCAS12, RCAS12, TCFP, RCFP, TTDP, RTDP, RXSDQ, and TXSDQ blocks. The FIFOs of the corresponding channels will be reset and emptied when they are unprovisioned.

3. Set the POS_SEL register bits in the TCFP, RCFP, TTDP, RTDP, RXSDQ, and TXSDQ blocks to logic 1 for the desired POS/HDLC channels.

4. Program the RXPHY servicing algorithm. See Section 14.17 for details.

5. Set the RXSDQ Data Available threshold (DT[7:0]) values to the desired values. See Section 14.16 for details.

6. Enter the RXPHY BURST_SIZE[3:0]. See Section 14.16 for details.

7. Enter the TXSDQ Buffer Available Threshold (BT[4:0]). See Section 14.15 for details.

8. Enter the TXSDQ Data Available Threshold (DT[7:0]). See Section 14.16 for details.

9. Optionally, reset the performance monitoring counters in all blocks by writing to the S/UNI-MACH48 Global Performance Monitor Update register. TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

14.20 Setting Transparent Mode of Operation Over POS-PHY L3

To Send transparent data over the TelecomBus from the POS-PHY L3 bus, configure the S/UNI-MACH48 For Packet Over SONET mode as in section 14.18.1 with the following amendments:

1. Set the DELINDIS bits and clear the CRC_SEL bits of the TCFP and RCFP (for OC12c or OC48c channels) or of the TTDP and RTDP (for lower rate channels). Make sure that RBY_MODE is set in the RCFP to insure proper byte counting.

2. Make sure that the FIFO on the transmit side will never underrun. A FIFO underrun in Transparent mode would result in data corruption.

3. Data should be transferred over the POS-PHY Level3 bus broken up into 64 byte packets

14.21 SIRP Configuration Options

14.21.1 SIRP Concatenated Channel Configuration

Each SIRP processes STS frames in an STS-12c/STM-4c, STS-3c/STM-1 or STS-1/STM-0 data stream in the datapath section and in the remote alarm section. Note that channel numbers must correspond to the timeslot positions (per-STS-12 stream) for the LCD RDI indication to be mapped properly - STS-3c channel which starts at timeslot 0 of an STS-12 slice must be mapped to channel 0, 12, 24, or 36. STS-1 channel at timeslot 10 of an STS-12 slice must be mapped to channel 10, 22, 34, or 46.

To configure the SIRP to handle the variety of data streams, the following table of configuration examples can be applied:

Table 59 SIRP Configuration

Configuration	Timeslot											
	0	1	2	3	4	5	6	7	8	9	10	11
1 STS-12c (a)	P_a	U	U	U	U	U	U	U	U	U	U	U
4 STS-3c (a,b,c,d)	P_a	P_b	P_c	P_d	U	U	U	U	U	U	U	U
3 STS-3c (a,b,c) + 3 STS-1 (d,e,f)	P_a	P_b	P_c	P_d	U	U	U	P_e	U	U	U	P_f
2 STS-3c (a,b) + 6 STS-1 (c,d,e,f,g,h)	P_a	P_b	P_c	P_d	U	U	P_e	P_f	U	U	P_g	P_h
2 STS-3c (a,b) + 6 STS-1 (c,d,e,f,g,h)	P_c	P_a	P_d	P_b	P_e	U	P_f	U	P_g	U	P_h	U
1 STS-3c (a) + 9 STS-1 (b,c,d,e,f,g,h,i,j)	P_a	P_b	P_c	P_d	U	P_e	P_f	P_g	U	P_h	P_l	P_j
12 STS-1 (a,b,c,d,e,f,g,h,i,j,k,l)	P_a	P_b	P_c	P_d	P_e	P_f	P_g	P_h	P_i	P_j	P_k	P_l

P = Provisioned (TS***x***_PROV = 1)

x = timeslot

U = Unprovisioned (TS***x***_PROV = 0)

Note: Combinations of STS-3c data streams without STS-1 data streams are possible as well as combinations of smaller sets of STS-1data streams (i.e. 11 STS-1's, 10 STS-1's, 9 STS-1's, etc.). Other configurations are possible; not all configurations are shown in table.

Table 60 STS-48c Configuration

STS-48c Configuration	Timeslot											
	0	1	2	3	4	5	6	7	8	9	10	11
SIRP #1 (a)	P_a	U	U	U	U	U	U	U	U	U	U	U
SIRP #2	U	U	U	U	U	U	U	U	U	U	U	U
SIRP #3	U	U	U	U	U	U	U	U	U	U	U	U
SIRP #4	U	U	U	U	U	U	U	U	U	U	U	U

P = Provisioned (TS***x***_PROV = 1)

x = timeslot

U = Unprovisioned (TS***x***_PROV = 0)

Note : A combination of n = 4 SIRP can be used to handle STS-(n x 12)c data streams. This involves provisioning only the first timeslot (#0) of the first SIRP to handle the J1 and G1 byte and leaving the remaining SIRP timeslots unprovisioned.

14.21.2 SIRP Modes of Operation

The remote alarm port RDI and REI values are sourced from an upstream SONET/SDH framer such as the PM5315 Spectra-2488, the PM5313 Spectra-622, or the PM5316 Spectra-4x155.

Register Controlled Mode (TS*x*_RMODE[1:0] =b'00)

In this mode, REI[3:0] and RDI[1:0] are both sourced from internal registers TS*x*_REI[3:0] and TS*x*_RDI[1:0] respectively. The remote alarm port is ignored as well as the RCFP's and RTDP's loss-of-cell-delineation LCD alarms (which is mapped to a programmable RDI code).

Remote Alarm Input Only Mode (TS*x*_RMODE[1:0] =b'01)

In this mode, the REI and RDI values transmitted are sourced entirely from the remote alarm port.

Remote Alarm Input With Loss Of ATM Cell Delineation Input Mode (TS*x*_RMODE[1:0] =b'10)

In this mode, the REI values are sourced from the remote alarm port and the RDI indication is generated by the receive cell processor's loss-of-cell delineation assertion state (which is mapped to a programmable RDI code).

Normal Error Reporting Mode (TS*x*_RMODE[1:0] =b'11)

In this mode, the REI and RDI values are sourced from the remote alarm port. If the extended RDI mode is enabled, the receive cell processor's loss-of-cell delineation state, which is mapped to a programmable RDI code if asserted, is compared with the remote port's RDI code. The higher priority RDI will take precedence.

14.22 PRBS Generator and Monitor (PRGM)

A pseudo-random (using the $X^{23}+X^{18}+1$ polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. It cannot be inserted into the ATM cell or packet payload. With PRBS data and incrementing data patterns, the payload envelope is filled with pseudo-random/incrementing bytes with the exception of POH and fixed stuff columns. In the case of the incrementing counts, the count starts at 0 and increments to FFh before the count starts over at 0 once again. The incrementing count is free to float within the payload envelope and therefore the 0 count is not associated with any fixed location within a payload envelope.

The user has the option to monitor a programmable sequence in all the B1 byte positions. The complement of these values are also monitored in the E1 byte positions. This is used to check for misconfiguration of STS-1 cross-connect fabrics. If a known STS-1 originated from a particular STS-1 port, the source can be programmed to send a B1 pattern that would be monitored at the other end.

14.22.1 Mixed Payload (STS-12c, STS-3c, and STS-1)

Each PRGM is designed to process the payload of a STS-12/STM-4 frame in a time-multiplexed manner. Each time division (12 STS-1 paths) can be programmed to a granularity of a STS-1. It is possible to process one STS-12c/STM-4c, twelve STS-1/STM-0 or four STS-3c/STM-1 or a mix of STS-1/STM-0 and STS-3c/STM-1 as long as the aggregate data rate is not more than one STS-12/STM-4 equivalent. The mixed payload configuration can support the three STS-1/STM-0 and STS-3c/STM-1 combinations shown below:

- Three STS-1/STM-0 with three STS-3c/STM-1
- Six STS-1/STM-0 with two STS-3c/STM-1
- Nine STS-1/STM-0 with one STS-3c/STM-1.

The STS-1 path that each one of the payload occupies, cannot be chosen randomly. They must be placed on STS-3c/STM-1 boundaries (group of three STS-1). See Table 7 and Table 9 for more details.

14.22.2 Synchronization

Before being able to monitor the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized the monitoring LFSR is able to generate the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving 3 PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The 8 newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

In master/slave configuration of the monitor (STS-48c/VC-4-16c concatenated payloads) more bytes are needed to recover the LFSR state, because the slaves needs a few bytes to be synchronized with the J1 byte indicator.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

An Out of Synchronization and Synchronized State is defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving 4 consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 3 erred bytes. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization.

It is important to note that the monitor can falsely synchronize to an all zero pattern or, if the incoming pattern is inverted, an all ones pattern. It is recommended that users poll the PRGM Monitor's LFSR value after synchronization has been declared to confirm that the value is neither all 1's or all 0's.

Upon detecting 3 consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take 4 consecutive non-erred PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

14.22.3 Master/Slave Configuration for STS-48c/STM-16c Payloads

To monitor STS-48c/STM-16c payloads, a master/slave configuration is available where each monitor receives 1/4 of the concatenated stream. In the case of a STS-48c/STM-16c, 4 PRGMs are used in a master/slave configuration. Because the payload is four bytes interleaved, after a group of four consecutive bytes, a jump in the sequence takes place. The number of bytes that must be skipped can be determined using the number of PRGMs in the master/slave configuration. For example, to process an STS-48c/STM-16c, the number of sequence to skip is (4 PRGMS * 4 bytes) – 3 = 13. So, 13 sequences will be skipped after each group of four consecutive bytes.

The PRBS monitor can be re-initialize by the user by writing in a normal register of the master PRGM. Since all the slave PRGMs use the LFSR state of the previous PRGM in the chain, they will be re-initialize too.

14.22.4 Special Note for Use of PRGM in STS-48c/STM-16c mode (TX48C = 1 or RX48C = 1)

The PRGMs always expect and generate data in the format shown in Table 52. For standard line-side STS-48c/STM-16c timeslot mappings, the IWTI_MODE[1:0], IPTI_MODE[1:0], OWTI_MODE[1:0], or OPTI_MODE[1:0] bits in the S/UNI-MACH48 Miscellaneous register can be set to ‘b00 to automatically provide the proper mapping to the PRGM for PRBS detection.

Because the system-side timeslot map that the master/slave configuration of the PRGMs in STS-48c/STM-16c mode is different than that required by the other blocks, the xxTI_MODE[1:0] bits previously mentioned may have to be altered. This may cause the other blocks to receive data in corrupted format, but they should not be in use in any case because the PRBS data stream from/to the PRGM block will not contain packet or ATM data that can be processed by the downstream S/UNI-MACH48 blocks.

14.22.5 Error Detection and Accumulation

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect byte errors in the payload. A byte error is detected on a comparison mismatch of the two bytes. Only a single byte error is counted regardless of the number of errored bits in the byte. All byte errors are accumulated in a 16 bit byte error counter. The error counter will saturate at its maximum value of FFFFh, ie it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the PRGM Monitor Error Count. An indirect read to that register will initiate a transfer of the error counter into the registers for reading. The error counter is cleared when transferred into the registers and the accumulation restarts at zero. When reading error counts for concatenated payloads of STS-3c /STM-1c or STS-12c/STM-3c sizes, it is only necessary to read the error count in the master slice (first associated STS-1).

All counts will be accumulated in the master slice when the error count transfer is initiated. In the case of STS-48c/STM-16c payloads, it is necessary to read the error count in the first STS-1 of each PRGM in the group of 4 PRGMs associated with the STS-48c/STM-16c monitor. Alternately, all STS-1 error counts belonging to a concatenated stream may be read. In this case, the error counts in each associated register must be summed by software. For each independent STS-1 monitored by a PRGM, the error count register for each individual STS-1 must be read.

Bit errors are accumulated only when the monitor is in synchronized state. To enter the synchronize state, the monitor must have synchronized to the incoming PRBS stream and received 4 consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced to by programming high the RESYNC register bit, or once it detects 3 consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated. However, the 3 errors which cause the PRGM to lose synchronization may in fact be counted as 3, 4, or 5 errors.

14.22.6 B1/E1 Overwrite and Detection

The B1 and E1 bytes can be used by the PRGM to perform point-to-point connection verification. One PRGM on one end of a cross-connect can set its B1/E1 bytes to a known value. At the opposite end of the cross-connect, the receiver's PRGM can be set up to expect that same B1/E1 value. An error interrupt can be generated if the values do not match.

The monitor is set-up for B1/E1 comparison by setting the B1E1_ENA bit in the PRGM Indirect Register 0H: Monitor Timeslot Configuration page for each timeslot . The expected value of B1 and E1 is set with the B1[7:0] bits in the The generator is set up to transmit user-defined B1/E1 values by setting the B1E1_ENA bit in PRGM Indirect Register 8H: Generator Timeslot Configuration Page for each timeslot. The desired B1/E1 value is set using the B1[7:0] bits in the PRGM Indirect Register BH: Generator B1/E1 Value Page. The E1 values are the complement of the B1 values.

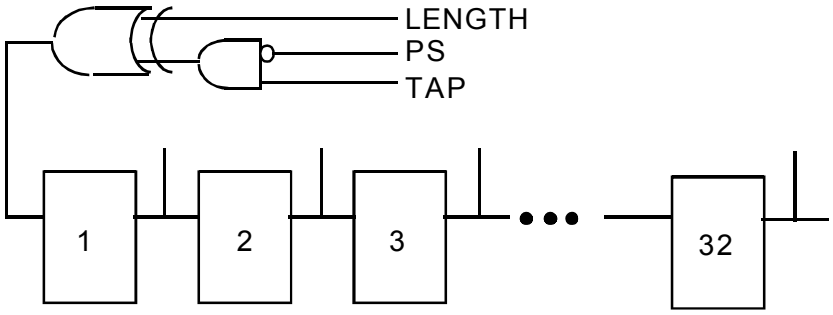
PRGM Indirect Register 3H: Monitor B1/E1 Value Page (E1[7:0] bits are the inverse of the B1[7:0] bits). The actual received B1 and E1 values are given in the PRGM Indirect Register 5H: Monitor Received B1/E1 Bytes Page. If a B1/E1 matching error interrupt is generated by the PRGM, the B1/E1 values in this register should be compared to the B1[7:0] value in PRGM Indirect Register 3H to see if they match or not.

14.23 DS3 PRBS and Repetitive Pattern Generation with PRGD

A pseudo-random or repetitive pattern can be inserted/extracted in the DS32 PLCP payload (if PLCP framing is enabled) or in the DS3 framing format payload (if PLCP framing is disabled). It cannot be inserted into the ATM cell payload.

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 23 below:

Figure 23 PRGD Pattern Generator



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

14.23.1 Generating and Detecting Repetitive Patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers. The repetitive pattern will then be continuously generated. The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream. It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences. Note that the PRGD does NOT look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers (which will then contain the 32 bits detected immediately prior to the strobe).

14.23.2 Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in the two tables below:

Table 61 Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	PT	PL	PI#1	PI#2	PI#3	PI#4	TINV	RINV
2^3 –1	00	02	FF	FF	FF	FF	0	0
2^4 –1	00	03	FF	FF	FF	FF	0	0
2^5-1	01	04	FF	FF	FF	FF	0	0
2^6 –1	04	05	FF	FF	FF	FF	0	0
2^7 –1	00	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1
2^9 -1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} –1	02	09	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} –1	02	10	FF	FF	FF	FF	0	0
2^{18} –1	06	11	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
2^{21} –1	01	14	FF	FF	FF	FF	0	0
2^{22} –1	00	15	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} –1	02	18	FF	FF	FF	FF	0	0

Pattern Type	PT	PL	PI#1	PI#2	PI#3	PI#4	TINV	RINV
$2^{28}-1$	02	1B	FF	FF	FF	FF	0	0
$2^{29}-1$	01	1C	FF	FF	FF	FF	0	0
$2^{31}-1$	02	1E	FF	FF	FF	FF	0	0

Table 62 Repetitive Pattern Generation (PS bit = 1)

Pattern Type	PT	PL	PI#1	PI#2	PI#3	PI#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

Notes for the Pseudo Random and Repetitive Pattern Generation Tables

1. The PS bit and the QRSS bit are contained in the PRGD Control register
2. PT = PRGD Tap Register
3. PL = PRGD Length Register
4. PI#1 = PRGD Pattern Insertion #1 Register
5. PI#2 = PRGD Pattern Insertion #2 Register
6. PI#3 = PRGD Pattern Insertion #3 Register
7. PI#4 = PRGD Pattern Insertion #4 Register
8. The TINV bit and the RINV bit are contained in the PRGD Control register

14.24 Interrupt Service Routine

The S/UNI-MACH48 will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the S/UNI-MACH48 Interrupt Block Identifier register (0011H). The “ID_…” bits point to the functional block(s) which caused the hardware interrupt. For instance, if a DS3 FRMR block caused the interrupt, the ID_DS3FRMRI bit will be logic 1. These bits get cleared when the interrupt is cleared.

2. Find the registers which correspond to the functional block(s) which were indicated to have caused the interrupt. These registers further isolate the interrupt source. For instance, the S/UNI-MACH48 DS3FRMR #0-15, #16-31, and #32-47 Interrupt Indication registers will identify which of the 48 DS3 FRMR blocks caused the interrupt.

3. Find the register address of the corresponding block which caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from steps 1 and 2 are cleared once these register has been read and the interrupt(s) identified.

4. Service the interrupt(s).

5. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 4 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

14.25 Accessing Indirect Registers

Indirect registers are used to conserve address space in the S/UNI-MACH48. Indirect registers are accessed by writing the indirect address register. The following steps should be followed for writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the desired configurations for the channel into the indirect data registers. Note that for the RXSDQ and the TXSDQ, all indirect data registers must be written for each indirect access.

3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

4. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

3. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

4. Read the indirect data registers to find the state of the register bits for the selected channel number.

14.26 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. The DS3 PMON, PLCP PMON, TCFP, RCFP, TTDP, RTDP, R8TD, RXSDQ, TXSDQ, PRGD, and PRGM all contain performance monitor registers. The counters have been sized to not saturate if polled every second.

Depending on the block, its counters can be accumulated independently in one of two ways: one of the registers which contain the latched counter values is written to or if its 'transfer trigger' register is written to. A device update of all the counters can be done by writing to the S/UNI-MACH48 Global Performance Monitor Update register (register 0000H). After this register is written to, the TIP bit in this register can be polled to determine when all the counter values have been transferred and are ready to be read.

14.27 Using the Internal DS3 FDL Transmitter

It is important to note that the access rate to the TDPR registers is limited by the rate of the high-speed system clock. Consecutive accesses to each TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/32 that of SYSCLK. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the S/UNI-MACH48, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value). An HDLC all-ones Idle signal will be sent while in this state. The TDPR is enabled by setting the EN bit to logic 1. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output and the S/UNI-MACH48 Interrupt Service Routine (Section 14.24) to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

Interrupt Driven Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for data to be transmitted. Once data is available to be transmitted, then go to step 2.

2. Write the data byte to the TDPR Transmit Data register.

3. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

4. If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

TDPR Interrupt Routine

Upon assertion of INTB, the source of the interrupt must first be identified by using the Interrupt Location procedure. Once the source of the interrupt has been identified as TDPR, then the following procedure should be carried out:

1. Read the TDPR Interrupt Status register.

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To re-enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

3. If OVRI=1, then the FIFO has overflowed. The packet which the last byte written into the FIFO belongs to has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

4. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

   If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

Polling Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

3. If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

4. If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step 6.

5. If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step 6.

6. If more data bytes are to be transmitted in the packet, then go to step 2.

7. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

14.28 Using the Internal DS3 FDL Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the internal high-speed system clock SYSCLK. Consecutive accesses to each RDLC Status and RDLC Data registers should be done at a rate no faster than 1/40 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default state). The RDLC Interrupt Control register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register to determine when to read the RDLC Data register. In the interrupt driven mode, the processor controlling the RDLC uses the S/UNI-MACH48 INTB output and the S/UNI-MACH48 Interrupt Service Routine (Section 14.24) to determine when to read the RDLC Data register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the S/UNI-MACH48 is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by following the S/UNI-MACH48 Interrupt Service Routine (Section 14.24). Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

1. RDLC Status register read. The INTR bit should be logic 1.

2. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3. If COLS = 1, then set the EMPTY FIFO software flag.

4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

5. Read the RDLC Data register.

6. Read the RDLC Status register.

7. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8. If COLS = 1, then set the EMPTY FIFO software flag.

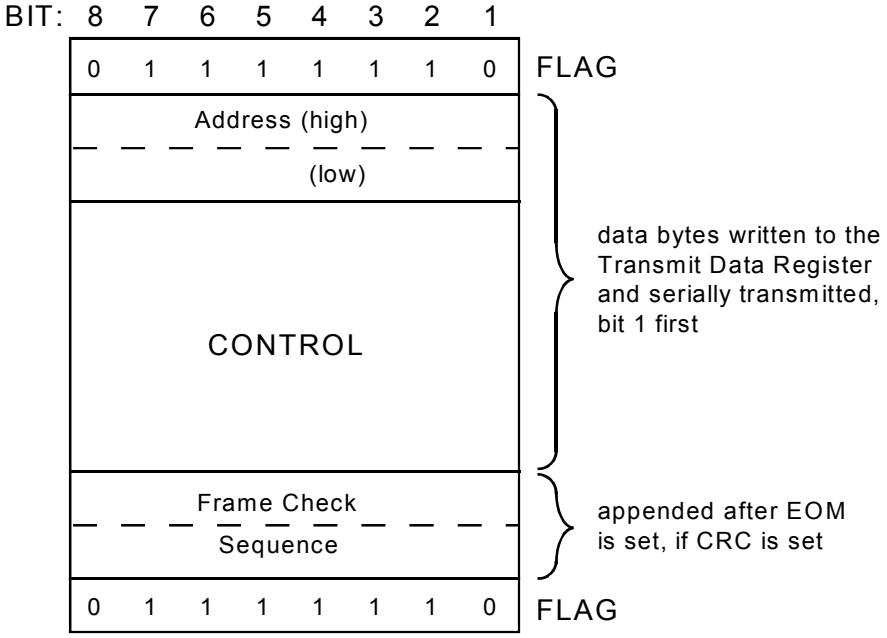
9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.
    - If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.
    - If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.
    - If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.
    - If PBS[2:0] = 000, store the packet data.
11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

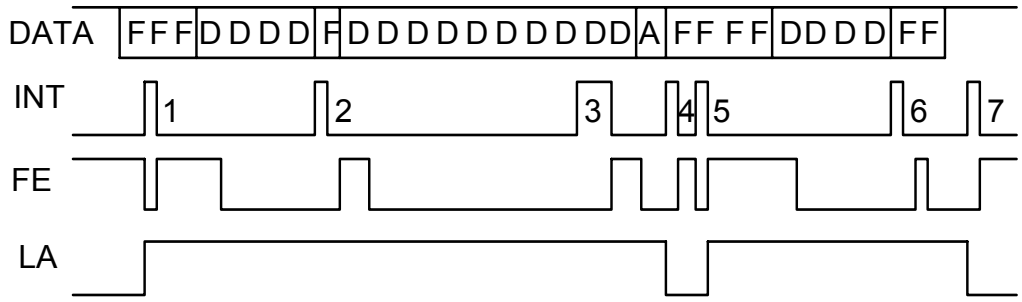
If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 24 Typical DS3 FDL Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 25 Example DS3 FDL Multi-Packet Operational Sequence



F - flag sequence (01111110)

A - abort sequence (01111111)

D - packet data bytes

INT - active high interrupt output

FE - internal FIFO empty status

LA - state of the LINK ACTIVE software flag

Figure 25 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

At points 1 and 5 the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

14.29 Transmitting Bit Oriented Codes

There are two ways that Bit Oriented Codes can be sent for DS3 frames: Polling mode and Interrupt mode.

For Polling Mode:

1. Determine the desired BOC code repetition value N.

2. Set RPT[3:0] in the XBOC Control register to equal N-1.

3. Set BC[5:0] to equal the desired BOC code. The BC[0] bit is the first bit of the BOC code to be transmitted.

4. Read RDY. When RDY is logic 1, then a new BC[5:0] can be entered or BOC transmission can be terminated by setting BC[5:0] to 'b111111. When the first BOC code has been transmitted N times, the new BOC code will begin.

And in Interrupt Mode:

1. Set BOCSMPE to logic 1 to enable the interrupt.

2. Determine the desired BOC code repetition value N.

3. Set RPT[3:0] in the XBOC Control register to equal N-1.

4. Set BC[5:0] to equal the desired BOC code. The BC[0] bit is the first bit of the BOC code to be transmitted.

5. Wait for interrupt on INTB. When INTB is asserted because of the assertion of BOCSMPI, then a new BC[5:0] can be entered or BOC transmission can be terminated by setting BC[5:0] to ‘b111111. When the first BOC code has been transmitted N times, the new BOC code will begin.

14.30 Loopback Operation

The S/UNI-MACH48 supports five loopback functions: Parallel TelecomBus Diagnostic Loopback, Channel-based Diagnostic Loopback, Serial TelecomBus Diagnostic Loopback, Parallel TelecomBus Line Loopback, and Serial TelecomBus Line Loopback.

Parallel TelecomBus Diagnostic Loopback is illustrated in Section 7.1. This loopback mode is set using the DLOOP bit in the S/UNI-MACH48 Configuration and Diagnostic register.

Channel-based Diagnostic Loopback is illustrated in Section 0. This loopback mode is set per channel (as per UL3 or POS-PHY L3 interface) using the CH***x***_LBEN register bits in the RCAS12 Channel Loopback Enable registers. For this loopback to work properly, channels in the transmit and receive directions must be programmed symmetrically.

Parallel TelecomBus Line Loopback is illustrated in Section 0. This loopback mode is set using the LLOOP bits in the S/UNI-MACH48 Configuration and Diagnostic register.

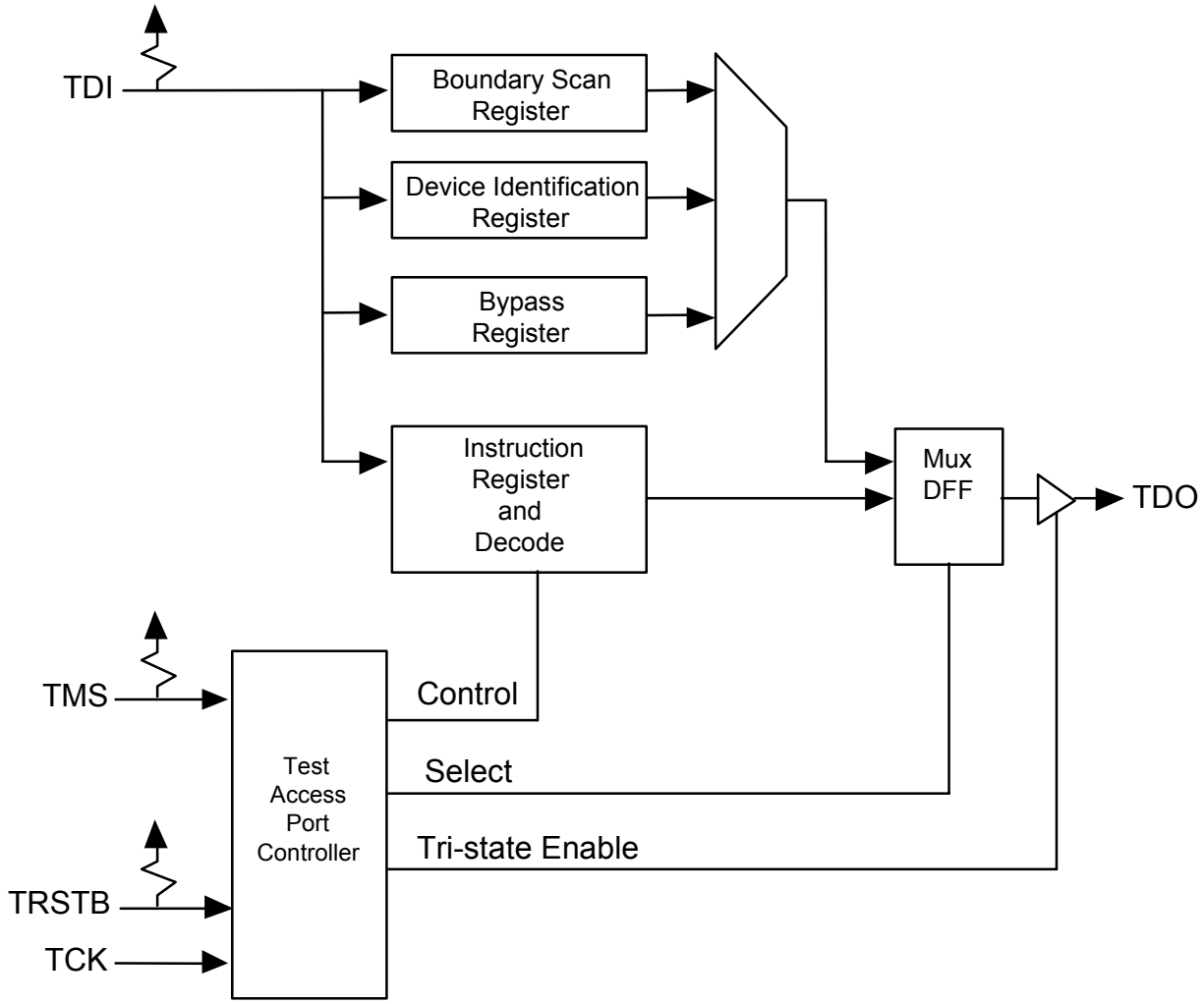
Serial TelecomBus Diagnostic Loopback is illustrated in Section 0. This loopback mode is set using the DLBEN bits in the R8TD Control and Status register. Each 777.6 Mb/s LVDS link can be looped back to its analogous receive link independently.

Serial Line Loopback is illustrated in Section 7.5. This loopback mode is set using the LLBEN bits in the T8TE Control and Status register. Each receive 777.6 Mb/s LVDS link can be looped back to its analogous transmit link independently. Note that the loop back serial data stream will no longer be aligned to the OJ0REF input signal.

14.31 JTAG Support

The S/UNI-MACH48 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 26 Boundary Scan Architecture



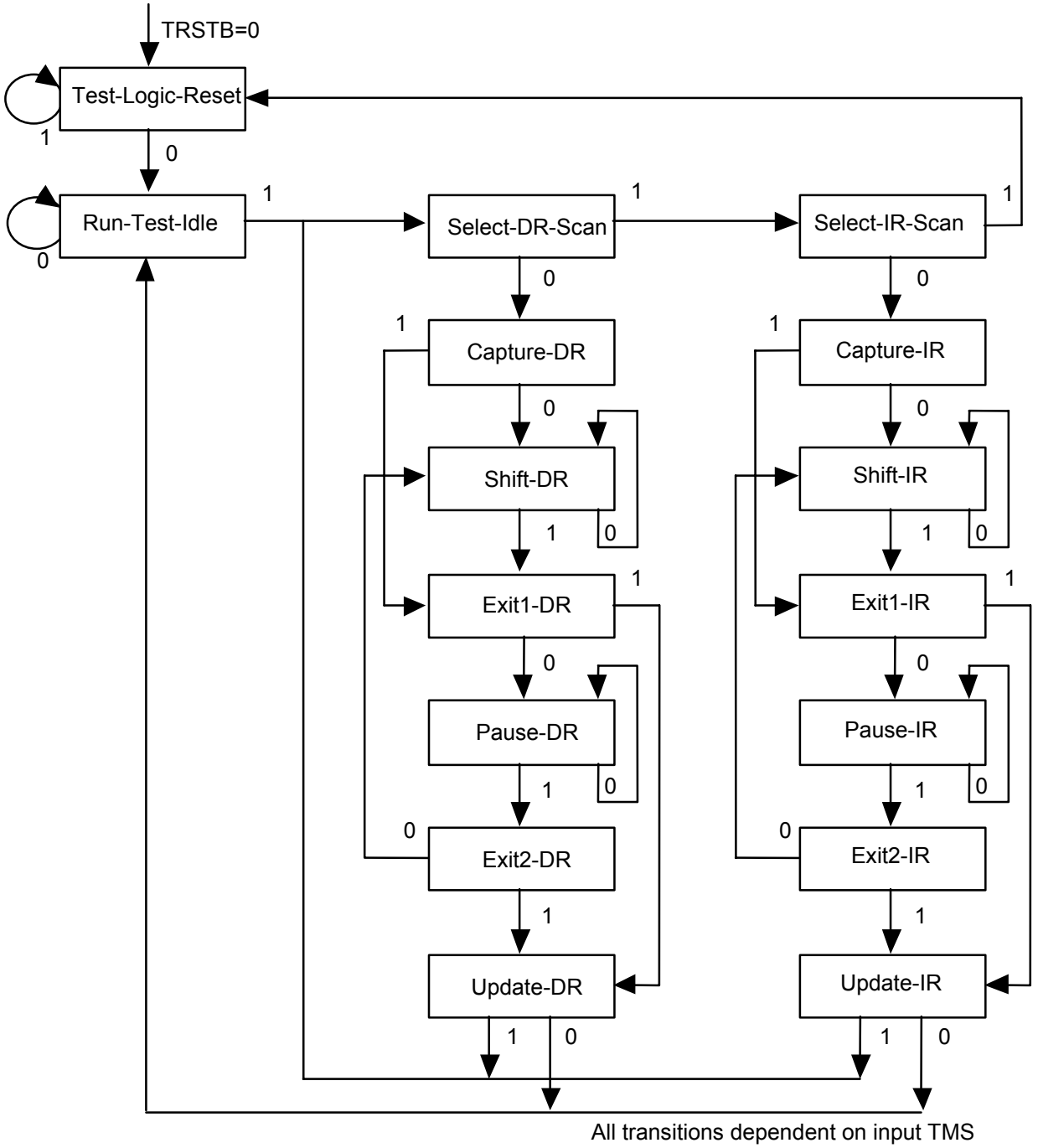
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

14.31.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 27 TAP Controller Finite State Machine



14.31.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

14.31.3 Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

14.32 Power Up Sequence

In order for the S/UNI-MACH48 to operate correctly, all 3.3V power supplies (AVDH and VDDO) must be on before the 1.8V supplies (AVDL and VDDI).

14.33 Reset Sequence

Whenever device reset is de-asserted (either RSTB going high, or writing '0' to the DRESET bit), there is a small probability that the TIP bit (Register 0000H) will lock up. If this lockup occurs, TXSDQ, RXSDQ and RHPP counters will not update, and TIP will never go low. The user must read the TIP bit after each time that device reset is de-asserted. If TIP is '1' for this read, then device reset must be cycled again until TIP is read as '0'. Note that a minimum of 16 TFCLK, RFCLK and SYSCLK clock cycles must occur after reset being de-asserted for the read of the TIP bit to be valid.

14.34 Clock Glitch Recovery

If the TFCLK input is removed and re-connected, the resulting clock glitches can cause the TCA (or PTPA/STPA) to lock up. The following procedure should be executed if the TFCLK_DLL's ERRORI interrupt is asserted:

1. toggle the reset in the TFCLK_DLL
2. unprovision and flush the TXSDQ (stops the upstream device from transmitting)
3. toggle reset in the TXPHY
4. provision the TXSDQ

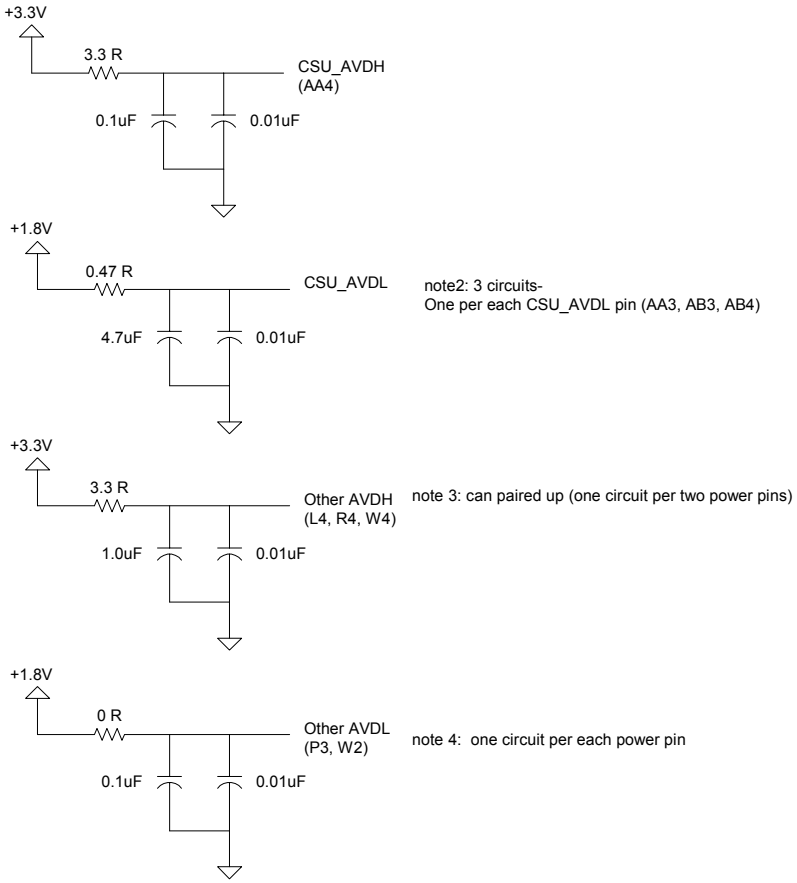
If the RFCLK input is removed and re-connected, the resulting clock glitches can cause the RCA to lock up, or cause the PL3 interface to stop transferring packets. The following procedure should be executed if the RFCLK_DLL's ERRORI interrupt is asserted:

1. toggle reset in the RFCLK_DLL
2. set the CHx_DIS bits to disable receive channels
3. unprovision the upstream cell/packet processors (RCFP and/or RTDP)
4. unprovision and flush the RXSDQ
5. toggle reset in the RXPHY
6. provision the RXSDQ
7. provision the RCFP and/or RTDP
8. clear the CHx_DIS bits to enable receive channels

14.35 LVDS Analog Power Filtering

For best noise tolerance, it is recommended to filter the analog power supplys with the following circuits.

Figure 28 Analog Power Supply Filtering Circuits

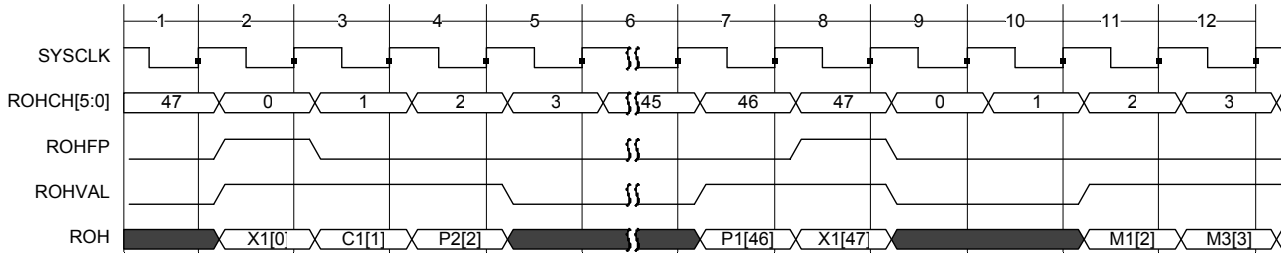


15 Functional Timing

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-MACH48 registers are set to their default states).

15.1 DS3 Overhead Extraction

Figure 29 DS3 Overhead Extraction



As shown in Figure 29, on each rising edge of SYSCLK, the ROHCH[5:0] channel ID increments (and rolls over from 2FH to 00H). If valid data is available for the channel indicated by ROHCH[5:0], then the DS3 Overhead bit for that channel appears on ROH, and ROHVAL is high. Otherwise ROHVAL is low and ROH and ROHFP is invalid. For each channel, ROHFP goes high once every 56 bits to mark the X1 bit for each active channel.

For each DS3 channel, the order of the overhead bit extraction is as follows, starting from the top left X1 bit, proceeding to the right, and then from sub-frame 1 to sub-frame 7:

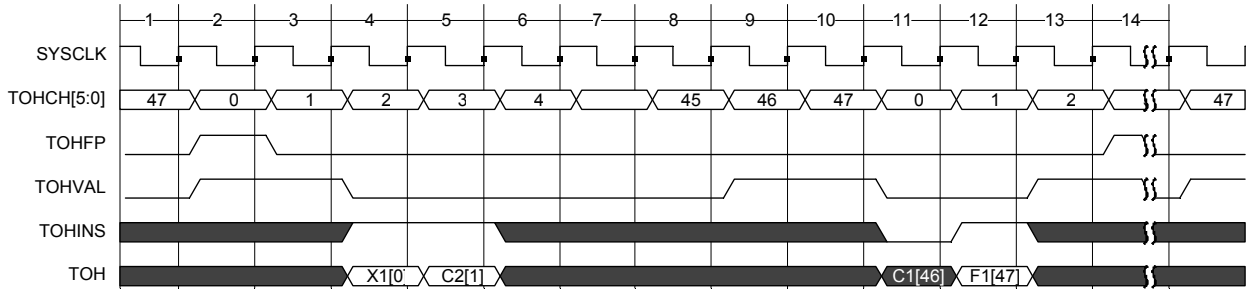
Table 63 DS3 Overhead Bit Extraction

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X1	N/U	C1	N/U	C2	N/U	C3	N/U
2	X2	N/U	C1	N/U	C2	N/U	C3	N/U
3	P1	N/U	C1	N/U	C2	N/U	C3	N/U
4	P2	N/U	C1	N/U	C2	N/U	C3	N/U
5	M1	N/U	C1	N/U	C2	N/U	C3	N/U
6	M2	N/U	C1	N/U	C2	N/U	C3	N/U
7	M3	N/U	C1	N/U	C2	N/U	C3	N/U

The F-bits are not extracted on the overhead port. They are marked not-used (N/U) in Table 63.

15.2 DS3 Overhead Insertion

Figure 30 DS3 Overhead Insertion



As shown in Figure 30, on each rising edge of SYSCLK, TOHCH[5:0] will increment and roll over from 2FH to 00H. If the DS3 processor for the channel indicated by TOHCH[5:0] is ready to receive an overhead bit, then TOHVAL will be high for that cycle. The values on TOH and TOHINS will then be sampled by the S/UNI-MACH48 for that channel on the 3rd rising edge of SYSCLK after the valid channel cycle began. If the sampled value of TOHINS for that channel is high, then the sampled value of TOH will be used to overwrite the current overhead bit. If TOHINS is low, the default DS3 overhead bit for that position is used. The particular bit being requested is indicated by the TOHFP signal which will be high for the bit being requested is the X1 bit for a channel. TOHFP will be low otherwise. When TOHVAL is low, TOHFP is invalid in the current cycle, and TOH and TOHINS are not sampled in the 3rd cycle.

For each DS3 channel, the order of the overhead bit insertion is as follows, starting from the top left X1 bit, proceeding to the right, and then from sub-frame 1 to sub-frame 7.

Table 64 DS3 Overhead Bit Insertion

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X1	F1	C1	F2	C2	F3	C3	F4
2	X2	F1	C1	F2	C2	F3	C3	F4
3	P1	F1	C1	F2	C2	F3	C3	F4
4	P2	F1	C1	F2	C2	F3	C3	F4
5	M1	F1	C1	F2	C2	F3	C3	F4
6	M2	F1	C1	F2	C2	F3	C3	F4
7	M3	F1	C1	F2	C2	F3	C3	F4

15.3 Incoming Parallel TelecomBus

Figure 31 shows the timing of the Incoming TelecomBus interface. Timing is provided by SYSCLK. SONET/SDH data is carried in the ID[*X*][7:0], where '*X*' denotes one of the four sections of the Incoming TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte.

A timeslot naming strategy and assignment on an ID[*X*][7:0] bus is shown in Figure 31. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The IPL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal IJ0J1[*X*] is set high with IPL[*X*] set low to mark the J0 byte of a transport frame. IJ0J1[*X*] is set high with IPL[*X*] also set high to mark the J1 byte of all the streams within ID[*X*][7:0].

High order streams in AIS alarm are indicated by the IPAIS[*X*] signal when the RHPP is disabled (If the RHPP is enabled, then an AIS-P condition detected from the H1/H2 pointers is the source of an AIS alarm). Assertion of the AIS alarm will cause the cell delineation blocks to lose alignment. If the RHPP is enabled, garbled received packets may leak through and FCS, Min Length and Max Length errors will be reported, so it is recommended that on receiveing a PAISI, PLOPI, PAISCI or PLOPCI interrupt that those channels in this errored state be disabled (CHx_DIS in the RCAS). The ICMP signal selects the active connection memory page in the Ingress Working Time-slot Interchange (IWTI) block. It is only valid at the J0 byte position and is ignored at all other positions within the transport frame. The J0 byte position on all four buses must be aligned.

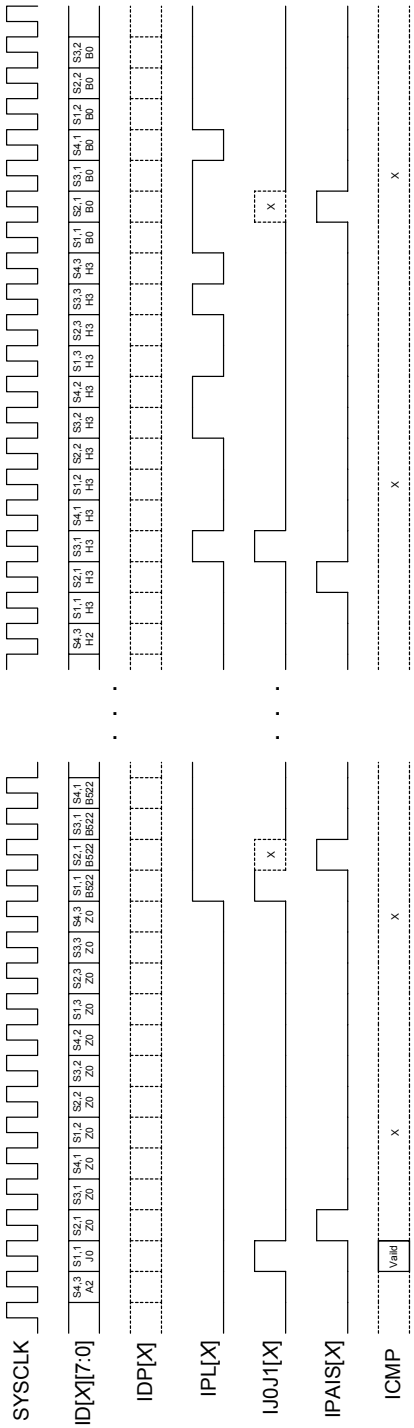
In Figure 31, timeslots numbers S1,x, S2,y, and S4,z are configured as STS-1/STM-0 operation. Timeslot number S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on IPL[*X*] and IJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path AIS (IPAIS[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by IJ0J1[*X*] being set high at byte S3,1/H3 and IPL[*X*] being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3.

For the case where an STS-48c/STM-16c is carried on the four buses ID[4:1][7:0], the J0 indication is expected on all four buses (IJ0J1[4:1] = 1 and IPL[4:1] = 0) at the same time. The J1 indication is expected only on the first bus (IJ0J1[1] = 1 and IPL[1] = 1, IJ0J1[4:2] = 0 and IPL[1] = 1).

ICMP is sampled at the clock cycle where the J0 indication is given (IJ0J1[*X*] is logic 1 and IPL[*X*] is logic 0). ICMP is used to select the incoming memory page in the IWTI when the parallel TelecomBus is in use.

The arrangement shown in Figure 31 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

Figure 31 Incoming Parallel TelecomBus Timing



15.4 Outgoing Parallel TelecomBus

Figure 32 shows the timing of the Outgoing TelecomBus interface. Timing is provided by SYSCLK. SONET/SDH data is carried in the OD[*X*][7:0], where '*X*' denotes one of the four sections of the Outgoing TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. The OWTI block can be used to rearrange timeslots between the system side and the line side of the S/UNI-MACH48.

The timeslot naming strategy and assignment is shown in Figure 32. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The OPL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. All four OJ0J1[4:1] signals are set high with all four OPL[4:1] signals set low to mark the J0 byte of a transport frame. OJ0J1[*X*] is set high with OPL[*X*] also set high to mark the J1 byte of all the streams within OD[*X*][7:0]. High order streams in alarm are indicated by the OALARM[*X*] signal which is set on a per-channel basis using the TCAS12 CH***x***_OALARM register bits. For Figure 32 OJ0REFDLY[13:0] is set to all zeros.

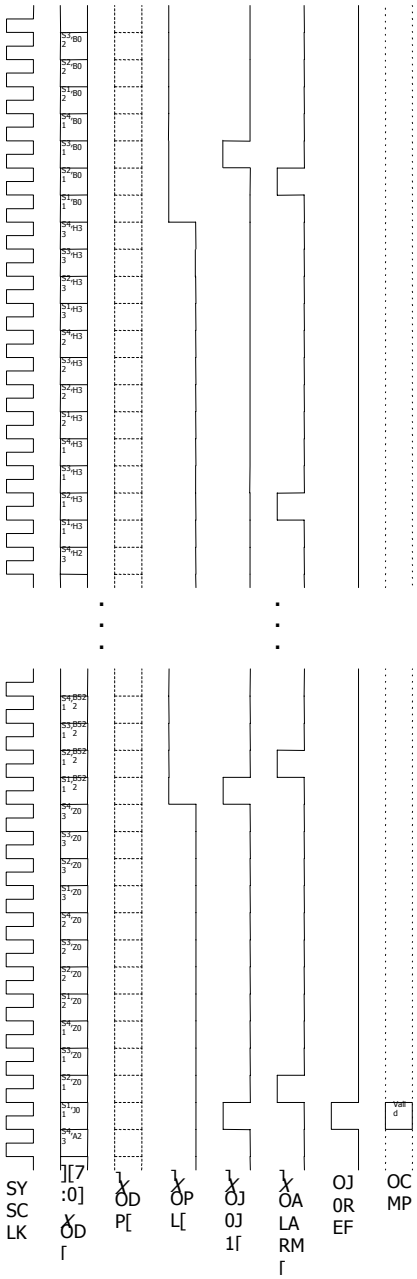
In Figure 32, timeslots S1,x, S2,y, and S4,z are configured for STS-1/STM-0 operation. Timeslot S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on OPL[*X*] and OJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path alarm (OALARM[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is configured in AU4 mode and is shown to have an active offset of 0 by the high level on OPL[*X*] and OJ0J1[*X*] at byte S1,3/B0.

For the case where an STS-48c/STM-16c is carried on the four buses OD[4:1][7:0], the J0 indication is given on all four buses (OJ0J1[4:1] = 1 and OPL[4:1] = 0) at the same time. The J1 indication is given only on the first bus (OJ0J1[1] = 1 and OPL[1] = 1, OJ0J1[4:2] = 0 and OPL[1] = 1).

OCMP is sampled at the clock cycle where the J0 indication is given (OJ0J1[*X*] is logic 1 and OPL[*X*] is logic 0). OCMP is used to select the incoming memory page in the OWTI when the parallel TelecomBus is in use.

The arrangement shown in Figure 32 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

Figure 32 Outgoing Parallel TelecomBus



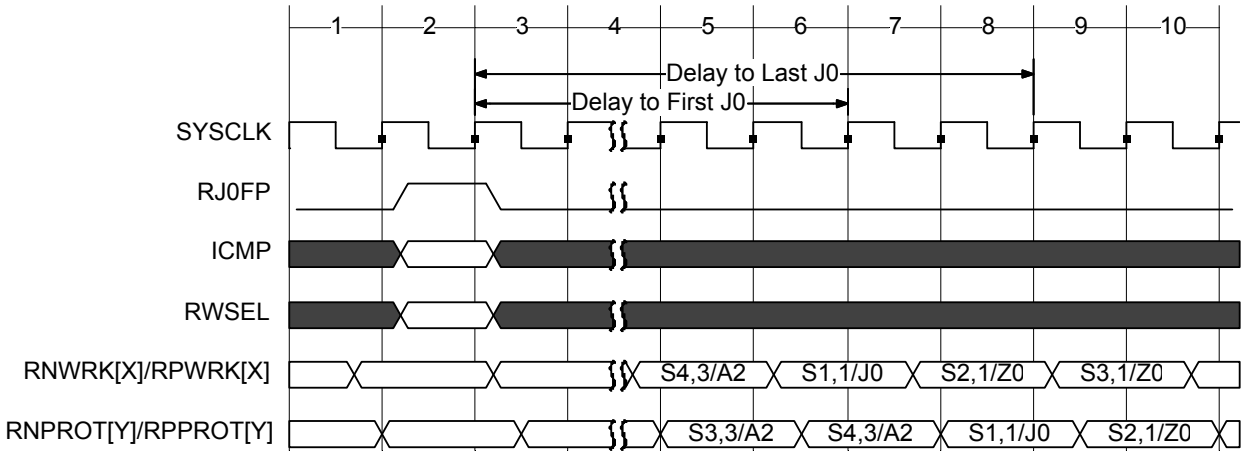
15.5 Incoming Serial TelecomBus

Figure 33 shows the relative timing of the receive serial TelecomBus LVDS links. Links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (RJ0FP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not phase aligned to each other but are frequency locked The delay from RJ0FP being sampled high to the first and last J0 character is shown in Figure 33. In this example, the first J0 is delivered by one of the four working links (RNWRK[4:1]/RPWRK[4:1]). The delay to the last J0 represents the time when the all the links have delivered their J0 character. In the example below, one of the protection links (RNPROT[4:1]/RPPROT[4:1]) is shown to be the slowest. The minimum value for the internal programmable delay (RJ0DLY[13:0]) is the delay to the last J0 character plus 15. The maximum value is the delay to the first J0 character plus 31. Consequently, the external system must ensure that the relative delays between all the receive LVDS links be less than 16 bytes (approximately 165ns).

The RWSEL and ICMP signals are sampled when RJ0FP is asserted to initiate the selection between the working and protection links or switching of the memory pages in the IWTI and IPTI blocks respectively.

The relative phases of the links in Figure 33 are shown for illustrative purposes only. Links may have different delays relative to other members of the same set (working or protection) and relative to links in the other set (working or protection) than what is shown.

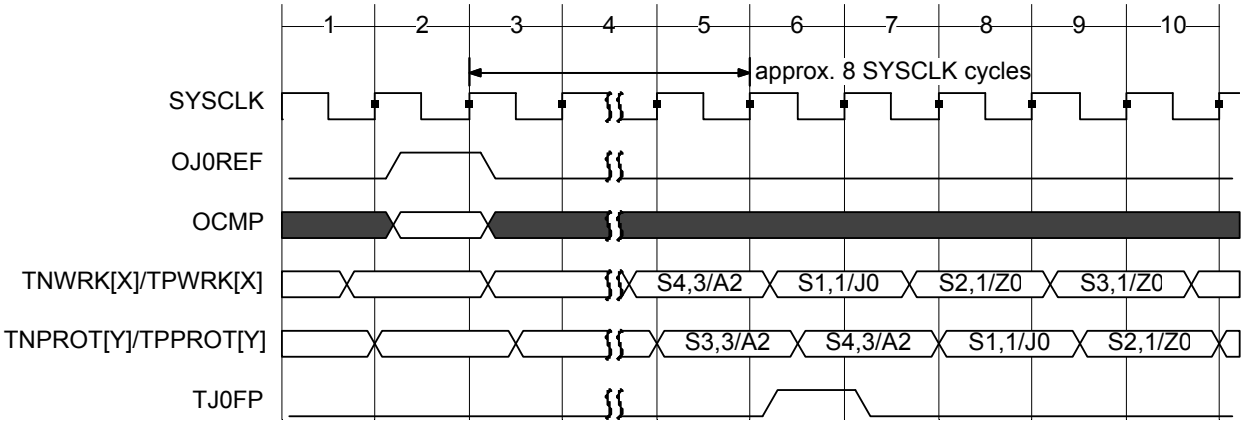
Figure 33 Receive Serial TelecomBus Link Timing



15.6 Outgoing Serial TelecomBus

Figure 34 shows the timing relationships around the OJ0REF signal. The Outgoing Memory Page selection signal (OCMP) is only valid at the SYSCLK cycle which OJ0REF is asserted. The Transmit J0 Frame Pulse (TJ0FP) signal indicates the approximate time at which the J0 byte is available on the Serial TelecomBus LVDS links. The TJ0FP signal is asserted approximately 8 clock cycles after OJ0REF is asserted. For Figure 34 OJ0REFDLY[13:0] is set to all zeros.

Figure 34 Outgoing Serial TelecomBus



15.7 ATM UTOPIA Level 3 System Interface

The ATM UTOPIA Level 3 System Interface is compatible with the UTOPIA Level 3 specification. The S/UNI-MACH48 only supports the 32-bit mode of operation and PHY addresses (channels) from 0 to 47.

15.7.1 Transmit UL3 Interface

The Transmit UTOPIA Level 3 System Interface Timing diagrams (Figure 35 and Figure 36) illustrate the operation of the system side transmit UL3 interface. The single PHY case shown in Figure 35 illustrates the behavior of the TCA signal. At the start of cycle 4, there is only enough FIFO buffer space for the cell being transferred so TCA is deasserted. The deassertion occurs on the TFCLK edge **after** TSOC of the cell (cell#1) being written to the FIFO is sampled. This cell will take the last remaining cell buffer space in the FIFO. This TCA behavior is consistent with the Utopia L3 specification which states that TCA is invalid on the TFCLK edge that initiates the transition of TSOC to logic 1.

On cycle 5, a cell has been read out of the FIFO to the S/UNI-MACH48 core so it now has room to accommodate the cell currently being transferred (cell#1) plus one additional cell (cell#2). At the start of cycle 8, the transfer of cell#1 is completed. TCA remains high because there is still buffer space for one more cell. At the start of cycle 10, transfer of cell#2 starts. TCA is deasserted at cycle 11 because besides the space for holding cell#2, there is no FIFO space for any more cells.

TCA will be deasserted for polling cycles during the first three cycles of a cell transfer for the phy being transferred. That is, for cycles 3, 4 and 5 the phy currently transferring a cell will say it has no more room even if it does. This prevents a false positive on TCA before the FIFO fill level can be re-evaluated.

Note that the single-PHY mode is handled exactly like the multi-PHY mode except that the PHY address is held at the value 0. If TENB is held low, back-to-back cell transfers on the same PHY can be performed without a dead cycle.

TSOC must be high during the first byte of the ATM cell structure and must be present for the start of each cell. Thus, TSOC will mark the H1 byte. If TSOC is asserted at the wrong time (not at proper cell boundaries), a corrupted (but complete) cell will be transmitted from the S/UNI-MACH48. This corrupted cell will contain the bytes from the runt cell transferred through the UL3 interface plus some random bytes to fill the remainder of the ATM cell.

The multi-PHY timing diagram of Figure 36 shows the TCA polling mechanism. The buffer available status is given on the next rising TFCLK edge after the address on TADR[5:0] is sampled. Also shown is how different PHYs are selected for data transfer. When TENB is logic 1, the address on TADR[5:0] is selected as the PHY for the next transfer once TENB returns to logic 0.

Figure 35 Transmit UTOPIA Level 3 System Interface Timing for Single PHY

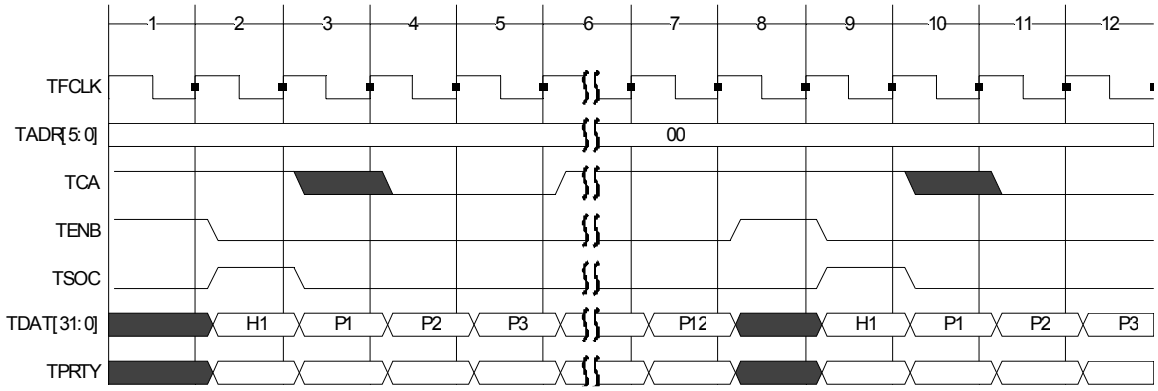
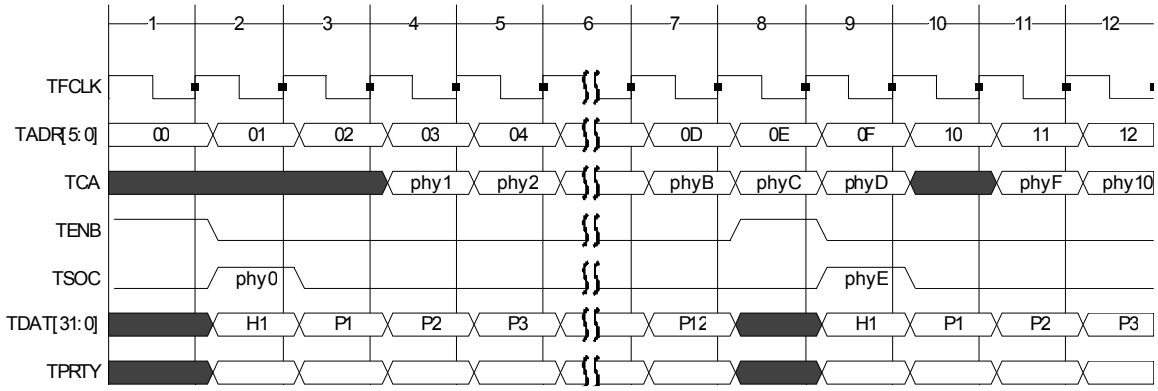


Figure 36 Transmit UTOPIA Level 3 System Interface Timing for Multi-PHY



15.7.2 Receive UL3 Interface

The Receive UTOPIA Level 3 System Interface Timing diagrams (Figure 37 and Figure 38) illustrate the operation of the system side receive interface.

The single PHY case shown in Figure 37 illustrates the behavior of the RCA signal. At the start cycle 3, RENB is sampled low which initiates a cell transfer from the S/UNI-MACH48. The transfer begins at cycle 4. The response to RENB always occurs on the rising RFCLK edge following the RFCLK edge which samples RENB. Also note that RENB must remain asserted during a cell transfer as specified by the Utopia L3 standard. In Figure 37, this occurs on the rising edge of RFCLK at the start of cycle 9.

RCA is deasserted in cycle 4 and 11 coincident with the RSOC assertion indicating that the cell transfer which has just started contains the last cell in the FIFO at this time. RCA may be asserted at any time due to the insertion of a complete cell into the FIFO.

RCA will be deasserted for polling cycles during the first two cycles of a cell transfer for the phy being transferred. That is, for cycles 4 and 5 the phy currently transferring a cell will say it has no more data even if it does. This prevents a false positive on RCA before the FIFO fill level can be re-evaluated.

Back-to-back cells from the same PHY can be handled by holding RENB asserted at logic 0 during cycle 8. In this case, cycle 10 for RSOC, RDAT[31:0], and RPRTY will be eliminated and the following cycles will be advanced. Otherwise, the single-PHY mode is handled exactly like the multi-PHY mode except that the PHY address is held at the value 0.

The multi-PHY timing diagram of Figure 38 shows the RCA polling mechanism. The data available status is given on the next rising RFCLK edge after the address on RADR[5:0] is sampled. Also shown is how different PHYs are selected for data transfer. When RENB is logic 1, the address on RADR[5:0] is selected as the PHY for the next transfer once RENB returns to logic 0.

Figure 37 Receive UTOPIA Level 3 System Interface Timing for Single PHY

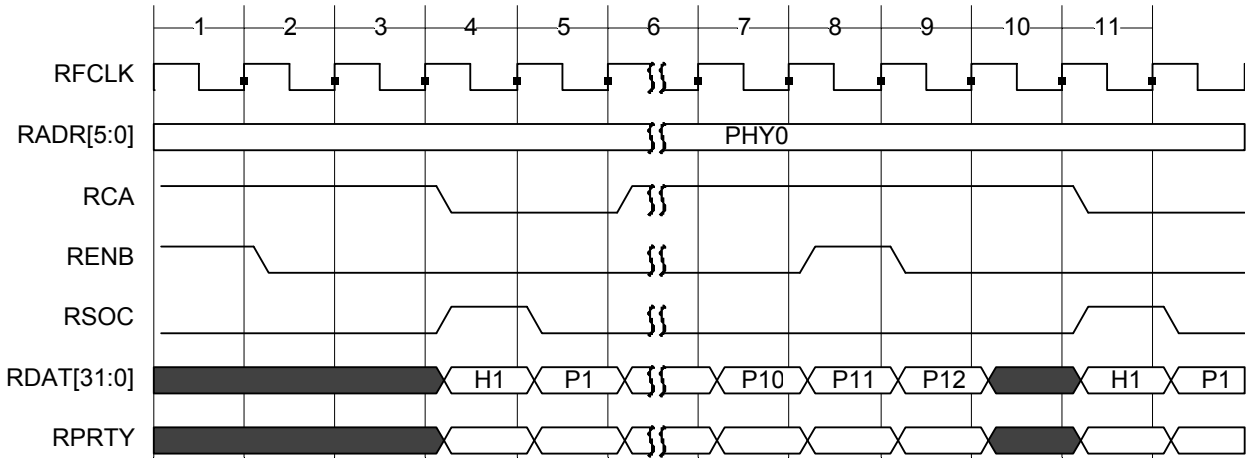
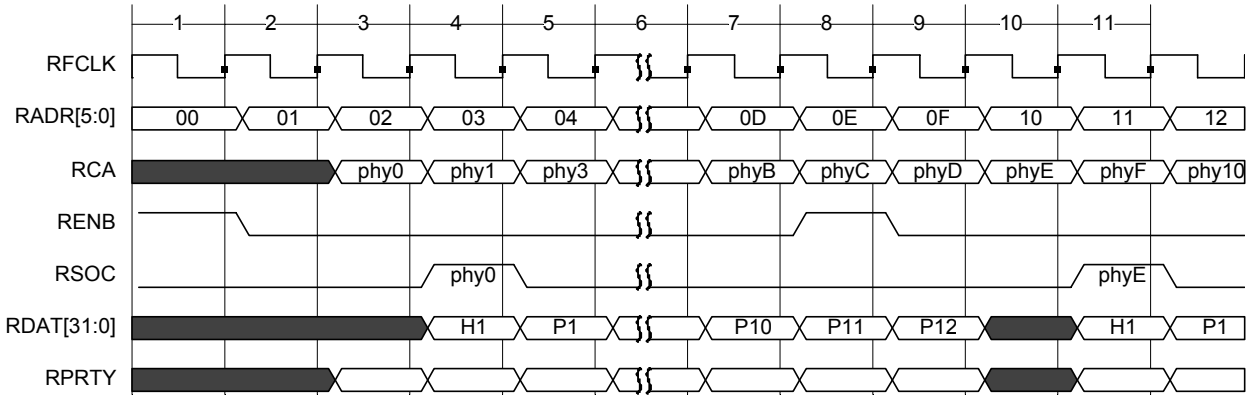


Figure 38 Receive UTOPIA Level 3 System Interface Timing for Multi-PHY



15.8 Packet over SONET (POS) Level 3 System Interface

The Packet over SONET (POS) Level 3 System Interface is compatible with the POS-PHY Level 3 specification. The S/UNI-MACH48 only supports the 32-bit mode of operation.

15.8.1 Transmit PL3 Interface

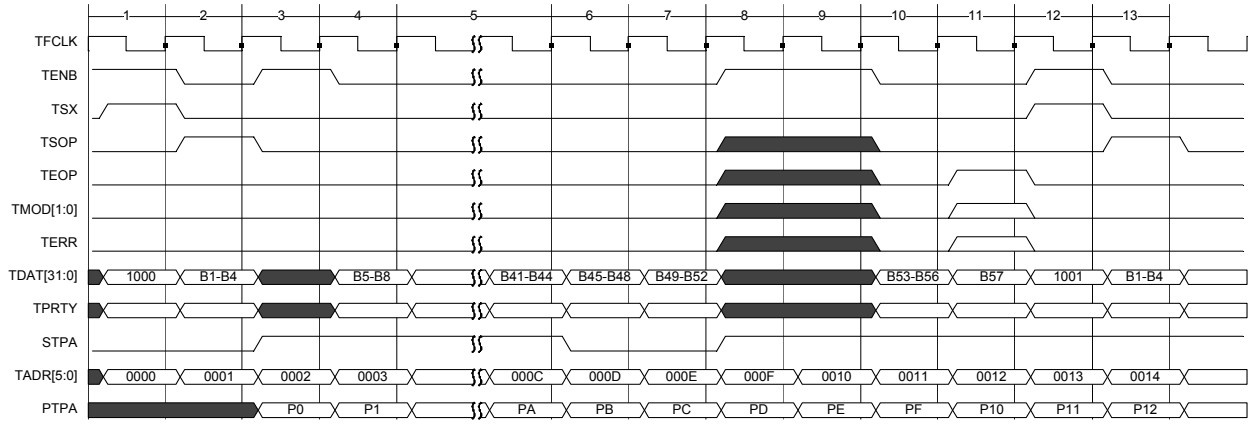
The Transmit POS Level 3 System Interface Timing diagram (Figure 39) illustrates the operation of the system side transmit FIFO interface. TENB, TSX, and TDAT[31:0] (because TSX is logic 1, TDAT[31:24] contains the Data Type Field - see register 004BH, TDAT[7:0] contains the in-band PHY address) are asserted in cycle 1 to start the transfer. STPA responds in cycle 3 to show that there is room in the FIFO (the FIFO fill threshold is user programmable) for PHY address 0. The packet data is transferred on TDAT[31:0] starting at the rising TFCLK edge at the start of cycle 3. TSOP is also asserted at this cycle to indicate the data on TDAT[31:24] contains the start-of-packet byte. TENB is deasserted in cycle 3 by the upstream device to pause the transfer. Data transfer continues in cycle 4. In cycle 6, STPA is deasserted indicating that the FIFO for PHY address 0 has fallen below the data available threshold (TXSDQ's BT[4:0] register bits). In the example shown here, the upstream device responds by stopping its transfer immediately at cycle 9 by deasserting TENB. With most set-up configurations, the upstream device does not need to stop immediately. It can complete the transfer of one more burst before stopping.

Because STPA is asserted again on cycle 8, transfers can be conducted again. TENB is asserted again before cycle 11 to continue the transfer. In cycle 11, TEOP is asserted to indicate that TDAT[31:0] contains one byte which is the end of the packet. TMOD[1:0] is valid at the same time to indicate which bytes in TDAT[31:0] contain valid data and thus the last byte of the packet can be inferred. TERR is also valid during this cycle to indicate whether or not this packet should be aborted because of an upstream error. If TERR is logic 1, the packet will be aborted by the S/UNI-MACH48's packet processor.

In cycle 12, TENB is deasserted and TSX is asserted to select a different PHY to transfer data to.

TSOP must be high during transfers which contain the first byte of a packet. TEOP must be high during transfers which contain the last byte of a packet. It is legal to assert TSOP and TEOP at the same time. This case occurs when TDAT[31:0] contain both the SOP and EOP. When TSOP is asserted and the previous transfer was not marked with TEOP, the system interface realigns itself to the new timing, and both the previous packet and the current packet may be corrupted and aborted.

Figure 39 Transmit POS Level 3 System Interface Timing



15.8.2 Transmit PL3 STPA and PTPA Behavior

The STPA signal gives the status of the FIFO which is being filled by the transmit PL3 interface. STPA is used for "word transfer mode" in the PL3 specification, and it is recommended only for use in single phy configurations. PTPA can also give this status, but it must be polled for the desired channel. PTPA is used for "burst transfer mode" in the PL3 specification, and is recommended for multi-phy configurations. The following discussion revolves around STPA, but also applies to PTPA if the corresponding channel is polled (presented on the TADR pins).

When STPA is logic 1, it indicates that the FIFO has enough room to absorb a pre-determined number of data transfers. Once the FIFO threshold has been exceeded, meaning that the FIFO can no longer absorb the pre-determined number of data transfers, then STPA will transition to logic 0.

The following diagrams show the behavior of STPA when the FIFO threshold is reached. It is critical that the upstream device respond properly in order to avoid any FIFO overflows in the TXSDQ.

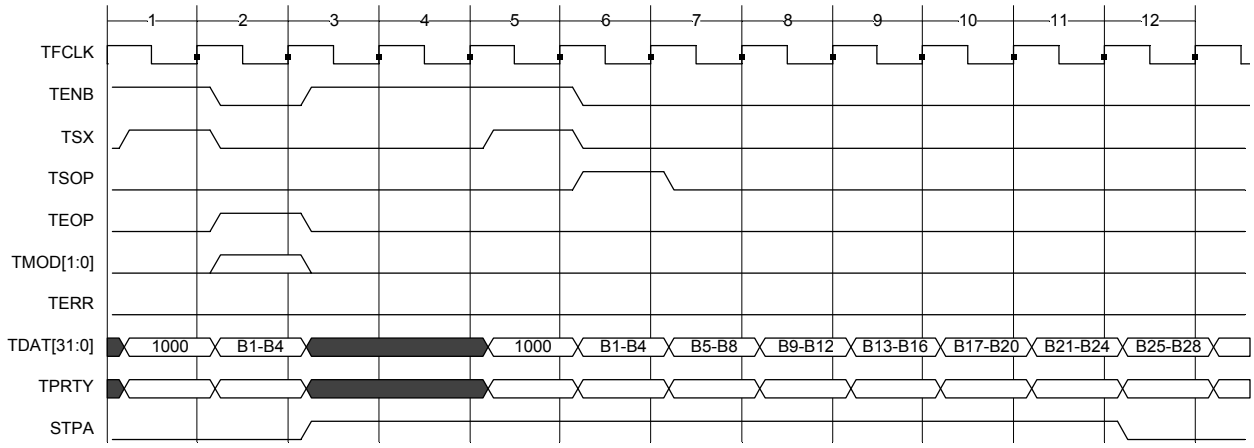
There are two basic methods of transferring data across the PL3 interface: burst-transfer mode, and word-transfer mode. Burst-transfer mode is similar to the UL3 interface. Where the UL3 interface will transfer one cell at a time, the PL3 interface will transfer a maximum number of bytes or end at an end-of-packet indication in one burst, whichever comes first. Polling the TPA signal will give the status of the FIFO for the next burst (with some latency) just like UL3's TCA indication. Setting TPAHOLD (register 0048H TXPHY Configuration) to logic 1 will configure the S/UNI-MACH48 to burst-transfer mode.

Word-transfer mode has no such limitations. The upstream device is expected to watch the PTPA signal to find when it can begin a transfer to a particular PHY channel. Once the transfer is started, it must observe the STPA signal and pause when required to prevent oveflowing the FIFO. Setting TPAHOLD to logic 0 will configure the S/UNI-MACH48 to word-transfer mode or hybrid word/burst-transfer mode.

TPAHOLD = 0

Figure 40 shows the behavior of STPA when the TPAHOLD register bit (in register 0048H TXPHY Configuration) is set to logic 0. This is the default operating mode. In this example, the write to the FIFO which occurs at the start of cycle 7 crosses the TXSDQ's BT[4:0] threshold. STPA responds on cycle 12. There is a 5 clock cycle delay between the write and the response on STPA.

Figure 40 TPAHOLD Set to 0



This 5 cycle delay can be dealt with in 2 ways. First, the upstream device can be programmed to wait for the response before sampling the new TPA status. For small transfers, this may affect the net throughput possible on the PL3 bus. For this case, the TXSDQ buffer threshold can be set equal or greater than the PL3 burst-size of the upstream device.

BT[4:0] ≥ burst-size – 1

Where burst-size is in units of blocks (1 block = 16 bytes).

Second, if the upstream device cannot account for the STPA delay or maximum throughput is desired on the PL3 bus, the TXSDQ's buffer threshold must be set to guarantee that any transfers which occur during the 5 cycle delay do not cause any overflows. To do this, the value of the TXSDQ's buffer threshold may need to be increased. It can be calculated by using the following equation:
BT[4:0] ≥ 1 + (num_min_pack * min_pack_size_in_blocks) + remainder – 1

Where:

Let m = minimum packet size

Let s = upstream device's response time to STPA (# of clocks after STPA for transfer to stop)

Let ovrhd_cycles = number of non-packet payload cycles per transfer (TSX cycle is usually 1, each guaranteed null cycle introduced by the upstream device counts as 1)

num_min_pack = downround ((5 + s - 1) / (m + ovrhd_cycles))

min_pack_size_in_blocks = upround (m / 4)

remainder = upround (((5 + s - 1) mod m) / 4)

Explanation:

The STPA and PTPA is late by 5 clocks and the link layer device takes s number of clocks after STPA to stop transfer, resulting in 5 + s words that can be written after the threshold gets exceeded.

- the '1' is to deal with the worst case where the threshold gets exceeded during the write of the final word of a packet whose size is one block greater than a multiple of 4 (eg. the EOP word of a 13 word packet, as this word wastes a whole block by itself).
- num_min_pack is the number of full minimum-sized packets that can be written during the 5 + s - 1 clocks. (The subtraction of 1 refers to the EOP word corresponding to point i)

eg. if s = 2, m = 5, ovrhd_cycles = 0,

num_min_pack = downround((5+2-1) / (5+0)) = 1.

That is, in those 6 clocks, there could be one full min-size packet that can be written

- min_pack_size_in_blocks is the number of blocks occupied by a minimum-sized packet.

eg. **if m = 5 clocks cycles, then min_pack_size_in_blocks is 2.**

- remainder refers to how many blocks of a partial packet gets written after the minimum-sized packets had been written. (5 + s – 1)mod m is a calculation of how many words are contained in the final partial packet. The number of blocks occupied is simply that value divided by 4 rounded up.
- the '-1' at the end of the equation refers to the fact that BT in the SDQ is one less than what's required.

Examples:

s = 2 (7 clock latency for response to STPA)

m = 1 (min 4-byte packet)

ovrhd_cycles = 0 (4 byte packet, no TSX cycle guaranteed between each packet/burst)

num_min_pack = downround ((5+2-1)/(1+0)) = 6

min_pack_size_in_blocks = upround(1/4) = 1

remainder = upround (((5+2-1)mod1)/4) = 0

BT[4:0] ≥ 1 + (6*1) + 0 – 1 = 6

s = 2 (7 clock latency for response to STPA)

m = 1 (min 4-byte packet)

ovrhd_cycles = 1 (4 byte packet, 1 TSX cycle guaranteed between each packet/burst)

num_min_pack = downround ((5+2-1)/(1+1)) = 3

min_pack_size_in_blocks = uproundround(1/4) = 1

remainder = uproundround (((5+2-1)mod1)/4) = 0

BT[4:0] ≥ 1 + (3*1) + 0 – 1 = 3

s= 2 (7 clock latency for response to STPA)

m = 13 (atm cell)

ovrhd_cycles = 0 (no TSX cycle or null cycles)

num_min_pack = downround ((5+2-1)/(13+0)) = 0

min_pack_size_in_blocks = uproundround(13/4) = 4

remainder = uproundround (((5+2-1)mod13)/4) = 2

BT[4:0] ≥ 1 + (0*4) + 2 – 1 = 2

This mode is practical for FIFO sizes equal to 48 or 192 blocks (STS-3c, STS-12c, and STS-48c sized FIFOs). It may not be practical for FIFO sizes of 16 blocks (DS3 and STS-1 sized FIFOs) because it will cause the FIFO to be under-utilized except in the condition when many consecutive small packets are transferred. The under-utilized space is constant regardless of FIFO size and will thus consume a larger percentage of the space of a small FIFO than of a large FIFO. (see Section 14.15 for restrictions on the relationship between TXSDQ's DT[7:0] and BT[4:0]).

For the optional PL3 mode where each burst is not terminated by a TENB transition to logic 1, TPAHOLD must be set to logic 0.

TPAHOLD = 1

Figure 41 shows the behavior of PTPA when the TPAHOLD register bit (in register 0048H TXPHY Configuration) is set to logic 1. This is the optional operating mode which decreases the TPA response delay from 5 cycles to 1 cycle. This optional mode is only usable when each burst is terminated by a TENB transition to logic 1. Because the PL3 interface is used in "burst-transfer mode", the STPA signal should not be used. Once a burst has been allowed by polling PTPA at logic 1, then one full burst is allowed. PTPA must be polled at logic 1 again before another burst can be started. It is envisioned that this mode will be used for multi-PHY configurations which have STS-1 or DS3 channels since it allows optimal usage of the smaller 256-byte FIFOs.

In this example, the write to the FIFO which occurs at the start of cycle 7 crosses the TXSDQ's BT[4:0] threshold. PTPA responds on cycle 8. There is a 1 clock cycle delay between the write and the response on PTPA.

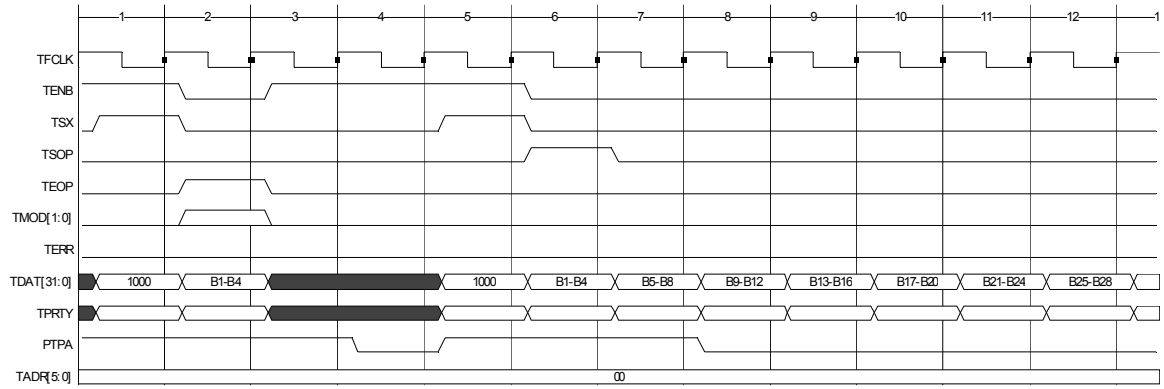
The TXSDQ's FIFO threshold must be set-up differently. For this mode to operate correctly, BT[4:0] = 2*burst-size – 1

Where burst-size is in units of blocks (1 block = 16 bytes).

While the TXSDQ's FIFO threshold is set so it transitions when less than 2 bursts remain available, the TPAHOLD feature will hold PTPA high until there is less than 1 burst available. Thus, the user can still fully utilize the entire FIFO.

Because we usually want the TXSDQ's data threshold (DT[7:0]) to be a fairly large value to prevent FIFO underruns, the burst-size must be set to a reasonable value (see Section 14.15 for restrictions on the relationship between TXSDQ's DT[7:0] and BT[4:0]). For the minimum FIFO size of 16 blocks, the burst-size cannot be larger than 64 bytes.

Figure 41 TPAHOLD Set to 1



15.8.3 Receive PL3 Interface

The Receive POS Level 3 System Interface Timing diagram (Figure 42) illustrates the operation of the system side receive interface. The SUNI-MACH48 performs the polling operation internally, selects the PHY for which data is to be transferred, and pushes data to the downstream reader.

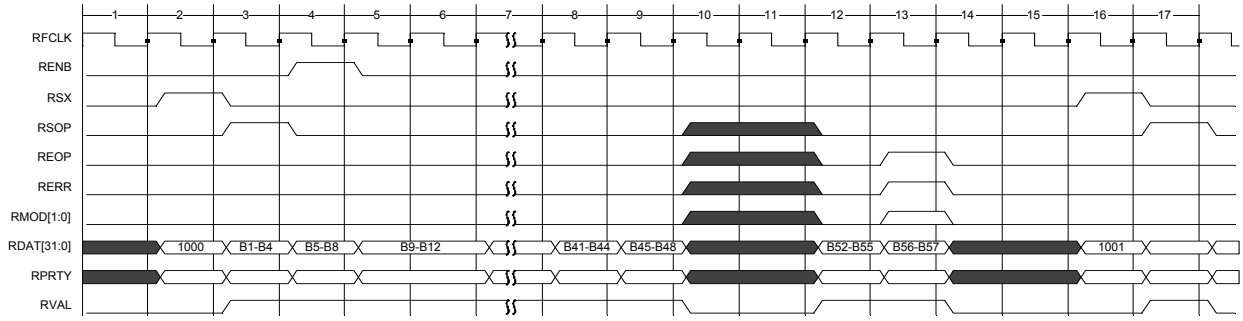
When data is available, the RVAL signal is asserted. RSX is also asserted in cycle 2 to indicate that the PHY address for which data is being transferred is present on RDAT[7:0]. RDAT[31:24] holds the Data Type Field (see register 0046H). At cycle 3, RSOP is asserted to indicate that the RDAT[31:24] contains the first byte of a packet. RENB is deasserted in cycle 4 because the downstream device wants to pause the data transfer.

Data transfer continues until cycle 10 when RVAL is deasserted. At cycle 12 and 13, the last two transfers for the packet are performed. In cycle 13, REOP signals the last byte of the packet is contained in RDAT[31:0] and the value of RMOD[1:0] indicates which bytes in RDAT[31:0] contain valid data. RERR is asserted along with REOP if errors were detected in this packet (aborted, length violation, FIFO overrun, FCS errors) so the downstream device may discard the packet. In cycle 16, a new transfer is initiated by reasserting RSX and a new PHY address and data type on RDAT[7:0] and RDAT[31:24] respectively.

The burst length of any transfer can be limited by setting the RXPHY's BURST_SIZE[7:0] register bits. The polling algorithm used for selecting the order in which data from different PHYs are transferred is completely user programmable using the CALENDAR_LENGTH[6:0], CALENDAR_ADDR[6:0] and CALENDAR_DATA[5:0] register bits of the RXPHY.

The FIFO threshold at which data transfer begins is set by the RXSDQ's DT[7:0] register bits. ATM cells can be transferred through the PL3 interface as fixed length packets. The DT[7:0] value should be set so that only complete ATM cells are transferred.

Figure 42 Receive POS Level 3 System Interface Timing



16 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 65 Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.3V to +4.6V
Voltage on Any Digital Pin	-0.3V to V_{VDDO}+0.3V
Voltage on LVDS Pin	-0.5V to Avdh+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA except RESK and LVDS pins
Latch-Up Current on LVDS pins	±90 mA
Latch-Up Current on RESK pin	±50 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C
Maximum Overshoot on Output pins *	-2.0 V to VDD+2.0V for 10ns, 20mA max (for pc3t10 pad)
Input pad overshoot tolerance	-2V < VDDO < +2V for 10ns, 100mA max

* Most output pins require termination circuitry.

17 D.C. Characteristics

T_A = -40°C to T_J =+125°C, V_{VDDI} = $VDDI_{typical}$ ± 5%, V_{VDDO} = $VDDO_{typical}$ ± 5%
(Typical Conditions: T_A = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V, V_{AVDH} = 3.3V)

Table 66 D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VVDDI	Power Supply	1.71	1.8	1.89	Volts	
VVDDO	Power Supply	3.13	3.3	3.47	Volts	
VAVDL	Power Supply	1.71	1.8	1.89	Volts	
VAVDH	Power Supply	3.13	3.3	3.47	Volts	
VIL	Input Low Voltage			0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.1	0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	VDDO – 0.2		Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.2			Volts	Applies to RSTB,TRSTB, SYSCLK, DS3TICLK, RFCLK and TFCLK only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB,TRSTB, SYSCLK, DS3TICLK, RFCLK and TFCLK only.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB and TRSTB only.
I_{ILPU}	Input Low Current	-200	-50	-10	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 2 and 3.
V_{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity			100	mV	
R_{IN}	LVDS Differential Input Impedance	85	100	115	Ω	
V_{LOH}	LVDS Output voltage high		1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025		mV	R_{LOAD}=100Ω ±1%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	85	110	115	Ω	
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I_{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

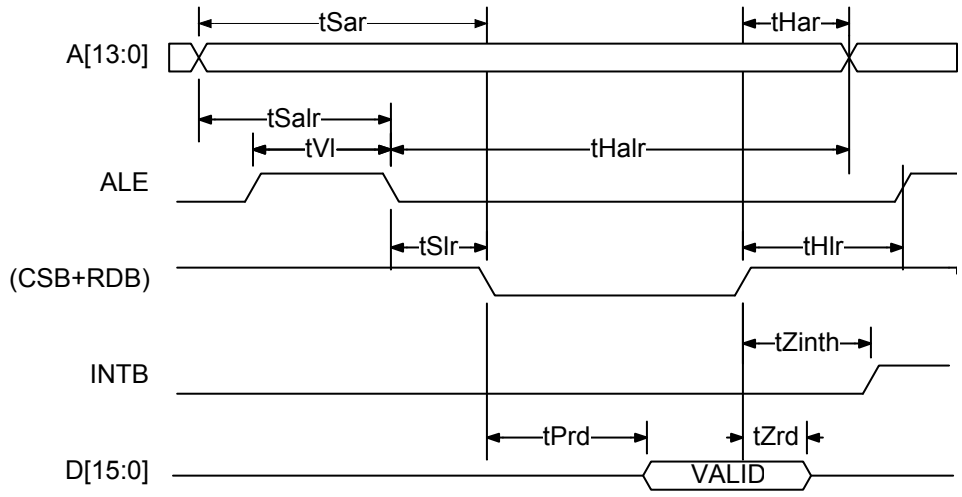
18 Microprocessor Interface Timing Characteristics

(T_A=-40°C to T_J=+125°C, V_{VDDI} = $VDDI_{typical}$ ± 5%, V_{VDDO} = $VDDO_{typical}$ ± 5%)

Table 67 Microprocessor Interface Read Access (Figure 43)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	10		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	10		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB High		50	ns

Figure 43 Intel Microprocessor Interface Read Timing



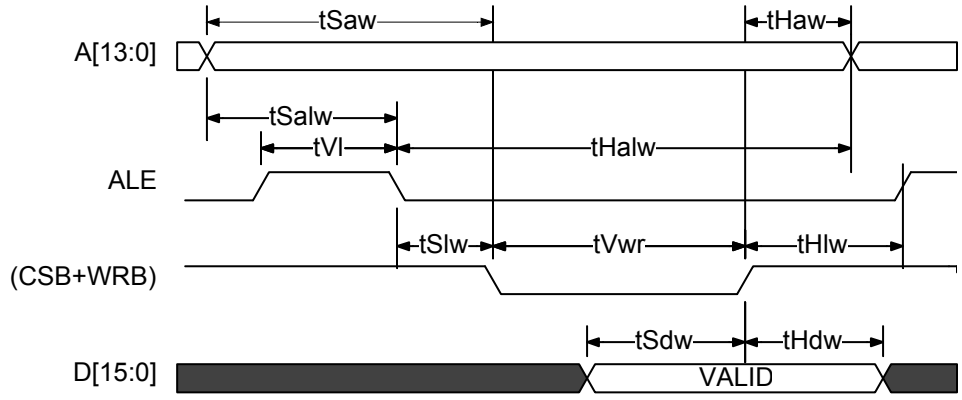
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]) and 50 pF load on INTB.
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_{L}, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 68 Microprocessor Interface Write Access (Figure 44)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	10		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	10		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 44 Intel Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

19 A.C. Timing Characteristics

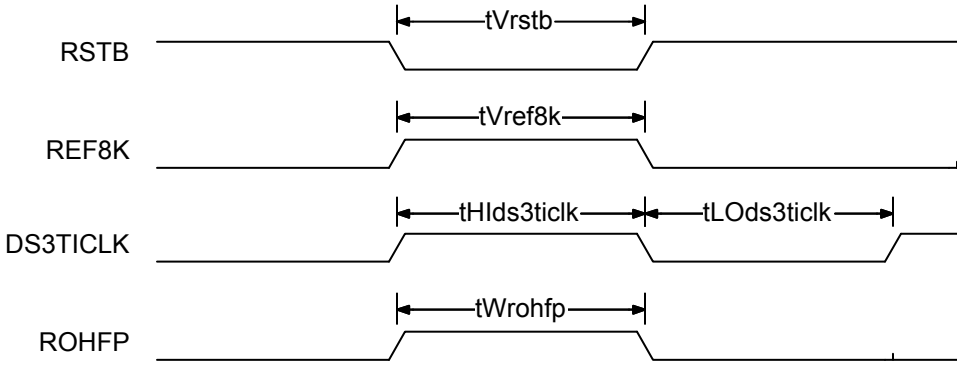
(T_A=-40°C to T_J=+125°C, V_{VDDI} = $VDDI_{typical}$ ± 5%, V_{VDDO} = $VDDO_{typical}$ ± 5%)

19.1 System Miscellaneous Timing

Table 69 System Miscellaneous Timing (Figure 45)

Symbol	Description	Min	Max	Units
t^{V}RSTB	RSTB input pulse width	100		ns
t^{V}REF8K	REF8K input pulse width	10		ns
t^{F}DS3TICLK	DS3TICLK frequency	44.3	44.87	MHz
t^{HI}DS3TICLK	DS3TICLK input hi pulse width	7		ns
t^{LO}DS3TICLK	DS3TICLK input low pulse width	7		ns
t^{W}ROHFP	ROHFP output pulse width	15	400	ns

Figure 45 System Miscellaneous Timing Diagram



19.2 System Interface Timing

Table 70 Receive System Interface Timing (Figure 46)

Symbol	Parameter	Min	Max	Units
fRFCLK	RFCLK Frequency	60	104	MHz
tHIRFCLK	RFCLK HI Pulse Width	3.85		ns
tLORFCLK	RFCLK LO pulse Width	3.85		ns
tS_{RADR}	RADR[5:0] Set-up time to RFCLK	2		ns
tH_{RADR}	RADR[5:0] Hold time to RFCLK	0.5		ns
tS_{RENB}	RENB Set-up time to RFCLK	2		ns
tH_{RENB}	RENB Hold time to RFCLK	0.5		ns
tPRVAL	RFCLK High to RCA/RVAL Valid	1.5	6	ns
tPRSOP	RFCLK High to RSOC/RSOP Valid	1.5	6	ns
tPREOP	RFCLK High to REOP Valid	1.5	6	ns
tPRPRTY	RFCLK High to RPRTY Valid	1.5	6	ns
tPRERR	RFCLK High to RERR Valid	1.5	6	ns
tPRSX	RFCLK High to RSX Valid	1.5	6	ns
tPRDAT	RFCLK High to RDAT[31:0] Valid	1.5	6	ns
tPRMOD	RFCLK High to RMOD[1:0] Valid	1.5	6	ns

Figure 46 Receive System Interface Timing Diagram

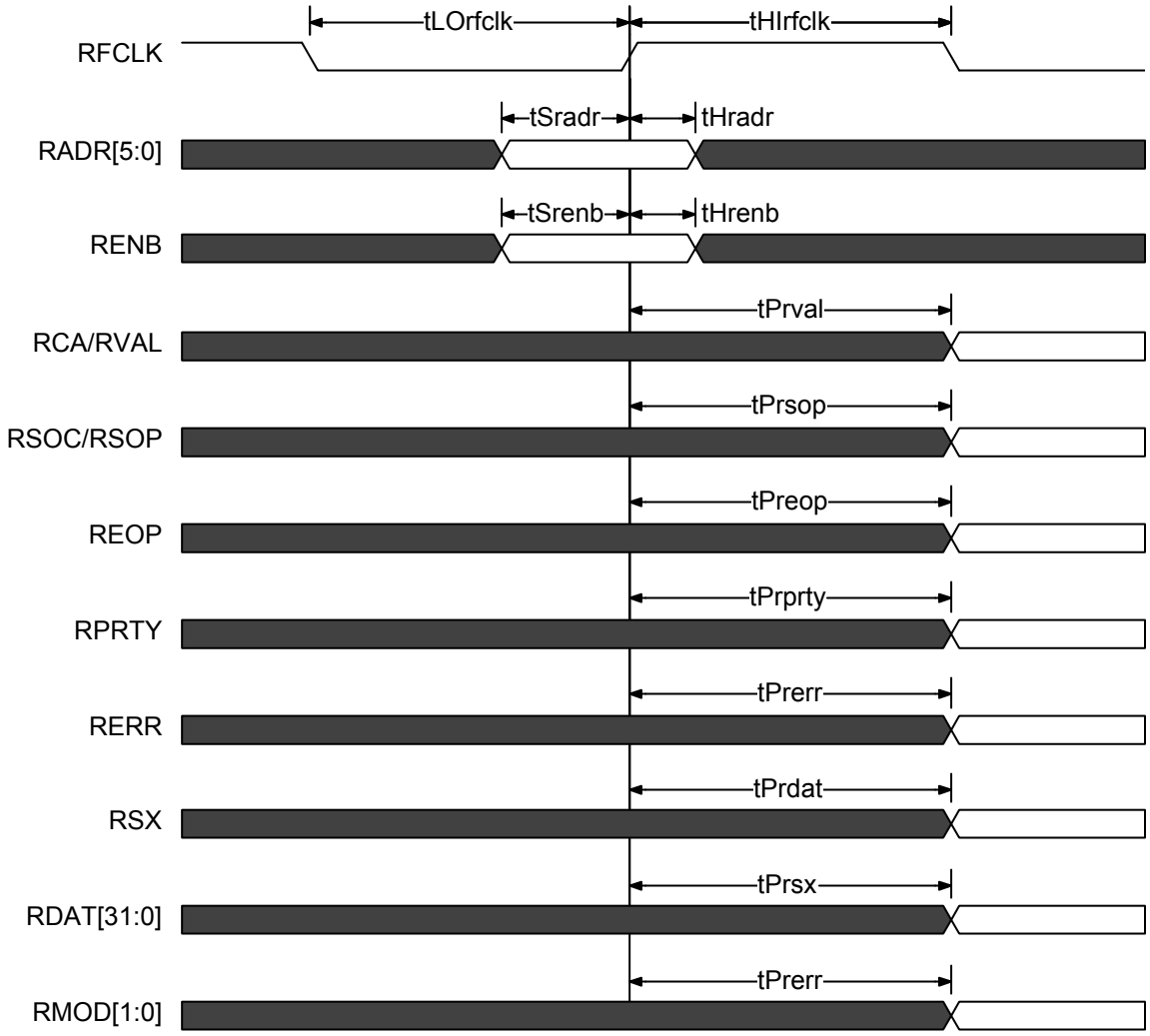
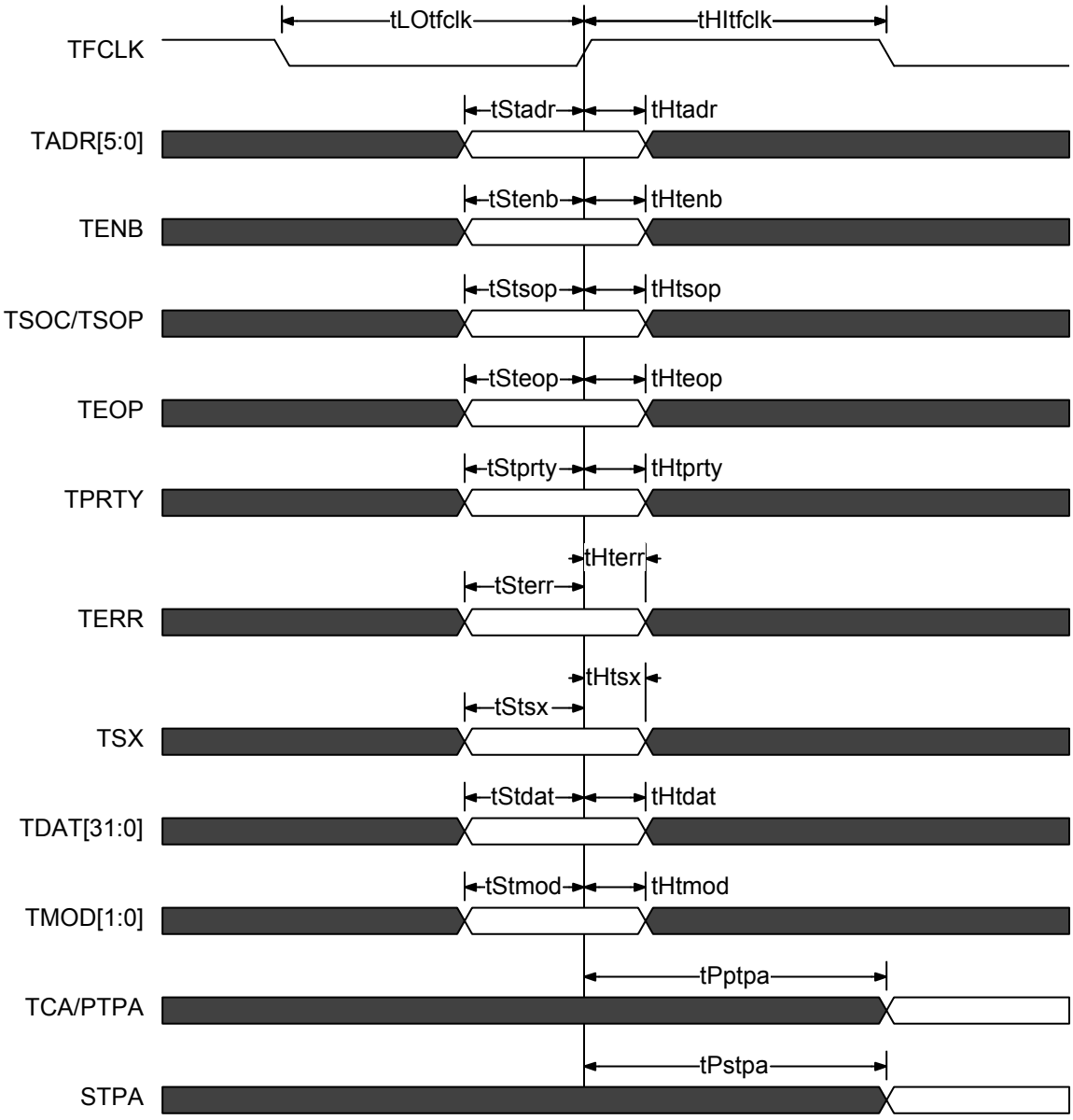


Table 71 Transmit System Interface Timing (Figure 47)

Symbol	Parameter	Min	Max	Units
fTFCLK	TFCLK Frequency	60	104	MHz
tHITFCLK	TFCLK HI Pulse Width	3.85		ns
tLOTFCLK	TFCLK LO pulse Width	3.85		ns
tS_{TADR}	TADR[5:0] Set-up time to TFCLK	2		ns
tH_{TADR}	TADR[5:0] Hold time to TFCLK	0.5		ns
tS_{TENB}	TENB Set-up time to TFCLK	2		ns

Symbol	Parameter	Min	Max	Units
tHTENB	TENB Hold time to TFCLK	0.5		ns
tSTSOP	TSOC/TSOP Set-up time to TFCLK	2		ns
tHTSOP	TSOC/TSOP Hold time to TFCLK	0.5		ns
tSTEOP	TEOP Set-up time to TFCLK	2		ns
tHTEOP	TEOP Hold time to TFCLK	0.5		ns
tSTPRTY	TPRTY Set-up time to TFCLK	2		ns
tHTPRTY	TPRTY Hold time to TFCLK	0.5		ns
tSTERR	TERR Set-up time to TFCLK	2		ns
tHTERR	TERR Hold time to TFCLK	0.5		ns
tSTSX	TSX Set-up time to TFCLK	2		ns
tHTSX	TSX Hold time to TFCLK	0.5		ns
tSTDAT	TDAT[31:0] Set-up time to TFCLK	2		ns
tHTDAT	TDAT[31:0] Hold time to TFCLK	0.5		ns
tSTMOD	TMOD[1:0] Set-up time to TFCLK	2		ns
tHTMOD	TMOD[1:0] Hold time to TFCLK	0.5		ns
tP_{TPA}	TFCLK High to TCA/PTPA Valid	1.5	6	ns
tP_{STPA}	TFCLK High to STPA Valid	1.5	6	ns

Figure 47 Transmit System Interface Timing



19.3 Line Interface Timing

Table 72 SYSCLK Input Timing (Figure 48)

Symbol	Description	Min	Max	Units
fSYSCLK	SYSCLK Frequency (nominally 77.76MHz)	77	78	MHz
tHISYSCLK	SYSCLK Hi Pulse Width	5		ns
tLOSYSCLK	SYSCLK Low Pulse Width	5		ns
tJITSYSCLK	SYSCLK Peak-to-peak Jitter		50	ps
tS_{IJ0J1}	IJ0J1[4:1] Set-up time to SYSCLK	3		ns
tH_{IJ0J1}	IJ0J1[4:1] Hold time to SYSCLK	0		ns
tS_{IDP}	IDP[4:1] Set-up time to SYSCLK	3		ns
tH_{IDP}	IDP[4:1] Hold time to SYSCLK	0		ns
tS_{ID}	ID[4:1][7:0] Set-up time to SYSCLK	3		ns
tH_{ID}	ID[4:1][7:0] Hold time to SYSCLK	0		ns
tS_{IPL}	IPL[4:1] Set-up time to SYSCLK	3		ns
tH_{IPL}	IPL[4:1] Hold time to SYSCLK	0		ns
tS_{IPAIS}	IPAIS[4:1] Set-up time to SYSCLK	3		ns
tH_{IPAIS}	IPAIS[4:1] Hold time to SYSCLK	0		ns
tS_{OJ0REF}	OJ0REF Set-up time to SYSCLK	3		ns
tH_{OJ0REF}	OJ0REF Hold time to SYSCLK	0		ns
tS_{ICMP}	ICMP Set-up time to SYSCLK	3		ns
tH_{ICMP}	ICMP Hold time to SYSCLK	0		ns
tS_{OCMP}	OCMP Set-up time to SYSCLK	3		ns
tH_{OCMP}	OCMP Hold time to SYSCLK	0		ns
tSRWSEL	RWSEL Set-up time to SYSCLK	3		ns
tHRWSEL	RWSEL Hold time to SYSCLK	0		ns
tSRJ0FP	RJ0FP Set-up time to SYSCLK	3		ns
tHRJ0FP	RJ0FP Hold time to SYSCLK	0		ns
tSTOH	TOH Set-up time to SYSCLK	3		ns
tHTOH	TOH Hold time to SYSCLK	0		ns
tSTOHINS	TOHINS Set-up time to SYSCLK	3		ns
tHTOHINS	TOHINS Hold time to SYSCLK	0		ns

Figure 48 SYSCLK Input Timing

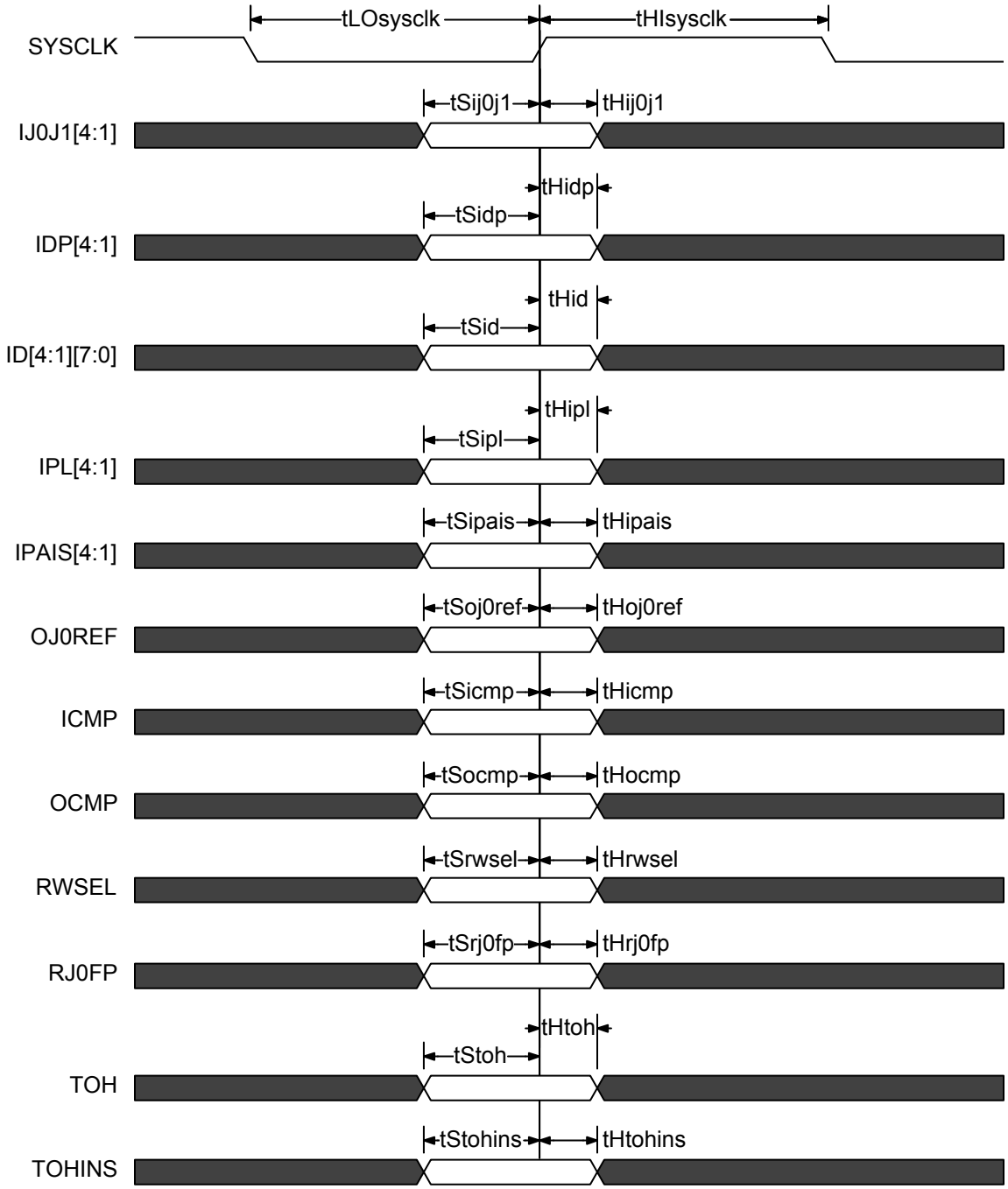
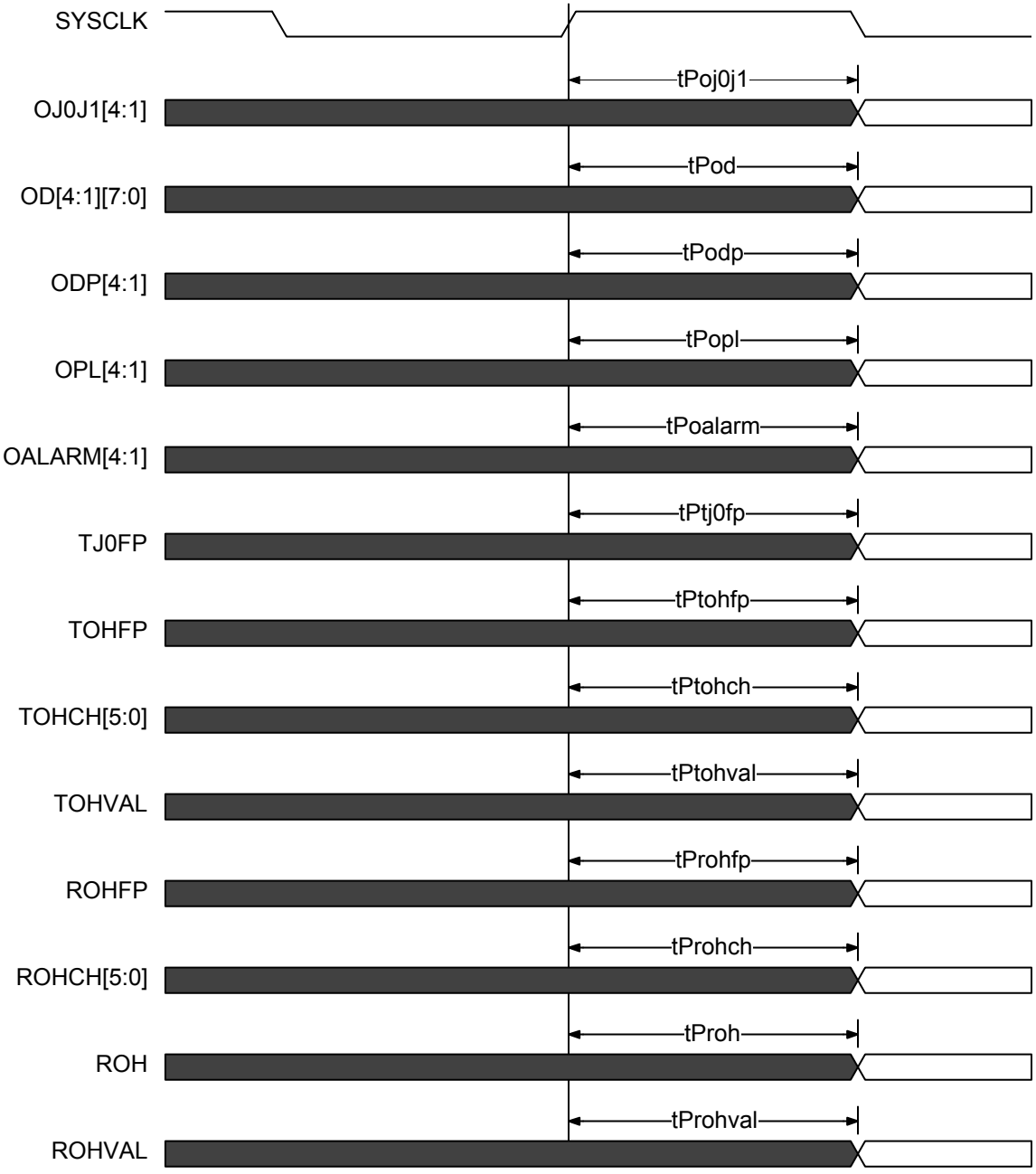


Table 73 SYSCLK Output Timing(Figure 49)

Symbol	Description	Min	Typ	Max	Units
tPOJ0J1	SYSCLK High to OJ0J1[4:1] valid	1		7	ns
tPOD	SYSCLK High to OD[4:1][7:0] valid	1		7	ns
tPODP	SYSCLK High to ODP[4:1] valid	1		7	ns
tPOPL	SYSCLK High to OPL[4:1] valid	1		7	ns
tPOALARM	SYSCLK High to OALARM[4:1] valid	1		7	ns
tPTJ0FP	SYSCLK High to TJ0FP valid		9		ns
tPTOHFP	SYSCLK High to TOHFP valid	1		7	ns
tPTOHCH	SYSCLK High to TOHCH[5:0] valid	1		7	ns
tPTOHVAL	SYSCLK High to TOHVAL valid	1		7	ns
tPROHFP	SYSCLK High to ROHFP valid	1		7	ns
tPROHCH	SYSCLK High to ROHCH[5:0] valid	1		7	ns
tPROH	SYSCLK High to ROH valid	1		7	ns
tPROHVAL	SYSCLK High to ROHVAL valid	1		7	ns

Figure 49 SYSCLK Output Timing



19.4 Serial TelecomBus Interface

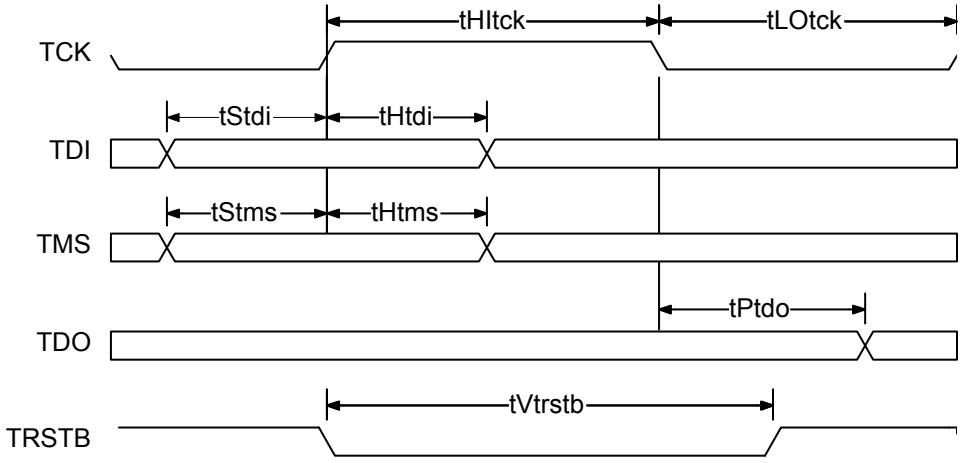
Symbol	Description	Min	Typical	Max	Units
^{f}RLVDS	RPWRK[4:1], RNWRK[4:1], RPPROT[4:1], RNPROT[4:1] Bit Rate	$10f_{SYSCLK}$ - 100ppm	$10f_{SYSCLK}$	$10f_{SYSCLK}$ - 100ppm	Mbps
^{t}FALL	V_{ODM} fall time, 80%-20%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
^{t}RISE	V_{ODM} rise time, 20%-80%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
^{t}SKEW	Differential Skew			50	ps

19.5 JTAG Test Port Timing

Table 74 JTAG Port Interface (Figure 50)

Symbol	Description	Min	Max	Units
fTCK	TCK Frequency		4	MHz
tHITCK	TCK HI Pulse Width	100		ns
tHITCK	TCK LO Pulse Width	100		ns
tSTMS	TMS Set-up time to TCK	25		ns
tHTMS	TMS Hold time to TCK	25		ns
tSTDI	TDI Set-up time to TCK	25		ns
tHTDI	TDI Hold time to TCK	25		ns
tPTDO	TCK Low to TDO Valid	2	25	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 50 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

3. Maximum output propagation delay on TDO is measured with a 50pF load.

20 Power Requirements

Table 75 Power Requirements

Conditions	Parameter	Typ1,3	High4	Max2	Units
DS3 disabled (all channels are STS1 rates or greater)	IDDOP vddo (3.3V)	0.28	0.321	0.355	A
	IDDOP vddi (1.8V)	1.29	1.490	1.667	A
DS3 enabled (DS3 channels are added into the mix above)	IDDOP vddo (3.3V)	0.303	0.350	0.390	A
	IDDOP vddi (1.8V)	1.553	1.760	1.964	A
Serial disabled	IDDOP avdh (3.3V)	0.014	0.020	0.026	A
	IDDOP avdl (1.8V)	0.027	0.031	0.034	A
Serial enabled	IDDOP avdh (3.3V)	0.106	0.113	0.120	A
	IDDOP avdl (1.8V)	0.137	0.159	0.186	A
Serial and DS3 enabled	Total Power	4.392	5.232		W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, Tj=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system.Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current.

2. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system.

3. High power values are a “normal high power” estimate, calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: Tj=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics.

4. Max power values are a “maximum high power” estimate, calculated in a similar manner to the High power values. IDDHigh values are calculated as the mean value plus six sigmas (6σ) of measured current under the same conditions as for the High power values.

21 Ordering And Thermal Information

Table 76 Ordering Information

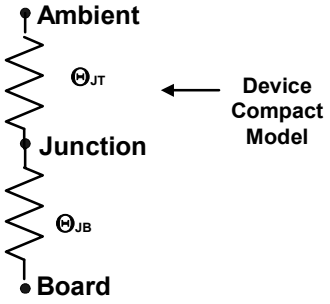
Part Number	Description
PM7390-BI	560-pin Ball Grid Array (UBGA)

This product is designed to operate over a wide temperature range and is suited for commercial applications such as central office equipment.

Maximum long-term operating junction temperature to ensure adequate long-term life	105 ^{0}C
Maximum junction temperature for short-term excursions with guaranteed continued functional performance.[1] This condition will typically be reached when local ambient reaches 70 Deg C.	125 ^{0}C
Minimum ambient temperature	-5 ^{0}C

Thermal Resistance vs Air Flow[2]			
Airflow	Natural Convection	200 LFM	400 LFM
Θ_{JA} (^{0}C/W)	8	6.7	6.3

Device Compact Model[3]	
Θ_{JT} (^{0}C/W)	0.1
Θ_{JB} (^{0}C/W)	# 4



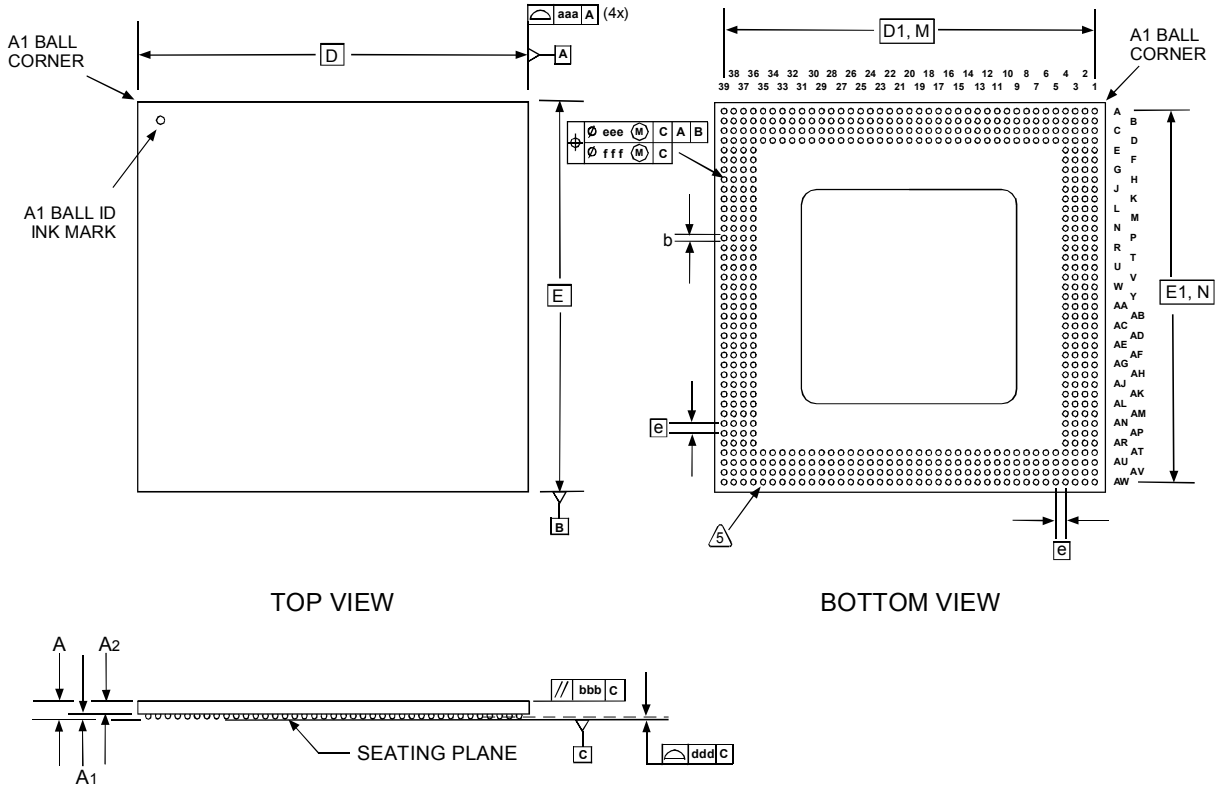
Operating power is dissipated in package (watts) at worst case power supply	
Power (watts)	5.5

Notes

1. Short-term is understood as the definition stated in Bellcore Generic Requirements GR-63-Core
2. Θ_{JA} , the total junction to ambient thermal resistance as measured according to JEDEC Standard JESD51 (2S2P)
3. Θ_{JB}, the junction-to-board thermal resistance and $\Theta_{JT,}$ the residual junction to ambient thermal resistance are obtained by simulating conditions described in JEDEC Standard, JESD 15-8

22 Mechanical Information

Figure 51 Mechanical Drawing 560 Pin Ultra Ball Grid Array (UBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) SOLDER MASK OPENING IS 0.45 +/- 0.025 MM DIAMETER (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MO-192, VARIATION AAU-1, BUT DOES NOT MEET eee.

PACKAGE TYPE : 560 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 40 x 40 x 1.47 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f	S
Min.	1.32	0.40	0.92	-	-	-	-	-	0.50	-	-	-	-	-	-	-
Nom.	1.47	0.50	0.97	40.00 BSC	38.00 BSC	40.00 BSC	38.00 BSC	39x39	0.63	1.00 BSC	-	-	-	-	-	-
Max.	1.62	0.60	1.02	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.30	0.10	-