PRELIMINARY
S/UNI-622-MAX
ERRATA
PMC-990340

PMC-Sierra, Inc.

ISSUE 2

PM5356 S/UNI-622-MAX

S/UNI-622-MAX REFERENCE DESIGN ERRATA

PM5356

S/UNI-622-MAX

SATURN
USER NETWORK INTERFACE
(622-MAX)

REFERENCE DESIGN ERRATA

PRELIMINARY

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PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	March 1999	Document created.
2	April 1999	Correct Optics module part number

CONTENTS

LIST OF FIGURES

1   ISSUE 2 ERRATA

This issue 2 document errata contains errata applied to document PMC-981407 S/UNI-622-MAX Reference Design Issue 1.
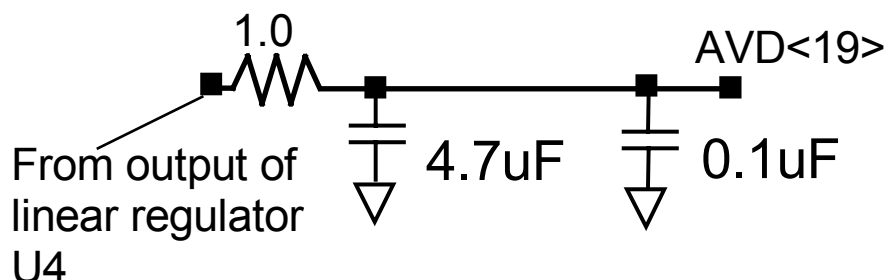
2   S/UNI-622-MAX REFERENCE DESIGN SCHEMATIC ERRORS

This section describes errors and required corrections on the schematics provided with the S/UNI-622-MAX Reference Design.

2.1   Missed Analog Power Filtering

On Page 3 of the S/UNI-622-MAX Reference Design schematics, Pin 19 of AVD<31..0> is tied directly to the output of the linear voltage regulator (U4). This pin should be filtered with the circuit shown below. Without this filtering, jitter performance of the device will be degraded.

Figure 1   - Filtering for AVD<19>

2.2   Incorrect Pullup/Pulldown Resistors

On Page 2 of the S/UNI-622-MAX Reference Design schematics, pins RRCLK+ and RRCLK- (or RRCLKP and RRCLKN respectively) are both pulled down to ground using 4.7 KOhm resistors. RRCLK+ should be tied to the opposite polarity as pin RRCLK-, e.g. since RRCLK- is tied to ground, RRCLK+ should be tied to 3.3V. When tying an input to ground, the pin may be connected directly to ground. When tying an input to 3.3V or 5V, a 4.7 KOhm resistor should be used in order to prevent latchup during power up. Failure to tie RRCLK+ and RRCLK- to complementary values will result in signal contention within the device witch may cause problems with device operation.

2.3   Incorrectly Referenced Optics Module

The optics modules HFBR-5208 and HFCT-5208 should be correctly referenced as HFBR-5208M and HFCT-5208M.

3   ADDITIONAL DESIGN NOTES

This section provides additional recommendations on designing with the S/UNI-622-MAX device.

3.1   PECL Interfacing Issues

All unused differential PECL inputs should be tied such that the positive input and negative input are complementary (have opposite logic values). For example; RRCLK+ is tied to 3.3V, therefore RRCLK- should be tied to ground. Or; RRCLK+ is tied to ground and RRCLK- should be tied to 3.3V.

The PECLV and PBIAS pins affect both the optical PECL interface as well as the REFCLK+/- interface. Therefore REFCLK+/- must have the same signal reference level as the optical PECL interface.

Traces between the optics and the S/UNI-622-MAX should be limited to a maximum of **4 cm** long. No vias should be present on the traces except where required for termination components. Any vias present on the traces will degrade jitter performance. Traces should be equal length with as few bends as possible.

Pages 8 and 9 of the S/UNI-622-MAX Reference design describe the optional use of optics with integrated clock and data recovery (HFBR/HFCT-5207). It should also be noted that, for HFBR/HFCT-5207 devices, the SD signal should be terminated using a 10 KOhm resistor to ground rather than the 330 Ohm specified in Figure 2 of the S/UNI-622-MAX Reference design.

3.2   JTAG Port

When unused, the JTAG port of the S/UNI-622-MAX should have TRSTB tied to RSTB. This will reset the JTAG port on reset of the system. TMS, TCK and TDI should be tied high. In addition, TMS may be tied high and TCK tied to a free running clock to ensure that the JTAG port logic is continuously put back into the correct state.

NOTES

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