PM5543

ADM155_REF

SONET/SDH 155 Mbit/s ADD/DROP MULTIPLEXOR WITH SINGLE MODE OPTICAL INTERFACE REFERENCE DESIGN (SARD)

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FEATURES

- Receives an OC-1/OC-3 optical signal and processes section, line and path SONET overhead.
- Performs arbitrary tributary cross-connection to produce a byte serial STS-1, STS-3 (STM-1, AU3), STS-3c (STM-1, AU4) signal.
- Transmits an OC-1/OC-3 [STS-1/STS-3 (STM-1)] stream with an option to overwrite all section, line and path overhead.
- Provides for loop back of both line-side and drop-side signals.
- Recovers line-side receive signal clock.
- Drop-side receive clock may be pleisiochronous to the line-side receive clock.
- Provides on board line-side transmit clock synthesis.
- Drop-side transmit clock may be pleisiochronous to the line-side transmit clock.
- Optionally translates received pointer justification events at the SPE level to tributary pointer justifications, thus locking the SONET SPE to accomplish tributary switching.
- Optionally cross-connects tributaries mapped in the receive stream to any arbitrary time slots in the drop-side stream.
- Allows broadcasting of tributaries over multiple tributaries.
- Provides line side OC-1/OC-3 transmit and receive signals on SC type optical single mode connectors.
- Provides an interface to a proprietary external mapping-demapping function via a 100-pin connector.
- Provides a 100-pin connector for ring expansion and ring control for connection to another PM5543 SARD board.
- Provides a 132-pin connector for microprocessor interface to a PM1501 EVMB motherboard.

OVERVIEW

The SONET/SDH 155 Mbit/s Add-Drop Multiplexor Single Mode Optical Reference Design allows for the evaluation, and demonstration of the PMC SONET/SDH add-drop multiplexor chipset. This reference design illustrates how to implement the front end optics and clock/ data recovery using the CY97B951 and the HP SDX1155 single mode transceiver. This design has been especially designed to mate with itself, the PMC PM1501 EVMB evaluation motherboard and an asynchronous system mapper/demapper daughter board (as yet unspecified) to form a complete add drop node for use in an ADM ring network. This document describes the function of this reference design and also provides complete layout information so that it can be easily duplicated or used as a part of another proprietary design.

This board utilizes four of the five PMC's Stel/ar (SONET Telecom Architecture) chipset together with the commercially available HP optical transceiver and the Cypress CY7B951 to make up a complete ADM ring node element. The SONET/SDH transport overhead, pointer processing (at the SONET/SDH SPE and VT/TU level) and tributary cross connection are completely handled by the Stel/ar chipset; the section and line is handled by the SONET/SDH Transport Overhead Transceiver (STXC), the path overhead and SPE pointer interpretation is handled by the SONET/SDH Path Overhead Terminating Transceiver (SPTX), the SPE pointer justifications are translated to VT/TU level justifications by the SONET/SDH Tributary Unit Payload Processor (TUPP or TUPP-Plus) and the tributary cross connection is handled by the SONET/SDH Tributary Unit Cross-Connect (TUDX1 and TUDX2).

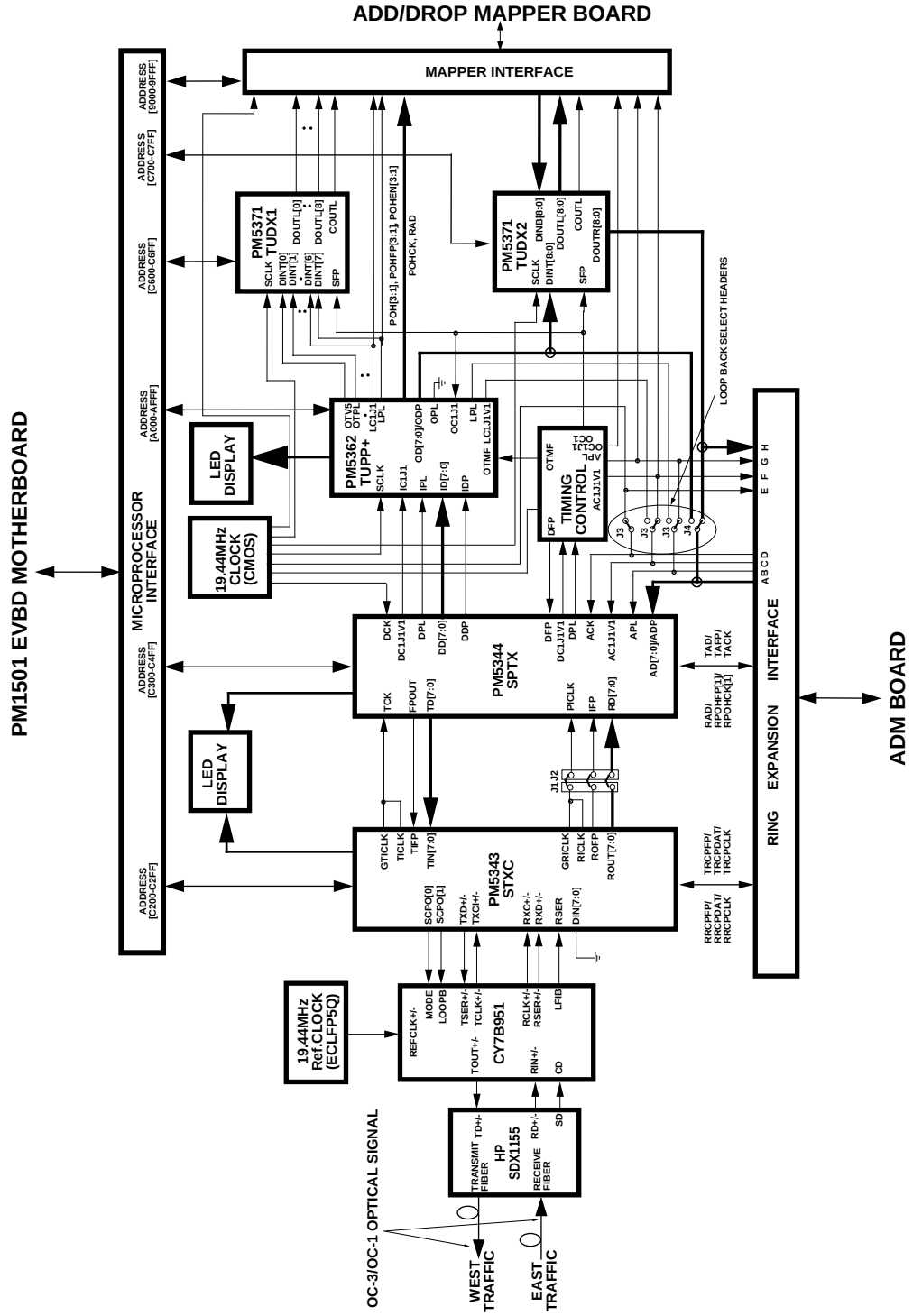
In the receive direction, the HP optical transceiver receives the OC-1 (or OC-3) optical signal and performs optical to electrical conversion to a differential serial STS-1 (or STS-3) stream. This serial stream is processed by the CY7B951 to extract clock and data before they are passed on to the inputs of the STXC. The STXC performs serial to parallel conversion and terminates the section and line transport overhead and passes the byte serial data to the SPTX. Besides termination of the path overhead, the SPTX supports decoupling of the line side synchronous timing to the system side synchronous timing, the differing rates (19.44MHz $\pm$ 20ppm) being adapted by SPE pointer justifications. Received pointer justifications at the system side are compensated by tributary pointer justifications while allowing the SPE envelope to be locked at offset 522 using the TUPP device or at an offset of 0 or 522 using the TUPP-Plus. The data outputs from the TUPP/TUPP-Plus are directly connected to the data inputs of the tributary cross-connect device, TUDX2. The TUPP/TUPP-Plus tributary SPE and tributary V5 position signals, OTSPE and OTV5 respectively, are sent to another TUDX, TUDX1 and TUPP-Plus OTPOH, AIS, IDLE, LC1J1V1, LPL and COUT signals also to be sent to TUDX1. These tributary and frame signals are cross-connected to arbitrary time slots by the two TUDX devices and the cross connected frame is presented to the ADD/DROP Mapper I/F or the Ring Expansion I/F for possible processing by an external mapper or second ADM function.

In the transmit direction, the reverse process to the receive direction is implemented. The SPTX receives an STS-3 (STM-1) or STS-1 byte serial stream from either the on board TUDX cross connect or the Ring Expansion Interface and inserts the path overhead. The STXC serializes the data to STS-1 or STS-3 rate and transfers the data to the HP optics via the cypress CY7B951. The OC-1/OC-3 signal is then transmitted out to the line.

The SARD board requires an external evaluation motherboard (PM1501 EVMB) for configuration and control. The PM1501 EVMB Evaluation Motherboard, based on a 68HC11 microcontroller, provides processing and communication capability with the daughterboard. The SARD board is connected with the microprocessor motherboard through a 96-pin edge connector. The microcontroller can be connected to a VT100-type terminal through an RS-232 interface.

For details on the operation of the Stel/ar chips or the PM1501 microprocessor motherboard, please consult their respective data sheets as listed in the reference section at the end of this document.

FUNCTIONAL DESCRIPTION



SARD Block Diagram

PM5101 Motherboard Interface

The micro control Interface includes all the interface logic required to connect to a standard PMC PM1501 EVMB evaluation motherboard. Bus buffers and transceivers are provided at the interface to reduce loading on the PM1501 EVBD's 68HC11 microprocessor and to increase the drive capability of the interface.

Decode logic provides memory mapped access to all of the on board PMC-Sierra Stel/ar devices (STXC, SPTX, TUPP/TUPP-Plus TUDX1 and TUDX2) and all board level registers. Three read/write registers are provided to control the STXC, SPTX, TUPP/TUPP-Plus , TUDX1 and TUDX2 devices. One of these registers is reserved for future use. The second one is dedicated to the STXC and TIMING CONTROL blocks and is used to control the configuration of these blocks. The third one is a general software reset register used for resetting any device on an individual basis.

Optical Interface

The optical interface consists of the HP SDX1155 intermediate reach (approximately 16 dB per link loss at 1.3 μm wavelength) single mode optical transceiver. This device is interchangeable with any multisourced 1X9 pin (lower or higher power) transceiver, or multimode LED transceiver for short haul applications. This reference design is not designed for the long reach separate optical receiver and transmitter modules available today. For long reach designs the layout must be changed to accompany the different footprints of the separate optics pair. However, it is expected that a long reach optical transceiver compatible with the footprint on this board will be available in the near future.

In the receive direction, the HP SDX1155 converts the OC-1 or OC-3 optical signal to a two-level (NRZ) bit serial electrical data stream at the STS-1 or STS-3(STM-1) rate.

In the transmit direction, the HP SDX1155 takes the bit serial STS-1 or STS-3 signal and modulates the laser output as an OC-1 or OC-3 optical data stream.

The optical transceiver uses dual SC/PC type connector.

CY7B951

The Cypress SONET/SDH Serial Transceiver (CY7B951) contains integrated clock and data recovery and clock synthesis. The internal receive PLL recovers a 155.52MHz or a 51.84MHz clock from an incoming NRZ or NRZI data. The differential input data is re-timed by the recovered clock and is presented as a differential PECL bit serial data output. The receive PLL requires a 19.44MHz reference clock to provide a 155.52MHz or 51.84MHz clock in the absence of input data. The reference clock is also used to improve the PLL lock time by training to the approximate frequency of the incoming data stream during optical LOS.

The transmit section of the Cypress (CY7B951) SONET/SDH Serial Transceiver contains a PLL that takes a reference clock and multiplies it by 8 to produce a 155.52MHz or 51.84MHz PECL differential output clock. This clock is used by the STXC to transmit PECL differential data. The PECL data from the STXC is then buffered by the CY7B951 before interfacing to the optics.

Reference Clock

The 19.44MHz reference is an ECL oscillator required for clock and data recovery by the CY7B951. The receive PLL of the CY7B951 utilizes this clock to generate a 155.52MHz or 51.84MHz clock in the absence of input data. Also, the CY7B951 synthesizes a 155.52MHz or 51.84MHz clock for the timing of the transmit bit serial stream. This clock is used by the STXC's TXCI input to time the output bit serial data stream on its TXD+/- outputs.

The reference clock is also used to improve the PLL lock time inside the CY7B951.

System Clock

A TTL/CMOS level clock is used as a byte serial system clock to drive the SPTX (drop side), TUPP/TUPP-Plus, TUDX1 and TUDX2 circuitry. This clock also accompanies the data sent out on the Mapper Interface and the Ring Expansion Interface.

STXC

The PM5343 SONET/SDH Transport Overhead Transceiver (STXC) processes the transport overhead (section and line overhead) of an STS-1 or STS-3 (STM-1) stream. The STXC operates to implement SONET/SDH-compliant line interfaces.

The STXC processes either byte serial data at 6.48 Mbyte/s (STS-1) or 19.44 Mbyte/s (STS-3, STM-1), or bit serial data at 51.84 Mbits/s (STS-1) or 155.52 Mbits/s (STS-3, STM-1) on the line side depending on the mode selected. In this design, the STXC implements the bit serial interface only during normal operation. When the optics and clock recovery front end detect a loss of light condition, the STXC is automatically configured to select the byte serial parallel interface. Because of the parallel interface input is tied to ground, the STXC receives all "0". Then the LOS is claimed. The 19.44 MHz RICLK clock input is also switched from the receive sourced clock GRICLK to the transmit sourced clock GTICLK. This allows the STXC to guarantee the detection of an LOS state. Otherwise the parallel interface is not utilized.

On the system side, the STXC either expects or outputs an STS-1 or an STS-3 (STM-1) byte serial stream as determined by the selected operating mode during Stel/ar device programming.

In the receive direction, the STXC frames to the incoming stream, optionally descrambles the receive stream, calculates and compares the bit interleaved parity

error detection codes (B1, B2) and accumulates BIP-8 errors (B1, B2) and retransmits the B2 errors as FEBE indications (Z2). Loss of signal (LOS), out of frame (OOF), loss of frame (LOF), far end receive failure (FERF), line alarm indication signal (AIS), and protection switching byte failure alarms are detected. In addition to extracting the entire transport overhead on a dedicated output port, the STXC also extracts and serializes the order wire channels (E1, E2), the data communication channels (D1-D3, D4-D12), the section user channel (F1) and the APS bytes (K1, K2) on their own dedicated output ports.

In the transmit direction, the STXC internally generates all transport overhead bytes with the exception of the H1, H2 and H3 bytes and inserts them into the outgoing SONET stream. Transport overhead bytes can also be inserted using a dedicated transport overhead insertion port or dedicated orderwire or data communication channel ports. In addition, the STXC provides FERF and AIS alarm insertion, loss of signal insertion, framing pattern error insertion, and coding violation insertion (B1 and B2) for diagnostic purposes.

A transmit and receive ring control port which allows alarm and maintenance signal control and status to be passed between mate STXCs is also provided. This feature is useful for ring-based add-drop multiplex applications and is taken advantage of in this design through the Ring Expansion Interface. When the Ring Expansion Interface is not used, the same STXC is used for both the receive and transmit sides of a ring connection.

SPTX

The SPTX device provides receive path termination for a SONET STS-1, STS-3 or STS-3c stream, or an SDH STM-1 stream carrying three AU3s or one AU4. SPTX interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope (virtual container). The extracted SPE (VC) is placed on a TeleCombus DROP bus. Frequency offsets (e.g., due to pleisiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the received data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus. In addition to its basic processing of the received SONET/SDH overhead, the SPTX provides convenient access to all path overhead bytes, which are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The SPTX device provides transmit path origination for a SONET STS-1, STS-3 or STS-3c stream or an SDH STM-1 stream carrying three AU3s or one AU4. SPTX generates the transmit payload pointers (H1, H2) and inserts the synchronous payload envelope (virtual container) from a TeleCombus ADD bus into the transmit stream. Frequency offsets (e.g., due to pleisiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the transmit data stream and the ADD buses are accommodated by pointer adjustments in the transmit stream. In addition to its basic processing of the transmit SONET/SDH overhead, the SPTX provides convenient

access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired. The SPTX also supports the insertion of a large variety of errors into the transmit stream, such as bit interleaved parity errors and inverted NDF flags, which are useful for system diagnostics and tester applications.

The SPTX device supports in-band error reporting where the path status byte (G1) inserted in the DROP bus reflects the number of BIP-8 errors (B3) detected and the path FERF status. The SPTX can be programmed to pass the path status byte on the ADD bus through unmodified. This feature allows the transmit path processor to be located remotely to the receive processor without having to incur the cost of routing an alarm port.

The SPTX device supports tandem connection termination applications where the tandem connection maintenance byte (Z5) carries the incoming B3 BIP-8 error count, a tandem data link, and a path AIS code. The B3 byte is passed through to the DROP bus after being compensated for the differing Z5 byte, otherwise the B3 byte is unaffected. The incoming error count is accumulated and the receive data link is serialized for external processing. A new data link can be inserted from a low speed serial input. An incoming signal failure alarm (ISF code with IEC field set to 'b1111) is used to convey path AIS in place of all-ones in the pointer (H1, H2).

The SPTX device maintains a large number of statistics for performance monitoring purposes. BIP-8 errors (B3) and tandem path incoming error counts (Z5 IEC) are accumulated. In addition, the SPTX is selectable to accumulate positive and negative pointer justifications that it receives or justifications that it generates on the DROP bus. It also accumulates positive and negative pointer justifications in the transmit stream. Excessive justifications may be indicative of clock synchronization failures.

TUPP & TUPP-Plus

Either TUPP or TUPP-Plus can be used in this design. When configured for SONET compatible operation, the TUPP or TUPP-Plus transfers all tributaries in the three STS-1 synchronous payload envelopes of an incoming STS-3 byte serial stream to the three STS-1 synchronous payload envelopes of an outgoing STS-3 byte serial stream. Similarly, when configured for SDH compatible operation, the TUPP transfers all tributaries in the single AU4 or three AU3 administrative units of an incoming STM-1 byte serial stream to a single AU4 or three AU3 administrative units of an outgoing STM-1 byte serial stream. The TUPP or TUPP-Plus compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) synchronous payload envelope frame rates through processing of the lower level (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, TU11) tributary pointers.

The TUPP or TUPP-Plus is configurable to process any legal mix of tributaries. Each VT group can be configured to carry any one of the four tributary types (VT1.5, VT2, VT3, or VT6) and each TUG2 can be configured to carry any one of three tributary

types (TU11, TU12, or TU2). TUG2s can be multiplexed into a VC3 or a TUG3. Alternatively, each TUG3 can be configured to carry a TU3.

The TUPP and TUPP-Plus provides useful maintenance functions. They include detection of loss of pointer and pointer re-acquisition for each tributary, and optional generation of interrupts. The TUPP also allows insertion of tributary path AIS or tributary idle (unequipped). The TUPP can also insert inverted new data flag fields that can be used to diagnose downstream pointer processing elements. The TUPP-Plus implements a superset of the TUPP functionality.

The TUPP-Plus contains tributary performance monitoring and tributary path overhead processing. These functions are not supported by the TUPP. The following functions are exclusive to the TUPP-Plus.

- The TUPP-Plus is configurable to process 16-byte or 64-byte format tributary path trace messages (tributary trail trace identifiers).

- Extracts and serializes the entire tributary path overhead for each tributary into lower speed serial streams.

- Extracts tributary size (SS) bits for each tributary into internal registers. Extracts tributary path trace message (trail trace identifier) for each tributary into internal buffers.

- Provides individual tributary path trace message buffer that holds the expected message and detects tributary path trace mismatch (trail trace identifier mismatch) alarms (TIM) and return to matched state for each tributary and optionally generates interrupts.

- Detects tributary path trace unstable (trail trace identifier unstable) alarms (TIU) and return to stable state for each tributary and optionally generates interrupts.

- Extracts tributary path signal label for each tributary into internal registers and detects change of tributary path signal label events (COPSL) for each tributary and optionally generates interrupts.

- Provides individual tributary path signal label register that hold the expected label and detects tributary path signal label mismatch alarms (PSLM) and return to matched state for each tributary and optionally generates interrupts.

- Detects tributary path signal label unstable alarms (PSLU) and return to stable state for each tributary and optionally generates interrupts.

- Detects tributary unequipped defect (UNEQ) and tributary path defect indication (PDI-V).

- Detects assertion and removal of tributary extended remote defect indications (RDI) for each tributary and optionally generates interrupts.

- Calculates and compares the tributary path BIP-2 error detection code for each tributary and configurable to accumulate the BIP-2 errors, on block or bit basis, in internal registers.

- Calculates and compares the TU3 path BIP-8 error detection code for each TU3 stream and accumulates the BIP-8 errors, on block or bit basis, in internal registers.

- Accumulates TU3 tributary far end block errors (FEBE) on a bit or a block basis, in internal registers.

- Allows insertion of all-zeros or all-ones tributary idle code with unequipped indication and valid pointer into any tributary under software control. Idle tributaries are identified by an output signal. Identifies outgoing tributaries that are in AIS state by an output signal.

- Allows software to force the AIS insertion on a per tributary basis.

- Inserts valid H4 byte and all-zeros fixed stuff bytes on the outgoing stream. Remaining path overhead bytes (J1, B3, C2, G1, F2, Z3, Z4, and Z5) can be configured to be set to all-zeros or to reflect the value of the corresponding POH bytes in the incoming stream.

- Inserts valid pointers, and all-zeros transport overhead bytes on the outgoing stream with valid "TeleCombus" control signals when configured to operate in locked mode.

- Supports in-band error reporting by updating the FEBE, RDI and auxiliary RDI bits in the V5 byte (G1 in TU3) with the status of the incoming stream.

- Provides low maximum tributary processing delay of 33 µs for VT1.5, 25 µs for VT2, 17 µs for VT3, and 9 µs for VT6 streams.

- provides independently configurable incoming and outgoing interfaces that operate in byte interface mode from a single 19.44 MHz clock or in nibble interface mode from a single 38.88 MHz clock.

- Provides a standard 5 signal IEEE P1149.1 JTAG test port for boundary scan test purposes.

TUDX

The PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect is a monolithic integrated circuit that allows non-blocking switching of tributaries within two SONET STS-3 or SDH STM-1 streams. Any tributary entering on either stream can be

connected to any same size tributary within either outgoing stream. The TUDX can be programmed to cross-connect a mix of SONET VT1.5, VT2, VT3, VT6, or STS-1 channels or SDH TU11, TU12, TU2, or TU3 channels. Programmable idle code can also be inserted into any of these channels. The TUDX allows cross-connection of up to 168 VT1.5 or TU11 streams, up to 126 VT2 or TU12 streams, or up to 42 VT6 or TU2 streams or any legal mix as permitted by the SONET or SDH mappings. In this reference design one stream is provided from the upstream TUPP/TUPP-Plus device whilst the other is provided from an external mapper daughterboard through the Mapper Interface connector. Two TUDXs are used in this design, TUDX1 and TUDX2. The TUDX2 device provides the main data interconnect between the external mapper function and the SARD board. The other TUDX, TUDX1, provides the accompanying control signals that indicate the data condition transported through TUDX2. These control signals are used by the external mapper to decode the presence of tributary payload bytes and tributary V5 bytes.

Timing Control

The Timing Control circuit contains a 4096 free running counter, a 64K PROM and some other miscellaneous glue logic. The counter starts counting from zero and is initialized to zero after every occurrence of the C1 pulse or a reset. The counter continues to count until the initialization occurs again at the next C1 pulse. The 12 outputs of the counter are used to address an on board PROM that acts as a lookup table. The lookup values are programmed to account for delays through the TUPP/TUPP-Plus and TUDX's. Because these delays are constant, the time when the C1 byte (say) appears on the output of the TUDX2 is predictable. The value of this delay is equal to 280 (5 clock cycles of TUPP/TUPP-Plus and 275 clock cycles of TUDX in STS-3/STS-3c mode)or 100 (5 clock cycles of TUPP/TUPP-Plus and 95 clock cycles of TUDX in STS-1 mode) bytes after the C1 byte appears on the output of the SPTX. These values are equivalent to a count value of 280 or 100 (again, depending on the mode of operation). Therefore, by programming a logic one at this specified location in the PROM a C1 pulse is generated for the data on the output of the TUDX2. By programming a series of such locations the AC1J1V1 and APL signals can be constructed and the outputs of the PROM can be used to control the ADD bus control signals of the SPTX.

The four page control bits (PAGE[0] to PAGE[3) from the board level programmable register(C080H) are used to address higher address's of the PROM and effectively segment the PROM into 16 pages, with each page being 4K deep. Page one is programmed to control the SARD board in STS-3 or STM-1(AU3) mode when the TUPP/TUPP-Plus output is locked with J1 at location 522. Page two is programmed to control the SARD board in STS-3c or STM-1(AU4) mode when the TUPP/TUPP-Plus J1 output is locked at location 522. Page three is programmed to control the SARD board in STS-1 mode with J1 output from TUPP/TUPP-Plus locked at location 522. Page four to six are similar to page one to three except this time the TUPP-Plus output is locked with J1 at location 0. Page seven to Page sixteen are reserved for future use.

Ring Expansion Interface

This interface contains all the necessary signals to interconnect to a second SARD board. A single SARD board is equivalent to a single ring network element. To construct a duel ring network element (NE), a second board is required to act as the counter rotating protection path. When one SARD board is dedicated to one ring whilst the other board is dedicated to the counter rotating ring, there is no need to interconnect the two boards via the Ring expansion Interface. The Ring Expansion Interface is required when one of the rings of a dual ring network utilizes half the circuitry on one board (for traffic being received by the NE) and half the circuitry on an adjoining board (for traffic being transmitted by the NE). These two configurations require that the Stel/ar devices must be programmed in two different ways. In the first configuration, where the clockwise ring is constructed utilizing board 1 and the counter-clockwise ring is constructed utilizing board 2, the Stel/ar devices must be configured such that they can receive traffic from the East and transmit traffic to the west. This will be referred to as the "East/West Cut" configuration. In the second configuration, where the clockwise ring is constructed by utilizing half of each Stel/ar device on board 1 and the other half of each Stel/ar device on board 2, the Stel/ar devices must be configured such that its receive circuitry handles traffic from the east (on one ring) and its transmit circuitry handles traffic to the east (on the second ring). This will be referred to as the "North/South Cut" configuration.

The Ring Expansion Interface is only useful when implementing the North/South Cut, otherwise there is no need to mate the two boards together. In this configuration, the receive clockwise ring utilizes half the circuitry whilst the transmit counter-clockwise ring utilizes the remaining half. Consequently, the circuitry on the adjoining SARD board must be linked to form a complete NE.

The Ring Expansion Interface contains all the control signals and data signals required to interconnect the traffic from one SARD board to the adjoining SARD board. This includes ring control signals that allow communication between the two remote half's of each Stel/ar device from one board to the other. Ring Expansion interface is activated by appropriately configuring the on board jumpers.

Mapper Interface

The Mapper Interface allows interfacing to an external asynchronous transport system, such as an E1, T1, E3 or DS3 system. Therefore, this interface includes the complete SONET/SHD frame data and control signals as well as the lower level tributary control signals.

The SONET/SDH drop traffic is interfaced via the DOUTL[8:0] outputs of the TUDX device and the AC1J1V1 and APL control signals from the TIMING CONTROL. The DOUTL[8:0] outputs of TUDX2 contain the SONET/SDH data and the DOUTL[1:0] outputs of TUDX1 contain the lower level tributary control signals OTSPE (or OTPL when TUPP_Plus is used), OTV5, OTPOH, AIS, IDLE, LC1J1V1, LPL and COUT. The 19.44MHz system clock is also passed through to the Mapper Interface.

The SONET/SDH add traffic is interfaced via the DINB[8:0] inputs of TUDX2 and the OC1J1 output of the TIMING CONTROL block. The OC1J1 indicates the frame alignment and pointer value that must be applied to the byte serial data inputs on the DINB[8:0] stream. As an option to the OC1J1 control signal, the control signals LC1J1V1 and LPL are also directly connected to the mapper interface to allow generation of SONET/SDH frames aligned to the same alignment as the frames generated by the TUPP-Plus.

The TUPP-Plus tributary overhead signals POH[3:1], POHFP[3:1], POHEN[3:1], POHCK and RAD are connected to the Mapper Interface to provide external tributary path overhead monitoring. Normally this is monitored in the TUPP-Plus and is not required to be done externally.

LED Displays

Two LED displays are provided to indicate the status of the STXC, SPTX and TUPP devices. When the LED's are lit they indicate the active condition on the STXC's OOF, LOF, LOS, LAIS and FERF outputs, the active condition on the SPTX's PFERF[3:1], PAIS[3:1] and LOP[3:1] outputs and the active condition on the TUPP's IDLE, AIS and LOM[3:1] outputs.

Configuration Headers/Jumpers

The SARD board contain four configuration headers/jumpers, J1, J2, J3 and J4.

Jumpers J1 and J2 are provided to allow prototype boards to be interconnected between the STXC to SPTX interface. Jumper J1 is a 12 by 1 strip and jumper J2 is a 10 by 1 strip. Normally all pins of jumper J2 are connected to the adjacent pins of jumper J1. The remaining pins of J1 are left unconnected and are for observation only.

The jumpers J3 and J4 provide SPTX an option to select ADD bus signal (ACK, APL, AC1J1V1 and AD[n]) from on board TUPP/TUPP-Plus, TUDX2 or from expansion board. When the Ring Expansion Interface is not used, jumpers J3 and J4 allows the SPTX to select traffic from the TUDX outputs or the TUPP outputs. When a second SARD board is connected to the Ring Expansion Interface, these jumpers must all be disconnected. See the SPTX ADD Bus Clock & Signal Selection Interface section for more information.

INTERFACE SIGNAL DESCRIPTION

Microprocessor Interface (Connector P1)

This interface consists of a 96 pin male connector that interfaces to the PM1501 EVBD motherboard. Signals on this interface are CMOS/TTL compatible and are used to read and write to on board registers and the memory mapped Stel/ar on chip registers. This interface also provides power and ground connections to the SARD board.

Microprocessor Interface Signal Description.

Signal Name	Type	P1 Pin	Function
ALE	I	C1	Address latch enable. When high, identifies that address is valid on AD[7:0].
E	I	C2	External Data Access Indication. Active high.
RWB	I	C3	Active low write, active high read enable.
RSTB	I	C4	Active low H/W reset.
A[15]	I	C5	Address bus bit 7.
A[14]	I	C6	Address bus bit 6.
A[13]	I	C7	Address bus bit 5.
A[12]	I	C8	Address bus bit 4.
A[11]	I	C9	Address bus bit 3.
A[10]	I	C10	Address bus bit 2.
A[9]	I	C11	Address bus bit 1.
A[8]	I	C12	Address bus bit 0.
AD[7]	I/O	C13	Multiplexed address/data bus bit 7.
AD[6]	I/O	C14	Multiplexed address/data bus bit 6.
AD[5]	I/O	C15	Multiplexed address/data bus bit 5.
AD[4]	I/O	C16	Multiplexed address/data bus bit 4.
AD[3]	I/O	C17	Multiplexed address/data bus bit 3.
AD[2]	I/O	C18	Multiplexed address/data bus bit 2.
AD[1]	I/O	C19	Multiplexed address/data bus bit 1.
AD[0]	I/O	C20	Multiplexed address/data bus bit 0.
PA3	I	C21	68HC11 Processor Port A bit 3.
PA4	I	C22	68HC11 Processor Port A bit 4.

PA5	I	C23	68HC11 Processor Port A bit 5.
PA6	I	C24	68HC11 Processor Port A bit 6.
PD2	O	C25	MISO. Master In Slave Out of Port D acting as SPI. Pulled up on motherboard.
PD3	I	C26	MOSI. Master Out Slave In of Port D acting as SPI. Pulled up on motherboard.
PD4	I	C27	SCK. Serial clock of Port D acting as SPI. Pulled up on motherboard.
PD5	I	C28	SS. Slave Select of Port D acting as SPI active low. Pulled up on motherboard.
IRQ	O	C29	Maskable interrupt.
XIRQ	O	C30	Non Maskable Interrupt. Not connected.
DISB	O	C31	EVMB memory disable. Pulling this signal low will disable MPU access to the EVMB's on-board RAM and EPROM. Not connected.
SP	O	C32	SPARE.
GND	O	A1-A28	Ground.
+5V	O	A29-A32	Power Supply.

Decoded Microprocessor Signal to Stel/ar chipset Interface

The following table describes the interface between the TUDX, STXC, SPTX and TUPP/TUPP_Plus, the Mapper Interface with the decoded outputs of the on board microprocessor interface logic. These signals are the inputs and outputs of sheet 7 and 8.

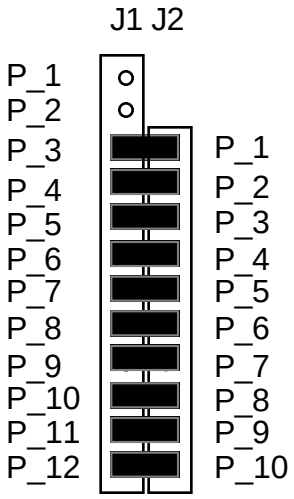
Signal	I/O	To/From	Description
ALE	O	All Stel/ar Devices and P3	Address latch enable. When high, identifies that address is valid on A[11:0].
INTB	I	All Stel/ar Devices and P3	Interrupt require signal. Active low.
WRB	O	All Stel/ar Devices and P3	Active low write strobe signal.
RDB	O	All Stel/ar Devices and P3	Active low Read enable select signal.
MC STXC RSTB	O	STXC	Active low H/W reset.
MC SPTX RSTB	O	SPTX	Active low H/W reset.
MC TUPP RSTB	O	TUPP/TUPP-Plus	Active low H/W reset.

MC TUDX1 RSTB	O	TUDX1	Active low H/W reset.
MC TUDX2 RSTB	O	TUDX2	Active low H/W reset.
MC MAP RSTB 1	O	P3	Active low H/W reset.
MC MAP RSTB 2	O	P3	Active low H/W reset.
MC MAP RSTB 3	O	P3	Active low H/W reset.
MC STXC CSB	O	STXC	Active low chip select.
MC SPTX CSB	O	SPTX	Active low chip select.
MC TUPP CSB	O	TUPP	Active low chip select.
MC TUDX1 CSB	O	TUDX1	Active low chip select.
MC TUDX2 CSB	O	TUDX2	Active low chip select.
MC MAP CSB	O	P3	Active low chip select.
A[11]	O	TUPP-Plus P3	Address bus bit 11.
A[10]	O	TUPP-Plus P3	Address bus bit 10.
A[9]	O	TUPP-Plus & P3	Address bus bit 9.
A[8]	O	SPTX TUPP-Plus P3	Address bus bit 8.
A[7]	O	SPTX TUPP TUPP-Plus P3	Address bus bit 7.
A[6]	O	STXC SPTX TUPP TUPP-Plus P3	Address bus bit 6.
A[5]	O	STXC SPTX TUPP TUPP-Plus P3	Address bus bit 5.
A[4]	O	All Stel/ar Devices P3	Address bus bit 4.
A[3]	O	All Stel/ar Devices P3	Address bus bit 3.
A[2]	O	All Stel/ar Devices P3	Address bus bit 2.
A[1]	O	All Stel/ar Devices P3	Address bus bit 1.
A[0]	O	All Stel/ar Devices P3	Address bus bit 0.
D[7]	I/O	All Stel/ar Devices P3	Data bus bit 7.
D[6]	I/O	All Stel/ar Devices P3	Data bus bit 6.
D[5]	I/O	All Stel/ar Devices P3	Data bus bit 5.
D[4]	I/O	All Stel/ar Devices P3	Data bus bit 4.
D[3]	I/O	All Stel/ar Devices P3	Data bus bit 3.
D[2]	I/O	All Stel/ar Devices P3	Data bus bit 2.
D[1]	I/O	All Stel/ar Devices P3	Data bus bit 1.
D[0]	I/O	All Stel/ar Devices P3	Data bus bit 0.
MC MAP CONTROL1	O	P3	Control bit reserved for future use

MC MAP CONTROL2	O	P3	Control bit reserved for future use
MC MAP CONTROL3	O	P3	Control bit reserved for future use
MC TDIS	O	STXC	Active high transmit disable signal.
MC PAGE[0]	O	TIMING CONTROL	PROM address bit 12.
MC PAGE[1]	O	TIMING CONTROL	PROM address bit 13.
MC PAGE[2]	O	TIMING CONTROL	PROM address bit 14.
MC PAGE[3]/CONCAT	O	TIMING CONTROL	PROM address bit 15.

Prototyping Jumper Interface

The SARD board provides access to the receive interface between the STXC and the SPTX. This interface can be used to manipulate the SPTX's RECEIVE bus interface. In normal operation the jumpers J1 and J2 are connected as shown below.

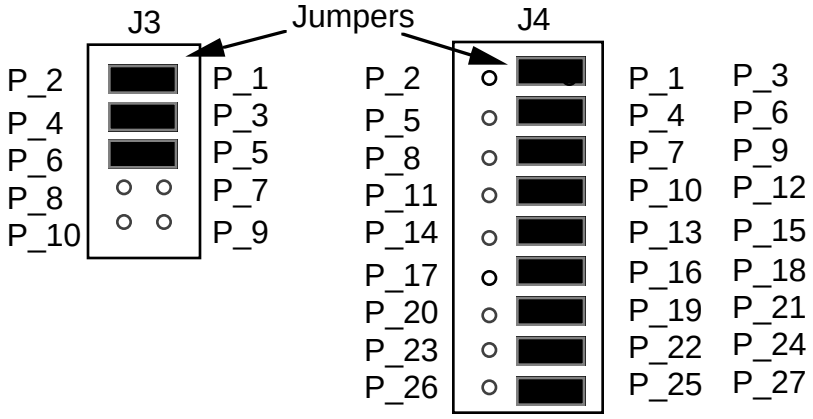


J1	J2	J2 Pin Description to	J1 Pin Description
P_1			MICRO_CONTROL PAGE[3]/CONCAT
P_2			STXC GRICLK
P_3	P_1	SPTX IFP	STXC ROFP
P_4	P_2	SPTX PIN[0]	STXC ROUT[0]
P_5	P_3	SPTX PIN[1]	STXC ROUT[1]
P_6	P_4	SPTX PIN[2]	STXC ROUT[2]
P_7	P_5	SPTX PIN[3]	STXC ROUT[3]
P_8	P_6	SPTX PIN[4]	STXC ROUT[4]

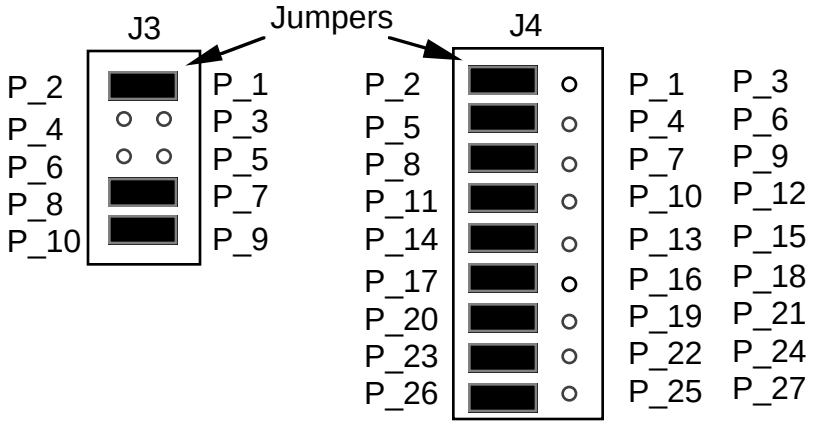
P_9	P_7	SPTX PIN[5]	STXC ROUT[5]
P_10	P_8	SPTX PIN[6]	STXC ROUT[6]
P_11	P_9	SPTX PIN[7]	STXC ROUT[7]
P_12	P_10		MICRO_CONTROL STXC RSTB

SPTX ADD Bus Clock & Signal Select Interface

When the Ring Expansion Interface is not used, jumpers J3 and J4 allows the SPTX to select traffic from the TUDX outputs or the TUPP outputs. When a second SARD board is connected to the Ring Expansion Interface, these jumpers must all be disconnected. The configuration shown below depicts the case where the TUDX is looped back to the SPTX's ADD bus.



The configuration shown below depicts the case where the TUPP/TUPP_Plus is looped back to the SPTX's ADD bus.



J3	Description
PIN 1-2 CLOSE	Selects the on board 19.44 MHz crystal as the DROP bus clock
PIN 3-4 CLOSE	Selects APL from TIMING CONTROL
PIN 5-6 CLOSE	Selects AC1J1V1 from TIMING CONTROL
PIN 7-8 CLOSE	Selects LPL from TUPP-Plus
PIN 9-10 CLOSE	Selects LC1J1V1 from TUPP-Plus
ALL PINS OPEN	Selects the Ring Expansion Interface

J4	Description
PIN 1-3 CLOSE	Selects the on board TUDX2 DOUTR(0) for loop back
PIN 4-6 CLOSE	Selects the on board TUDX2 DOUTR(1) for loop back
PIN 7-9 CLOSE	Selects the on board TUDX2 DOUTR(2) for loop back
PIN 10-12 CLOSE	Selects the on board TUDX2 DOUTR(3) for loop back
PIN 13-15 CLOSE	Selects the on board TUDX2 DOUTR(4) for loop back
PIN 16-18 CLOSE	Selects the on board TUDX2 DOUTR(5) for loop back
PIN 19-21 CLOSE	Selects the on board TUDX2 DOUTR(6) for loop back
PIN 22-24 CLOSE	Selects the on board TUDX2 DOUTR(7) for loop back
PIN 25-27 CLOSE	Selects the on board TUDX2 DOUTR(8) for loop back
PIN 2-3 CLOSE	Selects the on board TUPP-Plus OD(0) for loop back
PIN 5-6 CLOSE	Selects the on board TUPP-Plus OD(1) for loop back
PIN 8-9 CLOSE	Selects the on board TUPP-Plus OD(2) for loop back
PIN 1112 CLOSE	Selects the on board TUPP-Plus OD(3) for loop back
PIN 14-15 CLOSE	Selects the on board TUPP-Plus OD(4) for loop back
PIN 17-18 CLOSE	Selects the on board TUPP-Plus OD(5) for loop back
PIN 20-21 CLOSE	Selects the on board TUPP-Plus OD(6) for loop back
PIN 23-24 CLOSE	Selects the on board TUPP-Plus OD(7) for loop back
PIN 26-27 CLOSE	Selects the on board TUPP-Plus ODP for loop back
ALL PINS OPEN	Select the ADD signal from mated ADM board

HP SDX1155 Optics to/from Cypress CY7B951 Interface

SDX Signal	SDX Type	CY7B-Type	CY7B-Signal	Description
RXDP	O	I	RINP	Bit serial line side receive data positive
RXDN	O	I	RINN	Bit serial line side receive data negative

SD	O	I	CD	Carrier detect signal, low fail
TXDP	I	O	TOUTP	Bit serial line side transmit data positive
TXDN	I	O	TOUTN	Bit serial line side transmit data negative

Cypress CY7B951 to/from STXC Interface

CY7B Signal	CY7B Type	STXC Type	STXC Signal	Description
RCLKP	O	I	RXCP	Receive clock positive
RCLKN	O	I	RXCN	Receive clock negative
RSERP	O	I	RXDP	Bit serial Receive data positive
RSERN	O	I	RXDN	Bit serial Receive data negative
MODE	I	O	SCPO(0)	Mode control, low STS-1, high STS-3/STM-1
LOOP	I	O	SCPO(1)	Loop control, low loopback, high open
LFI*	O	I	RESR	Line fault indication, low line fault
TCLKP	O	I	TXCP	Transmit clock positive
TCLKN	O	I	TXCN	Transmit clock negative
TSERP	I	O	TXDP	Bit serial transmit data positive
TSERN	I	O	TXDN	Bit serial transmit data negative

STXC to/from SPTX Interface

STXC Signal	STXC Type	SPTX Type	SPTX Signal	Description
GRICLK	O	I	RCK	Byte serial receive clock
ROFP	O	I	IFP	Receive frame pulse
ROUT[7]	O	I	RD[7]	Byte serial data bit 7
ROUT[6]	O	I	RD[6]	Byte serial data bit 6
ROUT[5]	O	I	RD[5]	Byte serial data bit 5
ROUT[4]	O	I	RD[4]	Byte serial data bit 4
ROUT[3]	O	I	RD[3]	Byte serial data bit 3
ROUT[2]	O	I	RD[2]	Byte serial data bit 2
ROUT[1]	O	I	RD[1]	Byte serial data bit 1
ROUT[0]	O	I	RD[0]	Byte serial data bit 0
GTICLK	O	I	TCK	Byte serial transmit clock
TIFP	I	O	FPOUT	Transmit frame pulse

TIN[7]	I	O	TD[7]	Byte serial data bit 7
TIN[6]	I	O	TD[6]	Byte serial data bit 6
TIN[5]	I	O	TD[5]	Byte serial data bit 5
TIN[4]	I	O	TD[4]	Byte serial data bit 4
TIN[3]	I	O	TD[3]	Byte serial data bit 3
TIN[2]	I	O	TD[2]	Byte serial data bit 2
TIN[1]	I	O	TD[1]	Byte serial data bit 1
TIN[0]	I	O	TD[0]	Byte serial data bit 0

SPTX to/from TUPP/TUPP-Plus Interface

SPTX Signal	SPTX Type	TUPP Type	TUPP Signal	Description
DD[7]	O	I	DIN/ID[7]	Byte serial data bit 7
DD[6]	O	I	DIN/ID[6]	Byte serial data bit 6
DD[5]	O	I	DIN/ID[5]	Byte serial data bit 5
DD[4]	O	I	DIN/ID[4]	Byte serial data bit 4
DD[3]	O	I	DIN/ID[3]	Byte serial data bit 3
DD[2]	O	I	DIN/ID[2]	Byte serial data bit
DD[1]	O	I	DIN/ID[1]	Byte serial data bit 1
DD[0]	O	I	DIN/ID[0]	Byte serial data bit 0
DC1J1V1	O	I	IC1J1	C1, J1 and V1 frame pulse
DDP	O	I	IPAR/IDP	Data parity
DPL	O	I	ISPE/IPL	Payload active signal

SPTX to/from TIMING CONTROL(TC) block Interface

SPTX Signal	SPTX Type	TC Type	TC Signal	Description
DC1J1V1	O	I	DC1J1V1	C1, J1 and V1 frame pulse
DPL	O	I	DPL	Payload active signal

TUPP/TUPP-Plus to/from TUDX1 Interface

TUPP Signal	TUPP Type	TUDX Type	TUDX1 Signal	Description
OTV5	O	I	DINT[0]	Outgoing tributary V5 byte

OTSPE/ OTPL	O	I	DINT[1]	Outgoing tributary payload envelope
OTPOH	O	I	DINT[2]	Outgoing tributary path overhead signal
AIS	O	I	DINT[3]	Tributary alarm indication signal
IDLE	O	I	DINT[4]	Tributary idle indication signal
LC1J1V1	O	I	DINT[5]	Locked mode composite frame pulse
LPL	O	I	DINT[6]	Locked mode payload active signal
COUT	O	I	DINT[7]	Controlled output signal

TUPP/TUPP-Plus to/from TUDX2 Interface

TUPP Signal	TUPP Type	TUDX Type	TUDX2 Signal	Description
OPAR/ ODP	O	I	DINT[8]	Outgoing data parity signal
DOUT[7]/ OD[7]	O	I	DINT[7]	Byte serial data bit 7
DOUT[6]/ OD[6]	O	I	DINT[6]	Byte serial data bit 6
DOUT[5]/ OD[5]	O	I	DINT[5]	Byte serial data bit 5
DOUT[4]/ OD[4]	O	I	DINT[4]	Byte serial data bit 4
DOUT[3]/ OD[3]	O	I	DINT[3]	Byte serial data bit 3
DOUT[2]/ OD[2]	O	I	DINT[2]	Byte serial data bit 2
DOUT[1]/ OD[1]	O	I	DINT[1]	Byte serial data bit 1
DOUT[0]/ OD[0]	O	I	DINT[0]	Byte serial data bit 0

TUPP from TIMING CONTROL(TC) Interface

TUPP Signal	TUPP Type	TC Type	TC Signal	Description
OTMF	I	O	OTMF	Outgoing tributary multiframe pulse
OC1J1	I	O	OC1	C1 and J1 frame pulse

TUDX1 from TIMING CONTROL(TC) Interface

TUDX Signal	TUDX Type	TC Type	TC Signal	Description
OC1	I	O	OC1	C1 framepulse

TUDX2 from TIMING CONTROL(TC) Interface

TUDX Signal	TUDX Type	TC Type	TC Signal	Description
OC1	I	O	OC1	C1 frame pulse

19.44MHz System Clock Distribution Interface

System Clock (Hz)	To	Name at Destination	Description
19.44MHZ	MAPPER INTERFACE	CLK MAP	Clock to Mapper Interface
19.44MHZ	TIMING CONTROL	CLK TC	19.44Mbyte/s Clock to TIMING CONTROL
19.44MHZ	TUPP	SCLK TUPP	Byte serial down stream data clock
19.44MHZ	TUDX1	SCLK TUDX1	Byte serial tributary cross connection clock
19.44MHZ	TUDX2	SCLK TUDX2	Byte serial tributary cross connection clock
19.44MHZ	RING EXPANSION INTERFACE	ACK EXP	Clock to Ring Expansion Interface
19.44MHZ	J3	ACK	Byte serial up stream data loopback clock
19.44MHZ	SPTX	DCK	Byte serial Down stream data clock

TIMING CONTROL(TC) Interface

Signal	I/O	To/From	Description
DC1J1V1	I	SPTX	Required for counter synchronization
DPL	I	SPTX	Required for counter synchronization
CLK	I	TC	19.44Mbyte/s clock
OTMF	O	TUPP/ TUPP-Plus	Tributary multiframe synchronization
OC1	O	TUPP/ TUPP-Plus , TUDX1, TUDX2	C1 frame pulse

OC1J1	O	Mapper Interface	C1 and J1 synchronization for input data from Mapper Interface
AC1J1V1	O	J3, Ring Expansion Interface, Mapper Interface	C1, J1 and V1 synchronization for input data from TUDX2 output on matted ADM board or Mapper Interface.
APL	O	Ring Expansion Interface, Mapper Interface	Payload active signal for data on TUDX2 outputs.
OC1J1	O	Mapper Interface	Mapper ADD traffic C1 and J1 synchronization
SPA0	O	Unused	Unused
SPA1		Mapper Interface	Spare control bits for mapping interface
SPA2			

Ring Expansion Interface

Signal	I/O	P2 pin	Description
ACK EXP	O	A39	19.44MHz clock
TC APL	O	A35	ADD bus payload signal
TC AC1J1V1	O	A31	ADD bus C1, J1, V1 synchronization signal
EXP ACK	I	A61	19.44MHz clock
EXP APL	I	A65	ADD bus payload signal
EXP AC1J1V1	I	A69	ADD bus C1, J1, V1 synchronization signal
TUDX2 DOUTR[8]	O	A11	ADD bus data parity signal
TUDX2 DOUTR[7]	O	A13	ADD bus data bit 7
TUDX2 DOUTR[6]	O	A15	ADD bus data bit 6
TUDX2 DOUTR[5]	O	A17	ADD bus data bit 5
TUDX2 DOUTR[4]	O	A19	ADD bus data bit 4
TUDX2 DOUTR[3]	O	A21	ADD bus data bit 3

TUDX2 DOUTR[2]	O	A23	ADD bus data bit 2
TUDX2 DOUTR[1]	O	A25	ADD bus data bit 1
TUDX2 DOUTR[0]	O	A27	ADD bus data bit 0
EXP ADP	I	A89	ADD bus data parity signal
EXP AD[7]	I	A87	ADD bus data bit 7
EXP AD[6]	I	A85	ADD bus data bit 6
EXP AD[5]	I	A83	ADD bus data bit 5
EXP AD[4]	I	A81	ADD bus data bit 4
EXP AD[3]	I	A79	ADD bus data bit 3
EXP AD[2]	I	A77	ADD bus data bit 2
EXP AD[1]	I	A75	ADD bus data bit 1
EXP AD[0]	I	A73	ADD bus data bit 0
STXC RRCPCLK	O	A6	Receive Ring control port clock
STXC RRCPFP	O	A10	Receive Ring control port frame pulse
STXC RRCPDAT	O	A14	Receive Ring control port data
STXC TRCPCLK	I	A96	Transmit Ring control port clock
STXC TRCPFP	I	A92	Transmit Ring control port frame pulse
STXC TRCPDAT	I	A88	Transmit Ring control port data
SPTX RPOHCK1	O	A18	Receive path overhead clock1
SPTX RPOHFP1	O	A22	Receive path overhead frame pulse 1
SPTX RAD	O	A26	Receive alarm port data signal
EXP TACK	I	A84	Transmit alarm port clock
EXP TAFP	I	A80	Transmit alarm port frame signal
EXP TAD	I	A76	Transmit alarm port data signal

GND		A1 A2 A30 A49 A50 A99 A100	Ground

Mapper Interface

Signal	I/O	P3 pin	Description
CLK MAP	O	A40	19.44MHz clock
TUDX1 MAP DOUTL[0]	O	A36	DROP tributary V5 byte indication
TUDX1 MAP DOUTL[1]	O	A34	DROP tributary synchronous payload envelope signal marks
TUDX1 MAP DOUTL[2]	O	A32	Outgoing tributary path overhead signal
TUDX1 MAP DOUTL[3]	O	A30	Tributary alarm indication signal
TUDX1 MAP DOUTL[4]	O	A28	Tributary idle indication signal
TUDX1 MAP DOUTL[5]	O	A26	Locked mode composite frame pulse
TUDX1 MAP DOUTL[6]	O	A24	Locked mode payload active signal
TUDX1 MAP DOUTL[7]	O	A22	Controlled output signal
TUDX1 MAP COUTL	O	A18	Left control output signal
TUDX2 MAP COUTL	O	A27	Left control output signal
TUDX2 MAP DOUTL[8]	O	A31	DROP bus data parity signal
TUDX2 MAP DOUTL[7]	O	A33	DROP bus data bit 7
TUDX2 MAP DOUTL[6]	O	A35	DROP bus data bit 6
TUDX2 MAP DOUTL[5]	O	A37	DROP bus data bit 5
TUDX2 MAP DOUTL[4]	O	A39	DROP bus data bit 4

TUDX2 MAP DOUTL[3]	O	A41	DROP bus data bit 3
TUDX2 MAP DOUTL[2]	O	A43	DROP bus data bit 2
TUDX2 MAP DOUTL[1]	O	A45	DROP bus data bit 1
TUDX2 MAP DOUTL[0]	O	A47	DROP bus data bit 0
MAP TUDX2 DINB[8]	I	A38	ADD bus data parity signal
MAP TUDX2 DINB[7]	I	A67	ADD bus data bit 7
MAP TUDX2 DINB[6]	I	A65	ADD bus data bit 6
MAP TUDX2 DINB[5]	I	A63	ADD bus data bit 5
MAP TUDX2 DINB[4]	I	A61	ADD bus data bit 4
MAP TUDX2 DINB[3]	I	A59	ADD bus data bit 3
MAP TUDX2 DINB[2]	I	A57	ADD bus data bit 2
MAP TUDX2 DINB[1]	I	A55	ADD bus data bit 1
MAP TUDX2 DINB[0]	I	A53	ADD bus data bit 0
TC OC1J1	O	A46	ADD bus C1, J1 frame signal
TC APL	O	A48	ADD data payload signal
TC AC1J1V1	O	A50	ADD data C1, J1, V1 frame synchronization
TUPP POHEN [3:1]	O	A3 A5 A7	Tributary path overhead enable signals
TUPP POHFP [3:1]	O	A9 A11 A13	Tributary path overhead frame pulse signals
TUPP POH [3:1]	O	A15 A17 A19	Tributary path overhead signals
TUPP RAD	O	A21	Receive alarm port
TUPP POHCK	O	A23	Tributary path overhead enable signals

MC MAP RSTB[3:1]	O	A66 A64 A62	H/W reset bits
MC MAP CONTROL [3:1]	O	A60 A58 A56	Reserved for mapper control signals
MC MAP CSB	O	A70	Chip select signal
ALE	O	A90	Address latch enable
WRB	O	A87	write strobe signal
RDB	O	A89	read enable signal
D[7:0]	I/O	A88 A86 A84 A82 A80 A78 A76 A74	Data bus
A[11:0]	O	A92 A94 A93 A91 A85 A83 A81 A79 A77 A75 A73 A71	Address bus
INTB	I	A69	Interrupt signal from mapper side
SPARE1	O	A42	Reserved for future use
SPARE2	O	A52	Reserved for future use
VCC	O	A6 A8 A95 A96	+5 v power
GND		A1 A2 A97 A98 A99 A100	Ground

STXC and TUPP-Plus Status LED Display

LED D2	From	Signal	Description
LED1	STXC	OOF	Out of frame indicator
LED2	STXC	LOS	Loss of signal indicator
LED3	STXC	LAIS	Line alarm indication signal indicator
LED4	STXC	FERF	Far end receive failure indicator
LED5	STXC	LOF	Loss of frame indicator
LED6	TUPP-Plus	AIS	Tributary alarm indication signal indicator
LED7	TUPP-Plus	IDLE	Tributary idle indicator
LED8	TUPP-Plus	LOM[1]	Loss of multiframe indicator
LED9	TUPP-Plus	LOM[2]	Loss of multiframe indicator
LED10	TUPP-Plus	LOM[3]	Loss of multiframe indicator

SPTX status LED Display

LED D3	From	Signal	Description
LED1	SPTX	LOP[1]	Loss of pointer indicator
LED2	SPTX	LOP[2]	Loss of pointer indicator
LED3	SPTX	LOP[3]	Loss of pointer indicator
LED4	SPTX	PAIS[1]	Path alarm indication signal indicator
LED5	SPTX	PAIS[2]	Path alarm indication signal indicator
LED6	SPTX	PAIS[3]	Path alarm indication signal indicator
LED7	SPTX	PFERF[1]	Path far end receive failure indicator
LED8	SPTX	PFERF[2]	Path far end receive failure indicator
LED9	SPTX	PFERF[3]	Path far end receive failure indicator
LED10	NA	NA	Unused

SOFTWARE INTERFACE DESCRIPTION

The microprocessor interface provides the 68HC11 on the PM1501 EVBD access to the SARD board memory space via the 96 pin DIN edge connector. The SARD memory space contains three board level configuration registers, the register space of the STXC device, the register space of the SPTX device, the register space of the TUPP/TUPP-Plus device and the register space of the TUDX devices. The complete register map is shown below.

Address Range	Register
C000H	Reserved
C080H	STXC TDIS control , PAGE control and Mapper control Configuration
C100H	Device Reset
C200H-C2FFH	STXC device registers
C300H-C4FFH	SPTX device registers
9000H-9FFFH	Mapper Interface
A000H-AFFFH	TUPP/TUPP-Plus device registers
C600H-C6FFH	TUDX2 device registers
C700H-C7FFH	TUDX1 device registers

SARD General Registers

The SARD reference design contains the following general configuration registers to configure the STXC, SPTX, TUPP/TUPP-Plus and TUDX devices.

Register C080H:
STXC and CONTROL Configuration

Bit	Type	Function	Default
Bit 7	R/W	MCNTRL3	0
Bit 6	R/W	MCNTRL2	0
Bit 5	R/W	MCNTRL1	0
Bit 4	R/W	TDIS	0
Bit 3	R/W	PAGE[3]	0
Bit 2	R/W	PAGE[2]	0
Bit 1	R/W	PAGE[1]	0
Bit 0	R/W	PAGE[0]	0

TDIS:

The Transmit Disable (TDIS) controls overwriting of overhead bytes in the transmit stream of the STXC. When TDIS is set high, most of the overhead passes through unchanged (except K1, B1, B2). When TDIS is low, the overhead bytes will be overwritten as determined by the TTOH and TTOHEN inputs.

PAGE[0] to PAGE[3]:

Bits PAGE[0] through PAGE[3] together is an address which identifies one of the sixteen possible look up tables (4Kbytes deep) within a 64Kbytes on board PROM. PAGE[0] forms the least significant bit of the four most significant bits of the PROM address. PAGE[3] forms the most significant bit of the four most significant bits of the PROM address. One of sixteen tables in the PROM can be selected by these four address bits. Each table contains the timing control signal required by different operation mode. These operating modes are show in the Mode Select Table below.

Mode Select Table

Page[3]	Page[2]	Page[1]	Page[0]	Operation mode
0	0	0	0	STS-3/STM-1(AU3) J1 at location 522
0	0	0	1	STS-3c/STM-1(AU4) J1 at location 522
0	0	1	0	STS-1 J1 at location 522

0	0	1	1	STS-3/STM-1(AU3) J1 at location 0
0	1	0	0	STS-3c/STM-1(AU4) J1 at location 0
0	1	0	1	STS-1 J1 at location 0
Others				Reserved for future use

MCNTRL1 to MCNTRL3:

These bits are reserved for Mapping Interface use.

Register C100H:
Device Reset

Bit	Type	Function	Default
Bit 7	R/W	TUDX1_RSTB	0
Bit 6	R/W	TUDX2_RSTB	0
Bit 5	R/W	TUPP_RSTB	0
Bit 4	R/W	SPTX_RSTB	0
Bit 3	R/W	STXC_RSTB	0
Bit 2	R/W	MRSTB3	0
Bit 1	R/W	MRSTB2	0
Bit 0	R/W	MRSTB1	0

MRSTBn:

These bits are reserved for use by the Mappier Interface.

STXC_RSTB:

This active low reset bit controls the RSTB input of the STXC device. When set to logic one, the STXC device is allowed to operate normally. When set to logic zero, the STXC device is held in reset. The STXC devices remain in reset until a logic one is written to this bit.

SPTX_RSTB:

This active low reset bit controls the RSTB input of the SPTX device. When set to logic one, the SPTX device is allowed to operate normally. When set to logic zero, the SPTX device is held in reset. The SPTX devices remain in reset until a logic one is written to this bit.

TUPP_RSTB:

This active low device reset bit controls the RSTB input of the TUPP/TUPP_Plus device. When set to logic one, the TUPP/TUPP_Plus device is allowed to operate normally. When set to logic zero, the TUPP/TUPP_Plus

device is held in reset. The TUPP/TUPP_Plus device remains in reset until a logic one is written to this bit.

TUDX1_RSTB:

This active low reset bit controls the RSTB input of the TUDX1 device. When set to logic one, the TUDX1 device is allowed to operate normally. When set to logic zero, the TUDX1 device is held in reset. The TUDX1 devices remain in reset until a logic one is written to this bit.

TUDX2_RSTB:

This active low reset bit controls the RSTB input of the TUDX2 device. When set to logic one, the TUDX2 device is allowed to operate normally. When set to logic zero, the TUDX2 device is held in reset. The TUDX2 devices remain in reset until a logic one is written to this bit.

STXC Registers

The STXC address space extends from C200H to C2FFH. For further details, please refer to the SONET/SDH Transport Overhead Terminating Transceiver Datasheet.

Address	Register
C200	Master Configuration
C201	Master Control/Enable
C202	Master Interrupt Status
C203	Master Reset and Identity
C204	TLOP Control
C205	TLOP Diagnostic
C206	Transmit K1
C207	Transmit K2
C208	RLOP Control/Status
C209	RLOP Interrupt
C20A	B2 Error Count #1
C20B	B2 Error Count #2
C20C	B2 Error Count #3
C20D	FEBE Error Count #1
C20E	FEBE Error Count #2
C20F	FEBE Error Count #3
C210	RSOP Control
C211	RSOP Interrupt Status
C212	B1 Error Count #1
C213	B1 Error Count #2
C214	Output Port
C215	Input Port Interrupt Enable
C216	Unused
C217	Ring Control Port
C218	TSOP Control

C219	TSOP Diagnostic
C21A	Transmit Z1
C21B	Receive Z1
C21C	Reserved
C21D	Receive K1
C21E	Receive K2
C21F	Input Port Status/Value
C220	Section Trace Control
C221	Section Trace Status
C222	Section Trace Indirect Address
C223	Section Trace Indirect Data
C224	Section Trace AIS Insertion
C225-C2FF	Reserved for Test
SCPO[0]	CY7B951 mode control signal
SCPO[1]	CY7B951 loopback control signal
SCPO[2]	Indicator disable signal

SPTX Registers

The SPTX address space extends from C300H to C4FFH. For further details, please refer to the SONET/SDH Path Terminating Transceiver Payload Processor Datasheet.

Address	Register
C300	Master Configuration
C301	Master Alarm Configuration
C302	Master Parity Configuration
C303	Master Reset and Identity
C304	Master Interrupt Status #1
C305	Master Interrupt Status #2
C306	Master Transmit Control
C307	Master Loopback, ADD Bus Control
C308	Input Signal Activity Monitor, Accumulation Trigger
C309-0F	Reserved
C310	RPOP #1, Status and Control
C311	RPOP #1, Alarm Interrupt Status
C312	RPOP #1, Pointer Interrupt Status
C313	RPOP #1, Alarm Interrupt Enable
C314	RPOP #1, Pointer Interrupt Enable
C315	RPOP #1, Pointer LSB
C316	RPOP #1, Pointer MSB
C317	RPOP #1, Path Signal Label
C318	RPOP #1, Path BIP-8 Count LSB
C319	RPOP #1, Path BIP-8 Count MSB

C31A	RPOP #1, Path FEBE Count LSB
C31B	RPOP #1, Path FEBE Count MSB
C31C	RPOP #1, Tributary Multiframe Status and Control
C31D	RPOP #1, Tandem Connection and Ring Control
C31E	RPOP #1, Tandem Connection IEC Count LSB
C31F	RPOP #1, Tandem Connection IEC Count MSB
C320	Reserved
C321	PMON #1, Interrupt Enable and Status
C322-23	Reserved
C324	PMON #1, Receive Positive Pointer Justification Count
C325	PMON #1, Receive Negative Pointer Justification Count
C326	PMON #1, Transmit Positive Pointer Justification Count
C327	PMON #1, Transmit Negative Pointer Justification Count
C328	RTAL #1, Control
C329	RTAL #1, Interrupt Status and Control
C32A	RTAL #1, Alarm and Diagnostic Control
C32B- 2F	Reserved
C330	TPOP #1, Control
C331	TPOP #1, Payload Pointer Control
C332	TPOP #1, Source Control
C333	TPOP #1, Current Pointer LSB
C334	TPOP #1, Current Pointer MSB
C335	TPOP #1, Payload Pointer LSB
C336	TPOP #1, Payload Pointer MSB
C337	TPOP #1, Path Trace
C338	TPOP #1, Path Signal Label
C339	TPOP #1, Path Status
C33A	TPOP #1, Path User Channel
C33B	TPOP #1, Path Growth 1
C33C	TPOP #1, Path Growth 2
C33D	TPOP #1, Path Growth 3
C33E	TPOP #1, Concatenation LSB
C33F	TPOP #1, Concatenation MSB
C340	TTAL #1, Control
C341	TTAL #1, Interrupt Status and Control
C342	TTAL #1, Alarm and Diagnostic Control
C343-47	Reserved
C348	SPTB #1, Control
C349	SPTB #1, Status

C34A	SPTB #1, Indirect Address
C34B	SPTB #1, Indirect Data
C34C	SPTB #1, Expected Path Signal Label
C34D	SPTB #1, Path Signal Label Status
C34E-4F	Reserved
C350-5F	RPOP #2 Registers
C360-67	PMON #2 Registers
C368-6B	RTAL #2 Registers
C36C-6F	Reserved
C370-7F	TPOP #2 Registers
C380-83	TTAL #2 Registers
C384-87	Reserved
C388-8F	SPTB #2 Registers
C390-9F	RPOP #3 Registers
C3A0-A7	PMON #3 Registers
C3A8-AB	RTAL #3 Registers
C3AC-AF	Reserved
C3B0-BF	TPOP #3 Registers
C3C0-C3	TTAL #3 Registers
C3C4-C7	Reserved
C3C8-CF	SPTB #3 Registers
C3D0-FF	Reserved
C400	Master Test
C401-FF	Reserved for Test

TUPP & TUPP-Plus Registers

The TUPP address spaces extends from A000H to A0FFH and the TUPP-Plus address spaces extends from A000H to AFFFH. For further details, please refer to the SONET/SDH Tributary Unit Payload Processor Datasheet (PM5361 or PM5362).

Address	Register
A000	Master Incoming Configuration
A001	Master Outgoing Configuration
A002	Input Signal Activity Monitor
A003	Master Reset and Identity
A004	Tributary Payload Processor #1 Configuration
A005	Tributary Payload Processor #2 Configuration
A006	Tributary Payload Processor #3 Configuration
A007	Tributary Payload Processor and H4 OOF Interrupt Enable
A008	Tributary Payload Processor Interrupt Status and H4 OOF Status
A009	Parity Error and H4 OOF Interrupt

A00A-1F	Reserved
A020	TPP #1, TU3, or TU #1 in TUG2 #1, Configuration and Status
A021	TPP #1, TU #1 in TUG2 #2, Configuration and Status
A022	TPP #1, TU #1 in TUG2 #3, Configuration and Status
A023	TPP #1, TU #1 in TUG2 #4, Configuration and Status
A024	TPP #1, TU #1 in TUG2 #5, Configuration and Status
A025	TPP #1, TU #1 in TUG2 #6, Configuration and Status
A026	TPP #1, TU #1 in TUG2 #7, Configuration and Status
A027	TPP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt
A028	TPP #1, TU #2 in TUG2 #1, Configuration and Status
A029	TPP #1, TU #2 in TUG2 #2, Configuration and Status
A02A	TPP #1, TU #2 in TUG2 #3, Configuration and Status
A02B	TPP #1, TU #2 in TUG2 #4, Configuration and Status
A02C	TPP #1, TU #2 in TUG2 #5, Configuration and Status
A02D	TPP #1, TU #2 in TUG2 #6, Configuration and Status
A02E	TPP #1, TU #2 in TUG2 #7, Configuration and Status
A02F	TPP #1, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt
A030	TPP #1, TU #3 in TUG2 #1, Configuration and Status
A031	TPP #1, TU #3 in TUG2 #2, Configuration and Status
A032	TPP #1, TU #3 in TUG2 #3, Configuration and Status
A033	TPP #1, TU #3 in TUG2 #4, Configuration and Status
A034	TPP #1, TU #3 in TUG2 #5, Configuration and Status
A035	TPP #1, TU #3 in TUG2 #6, Configuration and Status
A036	TPP #1, TU #3 in TUG2 #7, Configuration and Status
A037	TPP #1, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt
A038	TPP #1, TU #4 in TUG2 #1, Configuration and Status
A039	TPP #1, TU #4 in TUG2 #2, Configuration and Status
A03A	TPP #1, TU #4 in TUG2 #3, Configuration and Status
A03B	TPP #1, TU #4 in TUG2 #4, Configuration and Status
A03C	TPP #1, TU #4 in TUG2 #5, Configuration and Status
A03D	TPP #1, TU #4 in TUG2 #6, Configuration and Status
A03E	TPP #1, TU #4 in TUG2 #7, Configuration and Status
A03F	TPP #1, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt
A040-5F	Tributary Payload Processor #2 Registers
A060-7F	Tributary Payload Processor #3 Registers
A080	Master Test
A081-FF	Reserved for Test

TUDX1 Registers

The TUDX1 address spaces extends from C700H to C7FFH. For further details, please refer to the SONET/SDH Tributary Unit Cross-connect Datasheet.

Address	Register
C700	Master Configuration
C701	Connection Memory Control
C702	Clock Monitor
C703	Master Reset/Revision ID
C704	Parity Configuration
C705	Parity Error Interrupt Enable
C706	Parity Error Interrupt Status
C707	Systolic Delay Control
C708	Left Switch Element Connection Address High
C709	Left Switch Element Connection Address Low
C70A	Left Switch Element Connection Data High
C70B	Left Switch Element Connection Data Low
C70C	Right Switch Element Connection Address High
C70D	Right Switch Element Connection Address Low
C70E	Right Switch Element Connection Data High
C70F	Right Switch Element Connection Data Low
C710	Master Test
C711-1F	Reserved for Test

TUDX2 Registers

The TUDX2 address spaces extends from C600H to C6FFH. For further details, please refer to the SONET/SDH Tributary Unit Cross-connect Datasheet.

Address	Register
C600	Master Configuration
C601	Connection Memory Control
C602	Clock Monitor
C603	Master Reset/Revision ID
C604	Parity Configuration
C605	Parity Error Interrupt Enable
C606	Parity Error Interrupt Status
C607	Systolic Delay Control
C608	Left Switch Element Connection Address High
C609	Left Switch Element Connection Address Low
C60A	Left Switch Element Connection Data High
C60B	Left Switch Element Connection Data Low

C60C	Right Switch Element Connection Address High
C60D	Right Switch Element Connection Address Low
C60E	Right Switch Element Connection Data High
C60F	Right Switch Element Connection Data Low
C610	Master Test
C611-1F	Reserved for Test

ON BOARD PROM

The PROM device can be programmed to generate various control signals. The output on U47 pin 3 (AC1J1V1) and the buffer(U38) pin Q4(APL) controls the SPTX's ADD bus and the outgoing traffic on the Mapper and Ring Expansion Interfaces. The output on the buffer pin Q0 controls the outgoing tributary multiframe on the TUPP/TUPP_Plus by clocking an external 2 bit counter. The output on buffer pin Q2(OC1) controls the frame sychronization on the TUDX1, TUDX2 devices and also controls the outgoing frame alignment of the TUPP/TUPP_Plus when it is operating in locked mode. The output on buffer pin Q5(OC1J1) controls the ADD traffic frame synchronization at the Mapper Interface. The buffer output pins Q6 and Q7 are routed to the Ring Expansion Interface and the Mapper Interface respectively and can be used as desired. The following table shows the contents of the PROM(U15) required for operation at STS-3, STS-3c and STS-1 when the J1 output from the TUPP/TUPP-Plus is locked at a pointer of 522 or 0.

PAGE 0 STS-3/STM-1(AU3) with J1 Locked at 522

ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	PROM DATA	Description
HEX	SPA2	SPA1	OC1J1	APL	AV1	OC1	SPA0	OTMF	HEX	Signal Name
0	1	1	0	1	0	0	0	1	D1	
1	1	1	0	1	0	0	0	1	D1	
2	1	1	0	1	0	0	0	1	D1	
3	1	1	0	0	0	0	0	1	C1	APL (9th row)
4	1	1	0	0	0	1	0	1	C5	APL & OC1
5	1	1	0	0	0	0	0	1	C1	APL
6	1	1	0	0	0	0	0	1	C1	APL
7	1	1	0	0	0	0	0	1	C1	APL
8	1	1	0	0	0	0	0	1	C1	APL
9	1	1	0	0	0	0	0	1	C1	APL
A	1	1	0	0	0	0	0	1	C1	APL
B	1	1	0	0	0	0	0	1	C1	APL
C-110	1	0	1	0	0	0	1	D1		
111	1	1	0	0	0	0	0	1	C1	APL (1st row)
112	1	1	0	0	0	0	0	1	C1	APL
113	1	1	0	0	0	0	0	1	C1	APL
114	1	1	0	0	0	0	0	1	C1	APL
115	1	1	0	0	0	0	0	1	C1	APL
116	1	1	0	0	0	0	0	1	C1	APL
117	1	1	1	0	0	0	0	1	E1	APL & C1
118	1	1	0	0	0	0	0	1	C1	APL
119	1	1	0	0	0	0	0	1	C1	APL

11A	1	1	1	1	0	0	0	1	F1	J1
11B	1	1	1	1	0	0	0	1	F1	J1
11C	1	1	1	1	0	0	0	1	F1	J1
11D	1	1	0	1	1	0	0	1	D9	V1
11E	1	1	0	1	1	0	0	1	D9	V1
11F	1	1	0	1	1	0	0	1	D9	V1
120-21E	1	1	0	1	0	0	0	1	D1	
21F	1	1	0	0	0	0	0	1	C1	APL(2nd row)
220	1	1	0	0	0	0	0	1	C1	APL
221	1	1	0	0	0	0	0	1	C1	APL
222	1	1	0	0	0	0	0	1	C1	APL
223	1	1	0	0	0	0	0	1	C1	APL
224	1	1	0	0	0	0	0	1	C1	APL
225	1	1	0	0	0	0	0	1	C1	APL
226	1	1	0	0	0	0	0	1	C1	APL
227	1	1	0	0	0	0	0	1	C1	APL
228-32C	1	1	0	1	0	0	0	1	D1	
32D	1	1	0	0	0	0	0	1	C1	APL (3rd row)
32E	1	1	0	0	0	0	0	1	C1	APL
32F	1	1	0	0	0	0	0	1	C1	APL
330	1	1	0	0	0	0	0	1	C1	APL
331	1	1	0	0	0	0	0	1	C1	APL
332	1	1	0	0	0	0	0	1	C1	APL
333	1	1	0	0	0	0	0	1	C1	APL
334	1	1	0	0	0	0	0	1	C1	APL
335	1	1	0	0	0	0	0	1	C1	APL
336-43A	1	1	0	1	0	0	0	1	D1	
43B	1	1	0	0	0	0	0	1	C1	APL (4th row)
43C	1	1	0	0	0	0	0	1	C1	APL
43D	1	1	0	0	0	0	0	1	C1	APL
43E	1	1	0	0	0	0	0	1	C1	APL
43F	1	1	0	0	0	0	0	1	C1	APL
440	1	1	0	0	0	0	0	1	C1	APL
441	1	1	0	0	0	0	0	1	C1	APL
442	1	1	0	0	0	0	0	1	C1	APL
443	1	1	0	0	0	0	0	1	C1	APL
444-548	1	1	0	1	0	0	0	1	D1	
549	1	1	0	0	0	0	0	1	C1	APL (5th row)
54A	1	1	0	0	0	0	0	1	C1	APL
54B	1	1	0	0	0	0	0	1	C1	APL
54C	1	1	0	0	0	0	0	1	C1	APL
54D	1	1	0	0	0	0	0	1	C1	APL
54E	1	1	0	0	0	0	0	1	C1	APL

54F	1	1	0	0	0	0	0	1	C1	APL
550	1	1	0	0	0	0	0	1	C1	APL
551	1	1	0	0	0	0	0	1	C1	APL
552-656	1	1	0	1	0	0	0	1	D1	
657	1	1	0	0	0	0	0	1	C1	APL (6th row)
658	1	1	0	0	0	0	0	1	C1	APL
659	1	1	0	0	0	0	0	1	C1	APL
65A	1	1	0	0	0	0	0	1	C1	APL
65B	1	1	0	0	0	0	0	1	C1	APL
65C	1	1	0	0	0	0	0	1	C1	APL
65D	1	1	0	0	0	0	0	1	C1	APL
65E	1	1	0	0	0	0	0	1	C1	APL
65F	1	1	0	0	0	0	0	1	C1	APL
660-764	1	1	0	1	0	0	0	1	D1	
765	1	1	0	0	0	0	0	1	C1	APL (7th row)
766	1	1	0	0	0	0	0	1	C1	APL
767	1	1	0	0	0	0	0	1	C1	APL
768	1	1	0	0	0	0	0	1	C1	APL
769	1	1	0	0	0	0	0	1	C1	APL
76A	1	1	0	0	0	0	0	1	C1	APL
76B	1	1	0	0	0	0	0	1	C1	APL
76C	1	1	0	0	0	0	0	1	C1	APL
76D	1	1	0	0	0	0	0	1	C1	APL
76E-872	1	1	0	1	0	0	0	1	D1	
873	1	1	0	0	0	0	0	1	C1	APL (8th row)
874	1	1	0	0	0	0	0	1	C1	APL
875	1	1	0	0	0	0	0	1	C1	APL
876	1	1	0	0	0	0	0	1	C1	APL
877	1	1	0	0	0	0	0	1	C1	APL
878	1	1	0	0	0	0	0	1	C1	APL
879	1	1	0	0	0	0	0	1	C1	APL
87A	1	1	0	0	0	0	0	1	C1	APL
87B	1	1	0	0	0	0	0	1	C1	APL
87C-97E	1	1	0	1	0	0	0	0	D0	OTMF trigger
97F-0FFF	1	1	1	1	1	1	1	1	FF	Unused

PAGE 1 STS-3c/STM-1(AU4) with J1 Located at 522

ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	PROM DATA	Description
HEX	SPA2	SPA1	OC1J1	APL	AV1	OC1	SPA0	OTMF	HEX	
1000	1	1	0	1	0	0	0	1	D1	

1001	1	1	0	1	0	0	0	1	D1	
1002	1	1	0	1	0	0	0	1	D1	
1003	1	1	0	0	0	0	0	1	C1	APL (9th row)
1004	1	1	0	0	0	1	0	1	C5	APL & OC1
1005	1	1	0	0	0	0	0	1	C1	APL
1006	1	1	0	0	0	0	0	1	C1	APL
1007	1	1	0	0	0	0	0	1	C1	APL
1008	1	1	0	0	0	0	0	1	C1	APL
1009	1	1	0	0	0	0	0	1	C1	APL
100A	1	1	0	0	0	0	0	1	C1	APL
100B	1	1	0	0	0	0	0	1	C1	APL
100C-1110	1	1	0	1	0	0	0	1	D1	
1111	1	1	0	0	0	0	0	1	C1	APL (1st row)
1112	1	1	0	0	0	0	0	1	C1	APL
1113	1	1	0	0	0	0	0	1	C1	APL
1114	1	1	0	0	0	0	0	1	C1	APL
1115	1	1	0	0	0	0	0	1	C1	APL
1116	1	1	0	0	0	0	0	1	C1	APL
1117	1	1	1	0	0	0	0	1	E1	APL & C1
1118	1	1	0	0	0	0	0	1	C1	APL
1119	1	1	0	0	0	0	0	1	C1	APL
111A	1	1	1	1	0	0	0	1	F1	J1
111B	1	1	0	1	0	0	0	1	D1	
111C	1	1	0	1	0	0	0	1	D1	
111D	1	1	0	1	1	0	0	1	D9	V1
111E	1	1	0	1	0	0	0	1	D1	
111F	1	1	0	1	0	0	0	1	D1	
1120-121E	1	1	0	1	0	0	0	1	D1	
121F	1	1	0	0	0	0	0	1	C1	APL (2nd row)
1220	1	1	0	0	0	0	0	1	C1	APL
1221	1	1	0	0	0	0	0	1	C1	APL
1222	1	1	0	0	0	0	0	1	C1	APL
1223	1	1	0	0	0	0	0	1	C1	APL
1224	1	1	0	0	0	0	0	1	C1	APL
1225	1	1	0	0	0	0	0	1	C1	APL
1226	1	1	0	0	0	0	0	1	C1	APL
1227	1	1	0	0	0	0	0	1	C1	APL
1228-132C	1	1	0	1	0	0	0	1	D1	
132D	1	1	0	0	0	0	0	1	C1	APL (3rd row)
132E	1	1	0	0	0	0	0	1	C1	APL
132F	1	1	0	0	0	0	0	1	C1	APL
1330	1	1	0	0	0	0	0	1	C1	APL
1331	1	1	0	0	0	0	0	1	C1	APL

1332	1	1	0	0	0	0	0	1	C1	APL
1333	1	1	0	0	0	0	0	1	C1	APL
1334	1	1	0	0	0	0	0	1	C1	APL
1335	1	1	0	0	0	0	0	1	C1	APL
1336-143A	1	1	0	1	0	0	0	1	D1	
143B	1	1	0	0	0	0	0	1	C1	APL (4th row)
143C	1	1	0	0	0	0	0	1	C1	APL
143D	1	1	0	0	0	0	0	1	C1	APL
143E	1	1	0	0	0	0	0	1	C1	APL
143F	1	1	0	0	0	0	0	1	C1	APL
1440	1	1	0	0	0	0	0	1	C1	APL
1441	1	1	0	0	0	0	0	1	C1	APL
1442	1	1	0	0	0	0	0	1	C1	APL
1443	1	1	0	0	0	0	0	1	C1	APL
1444-1548	1	1	0	1	0	0	0	1	D1	
1549	1	1	0	0	0	0	0	1	C1	APL (5th row)
154A	1	1	0	0	0	0	0	1	C1	APL
154B	1	1	0	0	0	0	0	1	C1	APL
154C	1	1	0	0	0	0	0	1	C1	APL
154D	1	1	0	0	0	0	0	1	C1	APL
154E	1	1	0	0	0	0	0	1	C1	APL
154F	1	1	0	0	0	0	0	1	C1	APL
1550	1	1	0	0	0	0	0	1	C1	APL
1551	1	1	0	0	0	0	0	1	C1	APL
1552-1656	1	1	0	1	0	0	0	1	D1	
1657	1	1	0	0	0	0	0	1	C1	APL (6th row)
1658	1	1	0	0	0	0	0	1	C1	APL
1659	1	1	0	0	0	0	0	1	C1	APL
165A	1	1	0	0	0	0	0	1	C1	APL
165B	1	1	0	0	0	0	0	1	C1	APL
165C	1	1	0	0	0	0	0	1	C1	APL
165D	1	1	0	0	0	0	0	1	C1	APL
165E	1	1	0	0	0	0	0	1	C1	APL
165F	1	1	0	0	0	0	0	1	C1	APL
1660-1764		1	1	0	1	0	0	0	1	D1
1765	1	1	0	0	0	0	0	1	C1	APL (7th row)
1766	1	1	0	0	0	0	0	1	C1	APL
1767	1	1	0	0	0	0	0	1	C1	APL
1768	1	1	0	0	0	0	0	1	C1	APL
1769	1	1	0	0	0	0	0	1	C1	APL
176A	1	1	0	0	0	0	0	1	C1	APL
176B	1	1	0	0	0	0	0	1	C1	APL
176C	1	1	0	0	0	0	0	1	C1	APL

176D	1	1	0	0	0	0	0	1	C1	APL
176E-1872		1	1	0	1	0	0	0	1	D1
1873	1	1	0	0	0	0	0	1	C1	APL (8th row)
1874	1	1	0	0	0	0	0	1	C1	APL
1875	1	1	0	0	0	0	0	1	C1	APL
1876	1	1	0	0	0	0	0	1	C1	APL
1877	1	1	0	0	0	0	0	1	C1	APL
1878	1	1	0	0	0	0	0	1	C1	APL
1879	1	1	0	0	0	0	0	1	C1	APL
187A	1	1	0	0	0	0	0	1	C1	APL
187B	1	1	0	0	0	0	0	1	C1	APL
187C-197E	1	1	0	1	0	0	0	0	D0	OTMF trigger
197F-1FFF	1	1	1	1	1	1	1	1	FF	Unused

PAGE 2 STS-1 with J1 Located at 522

ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	PROM DATA	Description
HEX	SPA2	SPA1	OC1J1	APL	AV1	OC1	SPA0	OTMF	HEX	
2000	1	1	0	1	0	0	0	1	D1	
2001	1	1	0	1	0	0	0	1	D1	
2002	1	1	0	1	0	0	0	1	D1	
2003	1	1	0	1	0	0	0	1	D1	
2004	1	1	0	1	0	1	0	1	D5	OC1
2005	1	1	0	1	0	0	0	1	D1	
2006	1	1	0	1	0	0	0	1	D1	
2007	1	1	0	0	0	0	0	1	C1	APL (9th row)
2008	1	1	0	0	0	0	0	1	C1	APL
2009	1	1	0	0	0	0	0	1	C1	APL
200A-2060	1	1	0	1	0	0	0	1	D1	
2061	1	1	0	0	0	0	0	1	C1	APL (1st row)
2062	1	1	0	0	0	0	0	1	C1	APL
2063	1	1	1	0	0	0	0	1	E1	APL & C1
2064	1	1	1	1	0	0	0	1	F1	J1
2065	1	1	0	1	1	0	0	1	D9	V1
2066-20BA	1	1	0	1	0	0	0	1	D1	
20BB	1	1	0	0	0	0	0	1	C1	APL (2nd row)
20BC	1	1	0	0	0	0	0	1	C1	APL
20BD	1	1	0	0	0	0	0	1	C1	APL
20BE-2114	1	1	0	1	0	0	0	1	D1	
2115	1	1	0	0	0	0	0	1	C1	APL (3rd row)
2116	1	1	0	0	0	0	0	1	C1	APL
2117	1	1	0	0	0	0	0	1	C1	APL

2118-216E	1	1	0	1	0	0	0	1	D1	
216F	1	1	0	0	0	0	0	1	C1	APL (4th row)
2170	1	1	0	0	0	0	0	1	C1	APL
2171	1	1	0	0	0	0	0	1	C1	APL
2172 -21C8	1	1	0	1	0	0	0	1	D1	
21C9	1	1	0	0	0	0	0	1	C1	APL (5th row)
21CA	1	1	0	0	0	0	0	1	C1	APL
21CB	1	1	0	0	0	0	0	1	C1	APL
21CC-2222		1	1	0	1	0	0	0	1	D1
2223	1	1	0	0	0	0	0	1	C1	APL (6th row)
2224	1	1	0	0	0	0	0	1	C1	APL
2225	1	1	0	0	0	0	0	1	C1	APL
2226-227C	1	1	0	1	0	0	0	1	D1	
227D	1	1	0	0	0	0	0	1	C1	APL (7th row)
227E	1	1	0	0	0	0	0	1	C1	APL
227F	1	1	0	0	0	0	0	1	C1	APL
2280-22D6	1	1	0	1	0	0	0	1	D1	
22D7	1	1	0	0	0	0	0	1	C1	APL (8th row)
22D8	1	1	0	0	0	0	0	1	C1	APL
22D9	1	1	0	0	0	0	0	1	C1	APL
22DA-232A	1	1	0	1	0	0	0	0	D0	OTMF trigger
232B-2FFF	1	1	1	1	1	1	1	1	FF	Unused

PAGE 3 STS-3/STM-1(AU3) with J1 Located at 0

ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	PROM DATA	Description
HEX	SPA2	SPA1	OC1J1	APL	AV1	OC1	SPA0	OTMF	HEX	
3000	1	1	0	1	0	0	0	1	D1	
3001	1	1	0	1	0	0	0	1	D1	
3002	1	1	0	1	0	0	0	1	D1	
3003	1	1	0	0	0	0	0	1	C1	APL (9th row)
3004	1	1	0	0	0	1	0	1	C5	APL & OC1
3005	1	1	0	0	0	0	0	1	C1	APL
3006	1	1	0	0	0	0	0	1	C1	APL
3007	1	1	0	0	0	0	0	1	C1	APL
3008	1	1	0	0	0	0	0	1	C1	APL
3009	1	1	0	0	0	0	0	1	C1	APL
300A	1	1	0	0	0	0	0	1	C1	APL
300B	1	1	0	0	0	0	0	1	C1	APL
300C-3110	1	1	0	1	0	0	0	1	D1	
3111	1	1	0	0	0	0	0	1	C1	APL (1st row)

3112	1	1	0	0	0	0	0	1	C1	APL
3113	1	1	0	0	0	0	0	1	C1	APL
3114	1	1	0	0	0	0	0	1	C1	APL
3115	1	1	0	0	0	0	0	1	C1	APL
3116	1	1	0	0	0	0	0	1	C1	APL
3117	1	1	1	0	0	0	0	1	E1	APL & C1
3118	1	1	0	0	0	0	0	1	C1	APL
3119	1	1	0	0	0	0	0	1	C1	APL
311A-321E	1	1	0	1	0	0	0	1	D1	
321F	1	1	0	0	0	0	0	1	C1	APL (2nd row)
3220	1	1	0	0	0	0	0	1	C1	APL
3221	1	1	0	0	0	0	0	1	C1	APL
3222	1	1	0	0	0	0	0	1	C1	APL
3223	1	1	0	0	0	0	0	1	C1	APL
3224	1	1	0	0	0	0	0	1	C1	APL
3225	1	1	0	0	0	0	0	1	C1	APL
3226	1	1	0	0	0	0	0	1	C1	APL
3227	1	1	0	0	0	0	0	1	C1	APL
3228-332C	1	1	0	1	0	0	0	1	D1	
332D	1	1	0	0	0	0	0	1	C1	APL (3rd row)
332E	1	1	0	0	0	0	0	1	C1	APL
332F	1	1	0	0	0	0	0	1	C1	APL
3330	1	1	0	0	0	0	0	1	C1	APL
3331	1	1	0	0	0	0	0	1	C1	APL
3332	1	1	0	0	0	0	0	1	C1	APL
3333	1	1	0	0	0	0	0	1	C1	APL
3334	1	1	0	0	0	0	0	1	C1	APL
3335	1	1	0	0	0	0	0	1	C1	APL
3336-343A	1	1	0	1	0	0	0	1	D1	
343B	1	1	0	0	0	0	0	1	C1	APL (4th row)
343C	1	1	0	0	0	0	0	1	C1	APL
343D	1	1	0	0	0	0	0	1	C1	APL
343E	1	1	0	0	0	0	0	1	C1	APL
343F	1	1	0	0	0	0	0	1	C1	APL
3440	1	1	0	0	0	0	0	1	C1	APL
3441	1	1	0	0	0	0	0	1	C1	APL
3442	1	1	0	0	0	0	0	1	C1	APL
3443	1	1	0	0	0	0	0	1	C1	APL
3444	1	1	1	1	0	0	0	1	F1	J1
3445	1	1	1	1	0	0	0	1	F1	J1
3446	1	1	1	1	0	0	0	1	F1	J1
3447	1	1	0	1	1	0	0	1	D9	V1
3448	1	1	0	1	1	0	0	1	D9	V1

3449	1	1	0	1	1	0	0	1	D9	V1
344A-3548	1	1	0	1	0	0	0	1	D1	
3549	1	1	0	0	0	0	0	1	C1	APL (5th row)
354A	1	1	0	0	0	0	0	1	C1	APL
354B	1	1	0	0	0	0	0	1	C1	APL
354C	1	1	0	0	0	0	0	1	C1	APL
354D	1	1	0	0	0	0	0	1	C1	APL
354E	1	1	0	0	0	0	0	1	C1	APL
354F	1	1	0	0	0	0	0	1	C1	APL
3550	1	1	0	0	0	0	0	1	C1	APL
3551	1	1	0	0	0	0	0	1	C1	APL
3552-3656	1	1	0	1	0	0	0	1	D1	
3657	1	1	0	0	0	0	0	1	C1	APL (6th row)
3658	1	1	0	0	0	0	0	1	C1	APL
3659	1	1	0	0	0	0	0	1	C1	APL
365A	1	1	0	0	0	0	0	1	C1	APL
365B	1	1	0	0	0	0	0	1	C1	APL
365C	1	1	0	0	0	0	0	1	C1	APL
365D	1	1	0	0	0	0	0	1	C1	APL
365E	1	1	0	0	0	0	0	1	C1	APL
365F	1	1	0	0	0	0	0	1	C1	APL
3660-3764		1	1	0	1	0	0	0	1	D1
3765	1	1	0	0	0	0	0	1	C1	APL (7th row)
3766	1	1	0	0	0	0	0	1	C1	APL
3767	1	1	0	0	0	0	0	1	C1	APL
3768	1	1	0	0	0	0	0	1	C1	APL
3769	1	1	0	0	0	0	0	1	C1	APL
376A	1	1	0	0	0	0	0	1	C1	APL
376B	1	1	0	0	0	0	0	1	C1	APL
376C	1	1	0	0	0	0	0	1	C1	APL
376D	1	1	0	0	0	0	0	1	C1	APL
376E-3872		1	1	0	1	0	0	0	1	D1
3873	1	1	0	0	0	0	0	1	C1	APL (8th row)
3874	1	1	0	0	0	0	0	1	C1	APL
3875	1	1	0	0	0	0	0	1	C1	APL
3876	1	1	0	0	0	0	0	1	C1	APL
3877	1	1	0	0	0	0	0	1	C1	APL
3878	1	1	0	0	0	0	0	1	C1	APL
3879	1	1	0	0	0	0	0	1	C1	APL
387A	1	1	0	0	0	0	0	1	C1	APL
387B	1	1	0	0	0	0	0	1	C1	APL
387C-397E	1	1	0	1	0	0	0	0	D0	OTMF trigger
397F -3FFF	1	1	1	1	1	1	1	1	FF	Unused

PAGE 4 STS-3c/STM-1(AU4) with J1 Located at 0

ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	PROM DATA	Description
HEX	SPA2	SPA1	OC1J1	APL	AV1	OC1	SPA0	OTMF	HEX	
4000	1	1	0	1	0	0	0	1	D1	
4001	1	1	0	1	0	0	0	1	D1	
4002	1	1	0	1	0	0	0	1	D1	
4003	1	1	0	0	0	0	0	1	C1	APL (9th row)
4004	1	1	0	0	0	1	0	1	C5	APL & OC1
4005	1	1	0	0	0	0	0	1	C1	APL
4006	1	1	0	0	0	0	0	1	C1	APL
4007	1	1	0	0	0	0	0	1	C1	APL
4008	1	1	0	0	0	0	0	1	C1	APL
4009	1	1	0	0	0	0	0	1	C1	APL
400A	1	1	0	0	0	0	0	1	C1	APL
400B	1	1	0	0	0	0	0	1	C1	APL
400C-4110	1	1	0	1	0	0	0	1	D1	
4111	1	1	0	0	0	0	0	1	C1	APL (1st row)
4112	1	1	0	0	0	0	0	1	C1	APL
4113	1	1	0	0	0	0	0	1	C1	APL
4114	1	1	0	0	0	0	0	1	C1	APL
4115	1	1	0	0	0	0	0	1	C1	APL
4116	1	1	0	0	0	0	0	1	C1	APL
4117	1	1	1	0	0	0	0	1	E1	APL & C1
4118	1	1	0	0	0	0	0	1	C1	APL
4119	1	1	0	0	0	0	0	1	C1	APL
411A -421E	1	1	0	1	0	0	0	1	D1	
421F	1	1	0	0	0	0	0	1	C1	APL (2nd row)
4220	1	1	0	0	0	0	0	1	C1	APL
4221	1	1	0	0	0	0	0	1	C1	APL
4222	1	1	0	0	0	0	0	1	C1	APL
4223	1	1	0	0	0	0	0	1	C1	APL
4224	1	1	0	0	0	0	0	1	C1	APL
4225	1	1	0	0	0	0	0	1	C1	APL
4226	1	1	0	0	0	0	0	1	C1	APL
4227	1	1	0	0	0	0	0	1	C1	APL
4228-432C	1	1	0	1	0	0	0	1	D1	
432D	1	1	0	0	0	0	0	1	C1	APL (3rd row)
432E	1	1	0	0	0	0	0	1	C1	APL
432F	1	1	0	0	0	0	0	1	C1	APL

4330	1	1	0	0	0	0	0	1	C1	APL
4331	1	1	0	0	0	0	0	1	C1	APL
4332	1	1	0	0	0	0	0	1	C1	APL
4333	1	1	0	0	0	0	0	1	C1	APL
4334	1	1	0	0	0	0	0	1	C1	APL
4335	1	1	0	0	0	0	0	1	C1	APL
4336-443A	1	1	0	1	0	0	0	1	D1	
443B	1	1	0	0	0	0	0	1	C1	APL (4th row)
443C	1	1	0	0	0	0	0	1	C1	APL
443D	1	1	0	0	0	0	0	1	C1	APL
443E	1	1	0	0	0	0	0	1	C1	APL
443F	1	1	0	0	0	0	0	1	C1	APL
4440	1	1	0	0	0	0	0	1	C1	APL
4441	1	1	0	0	0	0	0	1	C1	APL
4442	1	1	0	0	0	0	0	1	C1	APL
4443	1	1	0	0	0	0	0	1	C1	APL
4444	1	1	1	1	0	0	0	1	F1	J1
4445	1	1	0	1	0	0	0	1	D1	
4446	1	1	0	1	0	0	0	1	D1	
4447	1	1	0	1	1	0	0	1	D9	V1
4448	1	1	0	1	0	0	0	1	D1	
4449	1	1	0	1	0	0	0	1	D1	
444A-4548		1	1	0	1	0	0	0	1	D1
4549	1	1	0	0	0	0	0	1	C1	APL (5th row)
454A	1	1	0	0	0	0	0	1	C1	APL
454B	1	1	0	0	0	0	0	1	C1	APL
454C	1	1	0	0	0	0	0	1	C1	APL
454D	1	1	0	0	0	0	0	1	C1	APL
454E	1	1	0	0	0	0	0	1	C1	APL
454F	1	1	0	0	0	0	0	1	C1	APL
4550	1	1	0	0	0	0	0	1	C1	APL
4551	1	1	0	0	0	0	0	1	C1	APL
4552-4656	1	1	0	1	0	0	0	1	D1	
4657	1	1	0	0	0	0	0	1	C1	APL (6th row)
4658	1	1	0	0	0	0	0	1	C1	APL
4659	1	1	0	0	0	0	0	1	C1	APL
465A	1	1	0	0	0	0	0	1	C1	APL
465B	1	1	0	0	0	0	0	1	C1	APL
465C	1	1	0	0	0	0	0	1	C1	APL
465D	1	1	0	0	0	0	0	1	C1	APL
465E	1	1	0	0	0	0	0	1	C1	APL
465F	1	1	0	0	0	0	0	1	C1	APL
4660-4764	1	1	0	1	0	0	0	1	D1	

4765	1	1	0	0	0	0	0	1	C1	APL (7th row)
4766	1	1	0	0	0	0	0	1	C1	APL
4767	1	1	0	0	0	0	0	1	C1	APL
4768	1	1	0	0	0	0	0	1	C1	APL
4769	1	1	0	0	0	0	0	1	C1	APL
476A	1	1	0	0	0	0	0	1	C1	APL
476B	1	1	0	0	0	0	0	1	C1	APL
476C	1	1	0	0	0	0	0	1	C1	APL
476D	1	1	0	0	0	0	0	1	C1	APL
476E-4872		1	1	0	1	0	0	0	1	D1
4873	1	1	0	0	0	0	0	1	C1	APL (8th row)
4874	1	1	0	0	0	0	0	1	C1	APL
4875	1	1	0	0	0	0	0	1	C1	APL
4876	1	1	0	0	0	0	0	1	C1	APL
4877	1	1	0	0	0	0	0	1	C1	APL
4878	1	1	0	0	0	0	0	1	C1	APL
4879	1	1	0	0	0	0	0	1	C1	APL
487A	1	1	0	0	0	0	0	1	C1	APL
487B	1	1	0	0	0	0	0	1	C1	APL
487C-497E	1	1	0	1	0	0	0	0	D0	OTMF trigger
497F-4FFF	1	1	1	1	1	1	1	1	FF	Unused

PAGE 5 STS-5 with J1 Located at 0

ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	PROM DATA	Description
HEX	SPA2	SPA1	OC1J1	APL	AV1	OC1	SPA0	OTMF	HEX	
5000	1	1	0	1	0	0	0	1	D1	
5001	1	1	0	1	0	0	0	1	D1	
5002	1	1	0	1	0	0	0	1	D1	
5003	1	1	0	1	0	0	0	1	D1	
5004	1	1	0	1	0	1	0	1	D5	OC1
5005	1	1	0	1	0	0	0	1	D1	
5006	1	1	0	1	0	0	0	1	D1	
5007	1	1	0	0	0	0	0	1	C1	APL (9th row)
5008	1	1	0	0	0	0	0	1	C1	APL
5009	1	1	0	0	0	0	0	1	C1	APL
500A-5060		1	1	0	1	0	0	0	1	D1
5061	1	1	0	0	0	0	0	1	C1	APL (1st row)
5062	1	1	0	0	0	0	0	1	C1	APL
5063	1	1	1	0	0	0	0	1	E1	APL & C1
5066-50BA	1	1	0	1	0	0	0	1	D1	

50BB	1	1	0	0	0	0	0	1	C1	APL (2nd row)
50BC	1	1	0	0	0	0	0	1	C1	APL
50BD	1	1	0	0	0	0	0	1	C1	APL
50BE-5114	1	1	0	1	0	0	0	1	D1	
5115	1	1	0	0	0	0	0	1	C1	APL (3rd row)
5116	1	1	0	0	0	0	0	1	C1	APL
5117	1	1	0	0	0	0	0	1	C1	APL
5118-516E	1	1	0	1	0	0	0	1	D1	
516F	1	1	0	0	0	0	0	1	C1	APL (4th row)
5170	1	1	0	0	0	0	0	1	C1	APL
5171	1	1	0	0	0	0	0	1	C1	APL
5172	1	1	1	1	0	0	0	1	F1	J1
5173	1	1	0	1	1	0	0	1	D9	V1
5174 -51C8	1	1	0	1	0	0	0	1	D1	
51C9	1	1	0	0	0	0	0	1	C1	APL (5th row)
51CA	1	1	0	0	0	0	0	1	C1	APL
51CB	1	1	0	0	0	0	0	1	C1	APL
51CC-5222		1	1	0	1	0	0	0	1	D1
5223	1	1	0	0	0	0	0	1	C1	APL (6th row)
5224	1	1	0	0	0	0	0	1	C1	APL
5225	1	1	0	0	0	0	0	1	C1	APL
5226-527C	1	1	0	1	0	0	0	1	D1	
527D	1	1	0	0	0	0	0	1	C1	APL (7th row)
527E	1	1	0	0	0	0	0	1	C1	APL
527F	1	1	0	0	0	0	0	1	C1	APL
5280 -52D6	1	1	0	1	0	0	0	1	D1	
52D7	1	1	0	0	0	0	0	1	C1	APL (8th row)
52D8	1	1	0	0	0	0	0	1	C1	APL
52D9	1	1	0	0	0	0	0	1	C1	APL
52DA-532A	1	1	0	1	0	0	0	0	D0	OTMF trigger
532B-5FFF	1	1	1	1	1	1	1	1	FF	Unused

D.C. CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
VDD	+5V DC Power Supply Voltage	4.5	5.5	V	
IDD	+5V DC Power Supply Current		2.5	A	VDD =5.5
T_A	Ambient Temperature	0	50	°C	

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"FORTH: A Text and Reference", Mahlon G. Kelly, Nicolas Spies, Prentice-Hall 1986

"Understanding FORTH", J. Reymann, Alfred Publishing Co., 1983

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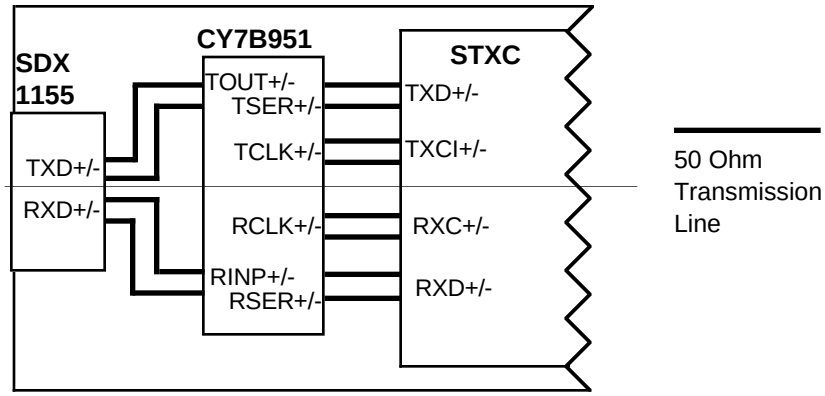
APPENDIX 1: SPECIAL LAYOUT CONSIDERATIONS

High Speed Signal Termination

Trace Impedance Control

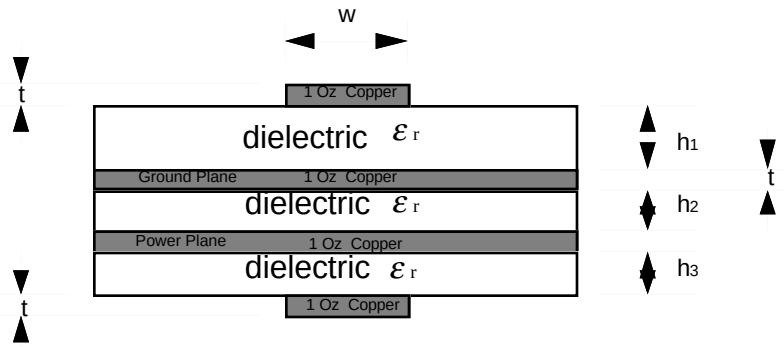
To reduce signal degradation due to reflection and radiation, the impedance of all high frequency signals should be treated as transmission lines and terminated with a matching impedance at the destination. In this design, all high speed signal traces use 50 Ohm transmission lines.



All high frequency traces are modeled as microstrip transmission lines. The calculation of the trace width is calculated using the following formula.

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

and based on the following layer setup:



where

ε_r = relative dielectric constant , nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected . For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric .

w = width of copper

The parameters h1, h2, and h3 can be specified. For example, if a 20 mil (including the copper thickness on both sides of the board) two layer core is selected, dielectric material that have the same relative dielectric constant can be added to both sides of the core to construct a 4 layer board.

Since all the controlled impedance traces are on the component side, only h1 is relevant in calculating the trace width. The calculation for the reference design is shown in the table below:

Note: The relative dielectric constant is specified to be between 4.8 and 5.4.

Parameter	Data			
ε_r	4.8	5.4	4.8	5.4
h (mil)	62	62	62	62
t (mil)	1.4	1.4	1.4	1.4
Zo (Ohm)	50	50	100	100
W (mil)	108.9	101.6	24.7	21.3

The value of the parameter h1 is chosen to be 62 mil. Since h1 is directly proportional to the width of the traces, a small h1 will result in the 100 Ohm traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication. In the layout enclosed, the width of the 100 Ohm traces is 24 mil and that of the 50 Ohm traces is 104 mil.

Routing

Routing is based on the design considerations as well as manufacturability. Several suggestions are listed below:

1. Turns and corners should be rounded to curves to avoid discontinuity in the signal path.

2. Allow at least 10 mil clearance among vias, traces, and pads to prevent shorts and reduce crosstalk. If possible, allow 20 mil or more clearance around vias as manufacturers may have minimum clearance requirements. For the traces that run between pads of the 100 pin edge connector, clearances of 6 mil and a trace width of 8 mil can be used. However, the number and lengths of such traces should be kept to a minimum.

3. The differential signal pairs should be of equal length so that both signals arrive at the inputs at the same time. They should also run parallel and close to one another for as long as possible so that noise will couple onto both lines and become common mode noise which is ignored by the differential inputs.

4. All power and ground traces should be made as wide as possible, up to 24 mil to provide low impedance paths for the supply current as well as to allow quick noise dissipation.

Termination

"Termination" applies to terminating a signal propagating down a transmission line to the characteristic impedance of line. If the line is not terminated to it's characteristic impedance, there will be reflection back down the line. The amount of reflection at the load (receiver) is given by the load reflection coefficient:

$$rL = (R_T - Zo)/(R_T + Zo)$$

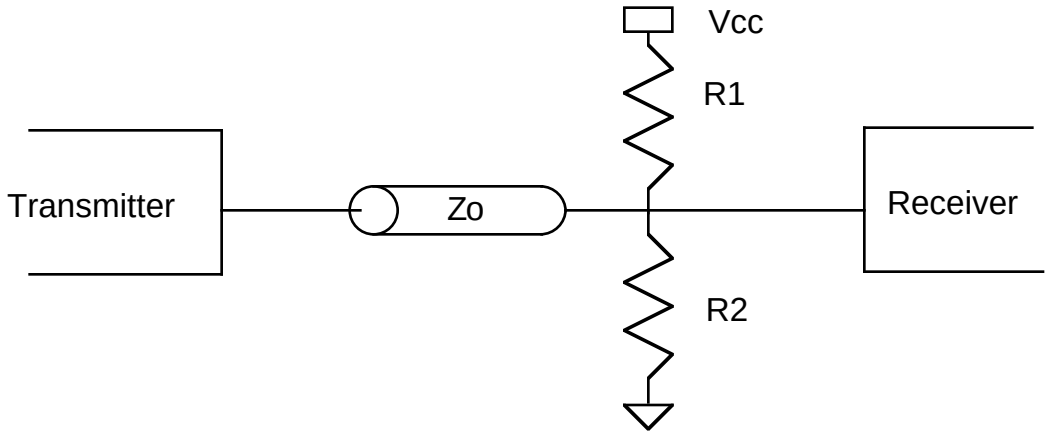
where R_T is the load impedance and **Zo** is the characteristic impedance of the line. The amount of reflection at the source (transmitter) is given by the source reflection coefficient:

$$rS = (R_S - Zo)/(R_S + Zo)$$

where R_S is the source impedance and **Zo** is the characteristic impedance of the line. The reflected signal propagates back and forth until the "ringing" dies out.

There are 4 basic types of terminations used for PECL (or ECL). They are open line termination, series termination, parallel termination, and Thévenin parallel termination. Since PECL (or ECL) signals only drive high, external biasing is need to pull the PECL signal low. This biasing has to be incorporated into the termination scheme.

In the design, the Thévenin termination method has been used. The terminated lines are terminated to the characteristic impedance and sets the terminating (V_T) voltage. The Thévenin equivalent parallel termination is shown below:

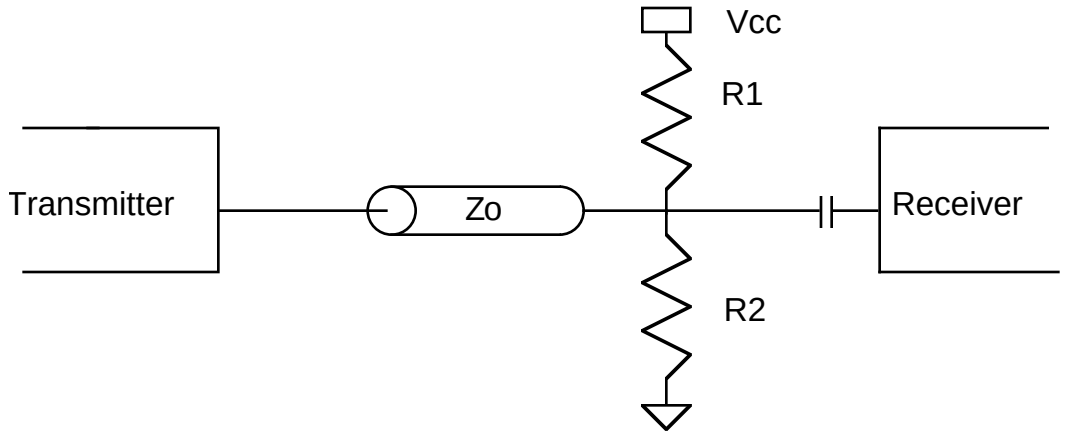


The resistors R1 and R2 in parallel must equal Zo and the voltage at the input must pull the output of the transmitting gate to Vcc - 2 Volts. Working out the equations for PECL +5 Volt supply for Vcc gives:

R2 = 2.5 * Zo

R1 = R2*2/3

Note that the above examples show only one of the differential inputs. With the Thévenin termination care must be taken so that the Vcc and grounds of the differential signals are taken in close proximity of each other or the noise on Vcc and ground will not be in common with each other. Also it is not necessary to use PECL (or ECL) transmitter and receivers to drive characteristic impedance lines. The STXC Transmit and receive signals are actually AC-coupled to CY7B951 in order to obtain proper signal level to and from CY7B951 inputs and output. The method for AC-coupling is shown in the drawing below:



Power and Ground Plane Noise Decoupling

Only one supply voltage, nominally +5 Volts, is used by all devices on the board and referenced to by all PECL signals. One solid ground plane is used. Ferrite beads are deployed to prevent digital noise from entering analog circuits.

Bypass capacitors can supply transient current and help filter out power and ground noise. They are placed as close to the pins as possible. A minimum of one 0.1 uF bypass capacitor per device is used. Wherever possible, one 0.1 uF bypass capacitor is placed at each power pin of each IC. For high speed IC's, such as the SDX1155, CY7B951 and STXC as well as oscillators, an additional 0.01 uF bypass capacitor is added to each power pin. The 10 uF electrolytic bypass capacitors are also deployed for some positions. Two large electrolytic bypass capacitors (100 uF) are placed near the 5 volt power supply input.

A special power plane is provided on the component side for the Cypress CY7B951 device. The power plane under the IC provides a low impedance path connecting pin 6, 17, and 19.

Pin 6 of the CY7B951 provides current for all output pins and is internally connected to pin 17 and 19. Its voltage fluctuates as the outputs switch. The voltage difference between pin 6 and pins 17 and 19 will be amplified, causing the voltage fluctuation on pin 6 to increase. When the voltage at pin 6 fluctuates, the outputs it drives will start to draw more current which causes the voltage on pin 6 to fluctuate further. Testing has shown this fluctuation can reach 2 V p-p.

The low impedance power plane guarantees that pins 6, 17, and 19 are at the same voltage level so that if pin 6 fluctuates due to outputs switching, pin 17 and 19 will follow, preventing any voltage difference between them.

It is also necessary to isolate the analog from the digital. The digital CMOS circuits have high immunity to external noise (approximately 0.3 * Vcc) whereas a small amount of external noise coupled into the analog circuits can be devastating. The analog circuits operate on low voltage swings (600 mVolts for the STXC PECL inputs) as compared to the large (5 Volt) of the CMOS inputs. The CMOS circuits can also generate a lot of switching noise, especially when a large number of circuits are running synchronously all timed to the same system clock.

If the analog power and grounds are not isolated from each other it is unlikely that the SARD board will be able to meet the 0.01 U.I. rms. jitter specified by Bellcore. Therefore, it is necessary to isolate the digital from the analog, otherwise the analog performance can be degraded to a point of non-conformance.

It is also necessary to isolate the transmit analog from the receive analog. Any noise on the receive analog power and ground or on the receive inputs will degrade jitter tolerance and add jitter to the recovered clock. It is also important to keep the analog optical receiver and CY7B951 receive path in common with the receive portion of the

STXC, especially the grounds. The STXC PECL inputs are internally self-biased between Vcc and ground and are AC-coupled. Since the inputs are not true differential inputs, if the STXC's ground and power are in common with the optical and CY7B951 receivers the common mode noise on the input signal is also common to the biasing reference. It is especially important to keep the ground plane between the optical receiver in common with the RAVS inputs of the STXC.

On the transmit side of the STXC, a 155.52 MHz clock is synthesized from a 19.44 MHz reference clock. Any added noise on the power or ground inputs impacts the resulting 155.52 MHz clock. The added noise will increase the intrinsic jitter of the transmitter. The power and ground of the CY7B951 and the optical transmitters can be in common with the analog transmit power and ground of the STXC.

Since only one ground plane and one power plane is normally available, the transmit, receive, and digital power and grounds can be isolated by channels cut into the respective planes. The power and grounds should be brought from a quiet part of the board, usually where the power and grounds enter the board. Ferrite beads can also be used on the receive and transmit analog powers to prevent digital noise from entering analog circuits of the STXC, the PECL oscillator, CY7B951 and the optical transceiver.

It is important to keep the receive analog power, analog ground of the STXC, the receive portion of the CY7B951 and optical transceiver power and ground common to each other.

Ferrite beads are mainly used on power rails to pass DC current but to attenuate the higher frequency noise that is created by other sources. The impedance of Ferrite beads increases with frequency. At DC the ferrite bead is like a short but at higher frequencies the impedance of a ferrite bead can increase to over 100 ohms (depending on the bead and frequency). Ferrite beads attenuate high frequency noise from the power supply from getting into a circuit, but they also stop high frequency noise from leaving the circuit. It is important, therefore, to use proper bypass decoupling when using ferrite beads.

Ferrite beads should be avoided on CMOS I/O power pins as the high current switching of the CMOS circuits causes a $\Delta I/\Delta t$ noise to be introduced into the power rail. Ferrite beads should also be avoided on the ground bus as this inhibits the return currents.

To reduce digital circuit switching noise, it is important to decouple every digital power pin of all devices so that the switching currents can be satisfied and thereby reduce the amount of noise introduced into the power plane.

APPENDIX 2: BILL OF MATERIAL

Item Number.	Part Name - Value	Part Number	Jedec Type	Ref Des	Qty
1	27512_DIP-BASE	27512	DIP28_6	U15	1
2	49FCT805_SOIC-BASE	49FCT805	SOIC20W	U18	1
3	74F163A_SOIC-BASE	74F163A	SOIC16	U8, U14, U17, U25	4
4	74F374_SOIC-BASE	74F374	SOIC20W	U38	1
5	74HC138_SOIC-BASE	74HC138	SOIC16	U20, U21	2
6	74HCT245_SOIC-BASE	74HCT245	SOIC20W	U19	1
7	74XXX04_SOIC-HCMOS	74HC04D	SOIC14	U5, U36, U49	3
8	74XXX08_SOIC-HCMOS	74HC08D	SOIC14	U3, U29, U32, U43, U51	5
9	74XXX257_SOIC-HCMOS	74HC257D	SOIC16	U16	1
10	74XXX273_SOIC-HCMOS	74HC273DW	SOIC20W	U24, U42, U44	3
11	74XXX32_SOIC-HCMOS	74HC32D	SOIC14	U22, U26, U47, U50	4
12	74XXX373_SOIC-HCMOS	74HC373DW	SOIC20W	U27, U28	2
13	74XXX541_SOIC-HCMOS	74HC541DW	SOIC20W	U2, U4, U6, U7, U9, U11-U13, U23, U30, U31, U33, U37, U40,U41, U48	16
14	CAP-100000PF	DIGI-KEY -	SMDCAP1206	C1-C3, C5, C7, C8,	148

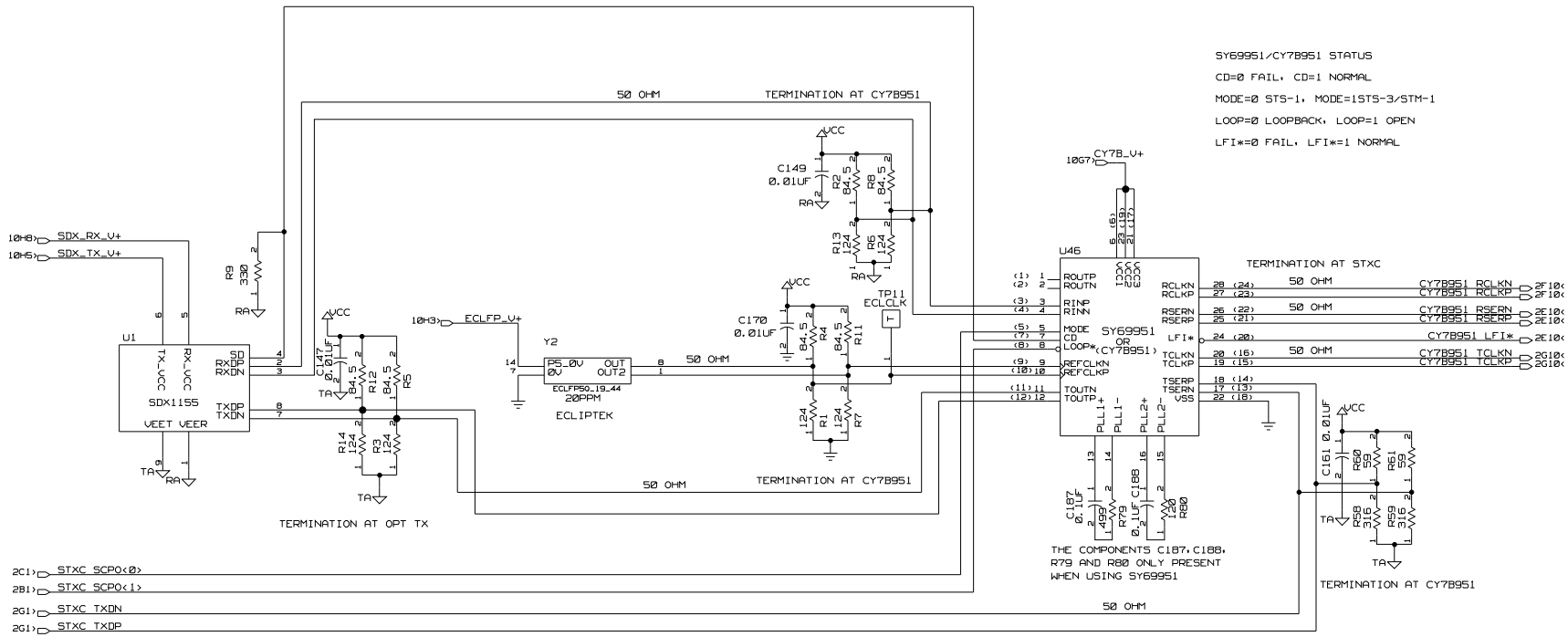
		PCC104BCT-ND		C10, C12, C13, C16-C21, C23-C31, C35-C44, C48-C60, C64-C96, C99, C108, C110, C113-C120, C124-C129, C131-C133, C136, C137, C139, C142, C143, C145, C146, C148, C150, C151, C153-C157, C159, C160, C163-C165, C167, C168, C171-C174, C176-C179, C181-C183, C185-C191	
15	CAP-10000PF	DIGI-KEY - PCC103BNCT-ND	SMDCAP805	C4, C6, C9, C1, C14, C15, C22, C34, C47, C63, C97, C109, C121, C144, C147, C149, C152, C158, C161, C162, C166, C169, C170, C175, C180, C184	26
16	CAPACITOR POL-100UF, 16V, ELECTRO	DIGI-KEY -P1211-ND	CAP320	C135, C138	2
17	CAPACITOR POL-10UF, 16V, TANT TEH	DIGI-KEY -- PCT3106CT-ND	SMDTANCAP_C	C32, C33, C45, C61, C62, C98, C111, C112, C122, C123, C130, C134, C140, C141	15
18	CONN100-AMP_103911-8	AMP - 103911-8	AMP_103911-8	P2, P3	2
19	DIN96_MALE-BASE	DIGI-KEY - A1254-ND	AMP_650473-5	P1	1
20	ECLFP5Q_19_44-BASE	ECLFP5Q	CRYS14	Y2	1

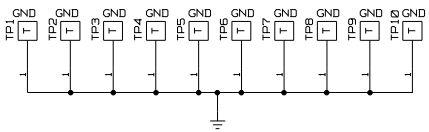
21	HEADER10-BASE	DIGI-KEY S1011-36-ND	SIP10	J2	1
22	HEADER12-BASE	DIGI-KEY S1011-36-ND	SIP12	J1	1
23	HEADER5X2-BASE	DIGI-KEY S2012-36-ND	HEADER_5X2	J3	1
24	HEADER9X3-BASE	DIGI-KEY S1011-36-ND	HEADER_9X3	J4	1
25	INDUCTOR-FB,50,	FAIR RITE --	INDUCTOR_FB	L1-L9	9
	FAIR RITE	2743019447			
26	LED-RED,1-5 MA,1.8V,	DIGI-KEY --	LED	D1	1
	PCB RIGHT A	LU20091-ND			
27	LED10-RED,25MA,2.1V	DIGI-KEY --	DIP20_LED	D2,D3	2
		LT1066-ND			
28	OSC_TTL_DIP-19.44MHZ ,20 PPM,CHA	K1110CA	CRYS14	Y1	1
29	RESISTOR-0,5%	DIGI-KEY -- P<VALUE>ABK-ND	SMDRES805	R15, R16, R18-R24, R29, R36, R38, R41, R42, R47, R50, R52, R57, R63, R64, R87	21
30	RESISTOR-1.0K,5%	DIGI-KEY -- P<VALUE>ABK-ND	SMDRES805	R10, R17, R2, R30, R31, R33, R46, R62, R65-R78, R81-R86, R88	29
31	RESISTOR-10K,5%	DIGI-KEY -- P<VALUE>ABK-ND	SMDRES805	R25,R37,R43	3
32	RESISTOR-120,5%	DIGI-KEY -- P<VALUE>ABK-ND	SMDRES805	R80	1
33	RESISTOR-124,1%	DIGI-KEY -- P<VALUE>CCT-ND	SMDRES805	R1, R3, R6, R7, R13, R14, R34, R40, R44, R48, R49, R55	12
34	RESISTOR-27,5%	DIGI-KEY -- P<VALUE>ABK-ND	SMDRES805	R26,R28	2
35	RESISTOR-270,5%	DIGI-KEY -- P<VALUE>ABK-ND	SMDRES805	R56	1
36	RESISTOR-316,1%	DIGI-KEY -- P<VALUE>CCT-ND	SMDRES805	R58,R59	2

37	RESISTOR-330,5%	DIGI-KEY -- P<VALUE>ABK-ND	SMDRES805	R9	1
38	RESISTOR-499,1%	DIGI-KEY -- P<VALUE>CCT-ND	SMDRES805	R79	1
39	RESISTOR-59,1%	DIGI-KEY --	SMDRES805	R60,R61	2
		P<VALUE>CCT-ND			
40	RESISTOR-634,1%	DIGI-KEY -- P<VALUE>CCT-ND	SMDRES805	R53	1
41	RESISTOR-84.5,1%	DIGI-KEY -- P<VALUE>CCT-ND	SMDRES805	R2, R4, R5, R8, R11, R12, R32, R35, R39, R45, R51, R54	12
42	RES_ARRAY_15_SMD-10K	DIGI-KEY -- 766-161-R<VALUE>-ND	SOIC16	RN5,RN15,RN16	3
43	RES_ARRAY_15_SMD-1K	DIGI-KEY - 766-161-R<VALUE>-ND	SOIC16	RN1-RN4, RN6, RN9, RN10, RN12-RN14, RN17	11
44	RES_ARRAY_15_SMD-270	DIGI-KEY -- 766-161-R<VALUE>-ND	SOIC16	RN8,RN11	2
45	RES_ARRAY_8_SMD-27	DIGI-KEY -- 766-163-R<VALUE>-ND	SOIC16	RN7	1
46	SDX1155-BASE	SDX1155	LCD-PMD-SOCKET	U1	1
47	SPTX-BASE	PM5344	PQFP160	U39	1
48	STXC-BASE	PM5343	PQFP160	U45	1
49	SY69951-BASE	SY69951	SOIC28W	U46	1
50	TST_PT-BASE	DIGI-KEY S1011-36-ND	TST_PT_1	TP1-TP14	14
51	TUDX-BASE	PM5371	PQFP160	U34,U35	2
52	TUPP_PLUS-BASE	PM5362	PQFP160	U10	1

APPENDIX 3: SCHEMATICS

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





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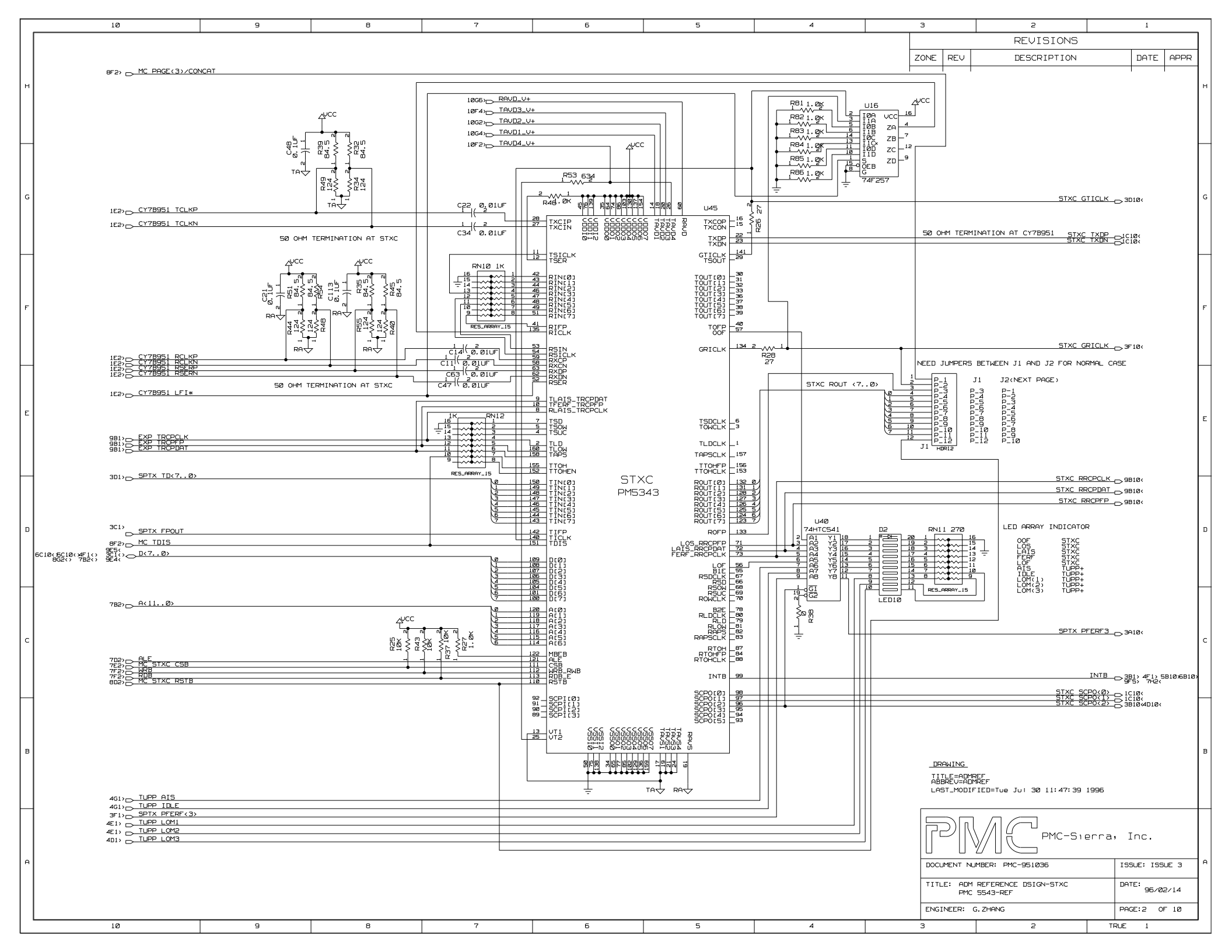
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-INTERFACE PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:1 OF 10


REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPR
STXC
PM5343
U45
U16
74F257
U40
74HTC541
D2
LED10
RN10 1K
RN12
RES_ARRAY_15
50 OHM TERMINATION AT STXC
50 OHM TERMINATION AT CY7B951
NEED JUMPERS BETWEEN J1 AND J2 FOR NORMAL CASE
J1
J2(NEXT PAGE)
HDR12
LED ARRAY INDICATOR
OOF STXC
LOS STXC
LAIS STXC
FERF STXC
LOF STXC
AIS TUPP+
IDLE TUPP+
LOM(1) TUPP+
LOM(2) TUPP+
LOM(3) TUPP+
MC PAGE(3)/CONCAT
CY7B951 TCLKP
CY7B951 TCLKN
CY7B951 RCLKP
CY7B951 RCLKN
CY7B951 RSERP
CY7B951 RSERN
CY7B951 LFI*
EXP TRCPCLK
EXP TRCPFP
EXP TRCPDAT
SPTX TD<7..0>
SPTX FPOUT
MC TDIS
D<7..0>
A<11..0>
ALE
MC STXC CSB
WRB
RDB
MC STXC RSTB
TUPP AIS
TUPP IDLE
SPTX PFERF<3>
TUPP LOM1
TUPP LOM2
TUPP LOM3
STXC GTICLK
STXC TXDP
STXC TXDN
STXC GRICLK
STXC ROUT <7..0>
STXC RRCPCLK
STXC RRCPDAT
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SPTX PFERF3
INTB
STXC SCPO<0>
STXC SCPO<1>
STXC SCPO<2>
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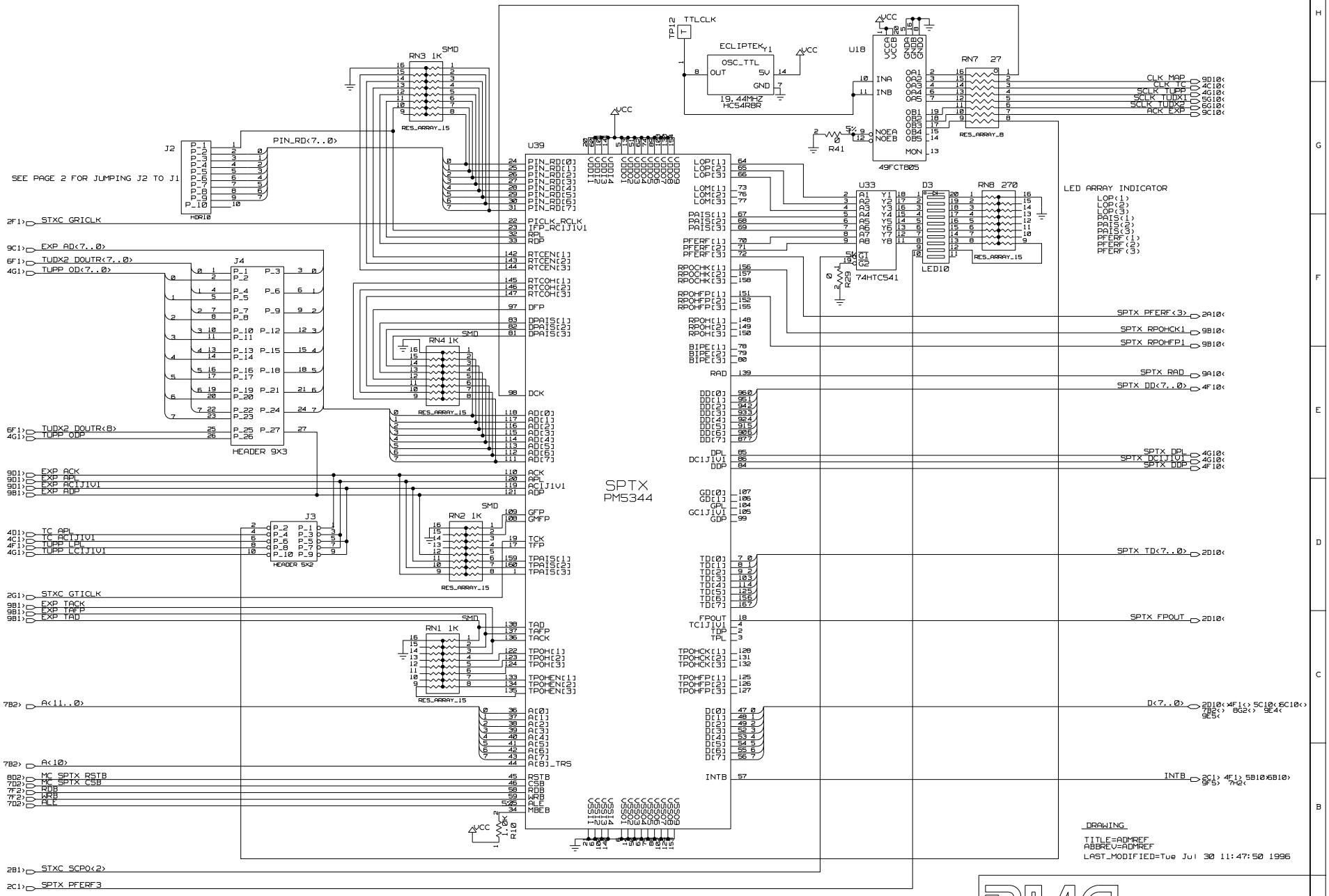
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-951036
ISSUE: ISSUE 3
TITLE: ADM REFERENCE DSIGN-STXC
PMC 5543-REF
DATE: 96/02/14
ENGINEER: G.ZHANG
PAGE:2 OF 10
TRUE 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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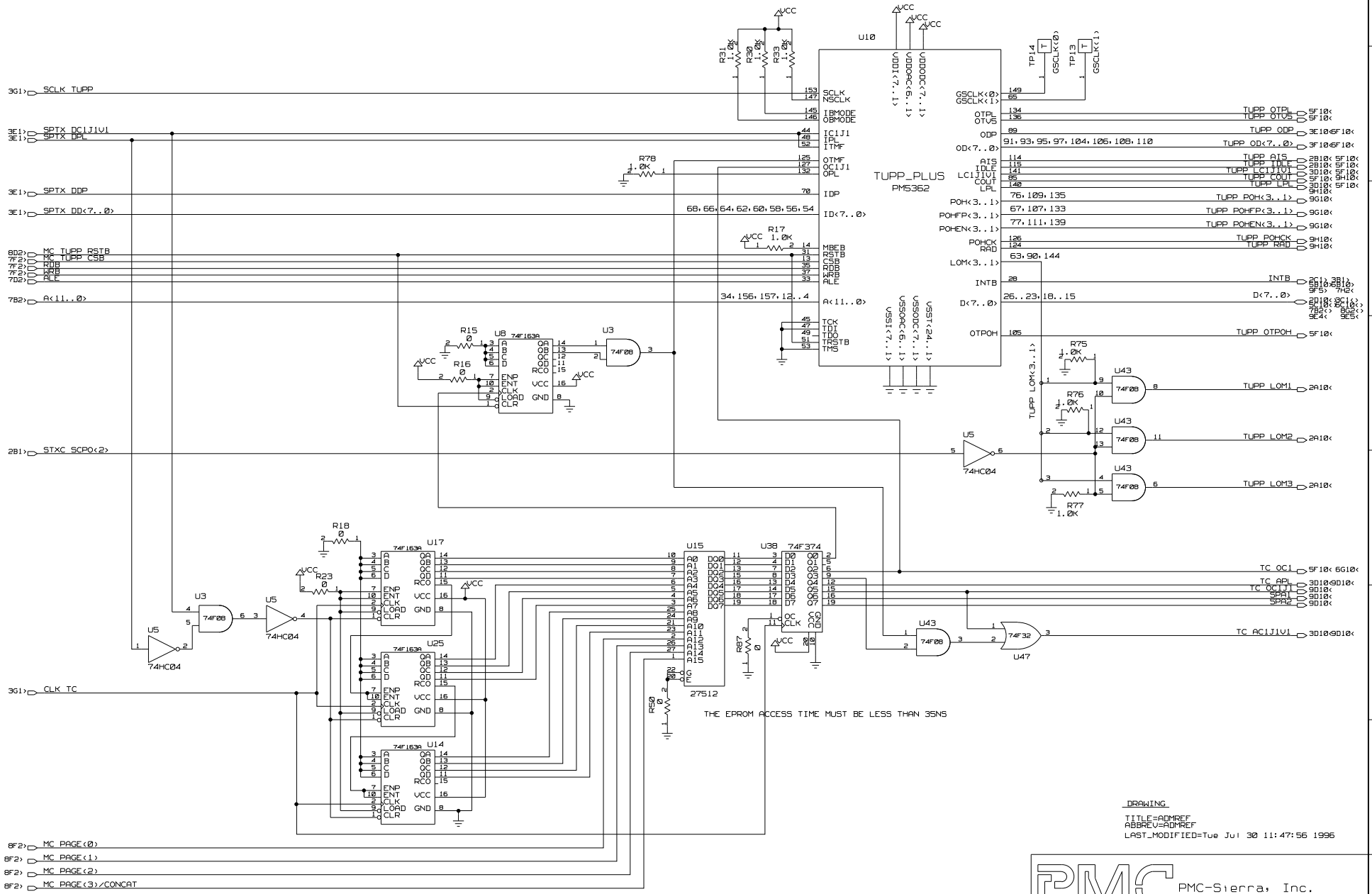
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-SPTX PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:3 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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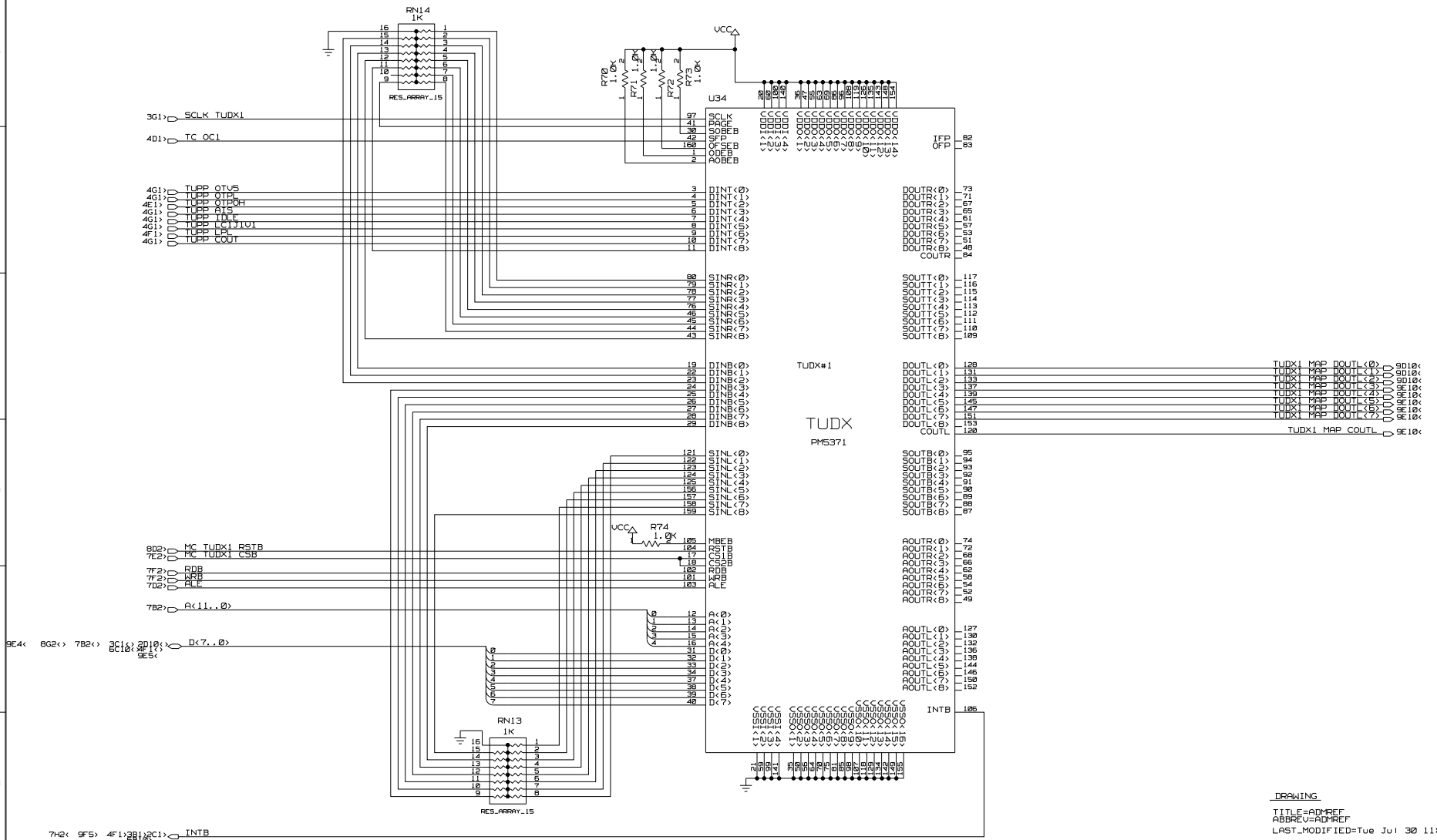
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-TC AND TUPP PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:4 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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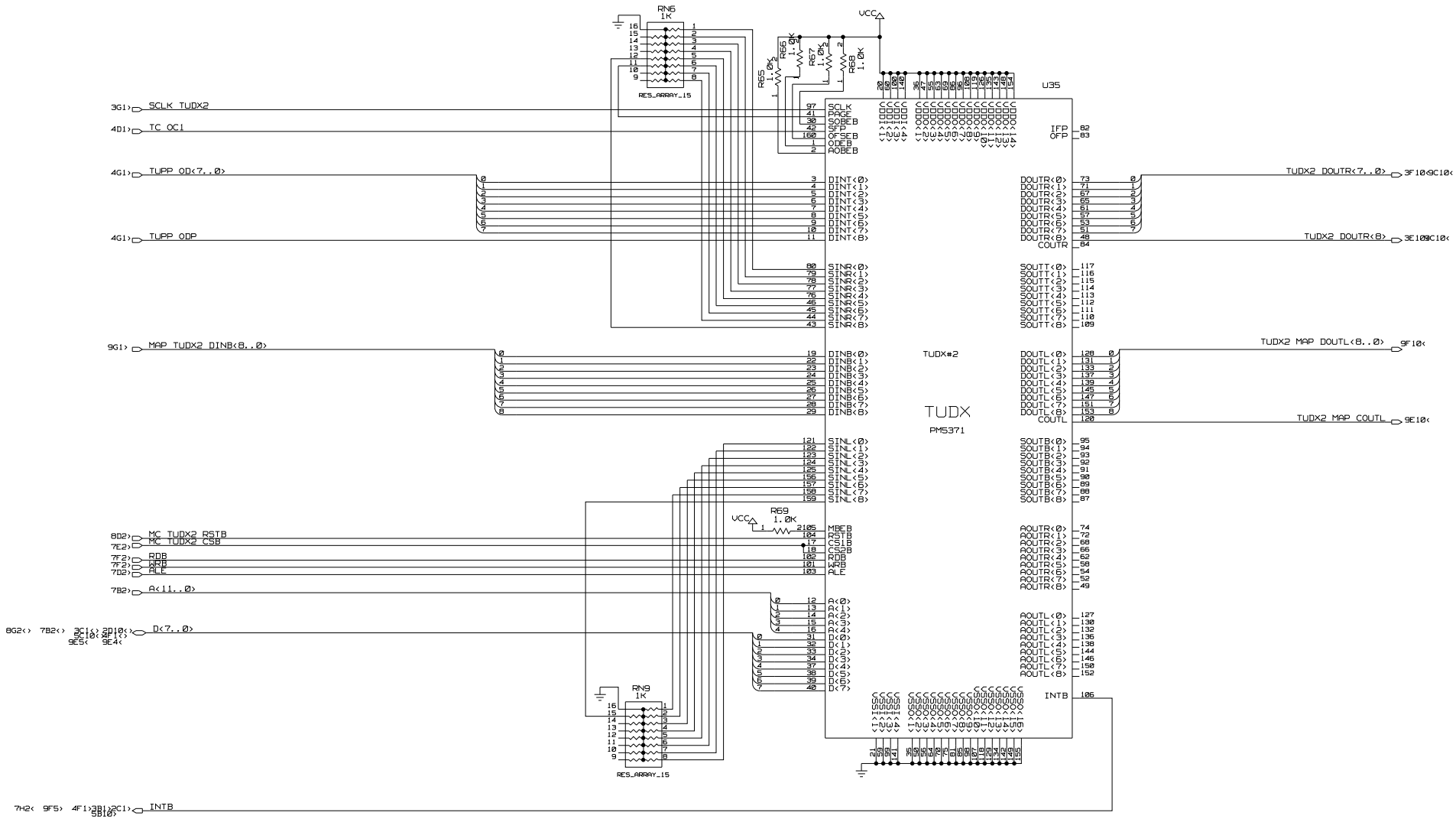
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-TUDX1-CONTROL PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:5 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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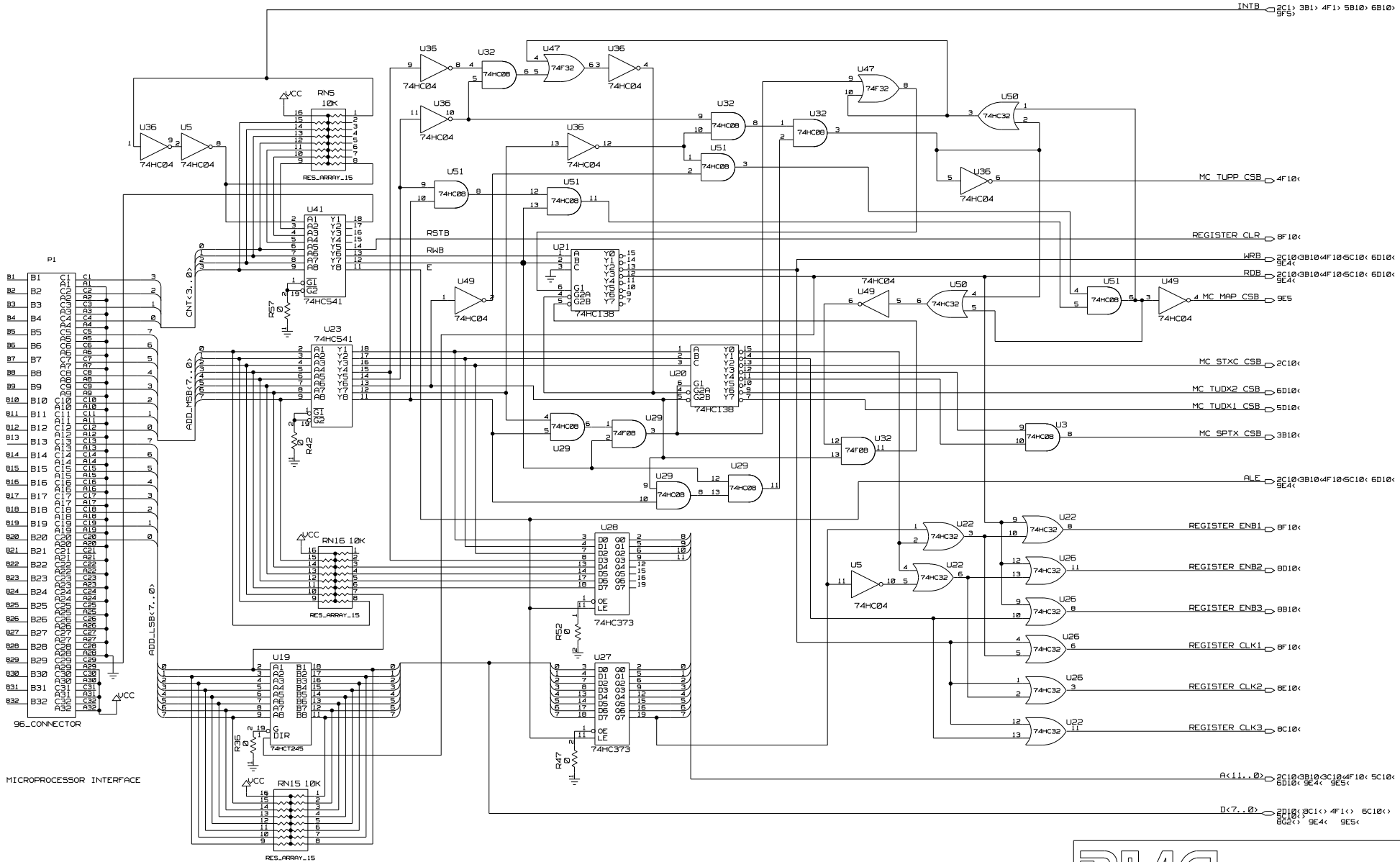
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-TUDX2-DATA PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:6 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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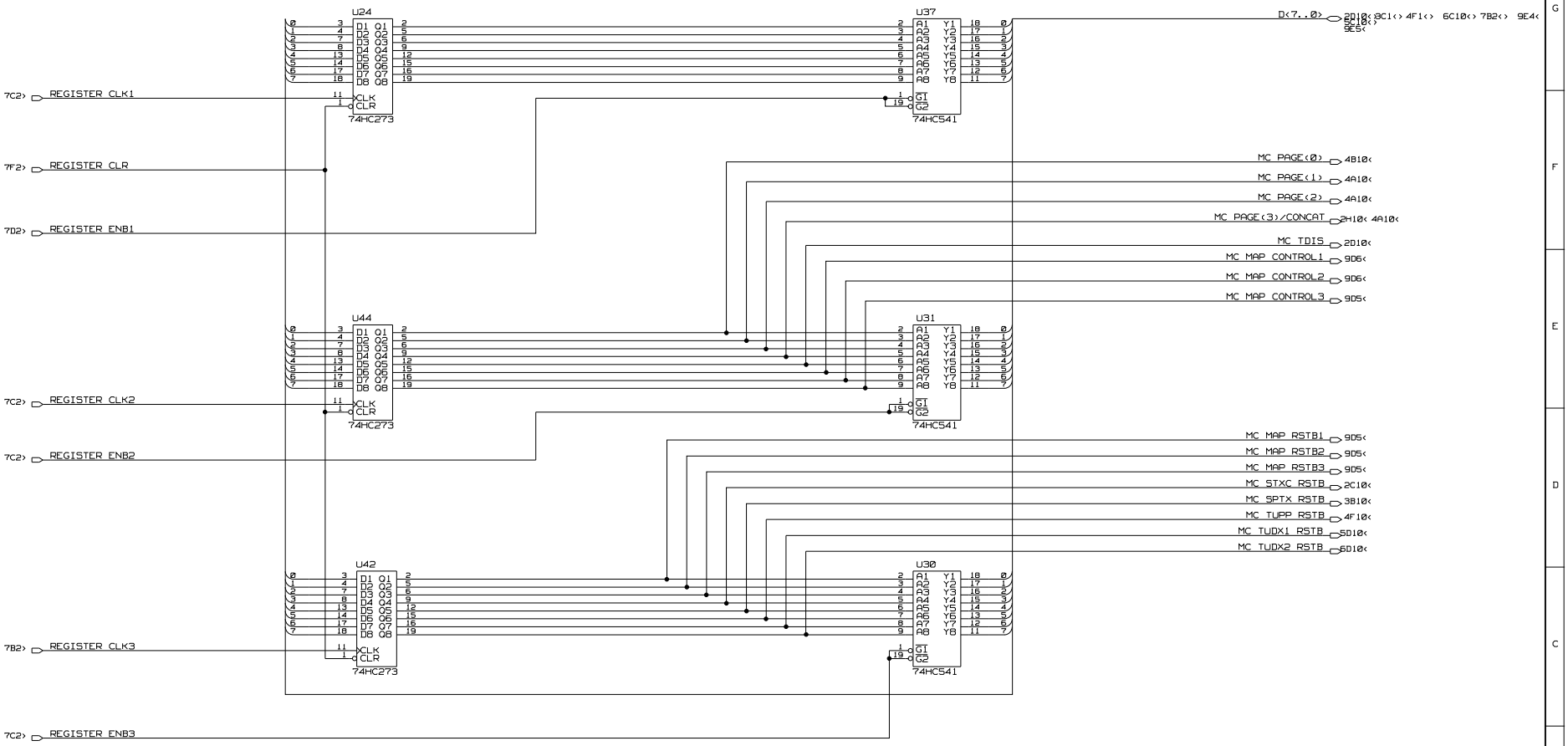
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-MICRO CONTROL PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:7 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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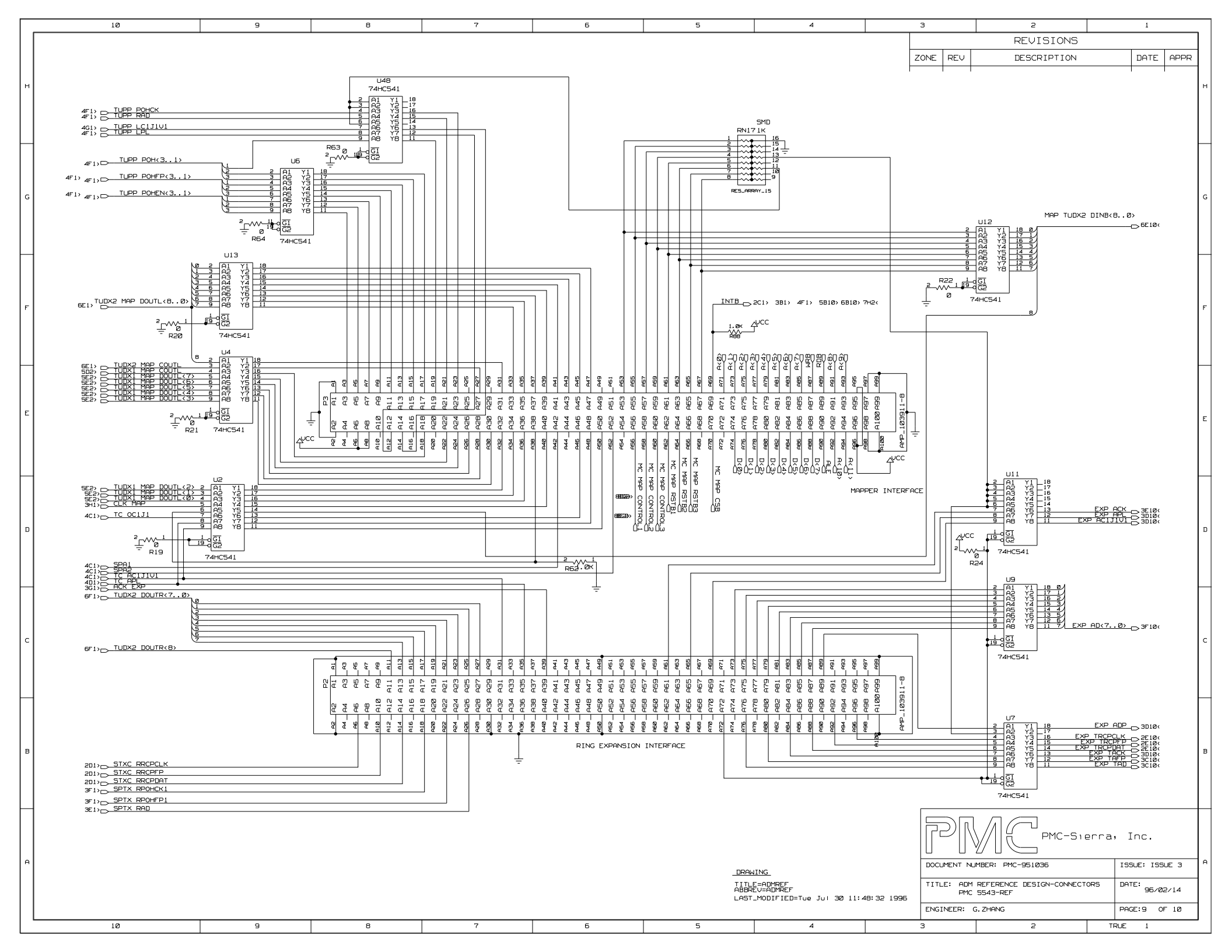
LAST_MODIFIED=Tue Jul 30 11:48:26 1996

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REF. DESIGN-CONTROL REGISTERS PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:8 OF 10


REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPR
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74HC541
U6
74HC541
U13
74HC541
U4
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U2
74HC541
U12
74HC541
U11
74HC541
U9
74HC541
U7
74HC541
SMD
RN171K
RES_ARRAY_15
MAP TUDX2 DINB<8..0>
TUPP POHCK
TUPP RAD
TUPP LC1J1V1
TUPP LPL
TUPP POH<3..1>
TUPP POHFP<3..1>
TUPP POHEN<3..1>
TUDX2 MAP DOUTL<8..0>
TUDX2 MAP COUTL
TUDX1 MAP COUTL
TUDX1 MAP DOUTL<7>
TUDX1 MAP DOUTL<6>
TUDX1 MAP DOUTL<5>
TUDX1 MAP DOUTL<4>
TUDX1 MAP DOUTL<3>
TUDX1 MAP DOUTL<2>
TUDX1 MAP DOUTL<1>
TUDX1 MAP DOUTL<0>
CLK MAP
TC OC1J1
SPA1
SPA2
TC AC1J1V1
TC APL
ACK EXP
TUDX2 DOUTR<7..0>
TUDX2 DOUTR<8>
STXC RRCPCLK
STXC RRCPFP
STXC RRCPDAT
SPTX RPOHCK1
SPTX RPOHFP1
SPTX RAD
INTB
MC MAP CONTROL1
MC MAP CONTROL2
MC MAP CONTROL3
MC MAP RSTB1
MC MAP RSTB2
MC MAP RSTB3
MC MAP CSB
MAPPER INTERFACE
RING EXPANSION INTERFACE
EXP ACK
EXP APL
EXP AC1J1V1
EXP AD<7..0>
EXP ADP
EXP TRCPCLK
EXP TRCPFP
EXP TRCPDAT
EXP TACK
EXP TAFP
EXP TAD
AMP_103911-8
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-951036
ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-CONNECTORS PMC 5543-REF
DATE: 96/02/14
ENGINEER: G.ZHANG
PAGE:9 OF 10
DRAWING
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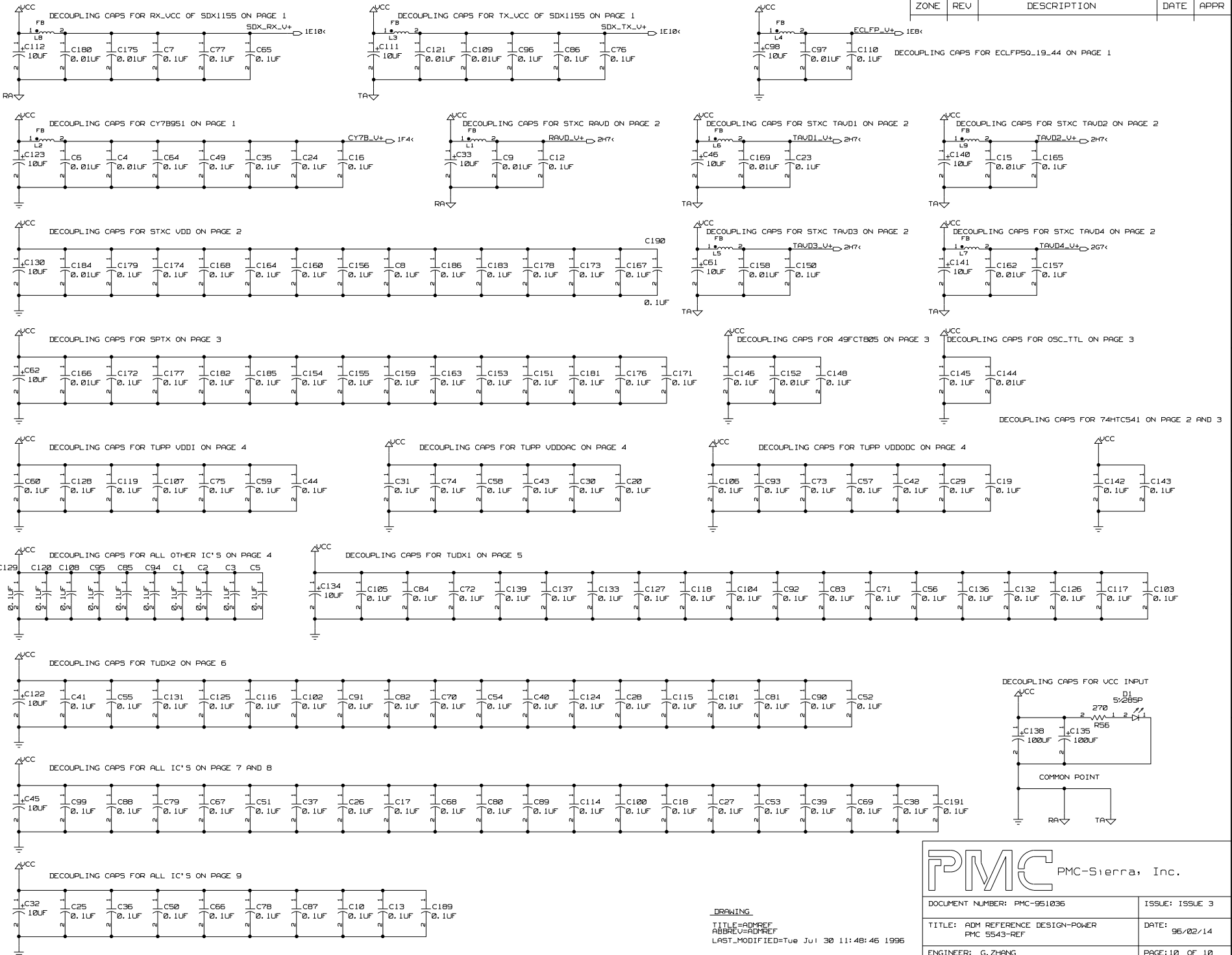
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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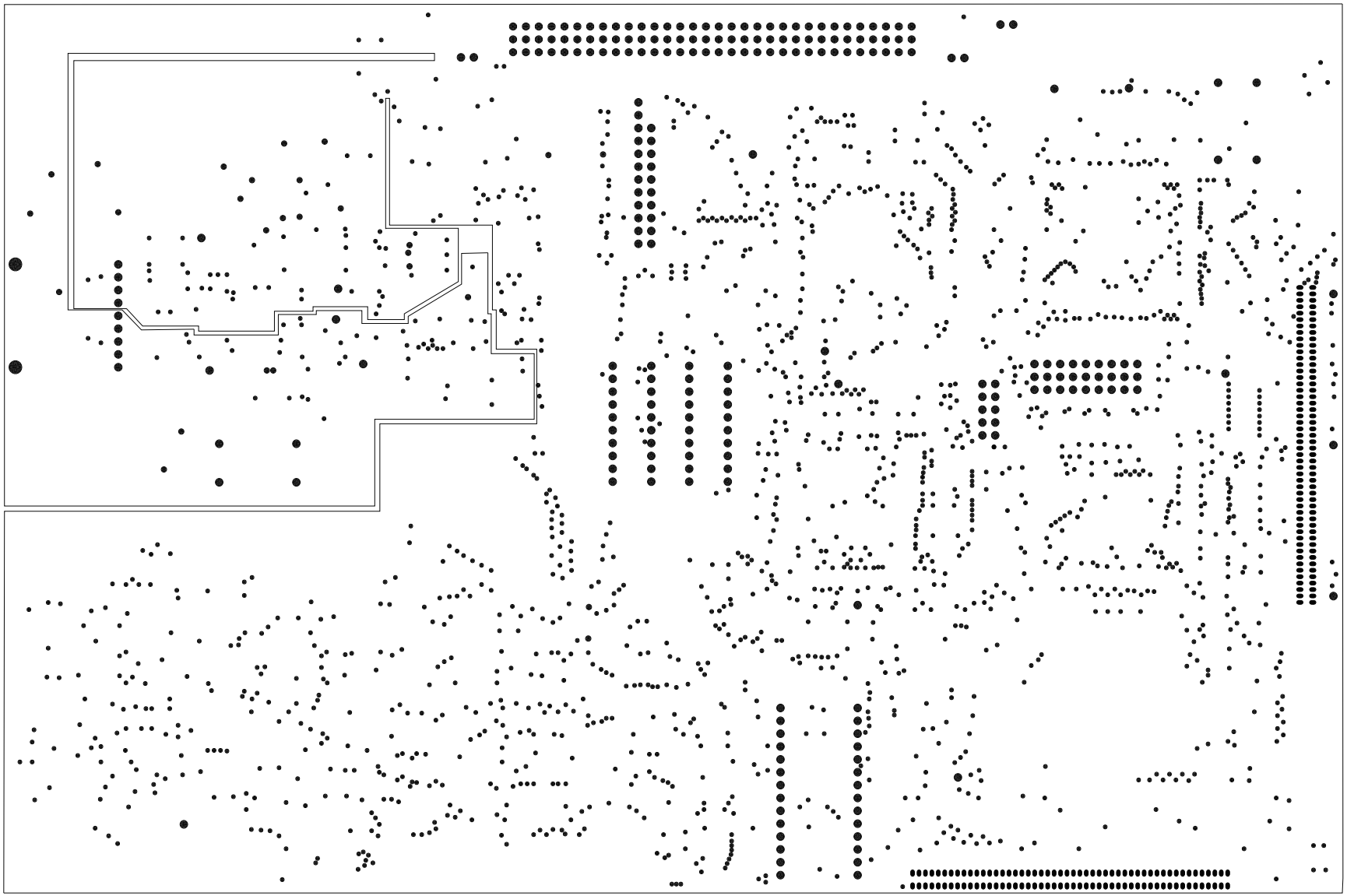
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-951036	ISSUE: ISSUE 3
TITLE: ADM REFERENCE DESIGN-POWER PMC 5543-REF	DATE: 96/02/14
ENGINEER: G.ZHANG	PAGE:10 OF 10

APPENDIX 4: OTHER LAYOUT DRAWINGS

GND_PLANE



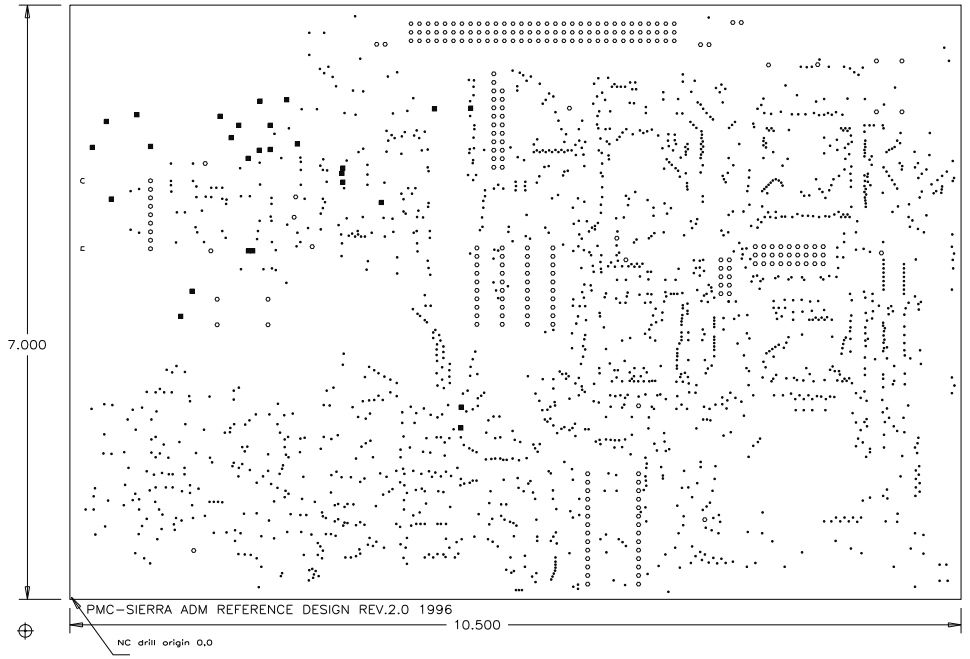
PMC-SIERRA ADM REFERENCE DESIGN REV.2.0 1996

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED
1.0	NCDRILL FIGURE	Sept. 1995			
1.0	MECHANICAL DRAWING	Sept. 1995			

Board Material Details

Material	Layer Type	Etch Name	Film type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	1.44 mil	-----
FR-4	DIELECTRIC	-----	-----	10 mil	4.2
COPPER	CONDUCTOR	GND_PLANE	POSITIVE	2.88 mil	-----
FR-4	DIELECTRIC	-----	-----	33.4 mil	4.2
COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	2.88 mil	-----
FR-4	DIELECTRIC	-----	-----	10 mil	4.2
COPPER	CONDUCTOR	BOTTOM	POSITIVE	1.44 mil	-----

Note: 50 ohm controlled impedence traces with trace width of 17 mil are on Top and Bottom layers.



ARTWORK FILM

TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
MECH. DRAWING

hole_chart

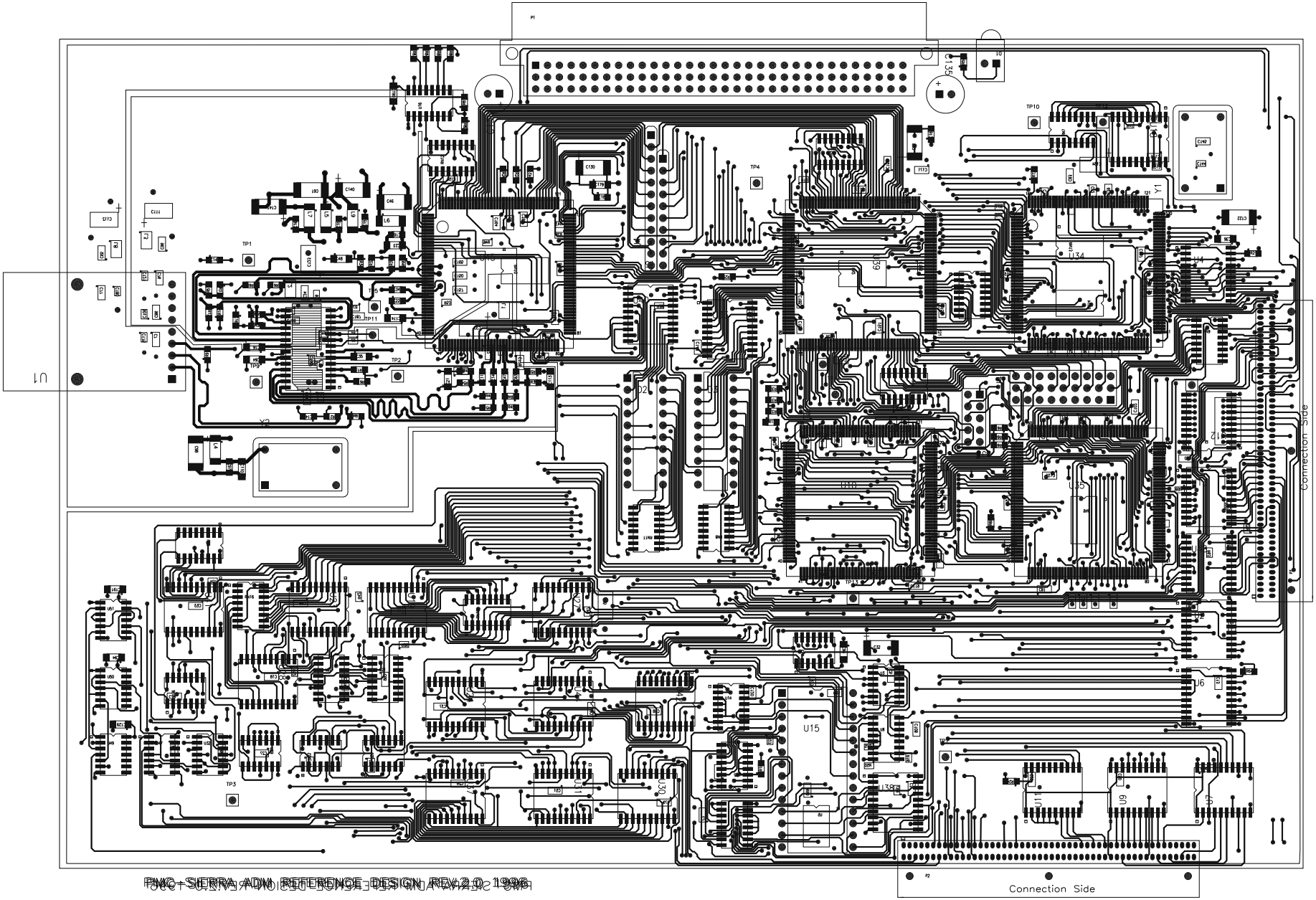
/ FIGURE /	HOLESIZE /	QTY /
•	15.000-P	1760
▲	22.000-P	200
■	25.000-P	27
o	36.000-P	257
o	42.000-P	9
c	79.000-P	2

Note: P = Plated
N = Non-Plated

Notes:

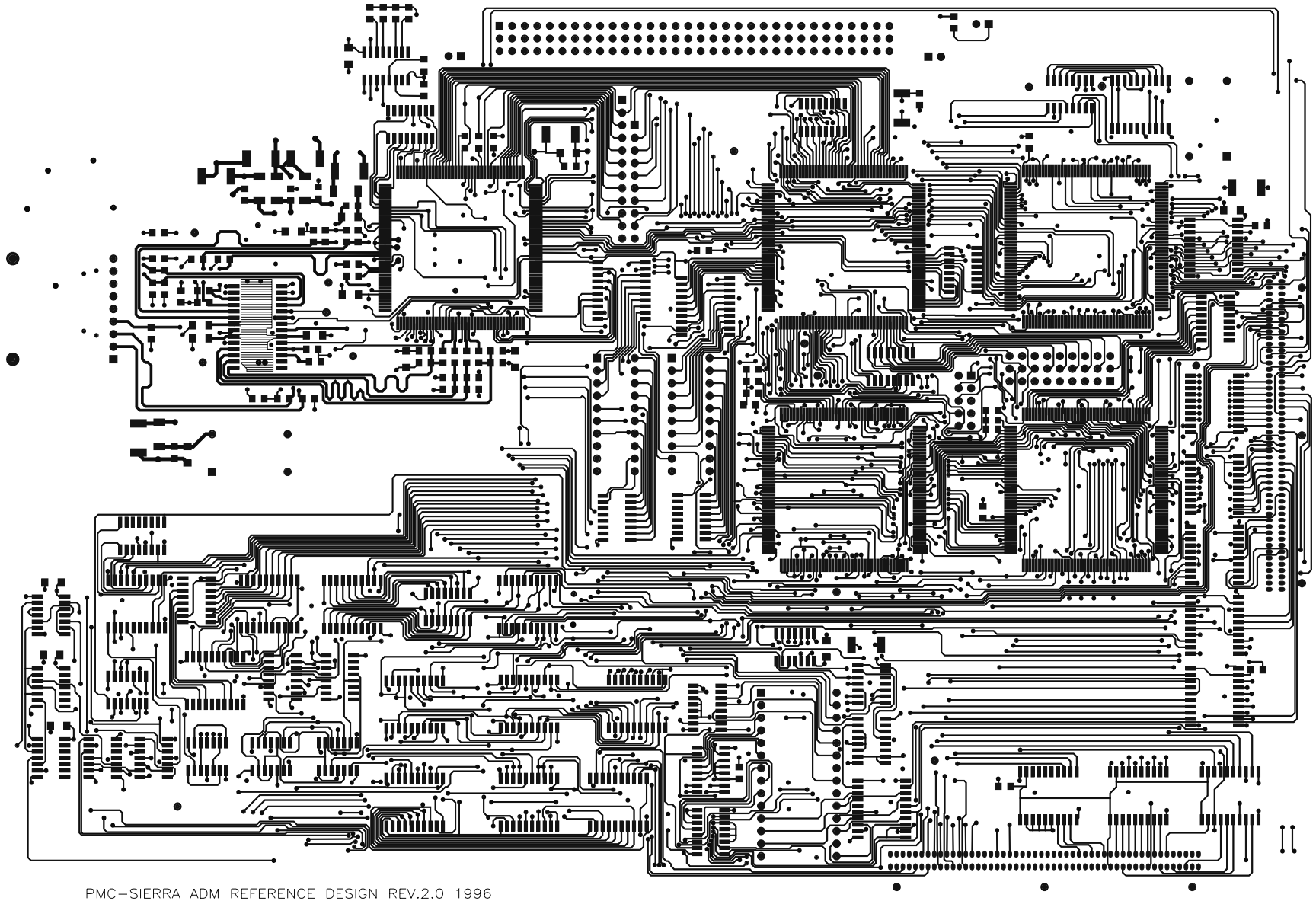
1. Copper thickness is 2 oz. on vcc_plane & gnd_plane, 1 oz. on all others layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are specified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil mimimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white based ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in./in. per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD	PMC-Sierra, Inc.
DIMENSIONS ARE IN INCHES	DRAWN G. ZHANG	960209			
TOLERANCES ON:	CHECKED				8501 Commerce Court, Burnaby B.C.
2 PL DECIMALS + +/- .03	ENGRG				Canada, V5A 4A5
3 PL DECIMALS + +/- .005	ISSUED				Tel: 604 668 7300 Fax: 604 668 7301
ANGLES +					SIZE B / FSCM NO / DWG NO
FRACTIONS +					SCALE NTS NTS / SHEET 1 OF 1



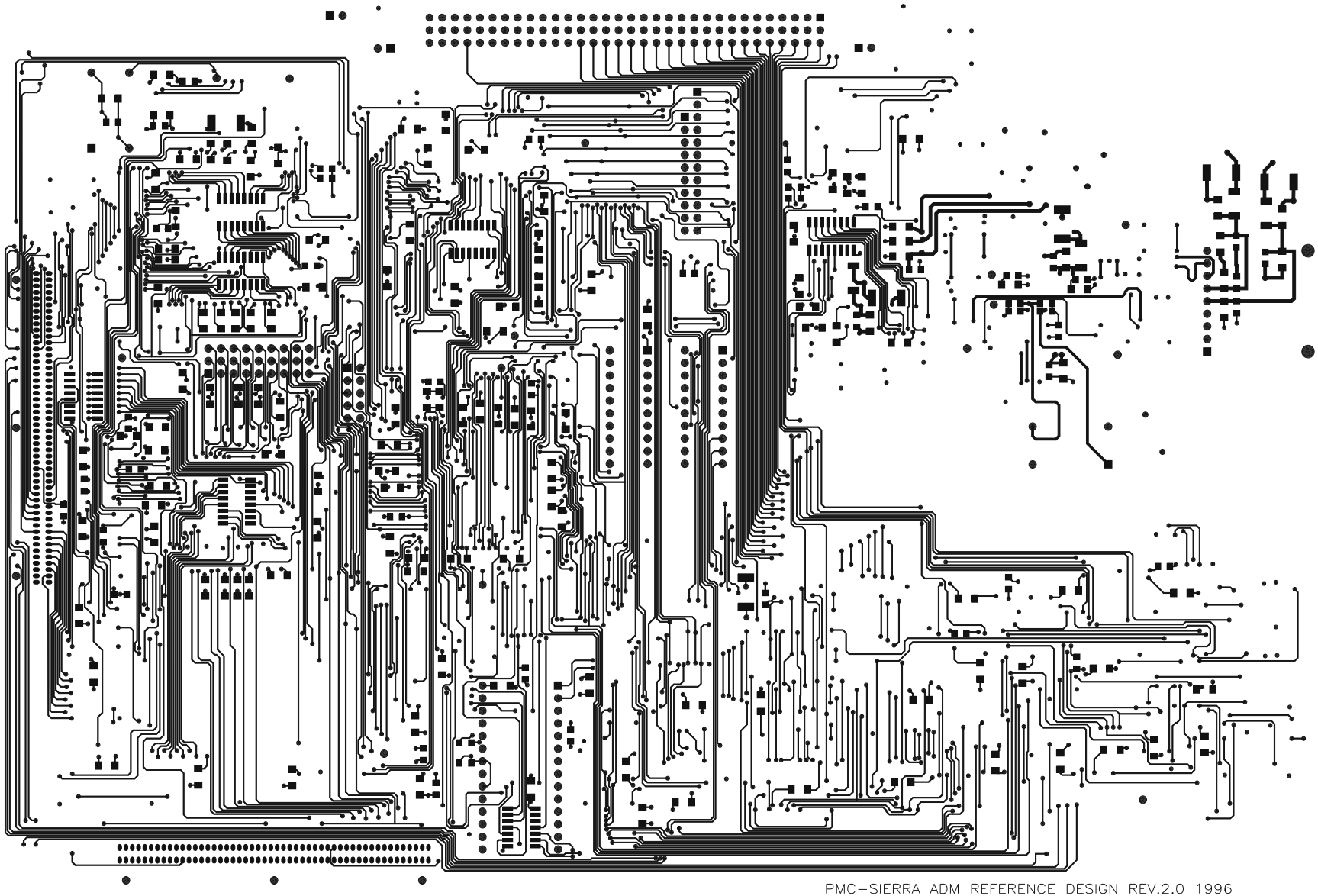
PWC-SIERRA ADM REFERENCE DESIGN REV2.0 1996

TOP LAYER



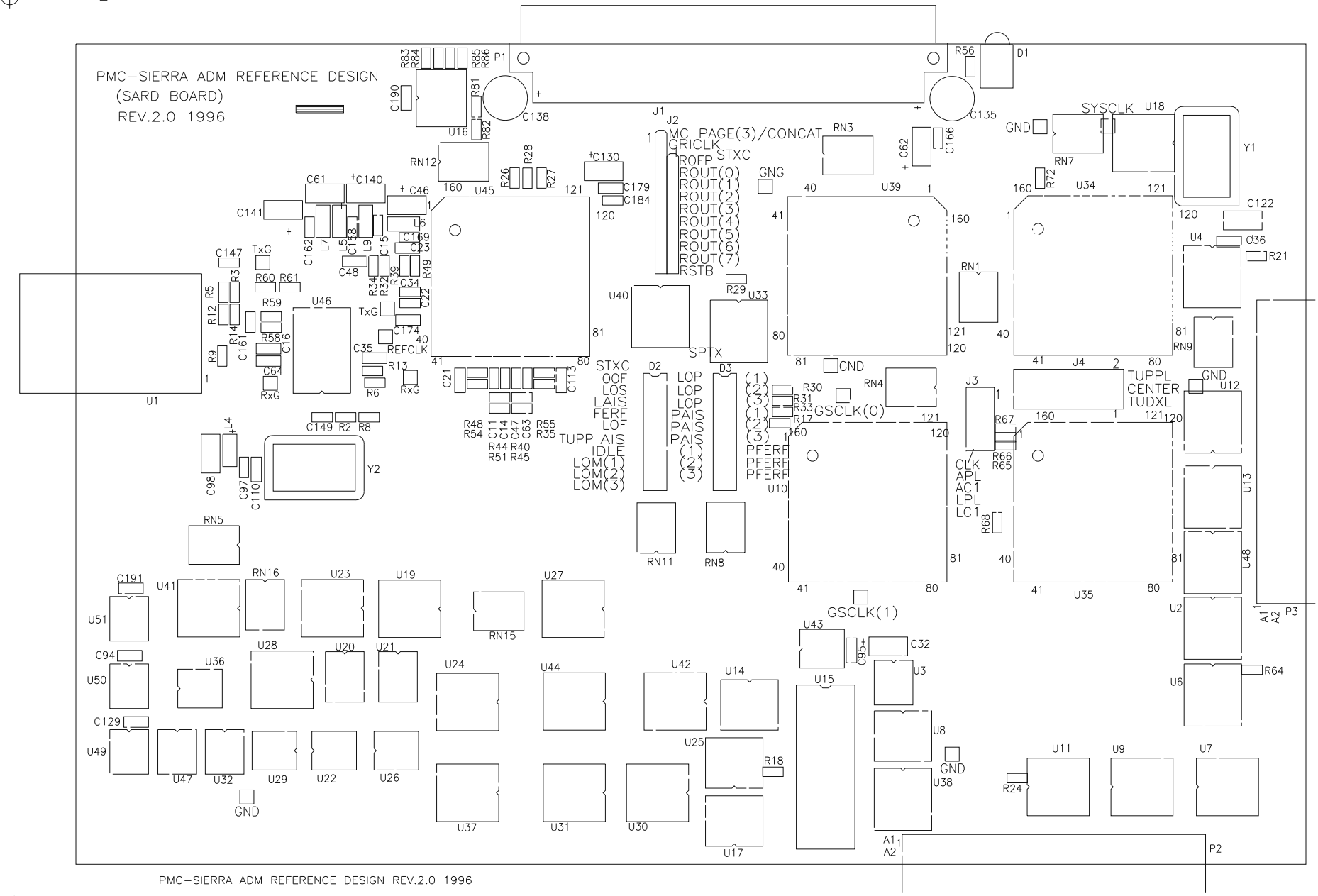
PMC-SIERRA ADM REFERENCE DESIGN REV.2.0 1996

BOTTOM_LAYER

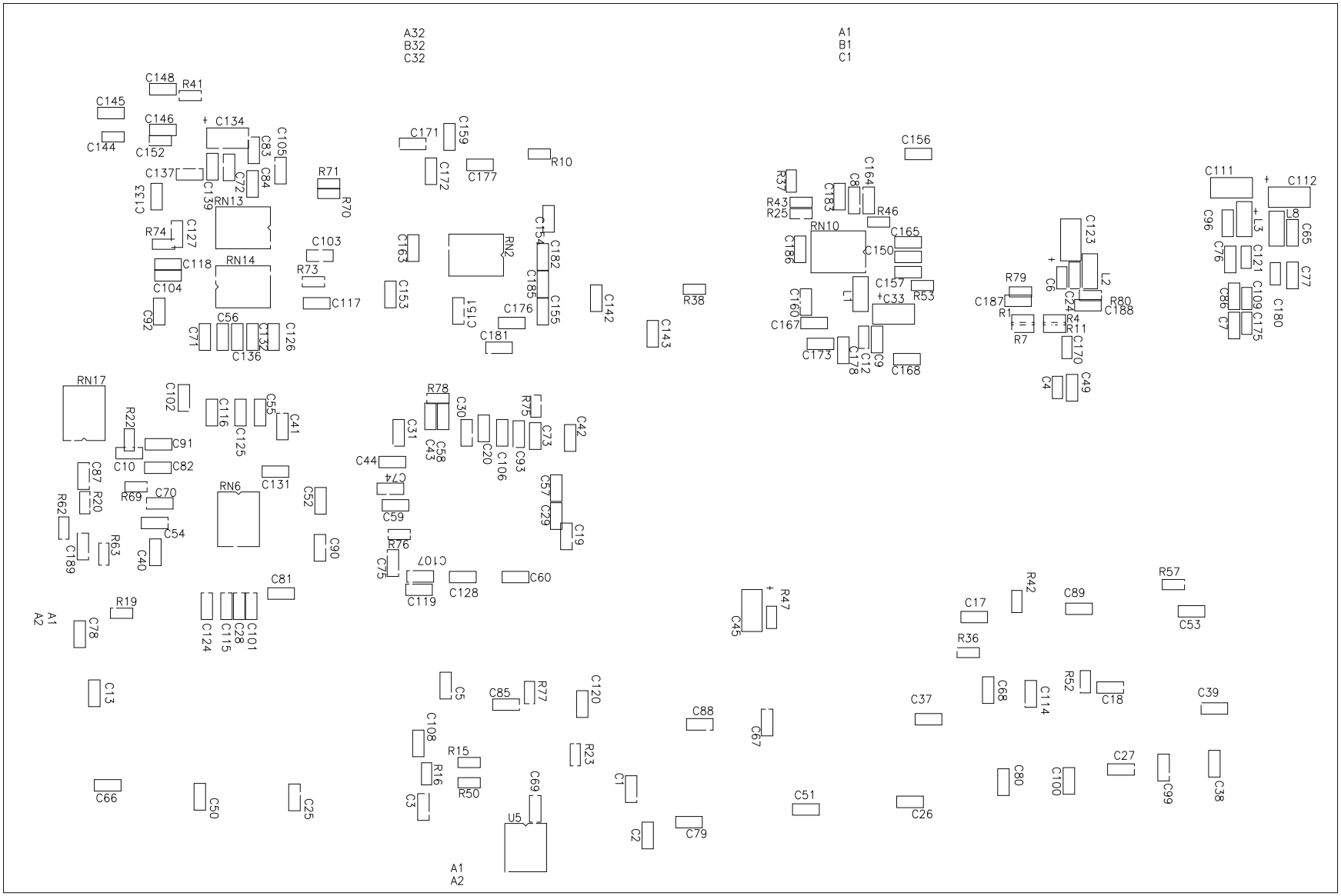


PMC-SIERRA ADM REFERENCE DESIGN REV.2.0 1996

RES_DES TOP



PMC-SIERRA ADM REFERENCE DESIGN REV.2.0 1996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B32
C32
A1
B1
C1
C148
R41
C145
C146
C134
C144
C152
C105
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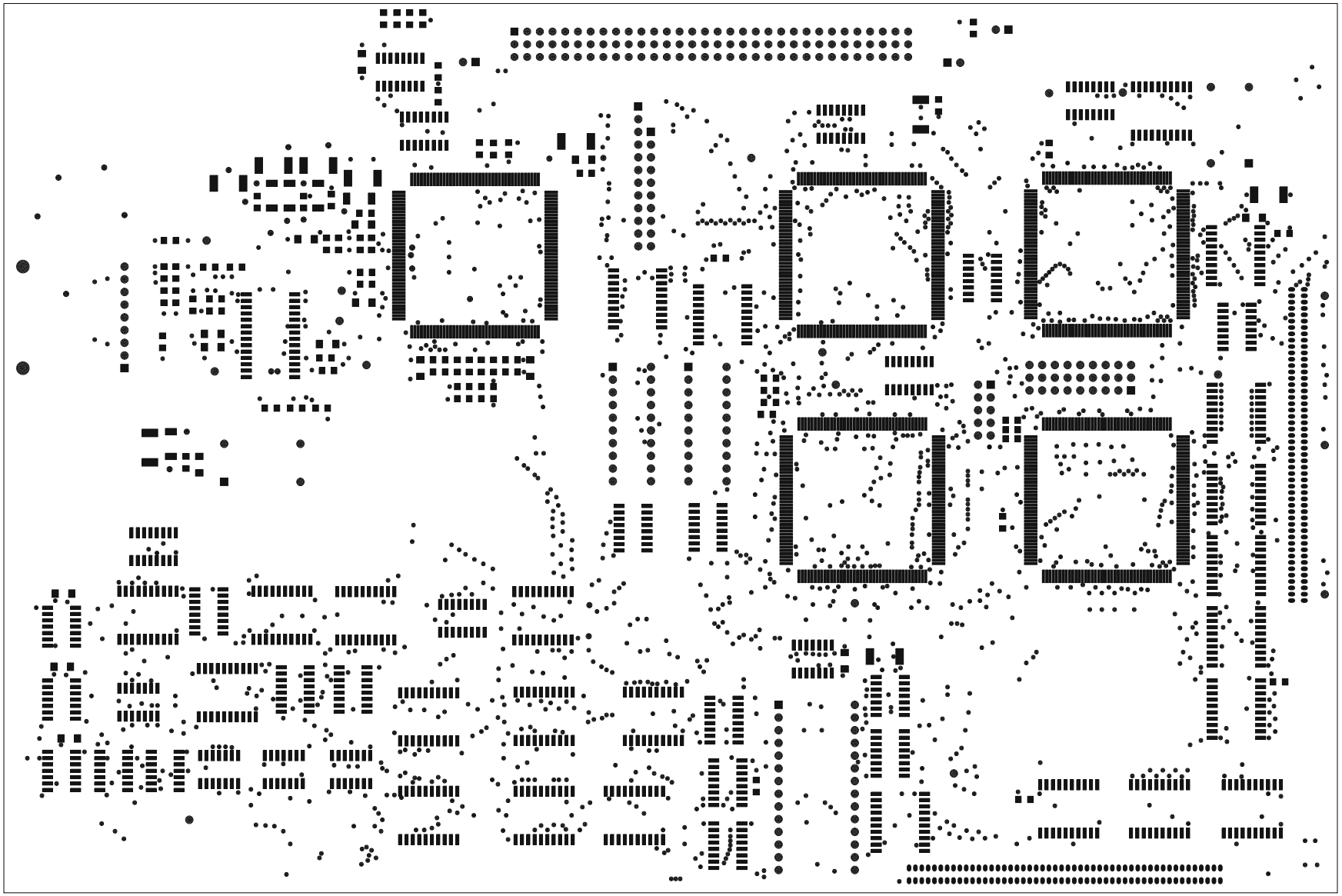
C72
C137
C139
C133
RN13
R71
R70
C103
R74
C127
C118
RN14
R73
C104
C92
C56
C71
C136
C126
C117
C171
C159
C172
C177
R10
C163
RN2
C154
C182
C185
C153
C151
C155
C176
C181
C142
C143
R38
C156
C164
R37
C183
C8
R43
R25
R46
RN10
C165
C186
C150
C157
C160
C167
L1
C33
R53
C173
C178
C9
C12
C168
C111
C112
C96
L3
C65
C76
C121
C109
C175
C77
C86
C7
C180
C123
C6
L2
R79
C187
R1
R7
C24
R4
R11
C170
R80
C188
C4
C49
RN17
C102
C116
C125
C55
C41
R22
C91
C10
C82
C87
R20
R62
C189
R69
C70
C54
R63
C40
RN6
C131
C52
C90
C81
R19
C78
C124
C101
C28
C115
C13
C66
C50
C25
R78
C30
C31
C58
C43
C44
C74
C59
R76
C75
C107
C119
C128
C60
R75
C73
C42
C20
C106
C93
C57
C29
C19
R47
C45
R57
C53
R42
C89
C17
R36
C68
C114
R52
C18
C37
C39
C88
C67
C27
C99
C38
C80
C100
C51
C26
C5
C85
R77
C120
C108
R15
R16
R50
C3
C69
U5
C1
C2
C79
R23
A1
A2

SOLDER_MASK TOP

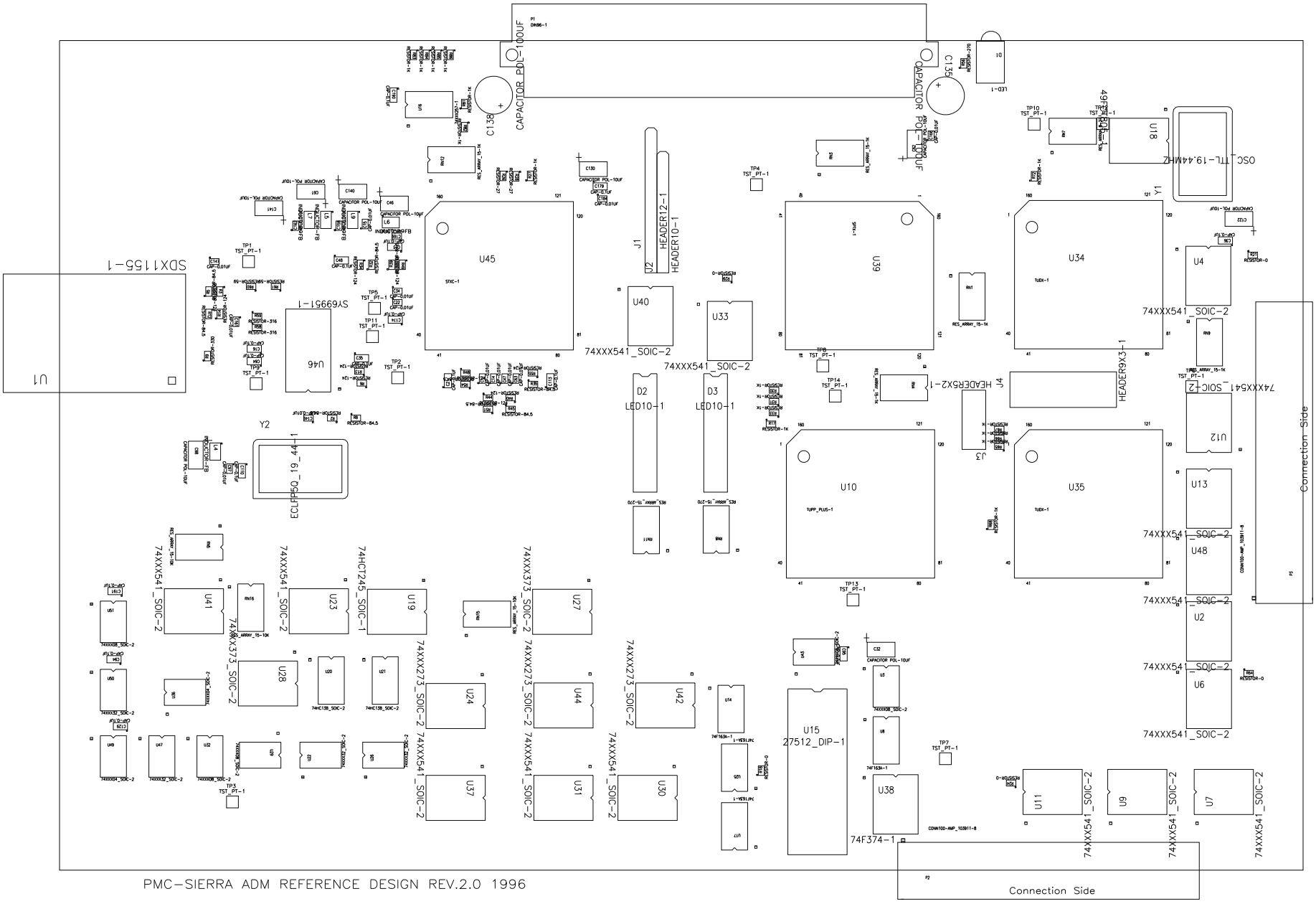


PMC–SIERRA ADM REFERENCE DESIGN REV.2.0 1996

SOLDER_MASK BOTTOM

PMC-SIERRA ADM REFERENCE DESIGN REV.2.0 1996

RES_DES TOP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U34
U40
U33
U10
U35
U15
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U38
74F374-1
U41
U23
U19
U28
U24
U44
U42
U37
U31
U30
U27
U4
U12
U13
U48
U2
U6
U11
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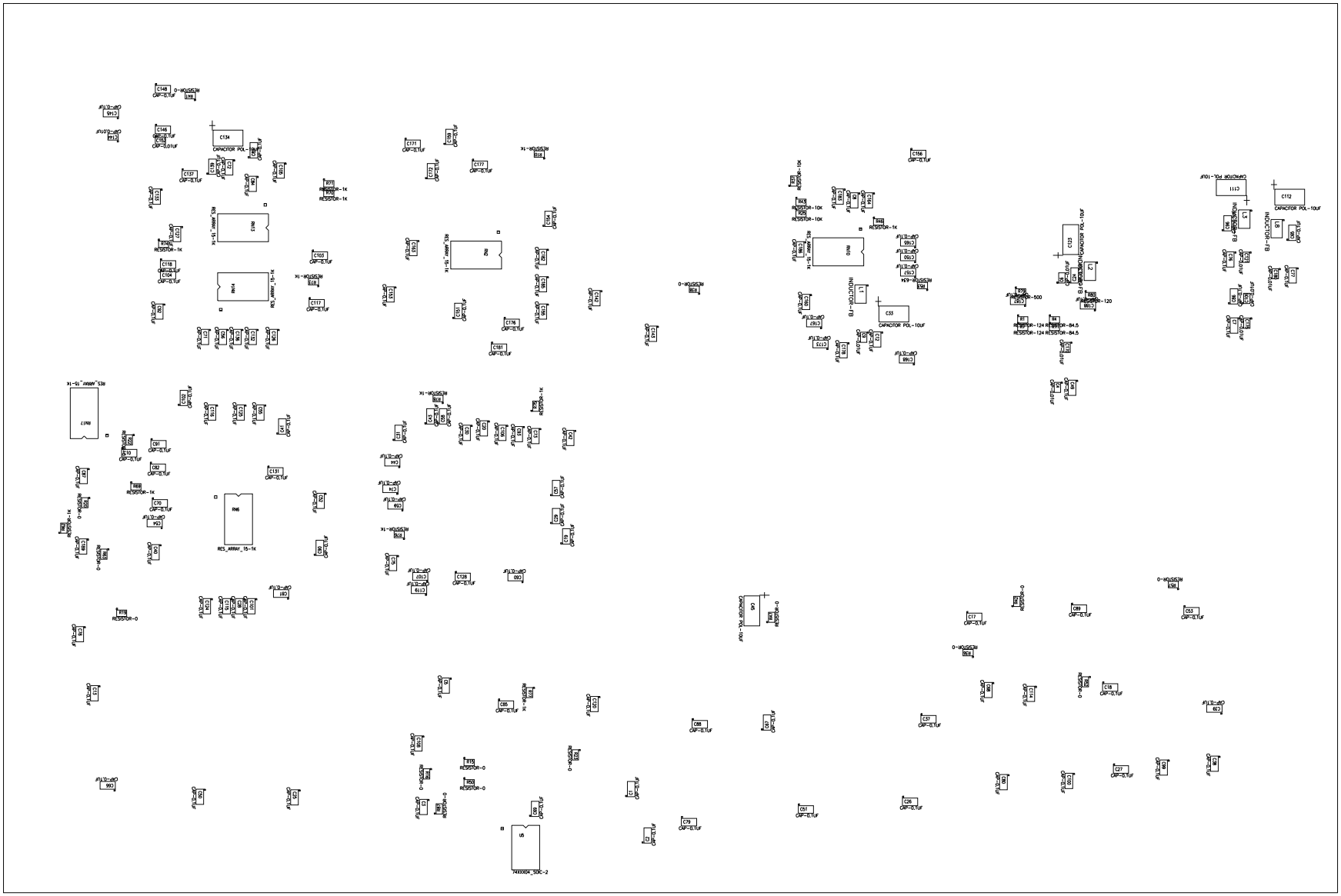
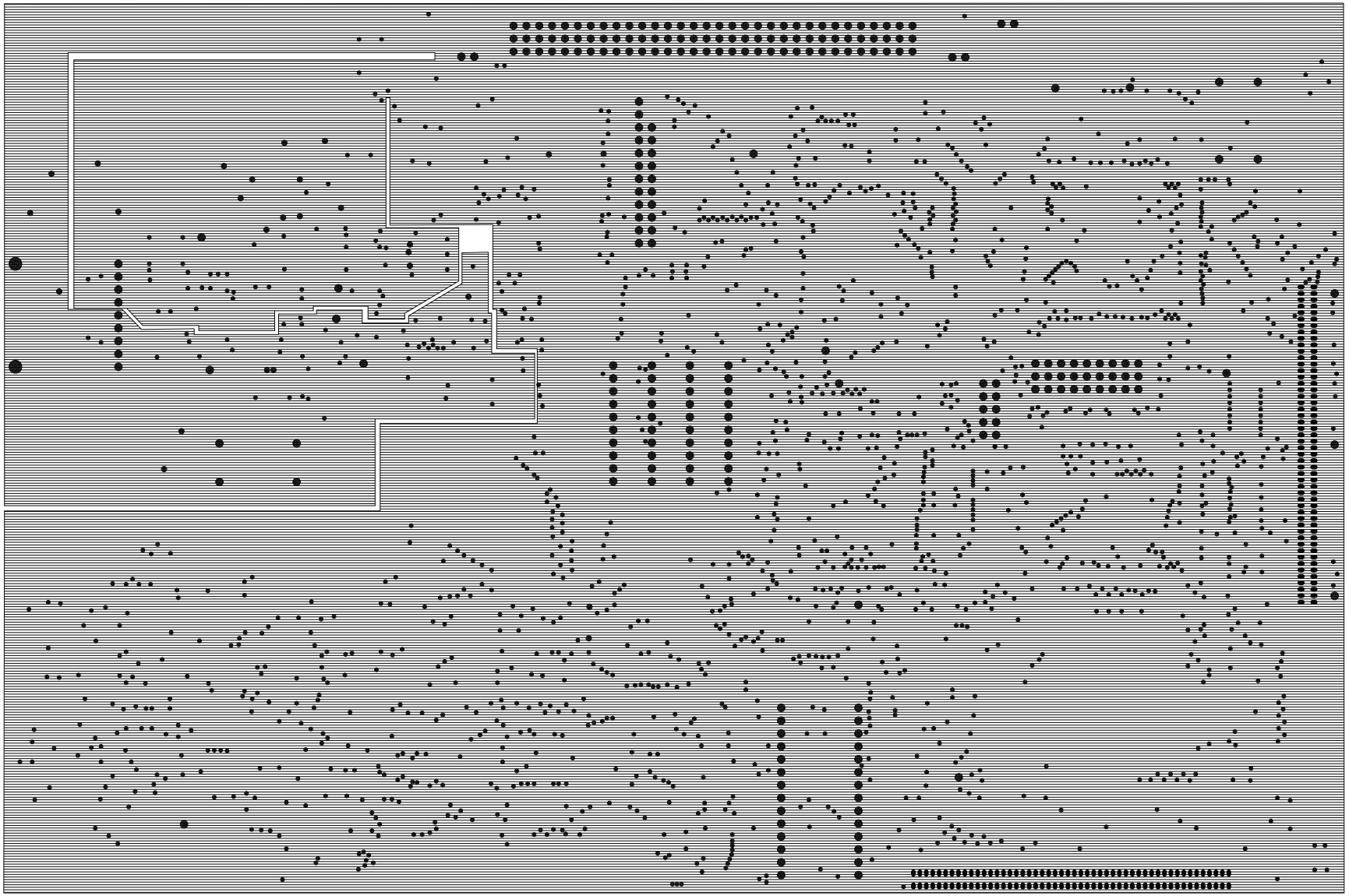


VCC_PLANE



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