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NTE7108
Integrated Circuit
1.3GHz Phase Locked Loop w/I²C Bus

Description:

The NTE7108 is an integrated circuit in an 18–Lead DIP type package and when used in combination with a VCO (tuner), comprises a digital programmable phase–locked loop (PLL) for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides a crystal–stable frequency for tuner oscillators between 16 ~ 1300MHz in the 62.5kHz raster. By including an external prescaler 1/2, the component can also be used for synthesizing applications of up to 2.4GHz (e.g. satellite receivers). As a result, the resolution is doubled to 125kHz. The tuning process is controlled via an I^2C bus by the microprocessor.

Features:

- Low Current Consumption
- Message Transmission Via I^2C Bus
- 4 Software–Controlled Outputs
- Cost–Effective and Space–Saving Design
- Prescaler Output Frequency is Free from Interference Radiation

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_S	–0.3V to 6V
Output PD, V_1	–0.3V to V_S
Crystal Q1, V_2	–0.3V to V_S
Crystal Q2, V_3	–0.3V to V_S
Bus Input/Output SDA, V_4	–0.3V to V_S
Bus Input SCL, V_5	–0.3V to V_S
Port Output P7, V_6	–0.3V to +16V
Port Output P6, V_7	–0.3V to +16V
Port Output P5, V_8	–0.3V to +16V
Port Output P4, V_9	–0.3V to +16V
Port Output P3, V_{10}	–0.3V to +16V
Port Output P2, V_{11}	–0.3V to +16V
Port Output P1, V_{12}	–0.3V to +16V
Port Output P0, V_{13}	–0.3V to +16V
Signal Input UHF/VHF, V_{15}	–0.3V to +2.5V
Reference Input REF, V_{16}	–0.3V to +2.5V
Output Active Filter V_D, V_{18}	–0.3V to V_S
Bus Output SDA (Open Collector), I_{4L}	–1mA to +5mA
Port Output P7 (Open Collector), I_{6L}	–1mA to +5mA

Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings (Cont'd): (Note 1)

Port Output P6 (Open Collector), I_{7L} . . . . . –1mA to +5mA
Port Output P5 (Open Collector), I_{8L} . . . . . –1mA to +5mA
Port Output P4 (Open Collector), I_{9L} . . . . . –1mA to +5mA
Junction Temperature, T_J . . . . . +125°C
Storage Temperature range, T_{stg} . . . . . –40°C to +125°C
Thermal Resistance, System to Ambient, $R_{\Theta SA}$ 80K/W

Note 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range:

Supply Voltage, V_S . . . . . 4.5V to 5.5V
Ambient Temperature range, T_A . . . . . 0° to +85°C
Input Frequency, I_{15} . . . . . 16MHz to 1300MHz
Crystal Frequency, $I_{2, 3}$ 4MHz
Divider Factor, N . . . . . 256 to 32767

Electrical Characteristics: (V_S = 5V, T_A = +25°C unless otherwise specified)

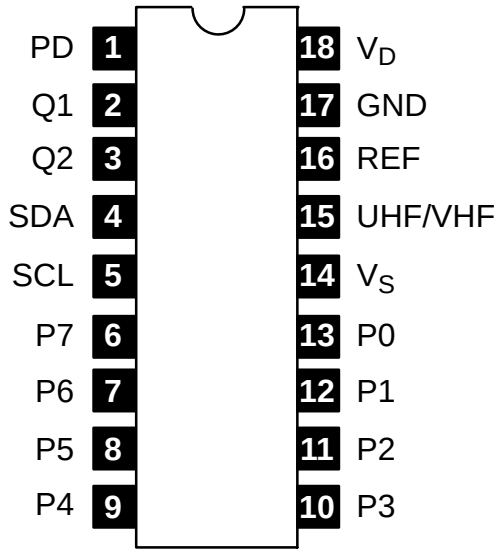
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Consumption	I_S		35	55	75	mA
Crystal Frequency Series Capacitance 18pF	$f_{2, 3*}$		–	–	4	MHz
Input Sensitivity UHF/VHF	a_{15}	f_{15} = 80 to 500MHz	–27/10	–	3/315	dBm/*
		f_{15} = 500 to 1000MHz	–24/14	–	3/315	dBm/*
		f_{15} = 1200MHz	–15/40	–	3/315	dBm/*
Band Selection Outputs P0 – P3 (Current Sinks ^{W}/Internal Resistance R_i = 12kΩ)						
Leakage Current	I_{13H}	V_{13H} = 13.5V	–	–	10	µA
Sink Current	I_{13L}	V_{13H} = 12V	0.7	1.0	1.5	mA
Port Outputs P4 – P7 (Switch ^{W}/Open Collector)						
Leakage Current	I_{9H}	V_{9H} = 13.5V	–	–	10	µA
Residual Voltage	V_{9L}	I_{9L} = 1.7mA	–	–	0.3	V
Phase Detector Output PD (V_S = 5V)						
Charge Pump Current	I_{1H}	5 I = High, V_1 = 2V	±90	±220	±300	µA
		5 I = Low, V_1 = 2V	±22	±50	±75	µA
Output Voltage Locked	V_{IL}		1.5	–	2.5	V
Active Filter Output V_D (Test Modus T0 = 1, PD = Tristate)						
Output Current	I_{1B}	V_{18} = 0.8V, I_{14} = 90µA	500	–	–	µA
Output Voltage	V_{18}	V_{1L} = 0V	–	–	100	mV
Bus Inputs SCL, SDA						
Input Voltage	V_{5H}		3.0	–	5.5	V
	V_{5L}		–	–	1.5	V
Input Current	I_{5L}	$V_{5H} = V_S$	–	–	50	µA
		V_{5L} = 0V	–	–	–100	µA

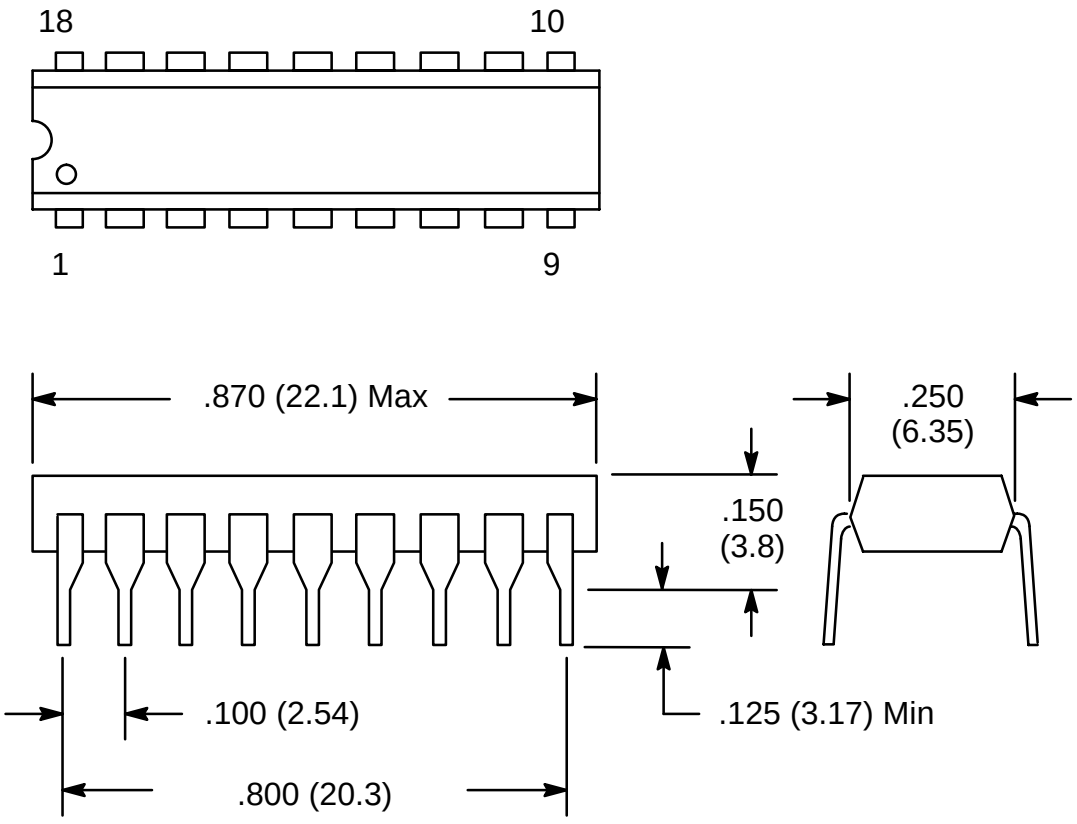
* Listed as mV_{rms} with 50Ω.

Electrical Characteristics (Cont'd): (V_S = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output SDA (Open Collector)						
Output Voltage	V_{4H}	I_{4H} = 5.5mA	–	–	12	V
	V_{4L}	I_{4L} = 2mA	–	–	0.4	V
Edges SCL, SDA						
Rise Time	t_R		–	–	15	µs
Fall Time	t_F		–	–	15	µs
Shift Register Clock Pulse SCL						
Frequency	f_5		0	–	100	kHz
Pulse Width	$t_{5\ HIGH}$		4	–	–	µs
	$t_{5\ LOW}$		4	–	–	µs
Start						
Set–Up Time	t_{SUSTA}		4	–	–	µs
Hold Time	t_{HDSTA}		4	–	–	µs
Stop						
Set–Up Time	t_{SUSTO}		4	–	–	µs
Bus Free Time	t_{BUF}		4	–	–	µs
Data Transfer						
Set–Up Time	t_{SUDAT}		0.3	–	–	µs
Hold Time	t_{HDDAT}		0	–	–	µs

Pin Connection Diagram




18
10
1
9
.870 (22.1) Max
.250
(6.35)
.150
(3.8)
.100 (2.54)
.125 (3.17) Min
.800 (20.3)