PM5351

S/UNI-155 TETRA WITH S/UNI ATLAS

REFERENCE DESIGN

RELEASED

ISSUE 1: SEPTEMBER 2001

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	September 2001	Document Created

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 DEFINITIONS

CPCI	Compact PCI. An adapted specification from the Peripheral Component Interconnect (PCI) Specification 2.1 or later using a mechanical form factor suitable for tugged environments.
FM	Fault Management. The mechanism used by the network to inform management entities and other network equipment of faults within the network.
MT-RJ	Form factor for fibre optic connectors which feature receive and transmit interfaces in a single plug.
OAM	Operations, Administration, and Maintenance. The maintenance of VCs within the network.
PCI	Peripheral Component Interconnect. A specification typically used to interconnect PC chipsets.
PM	Performance Management. The mechanism used by the network to monitor the performance parameters of a particular VC.
VC	Virtual Connection. This refers to either a Virtual Path Connection (VPC) or a Virtual Channel Connection (VCC) within a physical link.
VCC	Virtual Channel Connection. A virtual connection between two network elements. A virtual channel connection is normally a constituent member of a virtual path connection, where the VPC consists of one or more VCCs. This is sometimes known as an F5 connection.
VPC	Virtual Path Connection. A virtual connection between two network elements. A virtual path connection may span one or more physical links. This is sometimes known as an F4 connection.

2 FEATURES

The following features are supported by this reference design. Note that the list of features is not exhaustive, nor does it represent the full capabilities of the TETRA or the ATLAS.

- Support for up to 8K VCs (Virtual Connections)
- Ingress header translation
- Ingress cell rate policing (per-VC and per-PHY)
- OAM-FM on all VCs
- OAM-PM on 256 bidirectional VCs
- Egress header translation
- Four STS-3c interfaces using MT-RJ fibre optic connectors

3 APPLICATIONS

- ATM Switch Port Card

4 REFERENCES

1. PMC-1971154, “S/UNI-ATLAS Datasheet”, Issue 7, Jan 2000.

2. PMC-1971240, “S/UNI-TETRA Datasheet”, Issue 7, Feb 2000.

3. PICMG 2.0 R2.1, “CompactPCI Specification”, September 2, 1997

4. PMC-1980585, “S/UNI-ATLAS Programmers Guide and Example Software”, Issue 2, Feb 1999.

5. PMC-1981505, “S/UNI-ATLAS Datasheet Errata”, Issue 1, June 2001.

6. PMC-1980583,”Switch Port (SPORT) Card Reference Design”, Issue 3, Nov 1999.

7. PMC-1990330, “ATM Switch Using S/UNI-ATLAS, QRT, and QSE Reference Design”, Issue 2, July 1999.

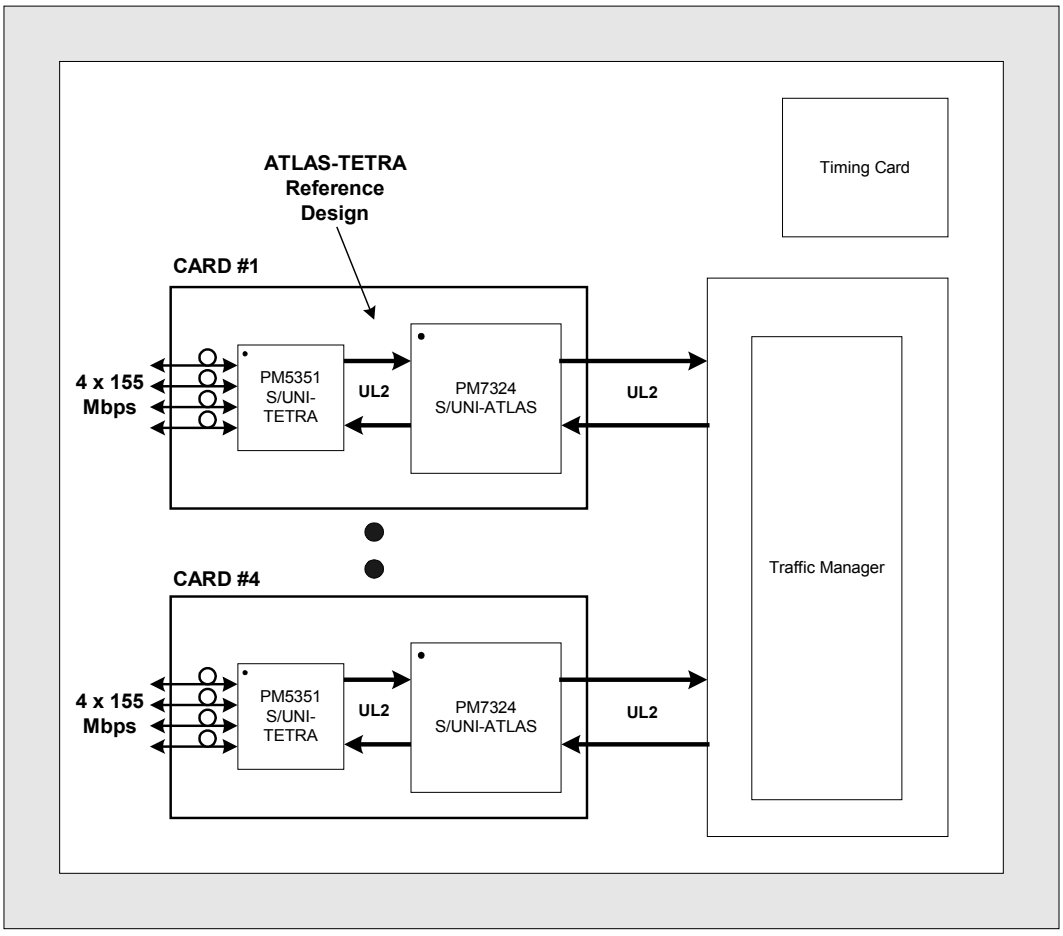
8. ATM Forum, “ATM Forum Traffic Management Specification Version 4.1”, Mar 1999.

5 APPLICATION EXAMPLES

5.1 ATM Switch Port Card

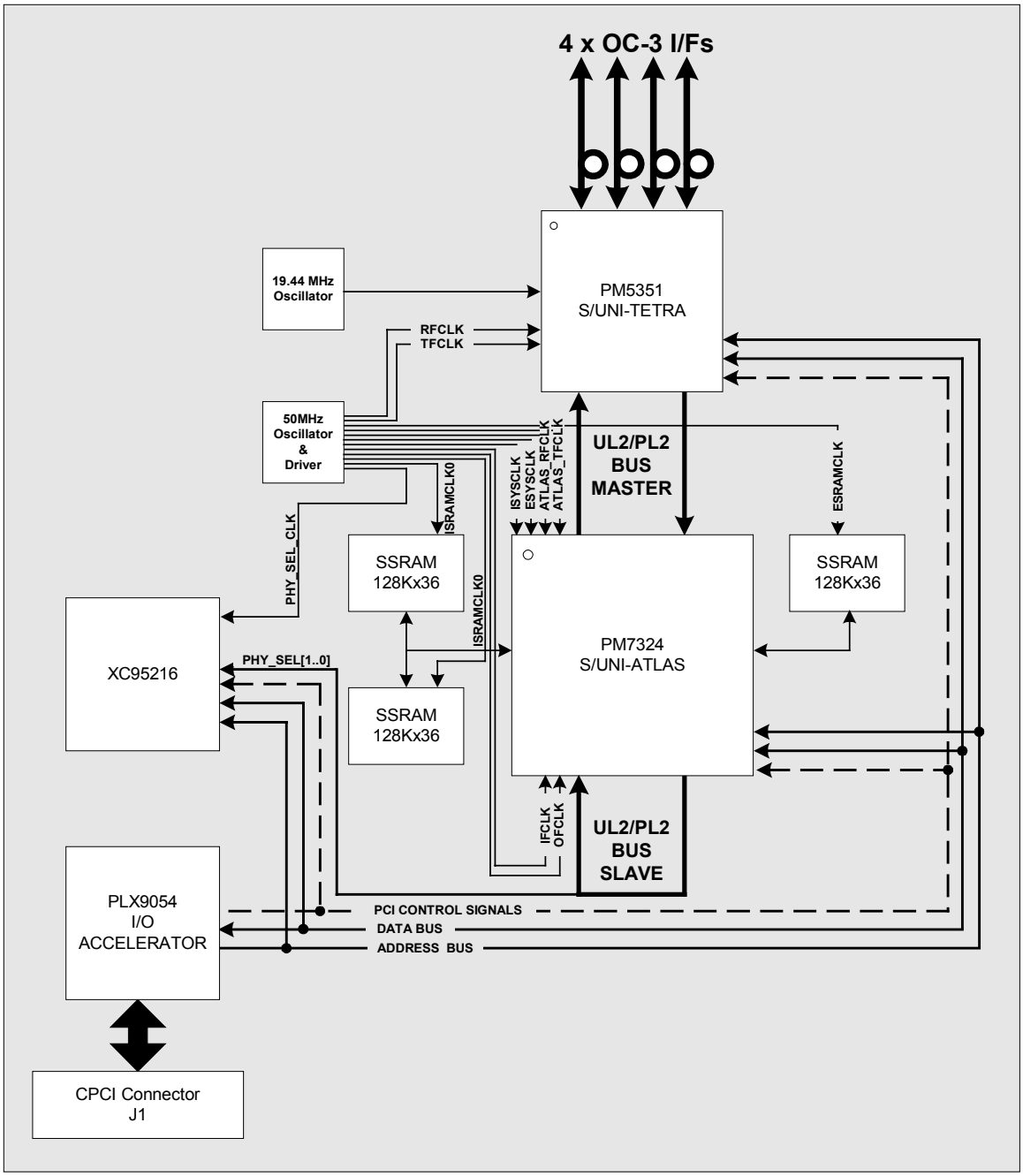
The figure below shows a complete ATM switch using the S/UNI 155 TETRA and S/UNI ATLAS on a line card. This design is explained in detail in PMC-1980583 “Switch Port (SPORT) Card Reference Design” and PMC-1990330 “ATM Switch Using S/UNI-ATLAS, QRT, and QSE Reference Design”

Figure 1 - ATM Switch Using S/UNI-155-TETRA and S/UNI-ATLAS



6 BLOCK DIAGRAM

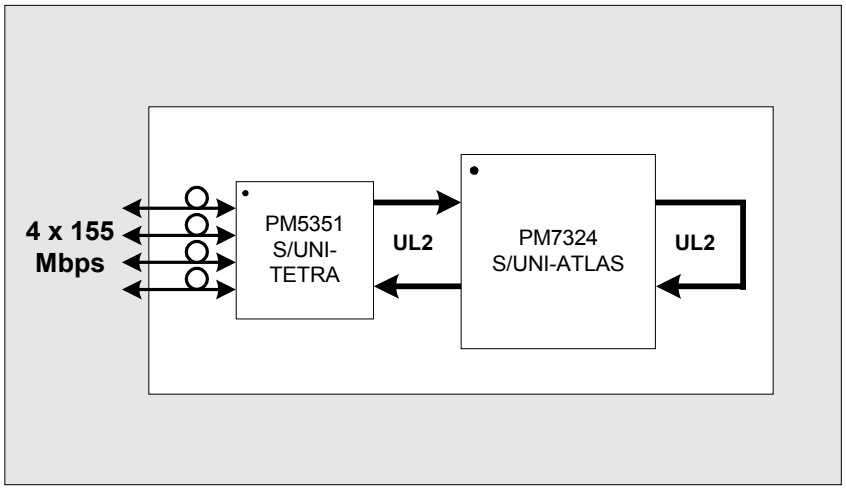
Figure 2 - Block Diagram of ATLAS-TETRA Reference Design



7 FUNCTIONAL DESCRIPTION

The S/UNI-155-TETRA with S/UNI-ATLAS reference board is designed to demonstrate the features of the PM5351 S/UNI-155-TETRA and the PM7324 S/UNI-ATLAS on a small form factor PCB. As a result, it is a subset of a complete ATM switch (see Section 5.1). On the receive side, the S/UNI TETRA takes SONET/SDH traffic from 4xOC3 PHYs and extracts ATM cells from the SONET/SDH frame for subsequent processing by the S/UNI-ATLAS device. Once the ATM cells are passed to the ATLAS via the UL2 master interface, they are processed according to their corresponding VC table. The processed cells are then passed to the slave UL2 interface that is looped back into the egress direction of the ATLAS device. After egress processing occurs, the cells are passed back to the S/UNI-TETRA for insertion into a SONET/SDH frame and subsequent transmission over the optical medium.

Figure 3 - Operation of the Reference Design



7.1 PM5351 S/UNI-155-TETRA

The TETRA is responsible for all physical layer functions. It features internal clock and data recovery for four 155 Mbps optical interfaces. MT-RJ connectors are used to interface to the optical fiber. For more information on the PM5351 S/UNI-TETRA, please refer to the S/UNI-TETRA Datasheet, PMC-1971240.

7.2 PM7324 S/UNI-ATLAS

The PM7324 S/UNI-ATM Layer Solution (S/UNI-ATLAS) is a PMC-Sierra standard product that implements the following ATM Layer functions:

- OAM processing according to ITU-T I.610 1998.
- Header Translation on full VPI/VCI address range.
- Prepend/Postpend tagging.
- Cell rate policing according to ITU-T I.371 using the Generic Cell Rate Algorithm.
- Per-PHY queuing to prevent head-of-line blocking.

In the receive direction, the S/UNI ATLAS takes cells from the S/UNI-155-TETRA and performs a lookup based on the PHY number, VPI, and VCI to identify the associated connection. Once the connection is identified, the cell is processed according to the configuration of the connection. In this application, the ATLAS can perform header translation, per-PHY and per-VC policing, performance monitoring, and fault management.

In the transmit direction, a direct lookup is performed by the ATLAS to identify the connection. The cell is then processed according to the configuration in the context table for that connection. Header translation and OAM processing can be done at the egress.

For a more detailed description of the S/UNI-ATLAS, please refer to the S/UNI-ATLAS Datasheet, PMC-1971154.

7.2.1 Note on S/UNI-ATLAS Throughput

This reference design uses a 50 Mhz clock for the UL2 bus. However, due to a throughput issue in the S/UNI-ATLAS, as explained in PMC-1981505 “S/UNI-ATLAS Datasheet Errata”, there are certain configurations that do not allow maximum throughput through the device. One workaround is to clock the ISYSCLK at 59.5 Mhz. On this reference design this is not possible as both the ISYSCLK and ESYSCLK are clocked from the same source. The ESYSCLK is limited to a maximum clock frequency of 57 Mhz. In addition, if the clock frequency on ISYSCLK is increased beyond 52Mhz, the HALFSECCLK can no longer be generated internally (it will be faster than ½ Second) and must be sourced externally. A more detailed description of workaround options can be found in PMC-1981505 “S/UNI-ATLAS Datasheet Errata”.

7.2.2 Ingress SRAM

The Ingress VC Table is a 15-row 64 bit data structure which contains context information for up to 65536 connections. The Ingress VC Table is used for connection identification, connection configuration and cell processing functions.

The connection identification fields of the VC Table are located in the first two rows of the structure, and the remaining rows are used for connection configuration and cell processing.

The Ingress VC Table is stored externally to the S/UNI-ATLAS in SRAM (Static Ram). The ingress SRAM data bus is 72 bits wide (8 bytes plus byte parity), with an address space of 20 bits (1M). This creates enough context address space for 64K VCs. The entire SRAM space does not have to be populated however. If less than 64K VCs are required, or a subset of ATLAS features is used, then the SRAM required is reduced. However, additional glue logic may be required to achieve the savings in SRAM. In this reference design, enough SRAM is used to provision up to 8K VCs.

For the ATLAS, synchronous flow-through non-pipelined SRAMs must be used for both the Ingress and Egress.

7.2.3 Egress SRAM

The Egress VC table is a 16-row 32-bit data structure which contains context information for up to 65536 connections. The Egress VC Table is used for connection identification, connection configuration and cell processing functions. The connection identification field of the Egress VC Table record is located in the first row of the structure, and the remaining rows are used for connection configuration and cell processing.

Like the Ingress VC Table, the Egress VC Table is stored external to the S/UNI-ATLAS in SRAM. The egress SRAM data bus is 36 bits wide (4 bytes plus byte parity), with an address space of 20 bits (1M). This allows for 64K connections, as with the Ingress VC Table. In this design, enough SRAM is provided to provision up to 8K VCs.

7.3 Compact PCI Interface

Microprocessor access to the devices on board is provided using a PLX 9050 PCI bridge chip between the compact PCI bus and the local microprocessor bus. An AMP HM 2mm connector is used in accordance with the CPCI standard.

For more information on the pin functions refer to CompactPCI Specification [10].

7.4 Microprocessor Port CPLD

A Xilinx 95216 CPLD is used perform the following functions.

- PHY output select

- Board reset

7.4.1 PHY Output Select

The CPLD allows the user to manually select which PHY the looped back data will be output to. Table 2 shows what values to write for each output channel.

Figure 4 - PHY Channel Selection

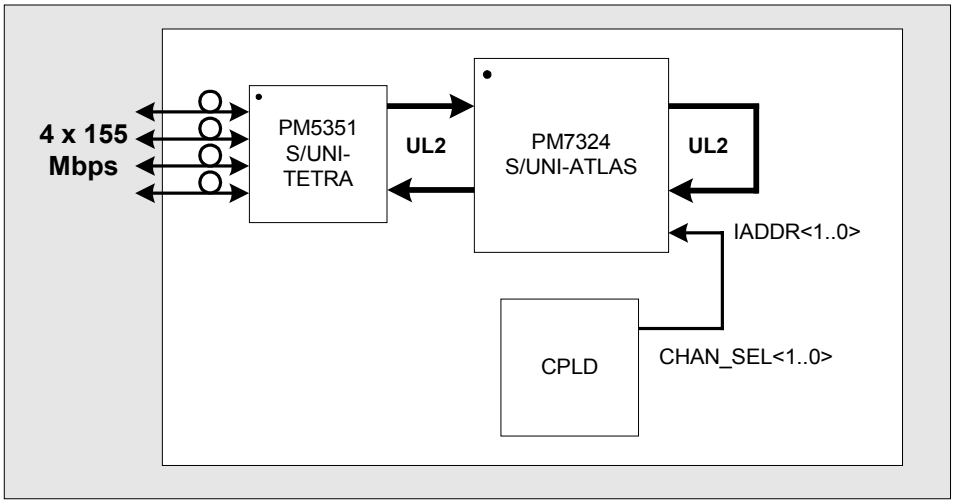


Table 1 below describes the function of bits in the Output Channel Select Register.

Table 1 - CPLD Output Channel Select Register 0x00h

Bit	Type	Function	Default
7..2		NOT USED	0
1	W	CHAN_SEL(1)	0
0	W	CHAN_SEL(0)	0

CHAN_SEL [1..0]

These bits are used to select the output PHY.

Table 2 - PHY Channel Select

CHAN_SEL[1..0]	Output Channel
00	1

CHAN_SEL[1..0]	Output Channel
01	2
10	3
11	4

7.4.2 Board Reset

The CPLD also performs a master reset on all of the devices (TETRA, ATLAS, PCI BRIDGE) when the reset button is pressed.

8 IMPLEMENTATION DESCRIPTION

This section details the hardware on the S/UN-155-TETRA reference design, with reference to the schematics in Section 9.

8.1 Sheet 1, Root Drawing

This sheet shows the interconnection between the functional blocks of the design.

8.2 Sheet 2-3, SUNI-TETRA Block

8.2.1 Sheet 2: TETRA Block

Sheet 2 shows the S/UNI-TETRA and it's surrounding connections. A 19.44MHz oscillator provides timing reference for the S/UNI-TETRA. A 1K resistor is used to prevent latchup when VDD exceeds VBIAS.

8.2.2 Sheet 3: TETRA Supply Filtering

Sheet 3 shows the power supply filtering for the S/UNI-TETRA.

8.3 Sheets 4 – 7, SUNI-ATLAS Block

8.3.1 Sheet 4: SCI-PHY Master Interface

Sheet 4 shows the Ingress Input and Egress Output cell interfaces of the ATLAS. RPOLL and TPOLL pins are both set high to enable PHY polling. Source terminations are used.

8.3.2 Sheet 5: SCI-PHY Slave Interface

Sheet 5 shows the Ingress Output and Egress Input cell interfaces of the ATLAS. J3 selects between UL2 polling mode and direct PHY mode. For normal operation, UL2 polling mode should be used. Y2 and U14 are the source for all 50MHz clocks on the board. Source terminations are used.

8.3.3 Sheet 6: Ingress and Egress SRAM Interfaces

Sheet 6 shows the Ingress and Egress SRAM interfaces.

8.3.4 Sheet 7: Microprocessor Interface

Sheet 7 shows the ATLAS microprocessor interface. TP9 is provided to allow BUSYB to interrupt the microprocessor. This may be useful for SRAM access software routines. The HALFSECCLK input is tied low, since it is not required when ISYSCLK and ESYSCLK is 52, 50, or 25 MHz. A 1K resistor is used to prevent latchup when VDD exceeds VBIAS. If 5V tolerance is not required, VBIAS may be tied to 3.3V.

8.4 PCI INTERFACE Block

8.4.1 Sheet 8: PLX9050 PCI Interface

Sheet 8 shows the PLX9050 PCI bridge chip and associated circuitry. U1 is a serial EEPROM used to provide configuration information to the PLX9050 on startup. Address and Data pins are non multiplexed. Separate RDB and WRB signals are provided and the clock output of the PLX9050 is buffered to drive the CPLD microprocessor interface. 10 Ohm stub terminations are provided as required by the CPCI specification.

8.4.2 Sheet 9 Microprocessor Port CPLD

Sheet 9 shows the CPLD used to perform interrupt identification and PHY output select. Headers are provided to allow in system programming of the CPLD.

The CPLD generates a free running clock for the JTAG interfaces of the ATLAS and TETRA. The free-run clock along with the TMS pin of these devices being tied high, continuously resets the JTAG circuitry ensuring proper operation.

8.5 Sheet 10, OPTICS Block

Sheet 10 shows the four MT-RJ optical transceivers. TXD+/- signal traces are terminated near the optics using two 49.9 Ohm resistors and a DC biasing network. RXD+/- signal traces are terminated with a 100 Ohm resistor across RXD+/-. All differential pairs are kept equal length.

8.6 Sheet 11, INGRESS SRAM

Sheet 11 shows the connections to the ingress SRAM interface. There is enough SRAM to support 8K connections at the ingress. If more connections are required, this configuration would be maintained, and banks would be added using ISA[13:15]. For instance, to add a second bank of SRAM, ISA[13] would

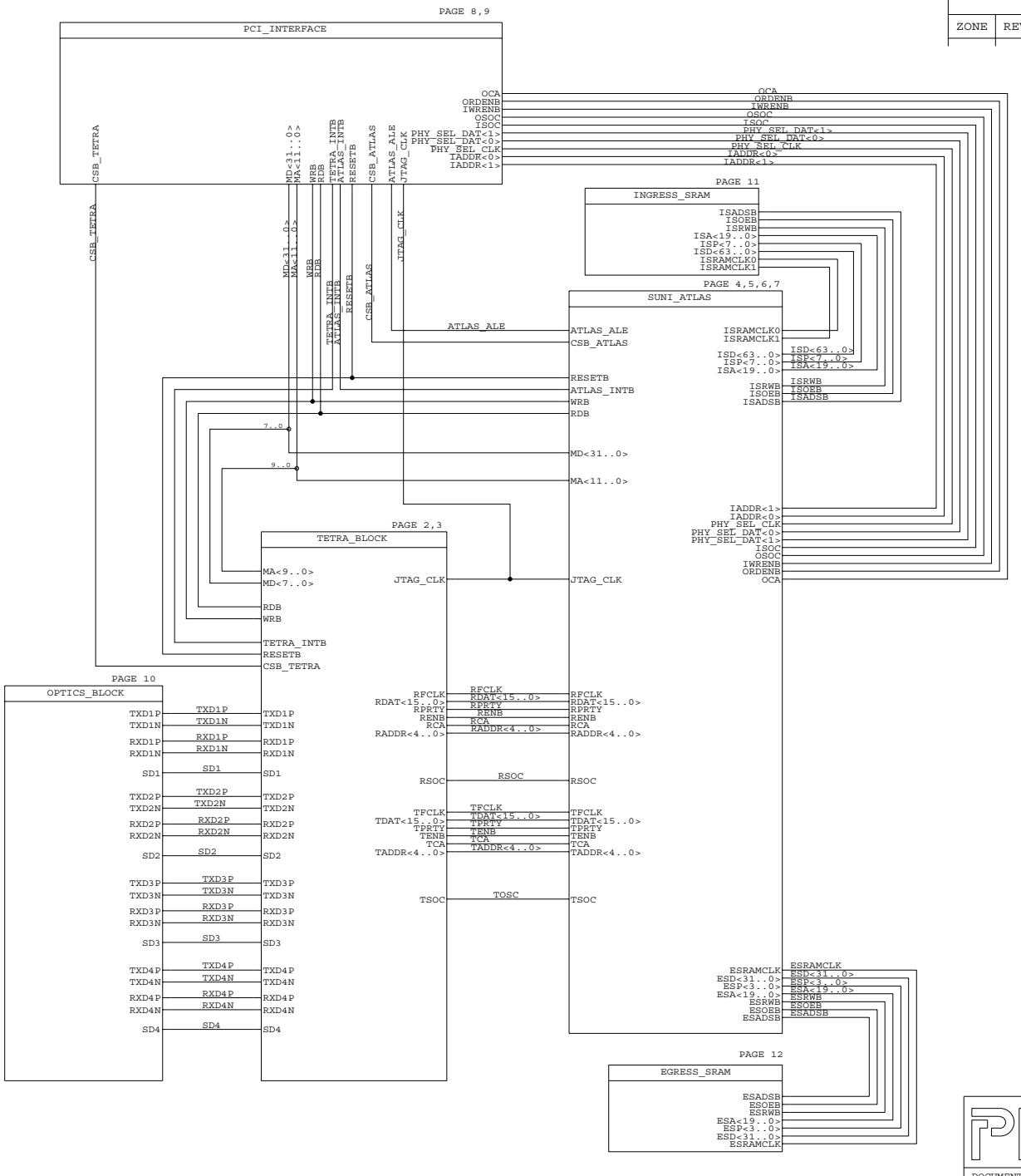
be used to select the second bank. Terminations are not required if the SRAMs are placed close enough to the ATLAS.

8.7 Sheet 12, EGRESS SRAM

Sheet 12 shows the connections to the egress SRAM interface. There is enough SRAM to support 8K connections at the egress. If more connections are required, this configuration would be maintained, and banks would be added using ESA[13:15]. Terminations are not required if the SRAMs are placed close enough to the ATLAS. GSI Technology SRAMS are recommended and have been tested with the S/UNI-ATLAS.

9 SCHEMATICS

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

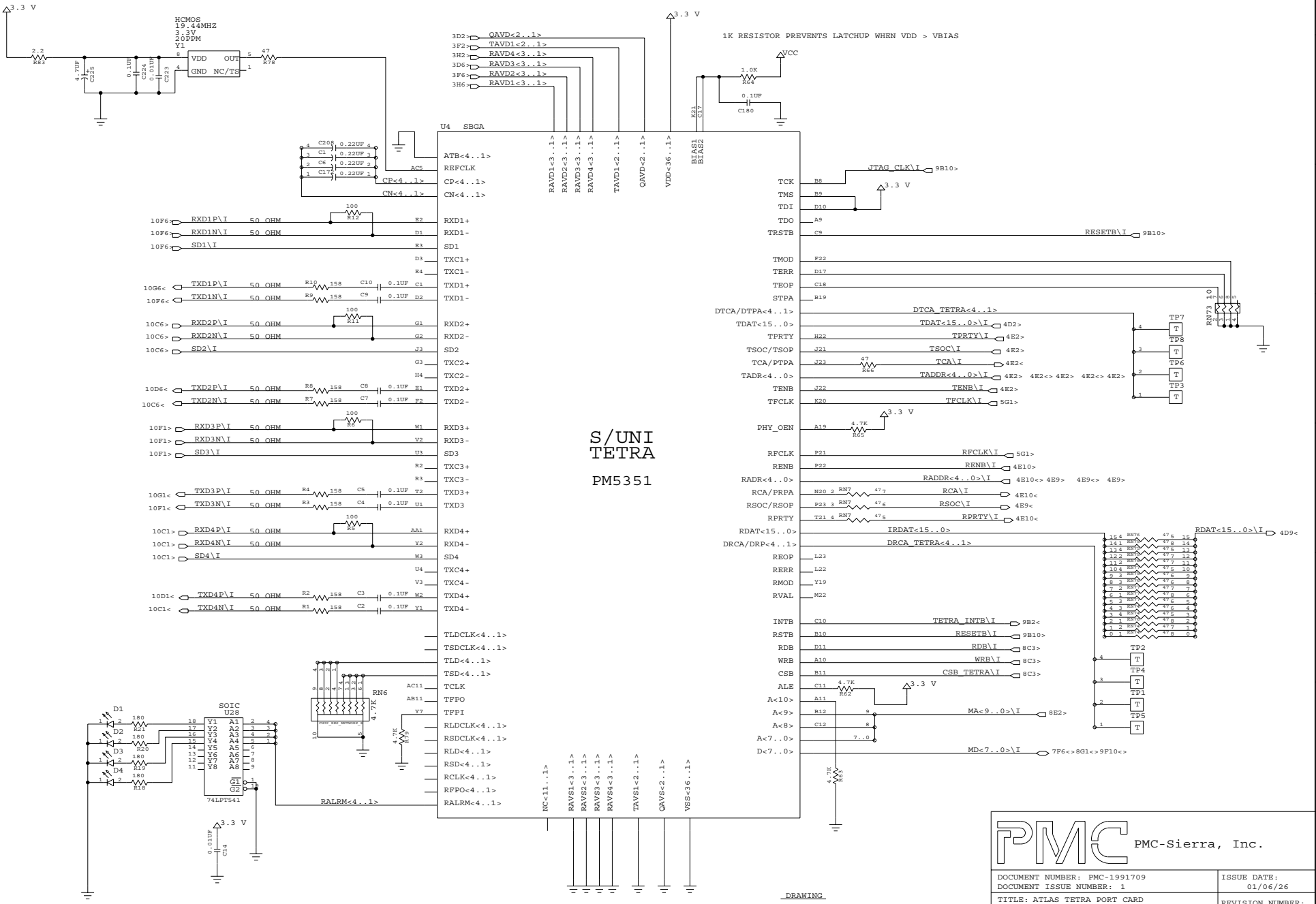


DRAWING:
TITLE=ATLAS ROOT
ABBREV=ATLAS ROOT
LAST_MODIFIED=Thu Jun 28 13:56:11 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD ROOT DRAWING	REVISION NUMBER: 2
ENGINEER: RS	PAGE:1 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

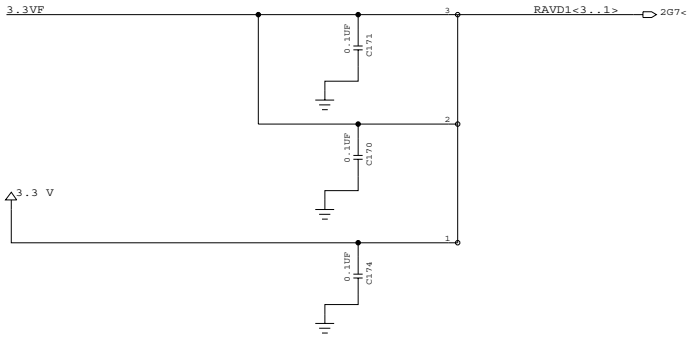
TITLE=TETRA_BLOCK
ABBREV=TETRA_BLOCK
LAST_MODIFIED=Thu Jun 28 13:59:04 2001

PMC-Sierra, Inc.

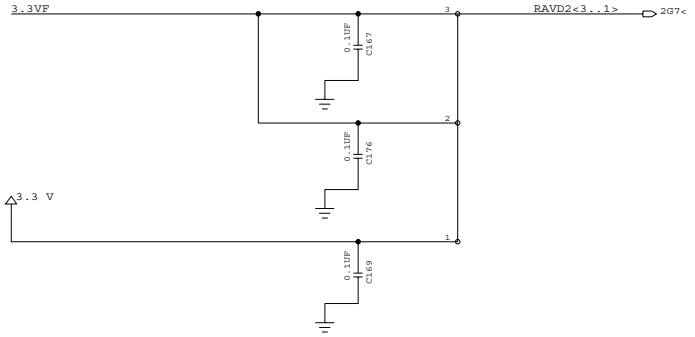
DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD TETRA BLOCK	REVISION NUMBER: 2
ENGINEER: RS	PAGE:2 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

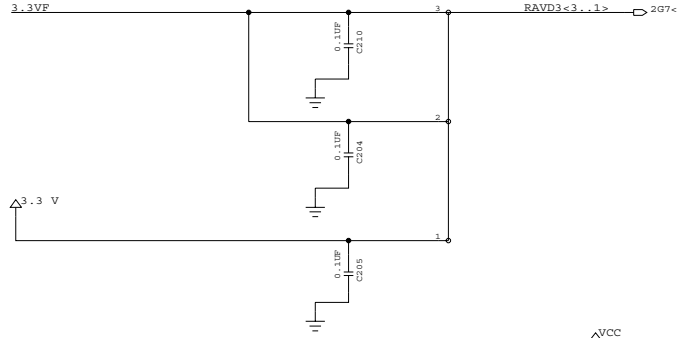
ANALOG RECEIVE 1



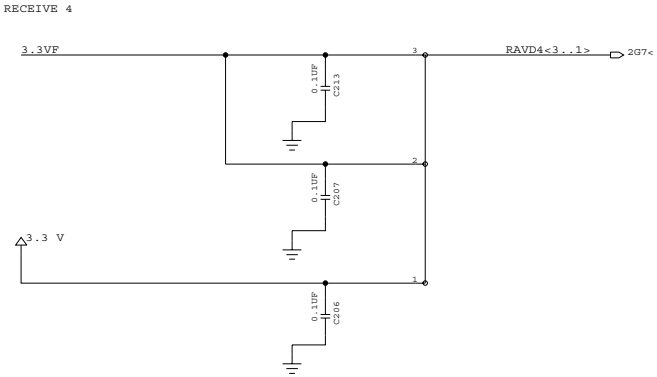
ANALOG RECEIVE 2



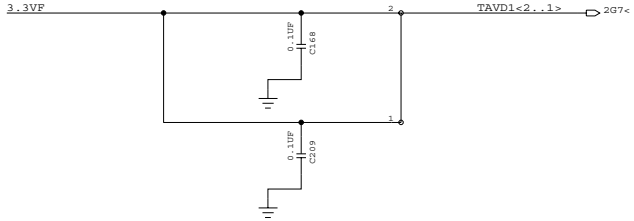
ANALOG RECEIVE 3



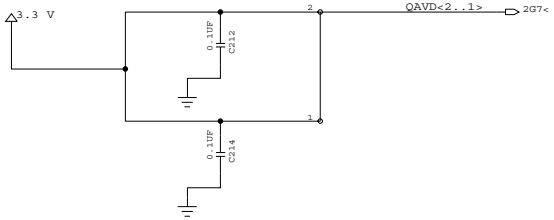
ANALOG RECEIVE 4



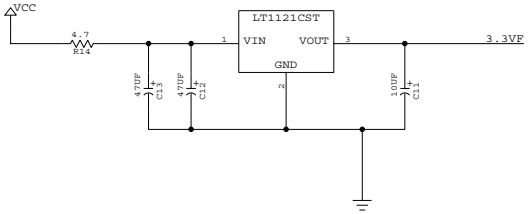
ANALOG TRANSMIT

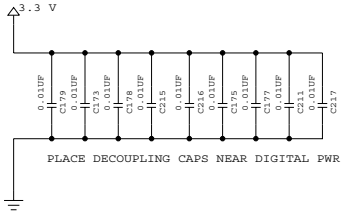


ANALOG QAVD



SOT
3.3V
U11





PLACE DECOUPLING CAPS NEAR DIGITAL PWR PINS

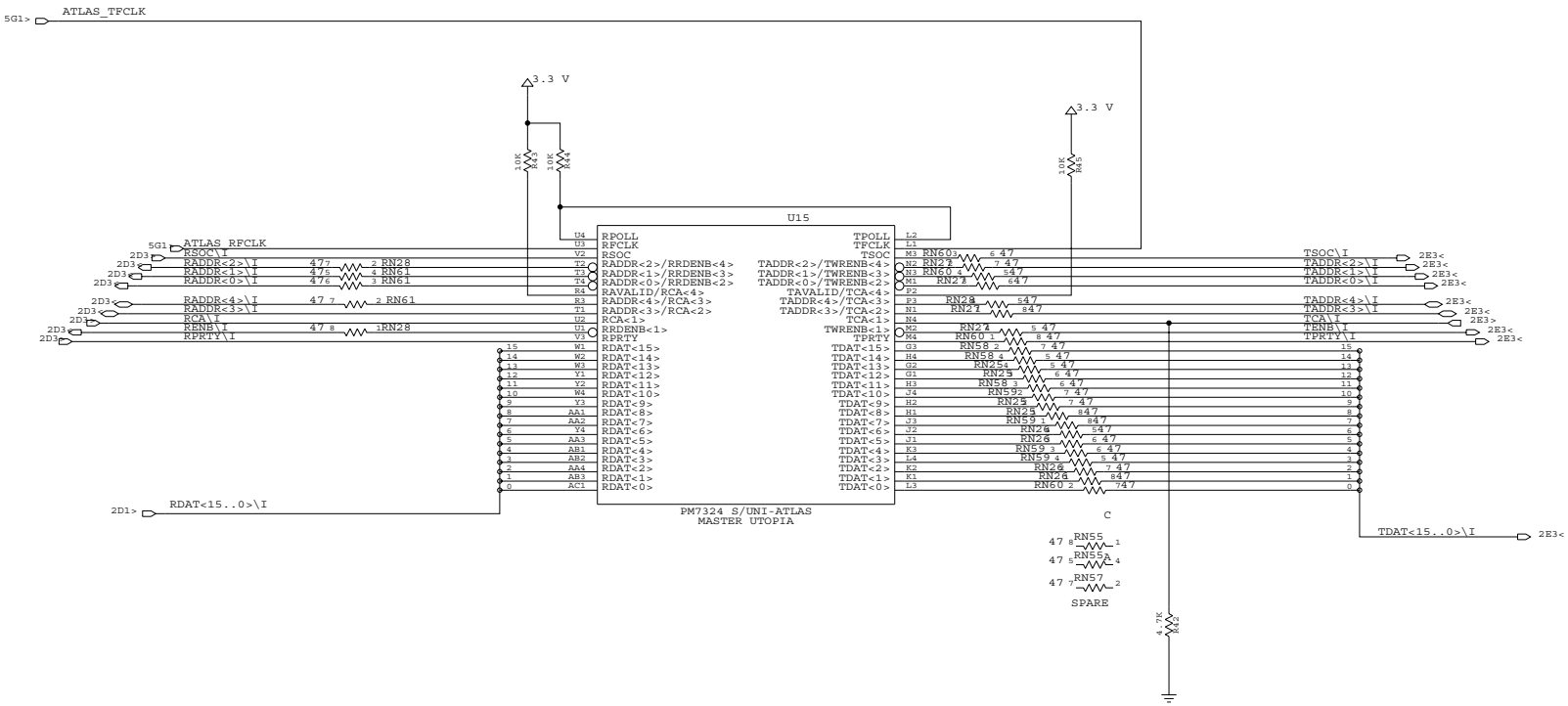
DRAWING

TITLE=TETRA_BLOCK
ABBREV=TETRA_BLOCK
LAST_MODIFIED=Thu Jun 28 13:59:06 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD TETRA BLOCK	REVISION NUMBER: 2
ENGINEER: RS	PAGE:3 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

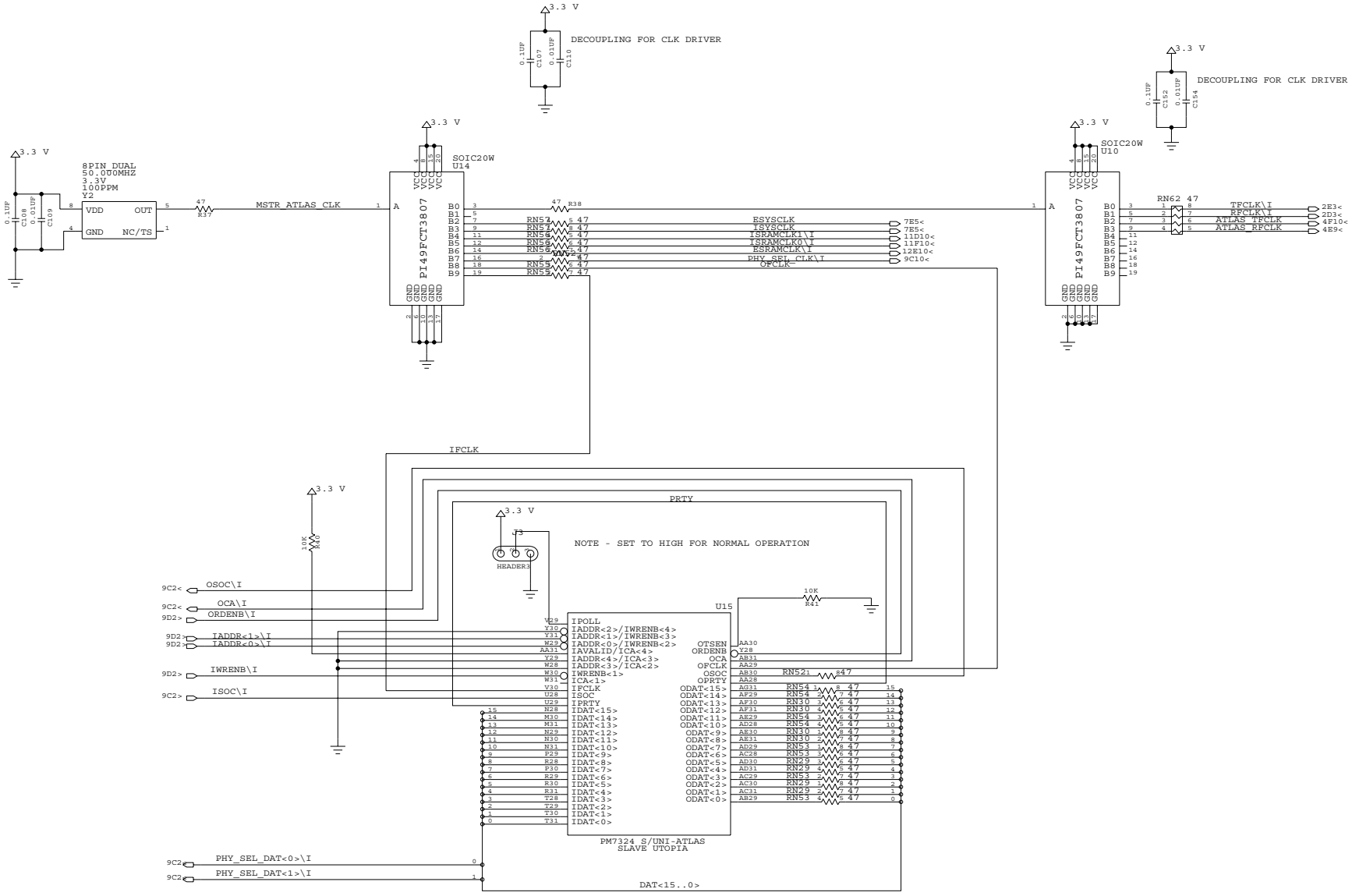


DRAWING:
TITLE=SUNI_ATLAS
ABBREV=SUNI_ATLAS
LAST_MODIFIED=Thu Jun 28 13:59:08 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD ATLAS SCI-PHY MASTER INTERFACE	REVISION NUMBER: 2
ENGINEER: RS	PAGE:4 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

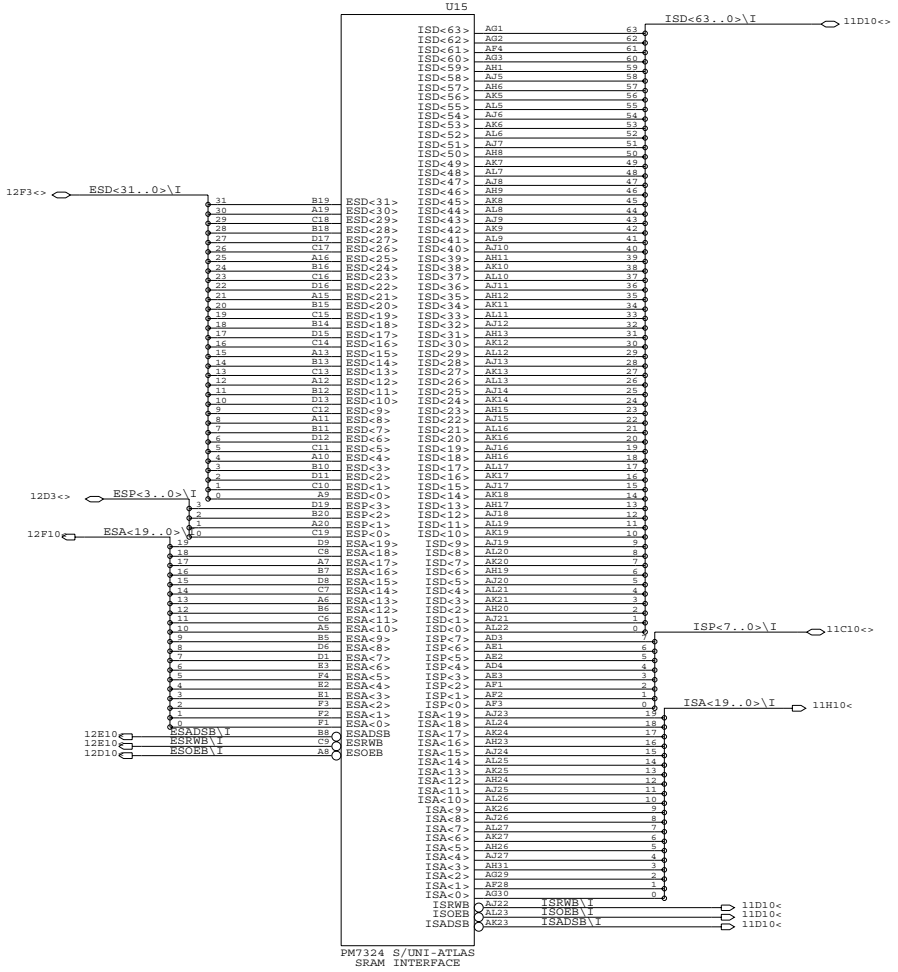


DRAWING:
TITLE=SUNI_ATLAS
ABBREV=SUNI_ATLAS
LAST_MODIFIED=Thu Jun 28 13:59:10 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD ATLAS SCI-PHY SLAVE INTERFACE	REVISION NUMBER: 2
ENGINEER: RS	PAGE:5 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

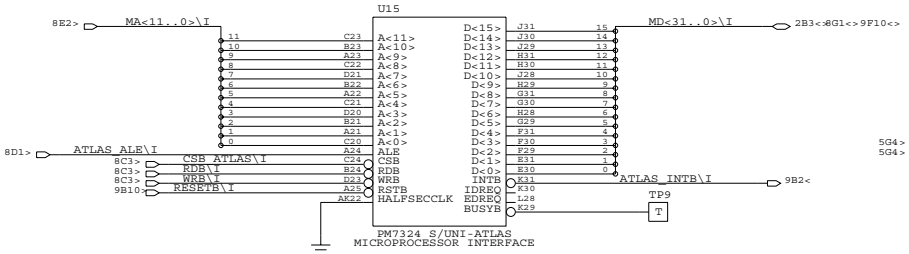


DRAWING:
TITLE=SUNI ATLAS
ABBREV=SUNI ATLAS
LAST_MODIFIED=Thu Jun 28 13:59:12 2001

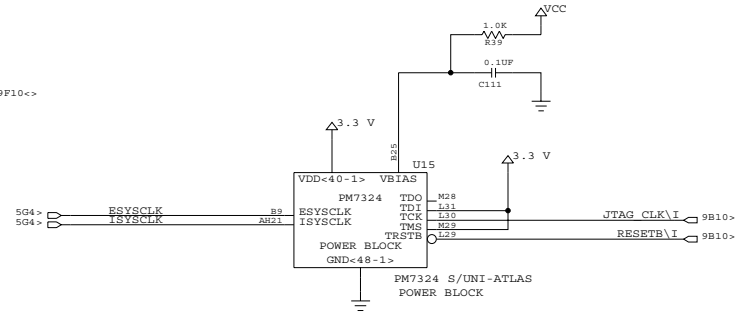
PMC-Sierra, Inc.

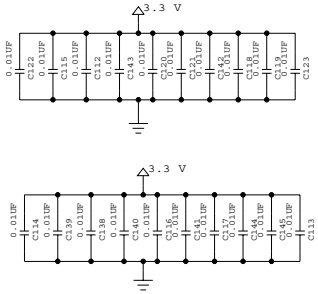
DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD ATLAS SRAM INTERFACES	REVISION NUMBER: 2
ENGINEER: RS	PAGE:6 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



1K RESISTOR PREVENTS LATCHUP WHEN VDD > VBIAS





DECOUPLING FOR ATLAS
1 CAP EVERY OTHER POWER PIN

DRAWING:
TITLE=SUNI_ATLAS
ABBREV=SUNI_ATLAS
LAST_MODIFIED=Thu Jun 28 13:59:14 2001

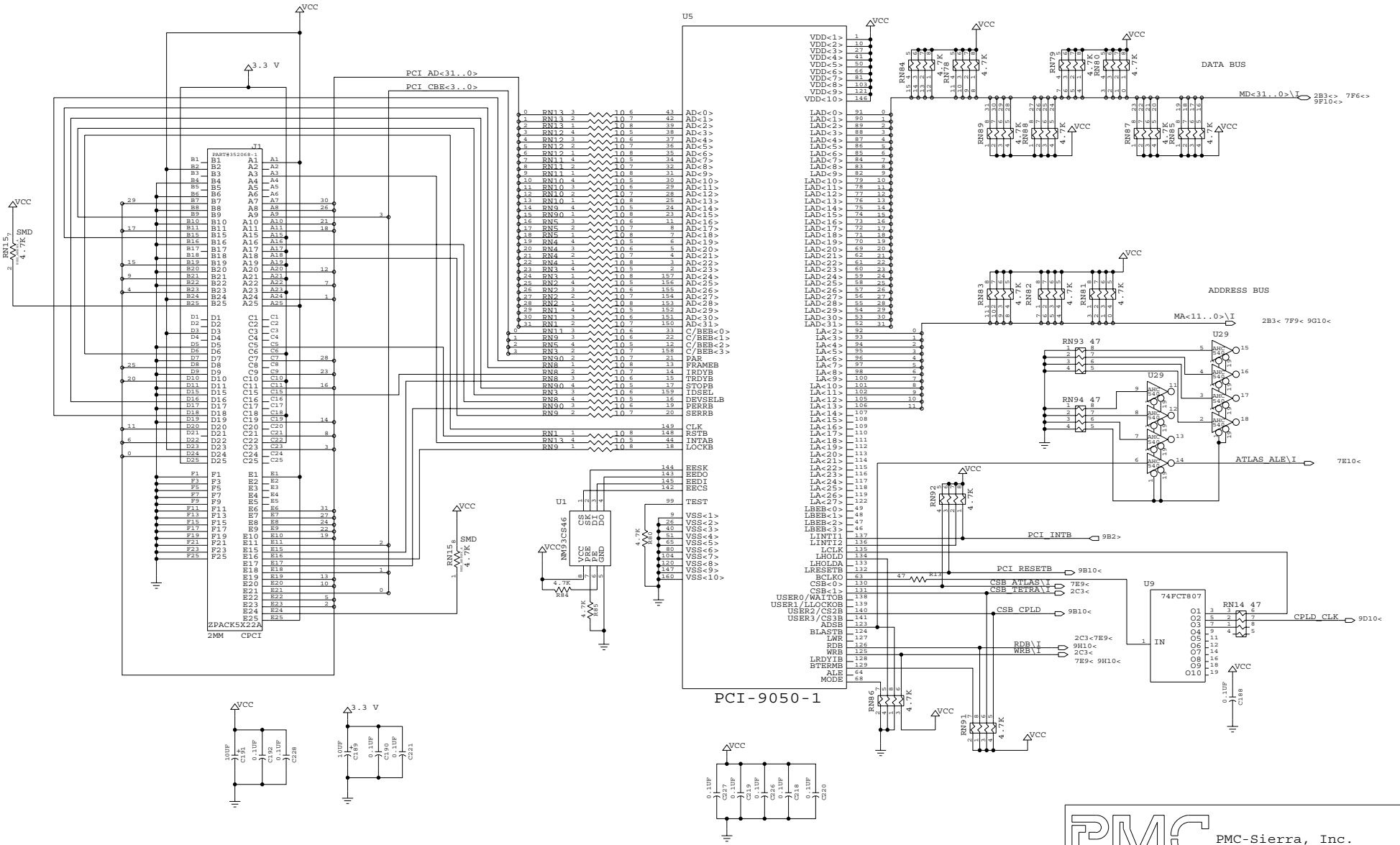
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD ATLAS MICRO INTERFACE AND POWER	REVISION NUMBER: 2
ENGINEER: RS	PAGE:7 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

CPCI CONNECTOR J1

5V SIGNALLING



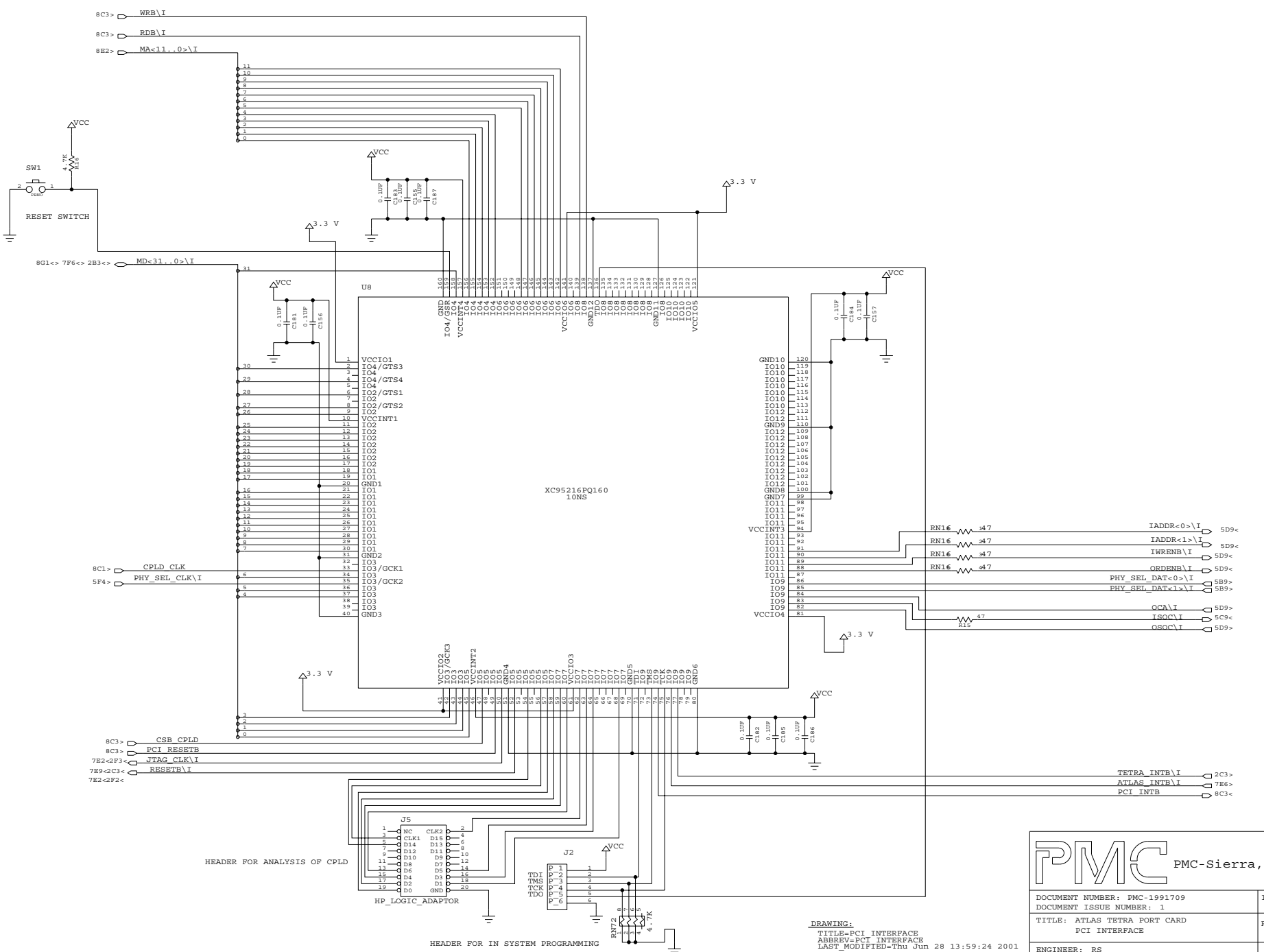
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD PCI INTERFACE	REVISION NUMBER: 2
ENGINEER: RS	PAGE:8 OF 12

DRAWING

TITLE=PCI_INTERFACE
ABBREV=PCI_INTERFACE
LAST_MODIFIED=Thu Jun 28 13:59:20 2001

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



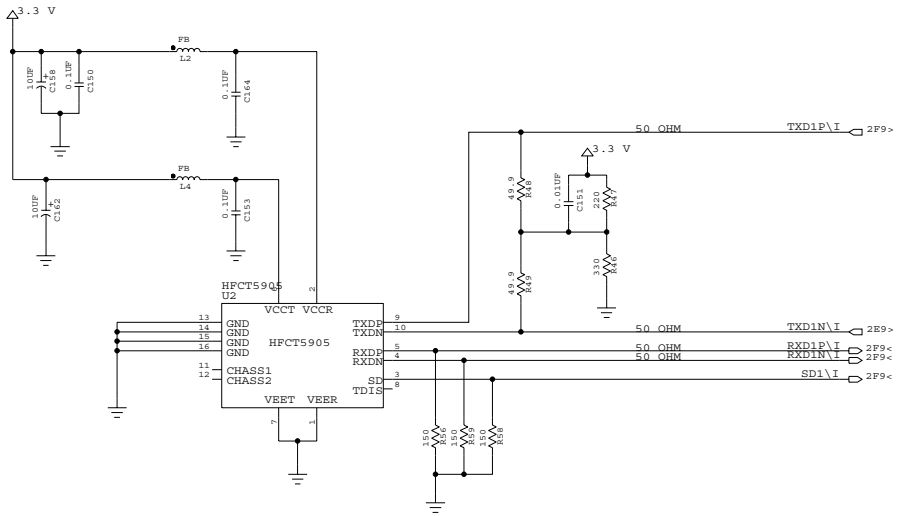
DRAWING:
TITLE=PCI_INTERFACE
ABBREV=PCI_INTERFACE
LAST_MODIFIED=Thu Jun 28 13:59:24 2001

PMC-Sierra, Inc.

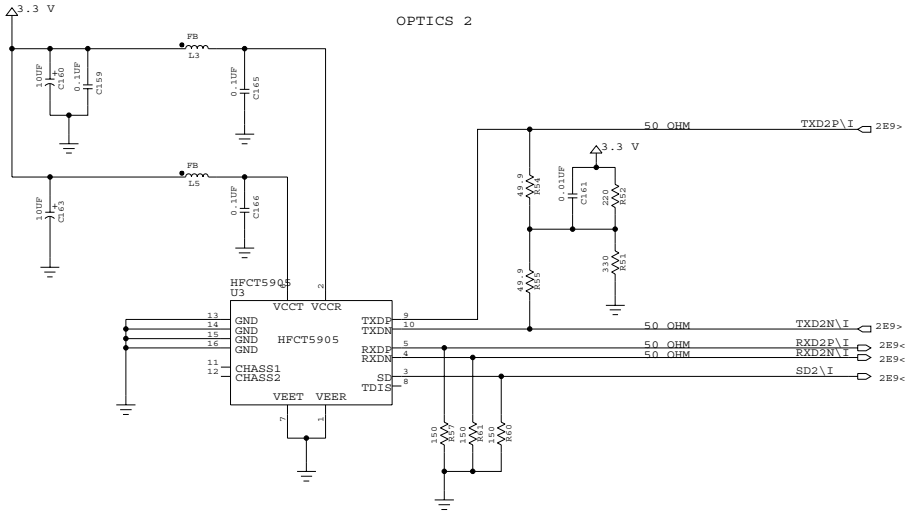
DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD PCI INTERFACE	REVISION NUMBER: 2
ENGINEER: RS	PAGE:9 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

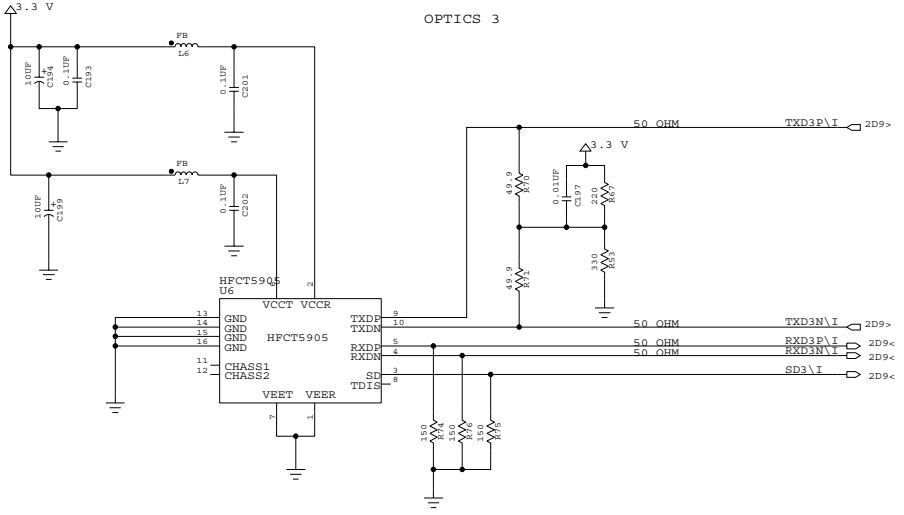
OPTICS 1



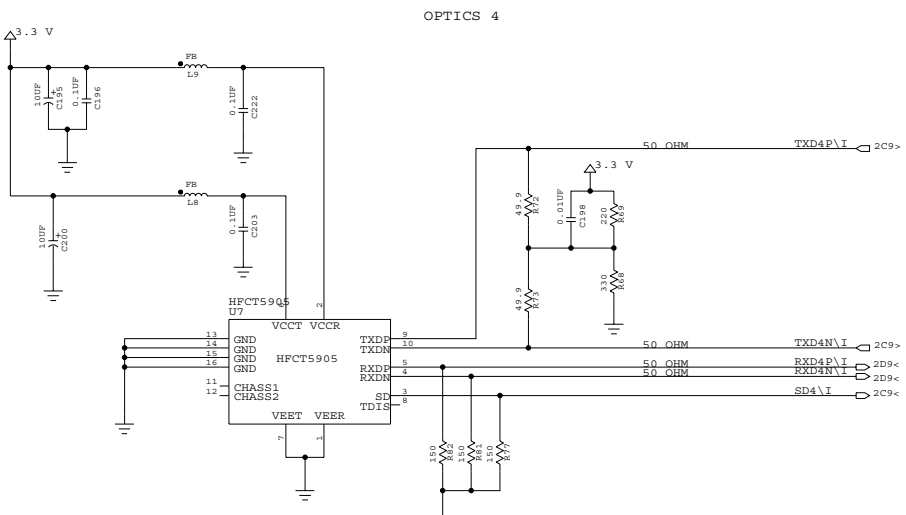
OPTICS 2



OPTICS 3



OPTICS 4



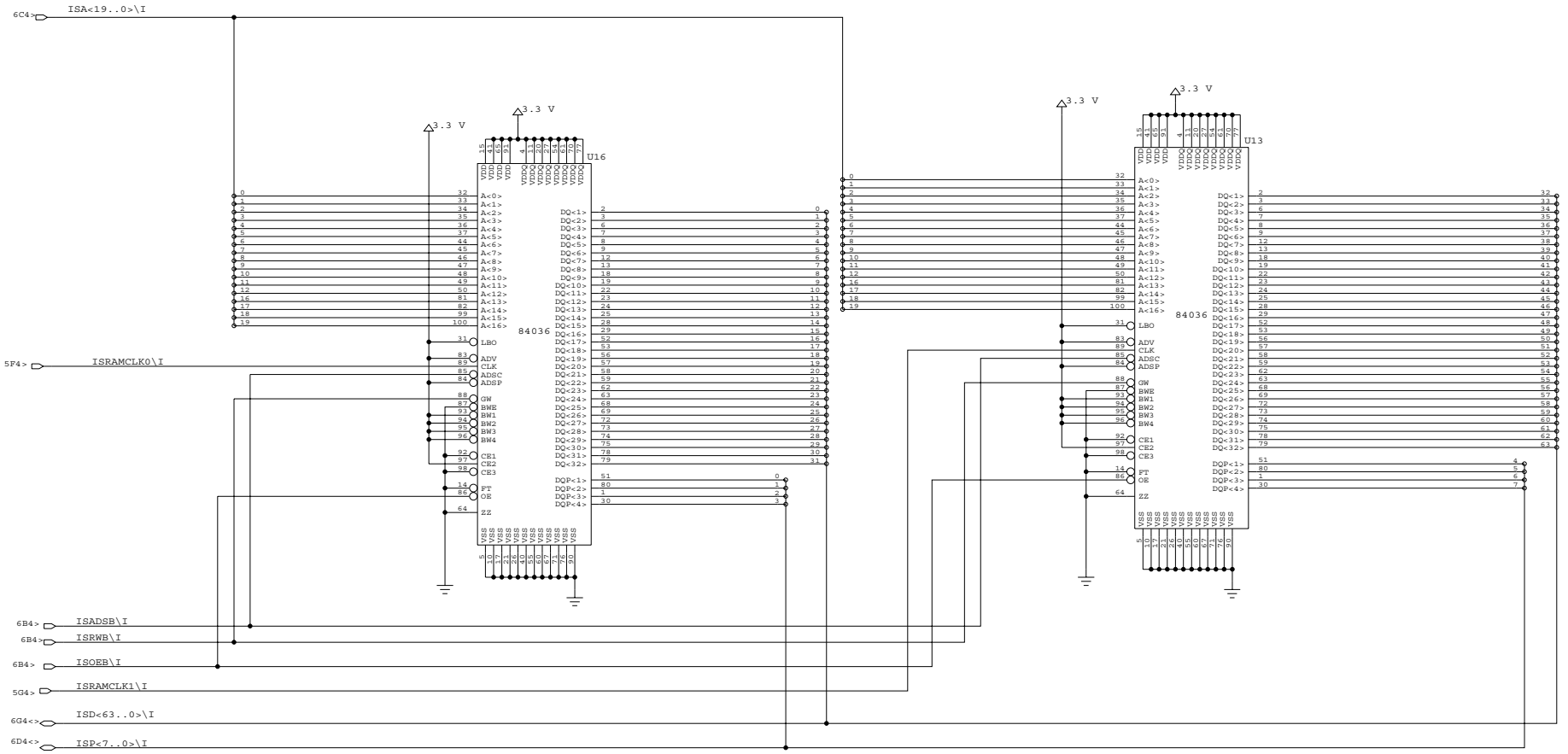
DRAWING

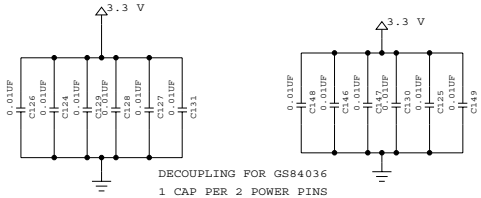
TITLE=OPTICS_BLOCK
ABBREV=OPTICS_BLOCK
LAST_MODIFIED=Thu Jun 28 13:59:01 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD OPTICS_BLOCK	REVISION NUMBER: 2
ENGINEER: RS	PAGE:10 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





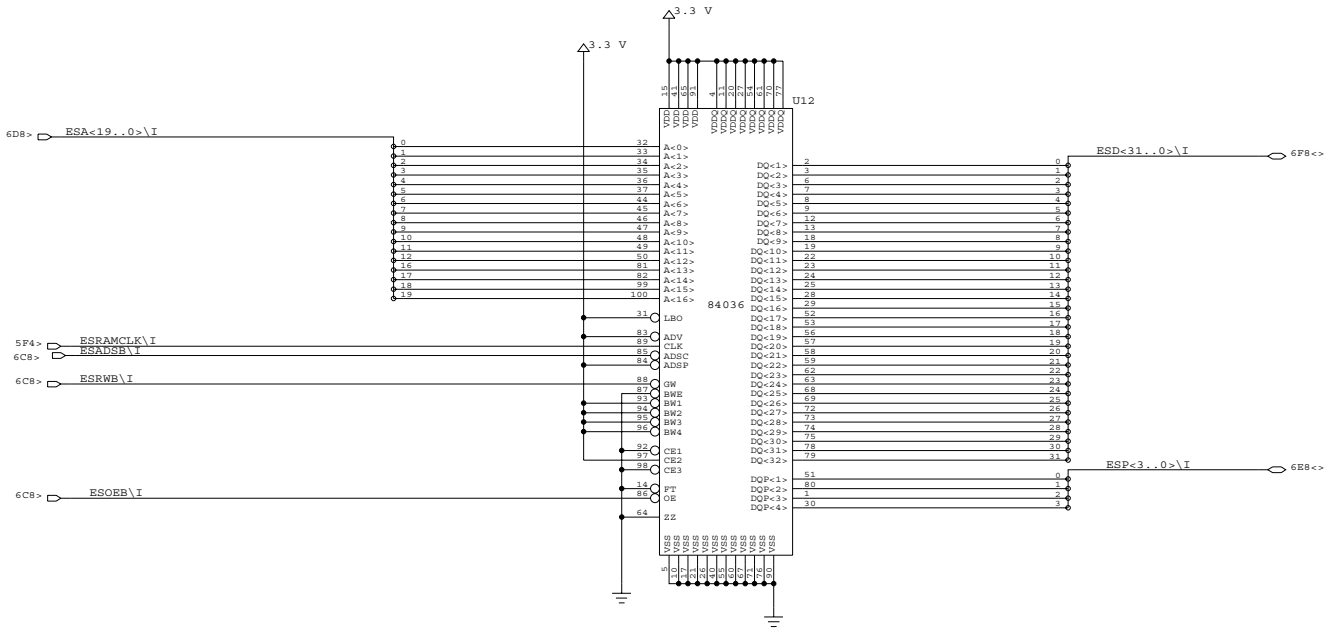
DECOUPLING FOR GS84036
1 CAP PER 2 POWER PINS

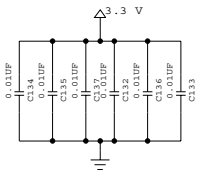
DRAWING:
TITLE=INGRESS_SRAM
ABBREV=INGRESS_SRAM
LAST_MODIFIED=Thu Jun 28 13:59:26 2001

PMC-Sierra, Inc.

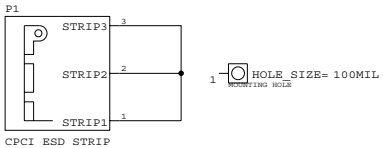
DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD INGRESS SRAM	REVISION NUMBER: 2
ENGINEER: RS	PAGE:11 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





DECOUPLING FOR GS84036
1 CAP PER 2 POWER PINS



CPCI ESD STRIP

DRAWING:
TITLE=EGRESS_SRAM
ABBREV=EGRESS_SRAM
LAST_MODIFIED=Thu Jun 28 13:58:59 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991709 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 01/06/26
TITLE: ATLAS TETRA PORT CARD EGRESS SRAM	REVISION NUMBER: 2
ENGINEER: RS	PAGE:12 OF 12

10 LAYOUT

11 BILL OF MATERIALS

Table 3 : Bill of Materials

NO.	Part Name	Part Number	Reference Descriptor	Qty
1	49FCT3807_SOIC-BASE	PERICOM PI49FCT807TS	"U10, U14"	2
2	74AHC540_SOIC-BASE-VCC=3_3V	SN74AHC540DW	U29	1
3	74FCT807_SOIC-BASE	IDT74FCT807BTSO	U9	1
4	74XXX541_SOIC-VCC=3_ 3V	PI74LPT541SA	U28	1
5	84036_TQFP-BASE	GSI GS84036T-166	"U12, U13, U16"	3
6	"CAPACITOR-0.01UF, 50V, X7R_805"	DIGI-KEY -- PCC103BNCT-ND	"C14, C109, C110, C112-C149, C151, C154, C161, C173, C175, C177-C179, C197, C198, C211, C215-C217, C223"	56
7	"CAPACITOR-0.1UF, 50V, X7R_805"	NEWARK -- 96F8740	"C2-C5, C7-C10, C107, C108, C111, C150, C152, C153, C155-C157, C159, C164-C171, C174, C176, C180-C188, C190, C192, C193, C196, C201-C207, C209, C210, C212-C214, C218-C222, C224, C226-C228"	62
8	"CAPACITOR-0.22UF, 50V, X7R_1210"	FAI 12105C224KATPS	"C1, C6, C172, C208"	4
9	"CAPACITOR-10UF, 16V, TANT TEH"	PCT3106CT-ND	"C11, C158, C160, C162, C163, C189, C191, C194, C195, C199, C200"	11
10	"CAPACITOR-4.7UF, 16V, TANT TEH"	DIGI-KEY -- PCT3475CT-ND	C225	1
11	"CAPACITOR-47UF, 6.3V, TANT TEH"	DIGI-KEY -- PCT1476CT-ND	"C12, C13"	2
12	CHIP_RES_NETWORK_8_SMD-4.7K	DIGI-KEY -- U7472CT-ND	RN6	1
13	HEADER3_100MIL-BASE	PZC36SAAN	J3	1
14	HEADER6_100MIL-BASE	PZC36SAAN	J2	1
15	HFCT5905	HFCT-5905E	"U2, U3, U6, U7"	4
16	HP_LOGIC_ADAPTOR-BASE	DIGI-KEY S2012-36-ND	J5	1
17	"INDUCTOR-FB, 50, FAIR RITE"	FAIR RITE – 2743019447	L2-L9	8
18	"LED-RED, PCB .29 RIGHT	DIGI-KEY -- L20361-ND	D1-D4	4

NO.	Part Name	Part Number	Reference Descriptor	Qty
	ANGLE"			
19	LT1121CST_SOT-3.3V	LT1121CST-3.3	U11	1
20	NM93CS46_DIP8-BASE	NM93CS46EN	U1	1
21	"OSC_CMOS_8PIN_DUAL-H CMOS, 19.44A"	MMD MB3020HH-19.440MH Z	Y1	1
22	"OSC_CMOS_8PIN_DUAL-H CMOS, 50.00A"	MMD MB3100HH-50.000MH Z	Y2	1
23	PBNO_RIGHT_ANGLE-BASE	DIGIKEY -- CKN4002-ND	SW1	1
24	PCI9050_PQFP-BASE	PCI9050-1	U5	1
25	"RESISTOR-1.0K, 5%, 805"		"R39, R64"	2
26	"RESISTOR-100, 5%, 805"		"R5, R6, R11, R12"	4
27	"RESISTOR-10K, 5%, 805"		"R40, R41, R43-R45"	5
28	"RESISTOR-150, 5%, 805"		"R56-R61, R74-R77, R81, R82"	12
29	"RESISTOR-158, 1%, 805"		"R1-R4, R7-R10"	8
30	"RESISTOR-180, 5%, 805"		R18-R21	4
31	"RESISTOR-2.2, 5%, 805"		R83	1
32	"RESISTOR-220, 5%, 805"		"R47, R52, R67, R69"	4
33	"RESISTOR-330, 5%, 805"		"R46, R51, R53, R68"	4
34	"RESISTOR-4.7, 5%, 805"		R14	1
35	"RESISTOR-4.7K, 5%, 805"		"R16, R42, R62, R63, R65, R79, R80, R84, R85"	9
36	"RESISTOR-47, 5%, 805"		"R13, R15, R37, R38, R66, R78"	6
37	"RESISTOR-49.9, 1%, 805"		"R48, R49, R54, R55, R70-R73"	8
38	RES_ARRAY_4_SMD-10		"RN1-RN5, RN8-RN13, RN73, RN90"	13
39	RES_ARRAY_4_SMD-4.7K		"RN15, RN72, RN78-RN89, RN91, RN92"	16
40	RES_ARRAY_4_SMD-47		"RN7, RN14, RN16, RN25-RN30, RN52-RN62, RN74-RN77, RN93, RN94"	26
41	SUNIATLAS_SBGA-BASE	PM7324	U15	1
42	SUNITETRA_SBGA-BASE	PM5351	U4	1
43	XC95216PQ160-10NS	XC95216-10PQ160C	U8	1
44	ZPACK5X22FH_ASCPCI_2 MM	352068-1	J1	1

12 VHDL CODE

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use work.all;

entity Atlas_Tetra is
port (
ma:               inout std_logic_vector(11 downto 0);--PCI Address Bus
md:               inout std_logic_vector(31 downto 0);--PCI Data Bus
wrb:              in std_logic;           --PCI Write Enable
rdb:              in std_logic;           --PCI Read Enable
reset_switch:     in std_logic;           --Reset Switch Input
cpld_clk:         in std_logic;           --33MHz clock
phy_sel_clk:      in std_logic;           --50MHz clock
csb_cpld:         in std_logic;           --CPLD Chip Select
osoc:             in std_logic;           --Ingress Output Start of Cell
atlas_intb,tetra_intb:  in std_logic;     --PMC device interrupts
phy_sel_dat:      in std_logic_vector (1 downto 0);--PHY select bits
oca:        in std_logic;           --Ingress Output Cell Available
pci_resetb:       out std_logic;          --PCI Interface Reset
jtag_clk:         out std_logic;          --JTAG Clock out
resetb:           out std_logic;          --Reset output
iaddr:            out std_logic_vector(1 downto 0);--Egress Input PHY
address
iwrenb:           out std_logic;          --Egress Input Write Enable
ordenb:           out std_logic;          --Ingress Output Read Enable
isoc:             out std_logic;          --Egress Input Start of Cell
HP_out:           out std_logic_vector(9 downto 0);
pci_intb:         out std_logic);         --PCI Interface interrupt

end Atlas_Tetra;

architecture vhdl of Atlas_Tetra is

signal pci_data:  std_logic_vector(31 downto 0);

begin

--PROCESS GLOBAL_RESET:
--This process will reset the ATLAS,TETRA,and PLX PCI Bridge

global_reset: process(phy_sel_clk,reset_switch)

begin

if phy_sel_clk'event and phy_sel_clk='1' then
      if reset_switch = '0' then
            resetb<='0';
            pci_resetb<='0';
      else
            resetb<='1';
            pci_resetb<='1';
```

```
      end if;
end if;


end process global_reset;

--PROCESS RW_DATA:
--This process will assign the 2 LSB's from the data bus to the
--IADDR(1..0) lines

rw_data: process(cpld_clk,pci_data(31 downto 0),wrb,csb_cpld)

begin

if cpld_clk='1' and cpld_clk'event then
      if csb_cpld='0' then

            if wrb='0' then
                  pci_data(31 downto 0)<=md(31 downto 0);
                  iaddr(1 downto 0)<=md(1 downto 0);
            end if;

      else
            md(31 downto 0)<=(others=>'Z');
      end if;

end if;

end process rw_data;


--IWRENB and ORDENB are switched with OCA

pci_intb<='Z';
jtag_clk<=cpld_clk;
HP_out(9)<= phy_sel_clk;
ordenb<=oca;
iwrenb<=oca;
HP_out(7)<= oca;

--ISOC is switched with OSOC

isoc<=osoc;
HP_out(8)<= osoc;
ma<=(others=>'Z');


end vhdl;
```

13 EEPROM CONTENTS

The following table presents the contents of the EEPROM used for the PLX device initialization. Values are in little endian format.

Table 5 : EEPROM Contents

EEPROM Offset (Hex)	Value (Hex)	PLX Register
0	9050	Device ID
2	10B5	Vendor ID
4	0660	Class Code
6	0000	ClassCode
8	7324	Subsystem ID
A	11F8	Subsystem Vendor ID
C	FFFF	Max Latency and Min Grant (not loadable)
E	00FF	Interrupt Pin
10	0FFF	MSW of Address Space 0 Range
12	C000	LSW of Address Space 0 Range
14	0FFF	MSW of Address Space 1 Range
16	F000	LSW of Address Space 1 Range
18	0FFF	MSW of Address Space 2 Range
1A	FC00	LSW of Address Space 2 Range
1C	0000	MSW of Address Space 3 Range
1E	0000	LSW of Address Space 3 Range
20	0FFF	MSW of Expansion Rom Range
22	0000	LSW of Expansion Rom Range
24	0000	MSW of Address Space 0 Remap
26	0001	LSW of Address Space 0 Remap
28	0000	MSW of Address Space 1 Remap
2A	4001	LSW of Address Space 1 Remap

EEPROM Offset (Hex)	Value (Hex)	PLX Register
2C	0001	MSW of Address Space 2 Remap
2E	0001	LSW of Address Space 2 Remap
30	0000	MSW of Address Space 3 Remap
32	0000	LSW of Address Space 3 Remap
34	0000	MSW of Expansion Rom Remap
36	0000	LSW of Expansion Rom Remap
38	5481	MSW of Space 0 Bus Descriptor
3A	4100	LSW of Space 0 Bus Descriptor
3C	2081	MSW of Space 1 Bus Descriptor
3E	C0C0	LSW of Space 1 Bus Descriptor
40	0090	MSW of Space 2 Bus Descriptor
42	A840	LSW of Space 2 Bus Descriptor
44	0000	MSW of Space 3 Bus Descriptor
46	0000	LSW of Space 3 Bus Descriptor
48	0000	MSW of Expansion Rom Bus Descriptor
4A	0000	LSW of Expansion Rom Bus Descriptor
4C	0000	MSW of CS0 Register
4E	2001	LSW of CS0 Register
50	0000	MSW of CS1 Register
52	4801	LSW of CS1 Register
54	0001	MSW of CS2 Register
56	0005	LSW of CS2 Register
58	0000	MSW of CS3 Register
5A	0000	LSW of CS3 Register
5C	0000	MSW of Interrupt Control/Status
5E	0000	LSW of Interrupt Control/Status
60	0002	MSW of EEPROM and Misc. Control
62	44D2	LSW of EEPROM and Misc. Control

EEPROM Offset (Hex)	Value (Hex)	PLX Register
64 – 7F	FFFF	Unused

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Tel: (604) 415-4533
Fax: (604) 415-6206
Web Site: http://www.pmc-sierra.com

PMC-1991709 (R1) ref PMC-1971240 (R7) Issue date: September 2001