PM7380

FREEDM-32P672

FREEDM-32P672 WITH DS3 LIU

REFERENCE DESIGN

PRELIMINARY

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1 INTRODUCTION

The FREEDM-32P672 WITH DS3 LIU Reference Design entails the interfacing of PM7380 FREEDM-32P672 and TDK78P2241 DS3 LIU via PM8315 TEMUX. This document provides an application example for FREEDM-32P672 encompassing the reception and transmission of DS3 data, multiplexing 28 DS1 streams, and finally downstreaming HDLC data to a PCI bus.

1.1 Purpose

This design provide interfacing details to assist designers of routers and frame relay switches in building DS3 applications using PMC-Sierra's FREEDM-32P672 and TEMUX.

1.2 Scope

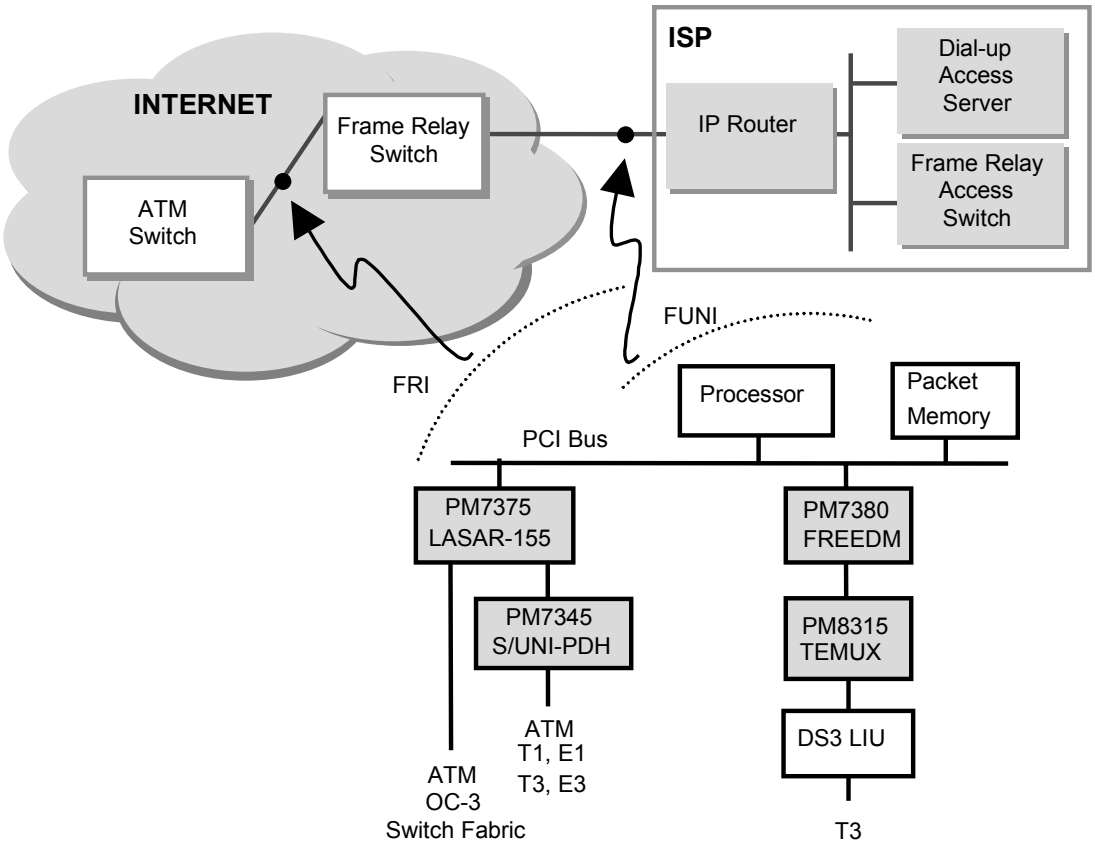
This document describes interfacing of DS3 data stream to a 32-bit PCI bus using a DS3 LIU, PMC TEMUX, PMC FREEDM-32P672, and PCI bridges. Functional blocks of this design are separately explained and implementation details are provided.

1.3 Application

The FREEDM-32P672 and DS3 LIU application lies within the realms of Frame relay networking. Frame relay is a multiplexed data networking technology – supporting connectivity between user equipment and the public frame relay network. The frame relay protocol supports data transmission over a connection-oriented path and enables the transmission of variable-length data units over an assigned virtual connection.

Frame relay technology can be used in LAN interconnection, Internet access and Internet backbones using link speeds ranging from 9600 baud to the DS3 rate. Figure 1 illustrates a typical implementation of a frame relay interface (FRI) and a frame relay user to network interface (FUNI) using T1, E1 and DS3 rates.

Figure 1 - Frame Relay Inter-networking Overview



Equipment such as routers, T1 multiplexers, nodal processors, packet switches, front end processors, and packet assemblers/dissemblers need to support the frame relay interface in order for them to be connected to a private or a public frame relay network.

In this application, the DS3 LIU enables interfacing to a T3 line. The FREEDM-32P672 provides the HDLC processing which is used in Frame Relay.

2 FEATURES

- Interfaces to a DS3 link carrying channelized or unchannelized data
- Able to support up to 672 bi-directional HDLC channels assigned to a maximum of 28/21 channelized T1/E1 links respectively
- Interfaces to a PCI bus (33MHz) which as a host processor and packet memory
- Control and monitoring of the TEMUX and FREEDM-32P672 devices is done by the host microprocessor via the PCI bridges and PCI interface
- JTAG access to the TEMUX and FREEDM-32P672 is achieved via the PCI interface
- Front panel LEDs for power and other status reports

3 BLOCK DESCRIPTION

3.1 Reference Design

The FREEDM-32P672 with DS3 LIU reference design card demonstrates an application of interfacing between T1/E1 and DS3 data streams, which is commonly found in Frame Relay to ATM internetworking or PPP processing applications. Frame relay packets arrive and depart at the DS3 LIU. Multiplexing/Demultiplexing of DS3 ⇔ DS1 data streams occurs in the TEMUX. The FREEDM-32P672 performs HDLC processing and interfacing to the PCI bus, which has the host processor and packet memory.

Figure 2 illustrates the reference design and its sub-blocks, which are explained in the following sections.

Figure 2 - FREEDM-32P672 with DS3 LIU Block Diagram

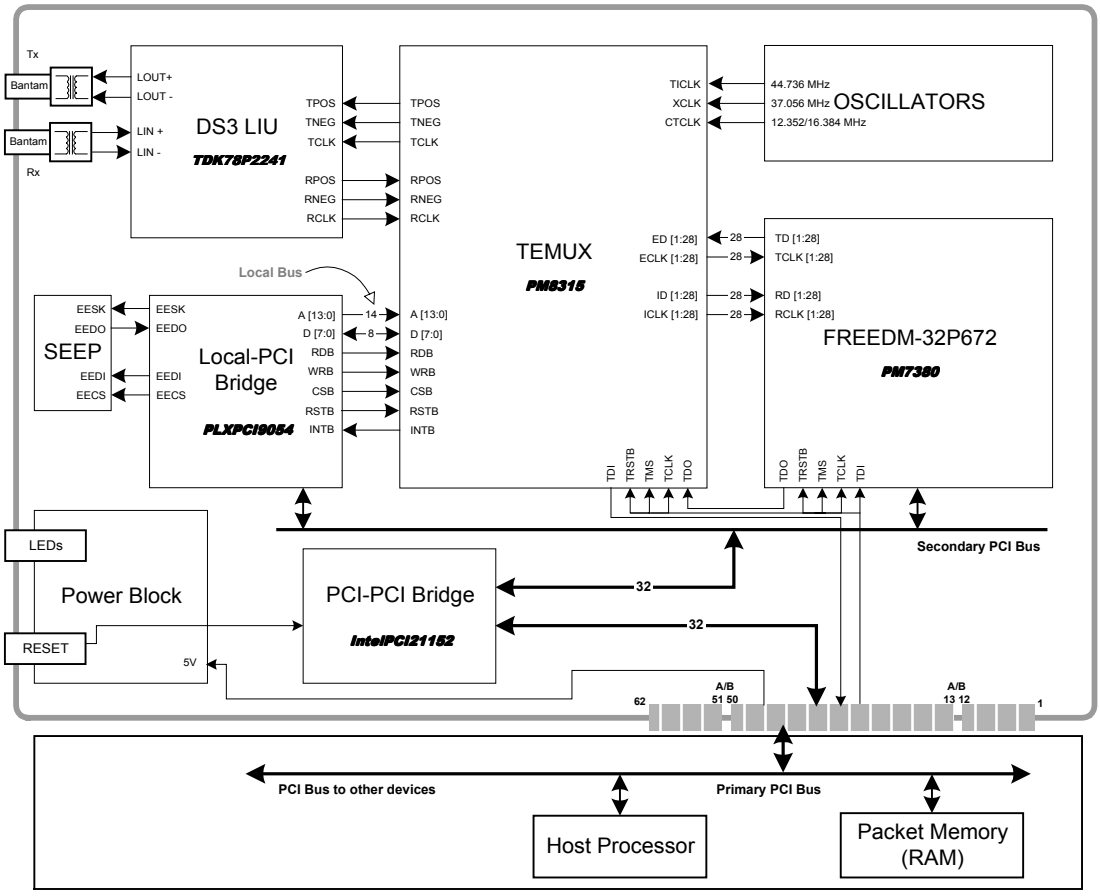
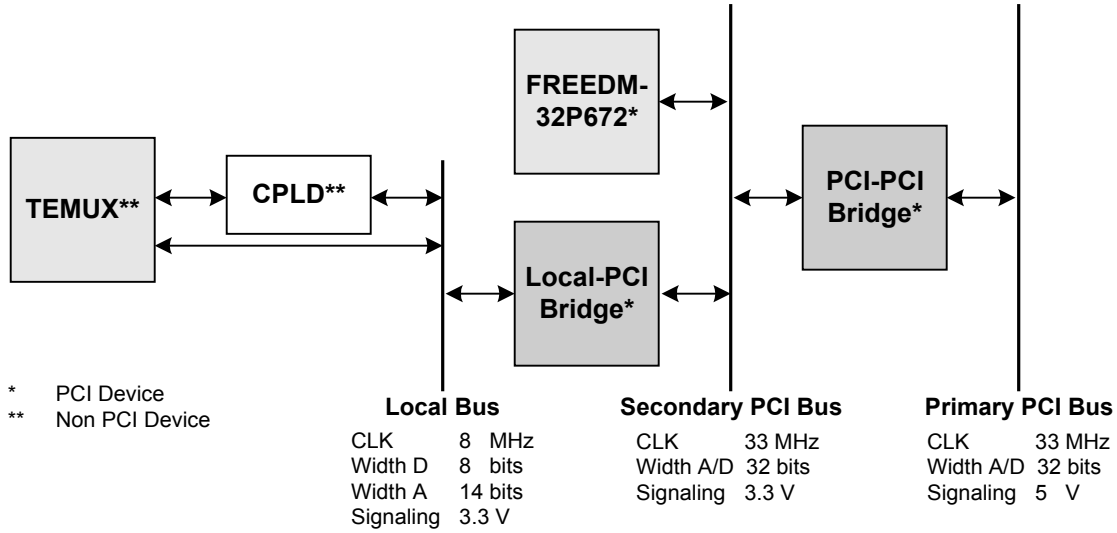


Figure 3 shows the bus architecture in the reference design. The PCI-PCI Bridge is necessary to satisfy PCI bus specifications, refer to document [7].

Figure 3 - Reference Design Bus Architecture



3.2 DS3 LIU

Interfacing to a T3 line is accomplished through the use of a TDK 78P2241 E3/DS3/STS-1 line interface transceiver IC, transformers, and several passive components. The line interface unit operates a DS3 signal at 44.736 Mbs.

The receiver recovers the clock and positive and negative data from a B3ZS/HDB3 encoded AMI signal. The transmitter generates an AMI pulse, which can drive a 75 Ω coaxial cable.

The /ENDEC pin must be set high to disable NRZ logic data generation. The TPOS/RPOS and TNEG/RNEG send and receive Positive and Negative AMI signal respectively. There is an onboard equalizer for combating intersymbol interference. There is also an internal PLL for locking on to the frequency of incoming data eliminating the need for high precision external clock.

Table 1 indicates the main parameter configurations for the desired behavior of the TDK78P2241. Refer to the datasheet [15] for further information.

The physical interface to the DS3 line will be via 75 Ω Bantam connectors.

Table 1 - DS3 LIU Configuration

Pin/Component	RFO	/E3	MON	ICKP	/ENDEC	TXEN
Value	5.23 kΩ	High	Low	Low	High	High
Pin/Component	/LPBK	RTT	RTR	CLF	LBO	
Value	High	301 Ω	75 Ω	0.047 µF	Cable < 225 ft High	Cable ≥ 225 ft Low

3.3 Local-PCI Bridge

The Local to PCI Bridge used is PLX Technology's PCI9054 PCI Bus Master I/O Accelerator (PCI 2.2 compliant). This device interfaces the TEMUX to the Secondary PCI bus. Along with the PCI-to-PCI bridge, the PCI9054 enables the TEMUX to be accessible from the host processor. The PCI9054 provides master and target mode interfaces, of which the latter is used in this design, i.e. the PCI9054 is a target on the (Secondary) PCI bus and a master on the Local bus. The PCI9054 supports 32-bit wide, 33MHz PCI bus interfacing. The Local bus interface of the PCI9054 is generic and very flexible, supporting 8, 16, and 32-bit data transfers operating in multiplexed or non-multiplexed modes, with big/little Endian conversion capabilities at a clock rate asynchronous to the PCI bus.

The device operates in 3 different modes, M, C, and J, of which, C is used in this design. Mode C provides a non-multiplexed interface on the Local side. In mode C, Direct Slave Transfer facilitates PCI access to the Local space. Read and

write operations occur in terms of single transfer accesses to the Local space. Therefore, a mapping must be configured between the PCI space and the Local space.

Direct Slave PCI-to-Local address mapping could be configured in any of the 3 distinct user-definable address spaces that are provided by the PCI9054. In this design, only one partition is required for the TEMUX.

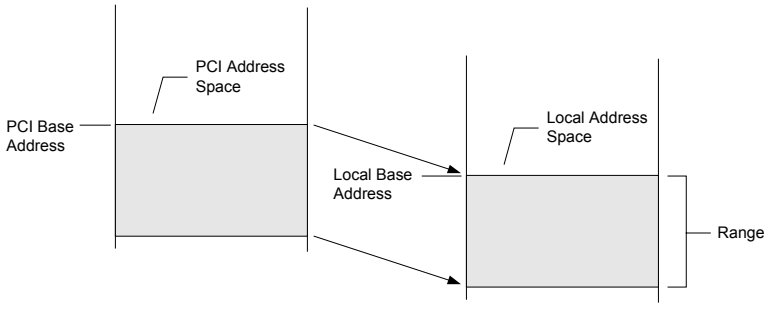
A 14-bit address and an 8-bit data bus are required by the TEMUX. Hence, the Local data bus is configured as 8-bits, non-multiplexed, big Endian, non-burst, and non-prefetchable. Configuration of bus width is done by hardware using the LBEB<3.0> or by software in the Bus Region Descriptors for PCI-to-Local Accesses register. The Local address spaces are allocated during initialization as in Table 2. This Local mapping allows address translation from the PCI Address Space to the Local Address Space.

Table 2 - PCI 9054 Local Address Space Allocation

Address Space	Function
0	TEMUX internal registers
1	None
ROM	None

Configuration is achieved via a serial EEPROM data download after power up and/or reset. After a PCI reset, the loaded software maps the Local Address space into the PCI Address space by programming the Local Address Range and PCI Base Address registers (since Address Space 0 is used, the registers are LAS0RR and LAS0BA). See Figure 4.

Figure 4 - Direct Slave Address Space Mapping



The PCI9054 also has an internal wait state(s) generator for timing of the address spaces. The Local bus is clocked at 8MHz by an on board oscillator.

A CPLD houses some glue logic, which is required to interface the PCI9054 to the TEMUX.

Refer to the PCI9054 datasheet [9] for more information.

3.4 Local-PCI SEEP

The NM93CS56L Serial EEPROM (2Kbit deep) from National Semiconductor is used to store configuration information for the PCI9054 bridge. PLX Technology recommends this specific SEEP; moreover it is suitable with the PCI9054 because it supports sequential read operations. The SEEP can be programmed over the PCI bus or Local bus, or by a Data I/O programmer, (in the latter case, the SEEP is socketed into the board.) In this design, the Data I/O programmer method is assumed. (The SEEP can also be programmed using the VPD function – refer to the PCI9054 datasheet [9] for details.)

The PCI9054 detects the SEEP and reads the first LWORD. Upon detection of programmed data, the configuration data is loaded into the PCI9054.

Refer to the PCI9054 datasheet [9] and the NM93CS56L datasheet [1] for detailed information on the format of the configuration data stored in the SEEP.

3.5 TEMUX

The TEMUX is a feature rich monolithic device, which integrates 28 T1 framers or 21 E1 framers and a full-featured M13 multiplexer with a DS3 framer. It is software configurable via access to its configuration registers. A generic microprocessor can be used with the address lines A [13:1] and data lines D [7:0]. However, in this reference design, the configuration registers are accessed via the PCI bus and brides, hence configured by the host processor.

The DS3 LIU interfaces to the DS3 framer sub block in the TEMUX, which asynchronously multiplexes/demultiplexes 28 T1/21 E1 streams to/from a serial DS3 (44.736 Mbs) data stream. The framer in each direction has a positive (TPOS/RPOS) and a negative (TNEG/RNEG) signal and its own clock (TCLK/RCLK). Set the OPMODE[1:0] bits in the Global Configuration register to configure the TEMUX as a DS3 framer.

Although the device can support SBI bus interface, it is used here with only one FREEDM-32P672 and it is serially connected. Each of the ingress (ID [1:28]) and egress (ED [1:28]) data streams has its own clock signal (ICLK [1:28]/ECLK [1:28]). In the case of Ingress direction, frame pulse signals are not used.

In the Egress direction, the TEMUX is operated in the Clock Master: NxChannel mode; modes are selected via the EMODE[2:0] bits in the T1/E1 Egress Serial Interface Mode Select register. For the Ingress direction the TEMUX is operated in the Clock Master: Full T1/E1 mode, which is selected via the IMODE[1:0] bits and INXCHAN[1:0] bits in the T1/E1 Ingress Serial Interface Mode Select register.

The TEMUX requires a Transmit Input Clock (TICLK = 44.736MHz) for the transmit direction and a Crystal Clock (XCLK = 37.056MHz) for timing many of the T1/E1 sub-blocks. Moreover, it needs a Common Transmit Clock (CTCLK = 12.352MHz (T1) 16.384MHz (E1)) for operation in Master modes.

The receiving/sending DS3 framers support B3ZS encoded signal, detect/insert RED alarm, AIS and idle signal, and FERF. The framers are off-line framers supporting OOF and COFA events. The C-bit parity FEAC channel and the path maintenance data link are also supported. The framers detect/insert parity or path parity errors, F-bit and M-bit errors, invalid X-bits, P-bits, and C-bits, LCV, or EXZ.

In the receiving framer, detection algorithms operate correctly in the presence of a 10^{-3} bit error rate. The transmitting framer can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF, RED, or AIS, and FEBE upon detection of C-bit parity error. The outgoing framer may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers that are accessible by a generic microprocessor bus.

Both T1 and E1 framing functionality are provided by the TEMUX. There are 28 T1 and 21 E1 framers. The T1 framers support both SF and ESF formats. Framers can be disabled to allow reception of unframed data. The E1 framers support FAS, NFAS, and CRC and CAS multiframe frame alignment and their respective framing bit errors. The framers support International/National bit extraction, distant alarms. Generate interrupts to signal a change in monitor bits or events, and on the basis of frames and multiframe.

After reset, The TEMUX defaults to 28 T1 framers multiplexed into the M13 multiplexer using the DS3 M23 multiplex format. However some configuration is necessary for proper operation.

The framers provide jitter attenuator for both directions using internal FIFOs and a jitter attenuated clock and reference clock XCLK (37.056MHz for T1 and 49.152MHz for E1).

Refer to the TEMUX datasheet [11] for further details.

3.6 FREEDM-32P672

The Frame Engine and Datalink Manager (FREEDM) is a family of advanced data link layer processors that is suitable for applications such as PPP interfaces for routers, TDM switches, Frame Relay interfaces for ATM or Frame Relay switches and multiplexers, internet access equipment, and Packet-based DSLAM equipment.

FREEDM-32P672 implements HDLC frame processing and PCI Bus memory management functions for a maximum of 672 bi-directional channels. The FREEDM-32P672 may be configured to support 32 physical links for HMVIP, channelized T1/J1/E1, or unchannelized traffic.

For channelized T1/J1/E1 links, the FREEDM-32P672 allows up to 672 bi-directional HDLC channels to be assigned to individual time-slots within a maximum of 32 independently timed T1, J1, or E1 links. Time-slots are determined using the gapped clock method. The channel assignment supports up to a maximum of 24 concatenated time-slots for T1/J1 and 31 for E1 link.

For unchannelized links, it processes up to 32 bi-directional HDLC channels within 32 independently timed links. The aggregate bandwidth of the unchannelized links must no exceed 65.536 Mbs in either direction.

Mixing of up to 32 channelized T1/J1/E1, unchannelized and H-MVIP links is supported; the number of channels in each direction is limited to 672 and the aggregate instantaneous clock rate over all 32 links is limited to 64MHz.

In the receive direction, the FREEDM-32P672 performs channel assignment and packet extraction and validation. For each HDLC channel, the receive HDLC processor performs flag sequence detection, bit de-stuffing, and CRC-CCITT or CRC-32 verification. The resulting packet data is placed into the internal 32 Kbytes partial packet buffer RAM. The partial packet buffer acts as a logical FIFO for each of the assigned channels. Partial packets are DMA'd out of the RAM, across the PCI bus and into the host packet memory.

In the transmit direction, the PCI Host provides packets to transmit using a transmit ready queue. For each HDLC channel, it DMA's partial packets across the PCI bus and into the partial packet buffer. The partial packets are read out of the packet buffer and a frame check sequence is optionally calculated and inserted at the end of each packet. The HDLC processor performs Flag insertion, bit stuffing, and CRC (CRC-32 or CRC-CCITT).

DMA controllers are provided for both directions. They are responsible for transferring data into the host memory from the partial packet buffer and vice-

versa. The capacity of partial packet buffer is 32 Kbytes, which is divided into 16 byte blocks.

On the system side, the FREEDM-32P672 provides a 66MHz, 32-bit PCI 2.1 compliant bus interface.

All transfers that occur between the FREEDM-32P672 and the host are done through data structures (ex. Receive Packet Descriptors (RPDs), reference queues) that are resident in the host memory.

Since in this design the FREEDM-32P672 is interfaced with the TEMUX, only 28 links out of its 32 are used.

Refer to the FREEDM-32P672 datasheet [12] for further details.

3.7 PCI-PCI Bridge

Intel provides the PCI to PCI Bridge, PCI21152. It is fully compliant with PCI Local Bus Specification 2.1 and PCI-PCI Bridge Specification 1.1. It is a transparent device; i.e. it requires no special driver software to bridge one PCI bus to another. However, it does require initialization code to set up its configuration space and allocate memory space on the Secondary bus.

The PCI21152 operates at 33MHz and has a standard PCI interface on the Primary bus side. On the Secondary bus side, it supports 4 PCI devices. It is also capable of arbitrating 4 devices on the Secondary side. It is also 3.3V and 5V tolerant.

For configuration of the device, there are two types of transactions. Type 0 transactions are when the intended target resides on the same PCI bus as the initiator; Type 1 transactions are issued when the intended target resides on another PCI bus. The PCI21152 configuration space (Table 3) is accessed only by the Primary interface via a Type 0 configuration transaction. Only the PCI-PCI bridge responds to Type 1 transactions, which then are translated into Type 0 transactions for an intended device on the Secondary bus. In Type 1 transactions, a device number is specified to aid the PCI21152 in asserting a unique IDSEL signal on the Secondary bus.

The Type 1 configuration format uses a 5-bit field at bits <15:11> in the address as a device number. A device number in Type 1 format is translated by the PCI21152 into an IDSEL line for Type 0 transactions on the target interface. It uses s_ad<31..16> as secondary IDSEL lines. There is a certain mapping that the device uses for translation of a device number to a s_ad pins. In this design, the FREEDM-32P672 is device #4 and the PCI9054 is device #8. Refer to the

datasheet [4] and specifications [7] and [8] for more details, such as interrupt binding for expansion cards.

Table 3 - PCI 21152 Configuration Space (main registers)

31	16	15	00	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
…				
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
…				
Bridge Control		Interrupt Pin	Reserved	3Ch
Arbiter Control		Diagnostic Control	Chip Control	40h
…				
Reserved	p_serr_l Status	Secondary Clock Control		68h
…				

Arbitration for the Primary bus is done externally; i.e. by the host. The PCI21152 must arbitrate for the devices on the Secondary bus. Arbitration is performed for use of the Secondary bus when forwarding downstream (Secondary to Primary) transactions. The Secondary bus arbiter is internal and is enabled by having the s_cfn_i pin pulled low. In this design, only two devices will be arbitrated, namely the FREEDM-32P672 and the PCI9054 Local-PCI bridge. The FREEDM-32P672 needs to have both master and target capability, but the PCI9054 needs only to be a target. FREEDM-32P672 should be configured as a high priority group member.

There is a Primary interface reset signal, p_rst_i, which is an input signal from the Primary bus. When a reset signal is received from the Primary bus, it is forwarded to all the devices residing on the Secondary bus via the output signal on the Secondary side, s_rst_i.

Data throughput analysis of the FREEDM-32P672 operating in conjunction with the PCI-PCI Bridge has not been conducted. Detailed software configuration of the PCI21152 is highly dependent on the host and is beyond the scope of this reference design. Rather, detailed hardware implementation is the intended goal of this document.

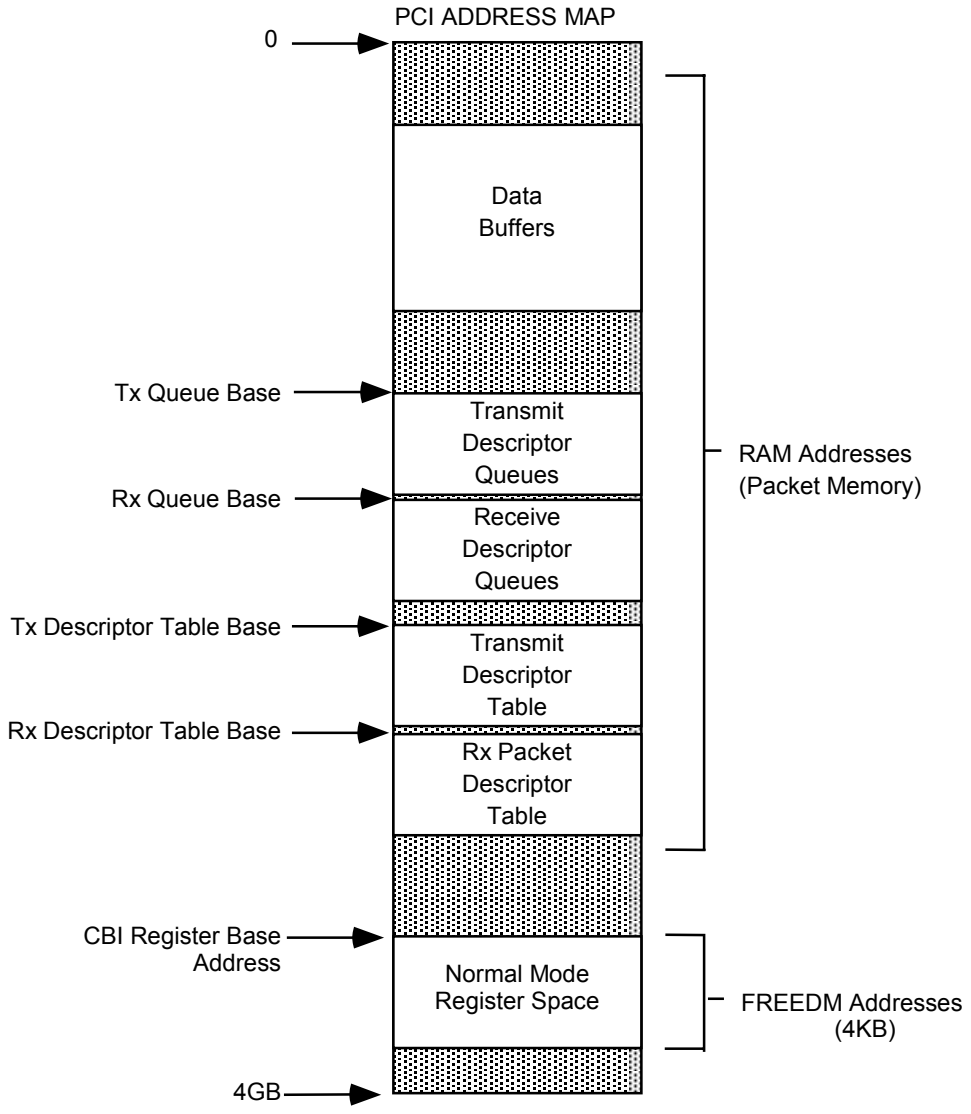
Please refer to the PCI21152 datasheet [4] for more details on configuring the Configuration register in Table 3, PCI Bus operations, addressing, arbitration, power management, ordering rules, and parity errors handling.

3.8 PCI Bus Interface to the Host Processor and Packet Memory

The FREEDM-32P672 is configured, controlled and monitored across the PCI bus interface by a host processor and packet memory (RAM). The GPIC sub-block provides a 32-bit Master and Target interface core that contains all the required control functions for full PCI Bus 2.1 Compliance. The GPIC supports up to 66MHz and is also backward compatible with 33MHz and will operate at 33MHz when connected to a 33MHz PCI bus. During a bus transaction, the FREEDM-32P672 device may act as the bus master in accessing the packet memory, or the host processor may act as the bus master in accessing the FREEDM-32P672 registers.

The data structures shown in Figure 5 are required to interface one FREEDM-32P672 to the PCI bus. In this figure, PCI addresses are 32-bit physical addresses, which can be observed at the address pins of the PCI bus interface.

Figure 5 - PCI Address Map



When multiple FREEDM-32P672's are attached to the bus each FREEDM-32P672 must have a unique set of the following data structures: Transmit Queue Space, Receive Queue Space, Transmit Descriptor Table, Receive Descriptor Table, and CBI Registers Space.

The data structures within packet memory are accessed by software running on the host processor or by the FREEDM-32P672. The software specifies the

location of these data structures by writing base addresses into the appropriate FREEDM-32P672 registers, before activating the FREEDM-32P672.

The data Buffers are filled with the data received by the FREEDM-32P672, or contain transmit data, which is read by the FREEDM-32P672. The descriptor tables and the queues are required to manage these buffers.

To manage and control the FREEDM-32P672 device, software running on the host processor accesses the Normal Mode Register space. The CBI Registers Base Address is used as the base address for registers that control the PCI interface. These registers are located in the FREEDM-32P672 and are accessed by the CBI bus interface.

The PCI Configuration Space does not reside in the PCI address map, but it is a requirement for all PCI devices. The Configuration Space is a block of 256 contiguous bytes that reside in the PCI device (the FREEDM-32P672 in this case), and is accessed by the host processor in a PCI bus Configuration Read (or Write) transaction, rather than a Memory Read (or Write) transaction. Access to this configuration space is system specific and a thorough description of it can be found in the PCI specification [7]. A description of the software can be found in the application note [14].

Note: Special care must be taken when configuring the software between the FREEDM-32P672 and the PCI21152.

3.9 Timing Block

There are four oscillator sources on the board.

The TEMUX requires a Transmit Input Clock (TICLK) of 44.736MHz for the transmit direction and a Crystal Clock (XCLK) of 37.056MHz (T1) or 49.152MHz (E1) for timing many of the T1/E1 sub-blocks. It also requires a Common Transmit Clock (CTCLK) of 12.352/16.384MHz (T1/E1) for operation in Master modes.

To support both T1 and E1, the corresponding oscillators (above) can be easily interchanged using socket-packaged oscillators.

An 8MHz clock is also need for the Local bus, and it is used by the CPLD and PCI9054.

3.10 Power Block

The majority of devices on the board will operate of the +3.3V rail, however, the TEMUX and FREEDM-32P672 devices require +3.3V for the I/O pads and +2.5V for the core logic. In this design, a Universal PCI back plane connector will provide a 5V supply, which is regulated to provide 2.5V and 3.3V power supplies. If designed otherwise, the 3.3V can also be used instead of the 5V to supply the 3.3V devices and regulate for the 2.5V source. The DS3 LIU, PCI-PCI Bridge, Local-PCI Bridge, SEEP, CPLD, logic gates, buffers, and oscillators will operate at +3.3V.

3.11 Front Panel

Front panel LEDs will be used to indicate status of the power supplies.

Reset circuitry is implemented using a voltage monitor and manual reset device. A reset command propagates throughout the whole board on either of the following conditions. The first condition is if a manual reset was performed; i.e. reset button was activated (low). The second condition is if the monitored voltage falls beyond a certain threshold of its intended value. The latter condition protects against data corruption caused by power supply instability.

Software reset control is also facilitated in the design using a standard PCI reset signal which is received through the PCI connector and passed on to all devices via the PCI-PCI Bridge. Moreover, individual devices can also be reset under software control, i.e. using internal control register.

4 DESIGN ISSUES

The following sections describe detailed design considerations of the reference design.

4.1 DS3 LIU

4.1.1 TDK78P2241 3.3V versus 5V

A new feature has been added in the 3.3V device, the LIN± are internally forced low when /LOS indicates low. This is to guard against the received signal from being lower than a certain threshold, which would otherwise cause signal corruption.

According to characterization results of the 3.3V device, the micro strips for the LOUT± and LIN± pins should be less than 12 inches (approximately) to avoid attributed signal degradation.

4.1.2 Power Supply

De-coupling capacitors are used on the power to reduce the effects of noise from the power supply.

4.1.3 Transformers

A 1:1 transformer is coupled to the receiver and a 2:1 transformer is coupled to the transmitter.

4.1.4 Termination Resistors

A 75 Ω resistor must terminate the AMI incoming line. A 301 Ω resistor must terminate the AMI outgoing line.

4.2 TEMUX

4.2.1 Power Supply

The TEMUX is operated at 2.5V for the core logic and at 3.3V for the I/O pads. The 5V is used for generating the 2.5V and 3.3V supplies. The 3.3V supply should be powered up before and powered down after the 2.5V.

4.2.2 De-coupling

Capacitors of 0.01 μF are used to achieve de-coupling of power pins on the device.

4.3 FREEDM-32P672

4.3.1 Power Supply

The FREEDM-32P672 is operated at 2.5V for the core logic and at 3.3V for the I/O pads. The 5V is used for generating the 2.5V and 3.3V supplies. The 3.3V supply should be powered up before and powered down after the 2.5V.

4.3.2 Timing

The FREEDM-32P672 core logic can be operated at clock of 25 to 40MHz, via the SYSCLK pin. In this design a buffered version of the PCI bus clock is used and it has a value of 33MHz.

4.3.3 De-coupling

Capacitors of 0.01 μF are used to achieve de-coupling of power pins on the device.

4.4 PCI 9054

4.4.1 Power Supply

The PCI9054 core logic is operated at 3.3V.

4.4.2 CPLD

A CPLD is used to house some glue logic, which is required to interface the PCI9054 to the TEMUX. The PCI9054 is a master and the TEMUX is a slave. The CPLD is implemented to meet the TEMUX micro interface timing requirements (refer to the datasheet [11] for more timing details). Read and Write timing diagrams are provided to illustrate the implementation of the CPLD. The clock provided to the CPLD is 8MHz, i.e. with a 125ns period. Please refer to the VHDL code segment in Appendix C: VHDL Code for Glue Logic. Assigning pin numbers to signals can easily be specified in VHDL code, however, this is not provided in the code segment given.

Figure 6 and Figure 7 show the timing requirements of the TEMUX for Read and Write operation, respectively.

Figure 6 - TEMUX Read Timing Diagram

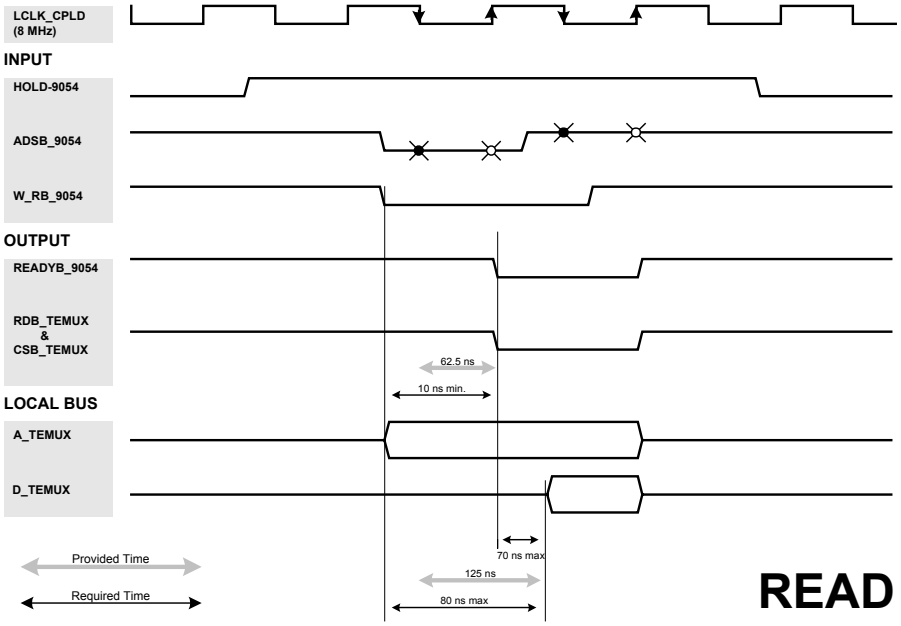
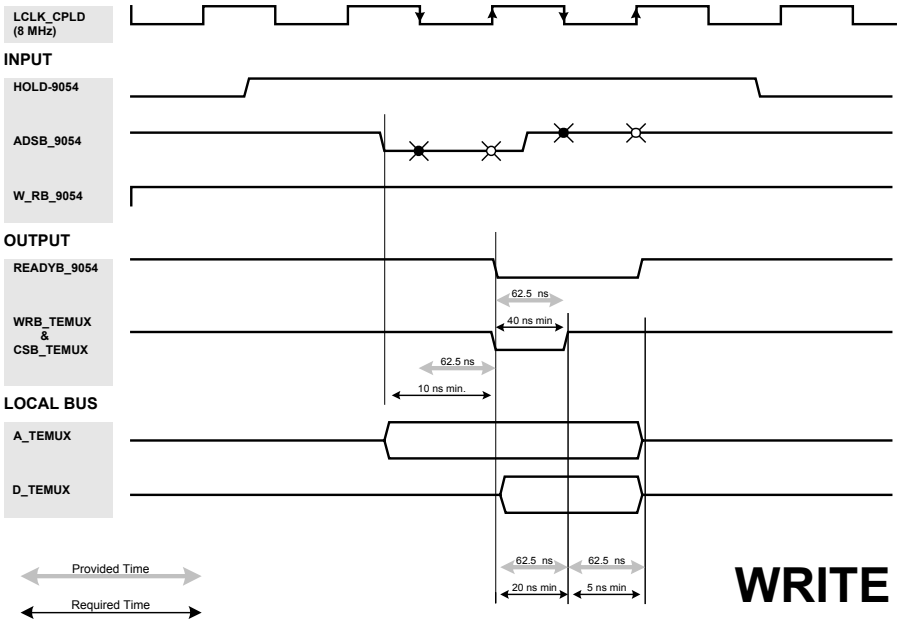


Figure 7 - TEMUX Write Timing Diagram



4.5 PCI 21152

4.5.1 Power Supply

The PCI21152 core logic is operated at 3.3V.

4.5.2 Timing

This device has 2 clock input signals (s_clk and p_clk) and 5 clock output signals (s_clk_o<4:0>). Input p_clk receives the Primary PCI bus clock signal. The output clocks s_clk_o<4:0> are for the Secondary bus devices, one of which is fed back into the s_clk input. Two Secondary devices require a clock signal each, that is, the FREEDM-32P672 and the PCI9054 Bridge. Hence, in total only 3 of the output s_clk_o are used.

The Primary and Secondary clocks must be synchronized with maximum skew of 7 ns. The skew between the Primary input (p_clk) and Secondary outputs (s_clk_o<4:0>) is 5 ns. Therefore, only 2 ns is allowed for Secondary clock etch returning to the s_clk input. Each Secondary clock output is limited to one load. It is recommended to use equivalent amount of etch on the board for all Secondary clocks, to minimize skew between them. It is also recommended to disable unused Secondary clock outputs to reduce power dissipation and noise in the system. They can be disabled using the Secondary clock control register in configuration space.

4.6 Timing Distribution

There are 4 timing sources in this design. Three of which are required by the TEMUX and are generated by on-board oscillators. These oscillators are powered at 3.3V.

The fourth source is the PCI bus clock. It is obtained from the PCI connector and fed into the PCI-to-PCI bridge Primary clock input signal. Clocks that are needed by the FREEDM-32P672 and the Local-to-PCI bridge are distributed by the PCI-to-PCI bridge as explained in the PCI21152 Timing section.

4.7 Power Requirements

The parts and their maximum power requirements for the FREEDM-32P672 with DS3 LIU reference design are listed in Table 4.

Table 4 - Component Power Consumption

Voltage	Components	Quantity	Current (mA)	Power (mW)
5V	LED	1	10	50
5V Total				**50**
3.3V	TDK78P2241	1	95	315
	Intel PCI21152	1	-	1200
	PLX PCI9054	1	-	1000
	Xilinx CPLD	1	15[1]	50
	Pericom 8-bit Driver	1	-	1000
	Fairchild Quad AND	1	-	500
	Oscillators	4	23[2]	304
	LED	1	10	33
3.3V Total				**4400**
2.5V	TEMUX	1	-	1300
	FREEDM-32P672	1	-	1350
	LED	1	10	25
2.5 Total				**2675**
	TOTAL	-	-	≈ **7127**

1 Estimated value as it highly depends on the design. 2 Averaged value. Values represent the worst case.

4.8 Connectors

4.8.1 JTAG Port

The PCI connector provides the JTAG pins. Only the TEMUX and FREEDM-32P672 support JTAG. The PCI9054 and PCI21152 support NAND-TREE testing, please refer to their respective datasheets for details.

4.8.2 PCI Connector

A universal PCI connector is used in this design. Positions A50/B50, A51/B51, A12/B12, and A13/B13 of the universal PCI connector are used for the keying mechanism. PCI implements a keying mechanism to differentiate 5V from 3.3V signaling. The keying mechanism is designed to prevent a board built with one buffer technology (3.3V or 5V) from being inserted into a system designed for the other buffer technology (5V or 3.3V, respectively). A universal PCI connector is meant for an environment that can support either 5V or 3.3V, hence allowing for more flexibility. For this design however, the back-plane signaling environment must provide 5V, since the 5V source is used to regulate the 2.5V and 3.3V supplies.

4.8.3 Headers

One, two, and four pin headers are used with several of the devices on the board for the purpose of probing or device configuration. Refer to the schematic details.

5 SOFTWARE INTERFACES

5.1 General Overview

Although, in this section some software issues are addressed, be advised that detailed software configuration is highly dependent on the environment and it is beyond the scope of this reference design. The intended goal of this document is to illustrate the hardware interfacing of the devices to achieve a DS3 application.

5.2 TEMUX

Configuration and monitoring of the TEMUX can be accomplished by the host processor via the PCI9054 bridge, PCI21152, and the PCI connector. Normal mode registers are used to configure and monitor the operation of the TEMUX. Normal mode registers are selected when TRS (A [13]) is low. Refer to the TEMUX register description document [13] for more details. Also refer to the TEMUX datasheet [11] for further clarification.

The interface from the PCI9054 bridge must provide an 8-bit bi-directional data bus and 14-bit address bus. Signal interfaces required are Interrupt (INTB), Chip Select (CSB), Read Enable (RDB), Write Strobe (WRB), and Reset (RSTB). Most of which are facilitated by the CPLD from a different set of signals that are provided by the PCI9054.

Address Latch Enable (ALE) pin is pulled high to disable multiplexing of data and address pins.

5.3 FREEDM-32P672

The FREEDM-32P672 is configured and monitored across the PCI bus interface by a host processor and packet memory (RAM). There are 2 types of registers: PCI Host Accessible registers and PCI Configuration registers. Description and handling of both PCI register types is detailed in the FREEDM-32P672 datasheet [12] and the application note [14].

5.4 FREEDM-32P672 PCI Configuration

Configuration of the interface is done by the GPIC target machine sub-block in the FREEDM-32P672. It provides the PCI Configuration registers.

The configuration registers can only be accessed through the PCI Host interface. These registers can only be accessed when the GPIC is a target and a configuration cycle is in progress as indicated using the IDSEL input.

The CBI bus interface provides access to the CBI address space of the FREEDM-32P672 blocks. The CBI address space is set by the associated BAR in the PCI Configuration registers.

Write transfers to the CBI space always write all 32 bits provided that at least one byte enable is asserted. A write command with all byte enables negated will be ignored. Read transfers always return the 32 bits regardless of the status of the byte enables, as long as at least one byte enable is asserted. A read command with all byte enables negated will be ignored. Refer to the datasheet [12] for more details.

5.5 PCI 9054 Configuration

Table 5 specifies the values that should be programmed into the SEEP for configuring the address mapping. These values will be loaded into the PCI9054 registers on power-up. Please refer to the PCI9054 datasheet [9] for further configuration details.

Before programming the SEEP with the values below, the SEEP should be initialized with known values (such as 0x0). This is to ensure safety when overwriting other register in the PCI9054 that are not indicated here. Also, many of the registers (not listed below) in the PCI9054 take on default values after reset, changing (overwriting) these values should be avoided. The values listed below are loaded in sequence of the SEEP offset, with the MSB loaded first. Refer to the PCI9054 datasheet [9] for more information.

Table 5 - PCI 9054 Configuration Registers Values

Register	SEEP Offset	Description	Value
PCIIDR[31:16]	0x00	Device ID	0x9054
PCIIDR[15:0]	0x02	Vendor ID	0x10B5
PCICCR[23:8]	0x04	Class Code	0x0680
PCICCR[7:0]	0x06	Class Code/Revision	0x0000
PCIIPR[7:0]	0x0A	Interrupt Pin/Interrupt Line Routing	0x0001
LAS0RR[31:16]	0x14	[1]MSW of Range for PCI-to-Local Address Space 0	0xFFFF
LAS0RR[15:0]	0x16	[1]LSW of Range for PCI-to-Local Address Space 0	0xC000
LAS0BA[31:16]	0X18	MSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	0x0000
LAS0BA[15:0]	0X1A	[2]LSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	0x0001
BIGEND[7:0]	0x22	LSW of local Bus Big/Little Endian Descriptor Register	0x0005
LBRD0[31:16]	0x2C	MSW of Bus Region Descriptors for PCI-to-Local Accesses	0x0000
LBRD0[31:16]	0x2E	LSW of Bus Region Descriptors for PCI-to-Local Accesses	0x0340

1 These values indicate to the PCI9054 a 14-bit address range to satisfy the TEMUX requirement. The values shown are actually the inverse of the address range – this representation is required by the PCI9054. 2 The lowest bit must be set to enable PCI host access to Local Address Space 0.

Note that in this design there is only one device, TEMUX, on the Local bus, consequently only one address space is required. Hence Address Space 0 is being used. Other address space can be configured if more devices are present on the Local bus.

Referring to Figure 4, the PCI Base Address is not included in Table 5 and is configured by the PCI initialization software.

Configuration registers can be written to via the SEEP or the Local or PCI bus.

5.6 PCI 21152 Configuration

The host initialization software is required to provide the following functions during the initialization process:

- Assigning PCI bus numbers
- Allocating address ranges
- Writing IRQ numbers into each device
- PCI bus numbers

To initialize the PCI21152 so that memory, I/O, and configuration transaction can be forwarded, use Table 6 to write to the bridge configuration registers. Numerical values are not provided in the table because it is dependent on the system. If this card is residing on a host system, which is behind another PCI Bridge then the numbering of PCI buses and bridges will differ accordingly. Refer to the PCI21152 datasheet [4] and the PCI-to-PCI Bridge Architecture Specification Rev. 1.1 [8].

Table 6 - PCI21152 Initialization of Configuration Registers

Register Name	Configuration Space Offset in PCI21152	Value	Notes
Subordinate/ Secondary/Primary bus numbers	18h	00XXYYZZh	XX = subordinate bus number = YY YY = Secondary bus number ZZ = Primary bus number
Secondary status/ I/O limit address/ I/O base address	1Ch	FFFFX0Y0h	Clear status bits. X = I/O limit address bits <15:12> Y = I/O base address bits <15:12>
Memory limit/ Memory base	20h	XXX0YYY0h	XXX = nonprefetchable memory limit address <31:20> YYY = nonprefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
PF memory limit/ PF memory base	24h	XXX0YYY0h	XXX = prefetchable memory limit address <31:20> YYY = prefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
Bridge control	3Ch	000X0000h	X = 0 (no ISA bus in system)
Primary status/ Command	04h	FFFF0007h	Clear status bits. Turn on I/O enable for downstream I/O. Turn on memory enable for downstream memory. Turn on master enable for upstream memory and I/O. **Write this register last.**

The PCI21152 has a set of Memory Mapped (MM) I/O base and limit address registers (Table 7) in configuration space that define MM I/O address range for I/O address forwarding. It supports 32-bit MM I/O addressing, which allows MM I/O downstream addressing to be mapped anywhere in a 4 GB MM I/O address space. MM I/O transactions with addresses that fall inside the range are forwarded downstream. MM I/O transactions with addresses that fall outside this range are forwarded upstream.

Table 7 - PCI21152 Memory-Mapped I/O Space Registers

Register Name	Configuration Space Offset in PCI21152	Field Width	Value	Representation
--	--	20	0	Memory_address <19:0> ≡ 0[1] for MM I/O Base Address; aligns address to 1MB boundary
--	--	20	0	Memory_address <19:0> ≡ F FFFFh[1] for MM I/O Limit Address; aligns address to 1MB boundary
Memory Base Address	20h	16	$Z_{15}..Z_4$ 0000h[2]	$Z_{15}..Z_4$ = memory address <31:20> for Base Address
Memory Limit Address	22h	16	$Z_{15}..Z_4$ 0000h[2]	$Z_{15}..Z_4$ = memory address <31:20> for Base Address

1 Assumed value 2 The bottom 4 bits are hardwired to a hexadecimal value of 0000.

To enable downstream forwarding of MM I/O transactions, the MM I/O enable bit must be set in the command register; similarly for upstream forwarding of MM I/O transactions, the master enable bit must be set in the command register. These configurations must be done after the base and Limit address configuration (above) and while both buses are idle.

Memory-Mapped (MM) I/O transactions are needed by the FREEDM-32P672 device.

Similar to the MM I/O addresses, the I/O enable bit and master bit must be set in the command register to enable downstream and upstream of I/O transactions, respectively. The I/O Base and Limit registers also define a range that the PCI21152 uses to determine when to forward I/O commands. Transactions are forwarded downstream if the address falls in the range and upstream outside the range. Table 8 lists the address range. This address range supports 32-bit addressing only. Address range configuration must be done before enabling the bits.

Table 8 - PCI21152 I/O Address Space Registers

Register Name	Configuration Space Offset in PCI21152	Field Width	Value	Representation
--	--	12	0	AD<11:0> ≡ 0[1] for Base Address; aligns address to 4KB boundary
--	--	12	0	AD<11:0> ≡ FFF[1] for Limit Address; aligns address to 4KB boundary
I/O Base Address	1Ch	8	ZZZZ 1111h[2]	ZZZZ = AD<15:12> of I/O Base Address
I/O Limit Address	1Dh	8	ZZZZ 1111h[2]	ZZZZ = AD<15:12> of I/O Limit Address
I/O Base Address Upper 16 bits	30h	16	$Z_{15}..Z_0$	$Z_0..Z_{15}$ = AD<31:16> of I/O Base Address
I/O Limit Address Upper 16 bits	32h	16	$Z_{15}..Z_0$	$Z_0..Z_{15}$ = AD<31:16> of I/O Limit Address

1 Assumed value 2 The bottom 4 bits are read only and have a hexadecimal value of 1111 to indicate that 32-bit I/O addressing is supported.

Similarly, the space address registers in the table above are not provided with numerical values, because it is dependent on the host system. Please refer to the PCI21152 datasheet [4] and specifications [7] and [8] for more details.

6 COMPONENT SELECTION

6.1 PCI-PCI Bridges

- Intel PCI21152 is the best suitable option for this design because the vendor has other current devices (already developed) in its family, which allows for potential of upgrading; for example support for 66MHz and 64bit. To further improve this design, Intel's PCI21154 can be used to allow for 66MHz bus. At this clock frequency the FREEDM-32P672 is utilized to its fullest potential. However, all other devices on the secondary bus must also operate at 66MHz. The limiting device in this design would be PLX's PCI9054, which operates at a maximum PCI bus frequency of 33MHz. PLX's PCI9610 would be ideal as it operates at 66MHz, however it is not available as of this date.

- HiNT HB1 is another device that is suitable. However, this product is the first in its line, so potential of upgrading is not as vast.

- TI PCI 2031 is also sufficient for the functionality needed. However, it supports PCI-PCI bridge specification ver. 1.0 and not 1.1, which takes into consideration delayed transactions. Also, It is the only active device in its line – again, limited upgrade potential.

6.2 Oscillator

The on-board oscillators provide timing references. The stability figure of an oscillator should include any variation due to calibration, temperature, voltage, load, aging, shock, and vibration, and is specified over the lifetime of the oscillator.

The TEMUX requires three oscillators. They should have stability of ±32ppm or better and 50% duty cycle.

Either CMOS or TTL oscillator can be used. The following are some vendors that provide these oscillators:

Table 9 - Oscillator Vendors

Vendor	±32ppm or better
MMD	Yes
Ecliptek	Yes
Champion	Yes

6.3 De-coupling and Bypass Capacitors

In this design, power pins de-coupling is achieved by 0.01 μF and 0.1 μF capacitors. Tantalum capacitors of 22 μF are used for bulk de-coupling.

6.4 Resistors

Resistors used for terminating the DS3 LIU should have tolerance of 1%. Other terminating, pull-up, and pull-down resistors can be of 5% tolerance.

7 GLOSSARY

AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
ATM	Asynchronous Transfer Mode
BAR	Base Address Register
CAS	Channel Associated Signaling
CBI	Control Block Interface
COFA	Change of Frame Alignment
ESF	Extended Superframe
EXZ	Excessive Zero
FAS	Frame Alignment Signal
FEAC	Far End Alarm Control
FEBE	Far End Block Failure
FERF	Far End Receive Failure
GPIC	General Purpose Peripheral Component Interconnect Controller (Sub block in the FREEDM-32P672)
HDLC	High-level Data Link Control (protocol)
IRQ	Interrupt Request
LOS	Loss of Signal
NFAS	No Frame Alignment Signal
OOF	Out of Frame
RAI	Remote Alarm Indication
SBI	Scalable Bandwidth Interconnect
SF	Standard Superframe

8 REFERENCES

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6. MindSahre Inc., "PCI System Architecture." Addison Wesley Longman Inc., 1999, 4th ed.

7. PCI Special Interest Group, "PCI Local Bus Specification Rev. 2.2." December 1998.

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9. PLX Technology Inc., "PCI 9054 Data Book." November 1998, ver. 1.0.

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11. PMC-Sierra Inc., PMC-981125, "TEMUX High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer Datasheet." June 1999 Issue 4.

12. PMC-Sierra Inc., PMC-990262, "FREEDM-32P672 - 32 Link, 672 Channel Frame Engine and Datalink Manager Datasheet." May 1999, Issue 2.

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14. PMC-Sierra Inc., PMC-990545, "Frame Engine and Datalink Manager 32P672 Programmer's Guide." June 1999, Issue 2.

15. TDK Semiconductor Corp., “Advanced Information 78P2241 E3/DS3/STS-1 Transceiver.” September 1999.

9 DISCLAIMER

This document is a paper reference design, and as such, has not been built or tested as of this date.

10 APPENDIX A: SCHEMATIC

This schematic is comprised of 9 pages as follows:

Sheet 1: Root Drawing

This sheet provides a block diagram of the interface signals between blocks. The transmit/receive signals start at the T3 Line Interface and propagate to the PCI-PCI Bridge block.

- The Secondary PCI bus connecting the FREEDM-32P672, Local-PCI-Bridge, and PCI-PCI-Bridge blocks is comprised of the standard PCI bus signals. In addition, interrupt signals are forwarded from the FREEDM-32P672 and Local-PCI-Bridge blocks to the Primary PCI Bus via the PCI-PCI-Bridge block. Also, secondary clocks are distributed by the PCI-PCI-Bridge block from the primary PCI clock to the FREEDM-32P672 and the Local-PCI-Bridge blocks.

- The FREEDM-32P672 and the TEMUX are programmed by the host processor via the PCI bridges.

- The TEMUX is not a PCI device and thus it requires a PCI bride, Local-PCI-Bridge block, to the interface to the PCI bus and ultimately the host processor.

- The Oscillator block provides timing for the TEMUX and the Local-PCI-Bridge blocks. Clock trace length should be kept to a minimum to reduce adverse affects. The secondary clock traces should have similar length to reduce skew.

- The reset signal from the Power block is routed to the PCI-PCI Bridge, and is then distributed via the secondary PCI bus to all other devices. The system is reset via the Primary PCI bus, whenever the host is reset, or when the reset switch is active.

- A JTAG chain is extended from PCI connector to connect the FREEDM-32P672 and TEMUX blocks and the CPLD in the Local-PCI-Bridge block.

- 75 Ω signals impedance is maintained throughout the whole design.

Sheet 2: Line Interface Unit

This sheet provides an interface to the T3 port using the TDK78P2241 DS-3 Line Interface Transceiver. Resistors and capacitors are connected as outlined in the manufacturer's datasheet for the device.

- LPBK header allows the user to manually enable/disable Loop-back. When /LPBK is tied low, analog (AMI) loop-back is selected; when float, Digital loop-back is selected; when high, no loop-back is selected. For typical operation, the jumper should be tied high.
- ICKP header allows the user to manually invert the RCLK and TCLK. When ICKP is tied low, both clocks are normal; when float, both are inverted; when high, RCLK is normal and TCLK is inverted.
- LBO head allows the user to setup the device appropriately according to the cable length. Logic low for $\geq$ 225ft of cable or logic high for $<$ 225ft of cable.
- A probe point is provided by J7 for monitoring the LIN$\pm$ for signal loss.
- The wires TCLK_LIU, TPOS, TNEG, RCLK_LIU, RPOS, and RNEG are provided in 75 Ω controlled impedance traces.
- The transformers used should have 3% tolerance.
- The Bantam connectors are connected to chassis ground for better isolation.
- Three pins (7, 17, 26) are connected to VCC, each of which requires de-coupling capacitors of 0.1 μF and 4.7 μF to stabilize any variations in the power supply.

Sheet 3, 4: TEMUX EGRESS (1/2) and TEMUX INGRESS (2/2)

These sheets provide the TEMUX. T1 functionality has been assumed and hence implemented in this design. The TEMUX provides the DS3 multiplexing/demultiplexing and the T1/E1 framing.

- The TEMUX operates at 2.5V for the core logic and 3.3V for the I/O pads.
- CTCLK is 12.352MHz since T1 is assumed. CTCLK, TICLK (44.736MHz), XCLK (37.056MHz), TCLK<27..0>, and RCLK<27..0> are all provided via 75 Ω controlled impedance traces.

- Unused input pins are disabled – either by pull up or down resistors of 4.7 KΩ or 330 Ω, respectively. Unused output pins are ignored. Since in this design, the TEMUX is connected serially with the FREEDM-32P672, it is operated in serial mode and unused pins are intended for other modes and interfaces that the TEMUX supports, such as SBI bus interface. The IFP<28..1> output signals are framing pulse signals intended for accompanying the Ingress data, but it is not needed by the FREEDM-32P672 in this design, since each signal has a corresponding clock signal.

- The micro interface is connected through the Local-PCI-Bridge and PCI-PCI-Bridge to the host processor.

- Termination resistors of 51 Ω along with the internal resistance (≈ 22 Ω) of the device match trace impedance of 75 Ω.

- Open drain pins such as interrupt pins are pulled up by 4.7 KΩ resistors.

- Capacitors of 0.01 μF are used on all power pins for de-coupling the power supply noise.

Sheet 5: FREEDM-32P672

This sheet provides the frame relay HDLC processor. The FREEDM-32P672 (PM7380).

- The FREEDM-32P672 has a standard PCI bus interface.

- The FREEDM-32P672 operates at 2.5V for the core logic and 3.3V for the I/O pads.

- The M66EN is set low for 33MHz PCI bus operation.

- It receives a 33MHz secondary clock from the PCI21152.

- The PCI1_IDSEL_FREEDM derived from PCI_AD<20> is fed into the IDSEL pin of the FREEDM-32P672 device. The PCI-PCI-Bridge, PCI21152, provides the PCI IDSEL signals for devices on the Secondary bus using selected address lines. PCI_AD<20> is understood as Device #4 by the PCI21152. It should be noted that PCI operations intended for the FREEDM-32P672 are routed via the PCI21152 using this device number along with the bus number. There are many other ways of selecting this device number – refer to the PCI21152 datasheet [4].

- Unused input pins are disabled – either by pull up or down resistors of 4.7 KΩ or 330 Ω, respectively. Unused output pins are ignored. Since in this design,

the FREEDM-32P672 is used with the TEMUX only 28 pins are connected for the transmit/receive data signals. Also the FREEDM-32P672 and TEMUX are connected serially with corresponding data and clock signals, consequently the M-VIP interface (T/RMVCK<3..0>, T/RMV8FPC, T/RMV8DC, T/RFPB, T/RFP8B) is not used. The PMCTEST pin is disable to allow for normal operation.

- Headers J6, J8, J9, and J10 provide access to the Transmit and Receive Bit Error Rate Test Data and Clock signals.
- Termination resistors of 51 Ω along with the internal resistance (≈ 22 Ω) of the device match trace impedance of 75 Ω.
- Open drain pins such as interrupt pins are pulled up by 4.7 KΩ resistors.
- Capacitors of 0.01 μF are used on all power pins for de-coupling the power supply noise.

Sheet 6: Oscillator Block

This sheet provides the timing for the TEMUX, PCI9054, and CPLD.

- The TEMUX requires Transmit Input Clock (TICLK) of 44.736MHz for the transmit direction and Crystal Clock (XCLK) of 37.056MHz (T1) or 49.152MHz (E1) for timing many of the T1/E1 sub-blocks. It also requires Common Transmit Clock (CTCLK) of 12.352/16.384MHz (T1/E1) for operation in Master modes.
- To support both T1 and E1, the corresponding oscillators can be easily interchanged using socket-packaged oscillators.
- An 8MHz clock is also need for the Local bus, and it is used by the CPLD and PCI9054.
- The TEMUX oscillators should have stability of ±32ppm or better and 50% duty cycle.
- Capacitors of 0.01 μF and 0.1 μF are used on all power pins for de-coupling the power supply noise.

Sheet 7: Local To PCI Bridge & CPLD

This sheet provides the Local to PCI bridge and glue logic to interface the TEMUX to the secondary PCI bus.

- The PCI9054 has a standard PCI bus interface.
- The PCI21152 core logic operates at 3.3V.
- The PCI1_IDSEL_9054 derived from PCI_AD<24> is fed into the IDSEL pin of the PCI9054 device. The PCI-PCI-Bridge, PCI21152, provides the PCI IDSEL signals for devices on the Secondary bus using selected address lines. PCI_AD<24> is understood as Device #8 by the PCI21152. It should be noted that PCI operations intended for the PCI9054 are routed via the PCI21152 using this device number along with the bus number. There are many other ways of selecting this device number – refer to the PCI21152 datasheet [4].
- It receives a 33MHz secondary clock signal (PCI9054_SCLK) from the PCI21152 for the PCI bus side and an 8MHz clock signal (LCLK_9054) for the Local side.
- Mode<1..0> pins are pulled low for C-Mode operation.
- To configure an 8-bit data bus, pins LBEB<1..0> are use as LA<1..0> and pins LBEB<3..2> are disabled.
- J11 is for accessibility to facilitate miscellaneous user I/O pins.
- The NM93CS56 is a SEEP device, used to load configuration data after reset. This device is dip socketed to allow for I/O data programming.
- Unused input pins are disabled – either by pull up or down resistors of 4.7 KΩ or 330 Ω, respectively. Unused output pins are ignored. The TEST pin is disabled to allow for normal operation. The BIGEND# pin is not used, rather software configuration of Big/Little Endian ordering is preferable.
- Signals HOLD, W_RB, READYB, and ADSB are used in the CPLD glue logic to interface to the TEMUX micro interface, which has the signals RDB_TEMUX, WRB_TEMUX, CSB_TEMUX, and RSTB_TEMUX.
- The INTB_TEMUX is just buffered and forwarded to LOC_INTB signal. It is passed through the CPLD for expandability purposes.
- Pins LHOLD and LHOLDA on the PCI9054 are connected since the PCI9054 is always the master of the Local bus.
- The CPLD is assumed to be socketed. However, JTAG programming is still possible via the J14 header. For normal JTAG testing short the header across and for CPLD programming use header pins (1, 3, 5, 7).

- Spare pins on the CPLD are connected to headers J12 and J13 for easier access. Each header is also connected to VDD 3.3V and GND.

- Pin assignment on the CPLD can be specified by VHDL code to match the schematic. However, this is not necessary as long as the CPLD pins are properly connected before layout.

- Open drain pins such as interrupt pins are pulled up by 4.7 KΩ resistors.

- Capacitors of 0.01 μF are used on all power pins for de-coupling the power supply noise.

Sheet 8: PCI To PCI Bridge

This sheet provides the PCI-PCI-Bridge and the PCI edge connector.

- The PCI21152 has standard PCI signals on both, the Primary and Secondary sides.

- The S_CFN_I is pulled low to enable the internal arbiter for the Secondary bus.

- The Secondary clock signals, S_CLK<2..0>, should have similar etch length to minimize skew. The other secondary clocks are disabled by software and pins S_CLK<3..4> are ignored.

- The AND gate provides the reset function upon receiving an activation from the Power block or the PCI connector.

- The S_VIO and P_VIO pins on the PCI21152 are both connected to 3.3V to configure both the Primary and Secondary sides to 3.3V signaling.

- Unused input pins on the PCI21152 are disabled – either by pull up or down resistors of 4.7 KΩ or 330 Ω, respectively. Unused output pins are ignored. Only S_REQ_I<0> and S_GNT_I<0> are used by the FREEDM-32P672, since it needs to be the master of the PCI Primary. The rest of the signals are disabled.

- The 3.3V pins are connected together but are not used; instead, the 5V supply is used since the commonly available motherboard provides 5V supply.

- Pins $V_{I/O}$ are dynamic in a Universal PCI connector, i.e. they can be 3.3V or 5V depending on the signaling environment and should be unconnected. For

this design to work properly, 5V supply must be available in the back-plane signaling environment.

- Both PRSNT1# and PRSNT2# should be grounded on the PCI connector to indicate a 7.5 W total power consumption by the card. For 15 W, PRSNT1# remains floating.

- Termination resistors of 51 Ω along with the internal resistance (≈ 22 Ω) of the device match trace impedance of 75 Ω.

- Open drain pins such as interrupt pins are pulled up by 4.7 Ω resistors.

- Capacitors of 0.01 μF are used on all power pins for de-coupling the power supply noise.

Sheet 9: Power Block

This sheet provides the 3.3V and the 2.5V power supplies for the reference design, as well as the reset circuitry.

- The 5V supply is received from the PCI connector. The 5V supply is regulated to provide the 2.5V and 3.3V supplies. The 2.5V is regulated by the LT1118-2.5 and the 3.3V by the LT1117-3.3.

- 3A fuse is used for reducing the risk of short circuit the power supply.

- LEDs are used to indicate the status of the power supplies. Resistors are used to limit the amount of current that flows into the LEDs to approximately 10A.

- 22 μF tantalum capacitors are used for bulk de-coupling.

- For the voltage regulator de-coupling, 22 μF and 10 μF are used as recommended by the manufacturer. It is also recommended that a 0.1 μF ceramic capacitor be paralleled with the output of the LT1118 to maintain quick settling time.

- The reset circuit VCC pin is not de-coupled so that it can sense any variations in the voltage.

- Reset circuitry is implemented using voltage monitor MAX811 from Maxim. A reset command propagates throughout all devices if a manual reset was performed; i.e. reset button was activated (low) or if the monitored voltage falls beyond a certain threshold. The threshold for MAX811S (3.3V monitor) is

min. 2.88V at +25°C. Also, MAX811S provides the de-bouncing for the reset button.

ROOT DRAWING

REVISIONS				
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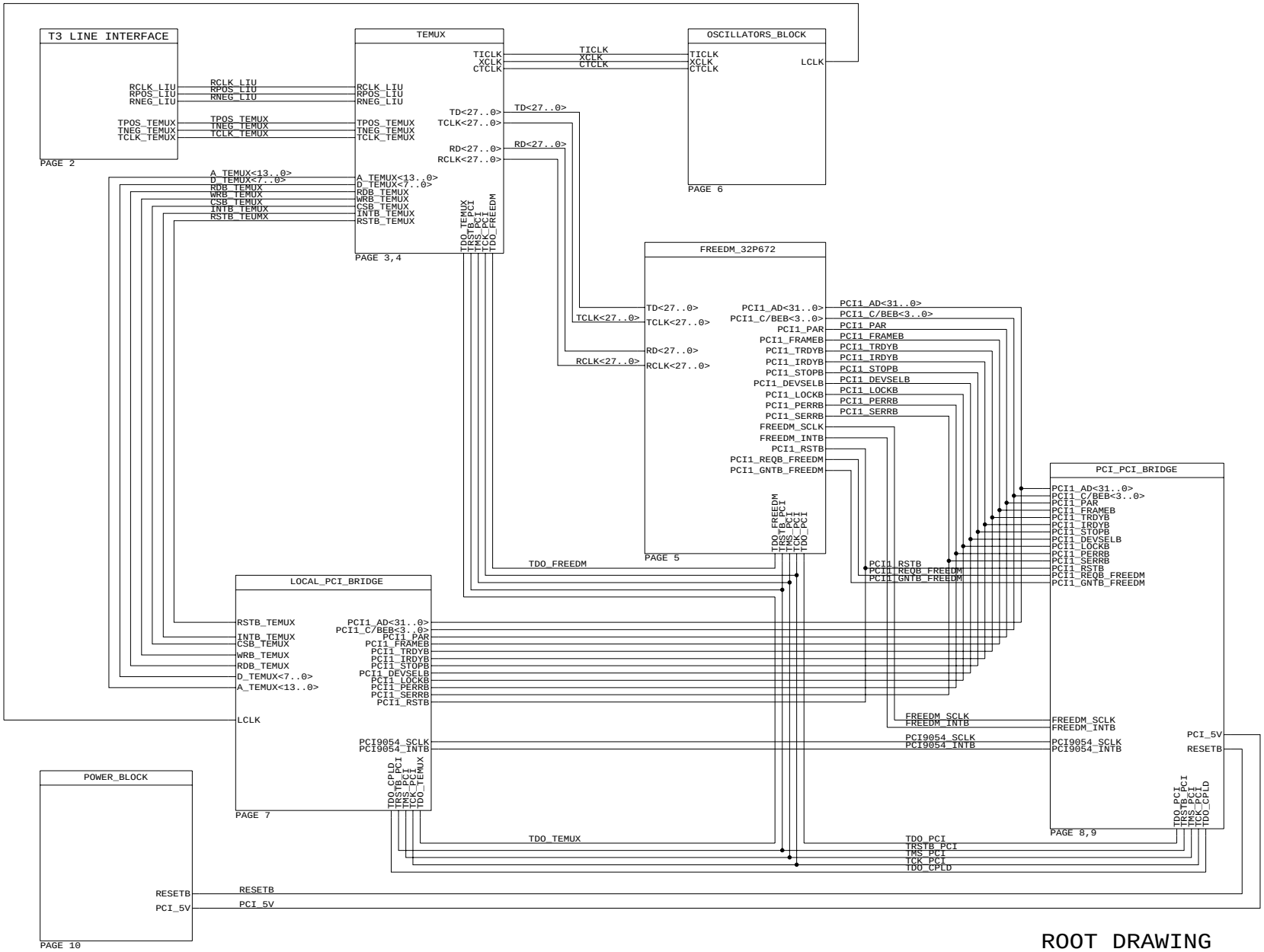

ROOT DRAWING

PMC-Sierra, Inc.

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TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN ROOT_DRAWING	REVISION NUMBER: 0
ENGINEER: TN	PAGE:1 OF 9

DRAWING

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LAST_MODIFIED=Tue Feb 8 11:00:09 2000

T3 LINE INTERFACE

REVISIONS				
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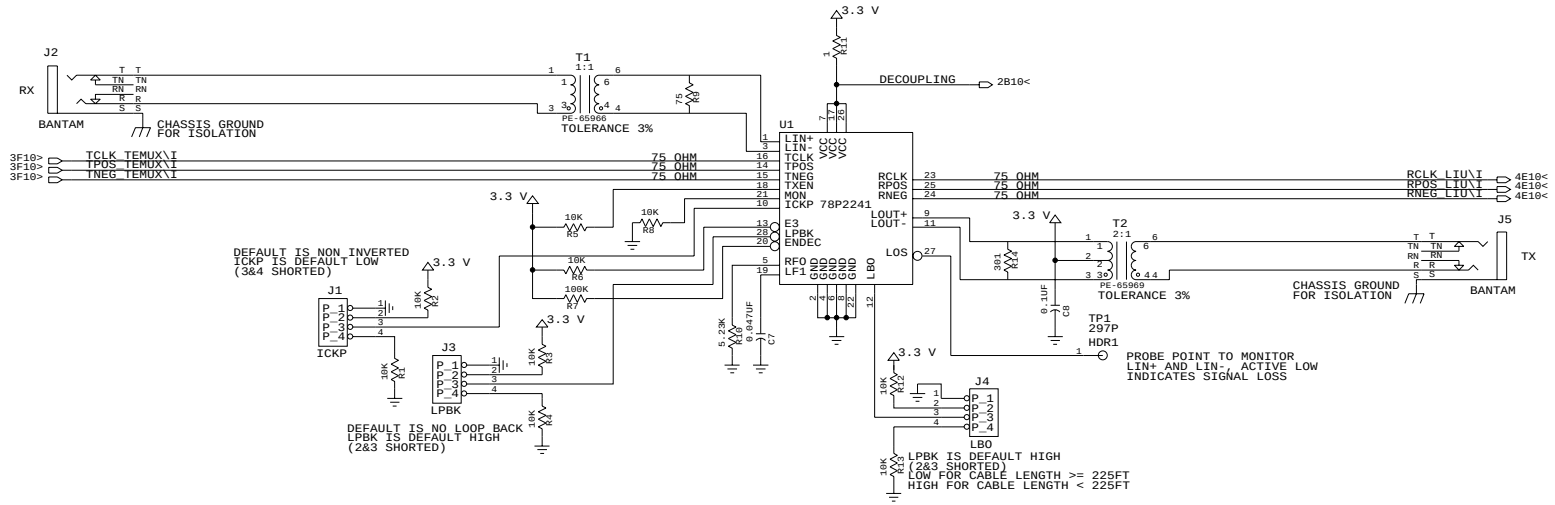

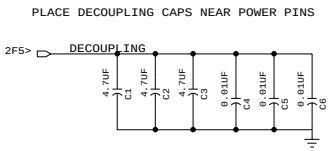

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LAST_MODIFIED=Wed Feb 9 18:14:52 2000

T3 LINE INTERFACE

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991724 DOCUMENT ISSUE NUMBER: 1 *PRELIMINARY*	ISSUE DATE: NOV. 08, 99
TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN T3_LINE_INTERFACE	REVISION NUMBER: 0
ENGINEER: TN	PAGE:2 OF 9

TEMUX EGRESS (1/2)

REVISIONS				
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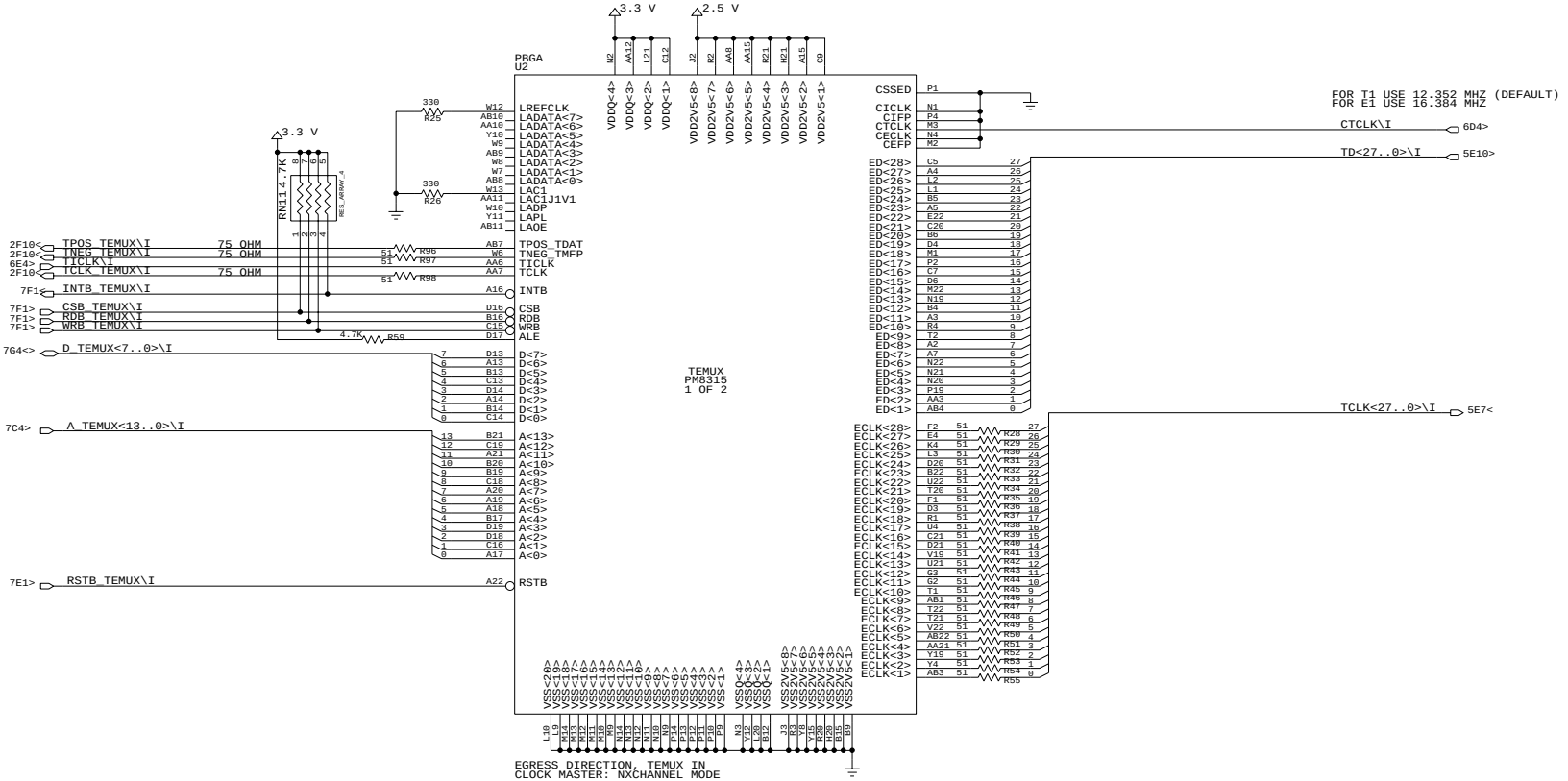
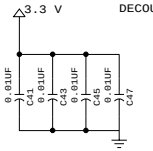
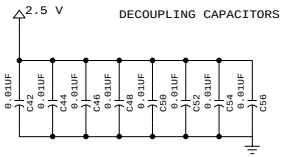




DECOUPLING CAPACITORS FOR VDD 3.3V



DECOUPLING CAPACITORS FOR VDD 2.5V

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LAST_MODIFIED=Wed Feb 9 18:15:01 2000

TEMUX EGRESS (1/2)

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991724 DOCUMENT ISSUE NUMBER: 1 *PRELIMINARY*	ISSUE DATE: NOV. 08, 99
TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN TEMUX EGRESS (1/2)	REVISION NUMBER: 0
ENGINEER: TN	PAGE:3 OF 9

TEMUX INGRESS (2/2)

REVISIONS				
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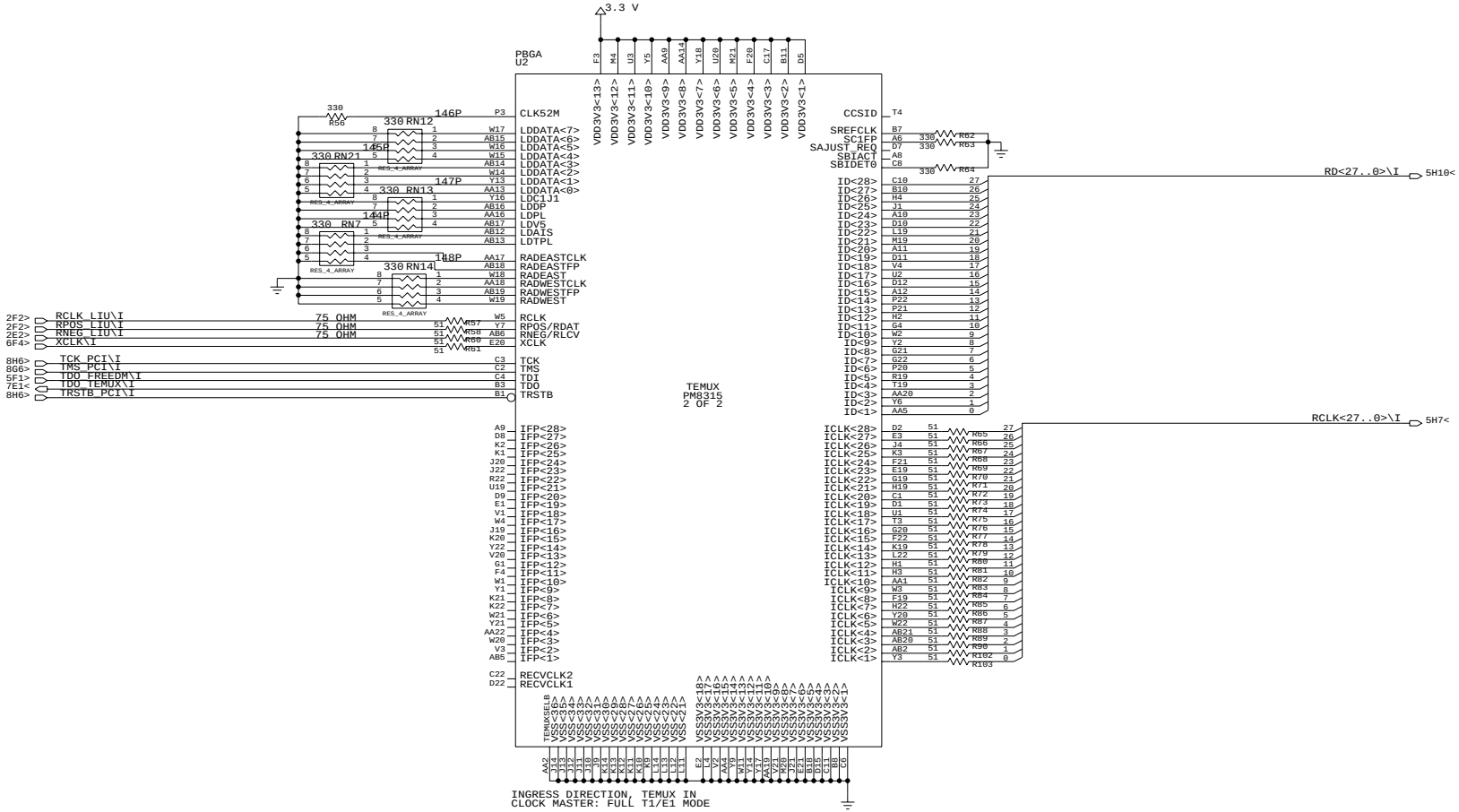

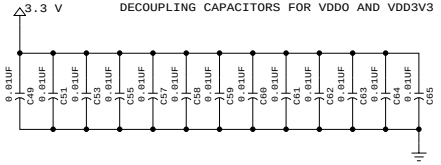

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TEMUX INGRESS (2/2)

PMC-Sierra, Inc.

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TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN TEMUX INGRESS (2/2)	REVISION NUMBER: 0
ENGINEER: TN	PAGE:4 OF 9

FREEDM32P672

REVISIONS				
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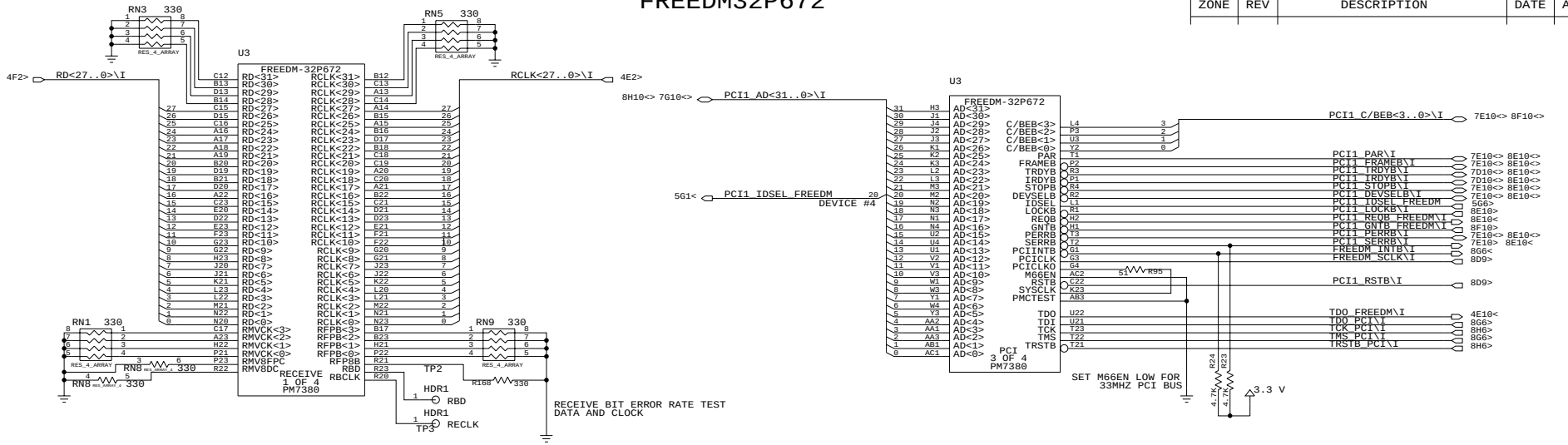

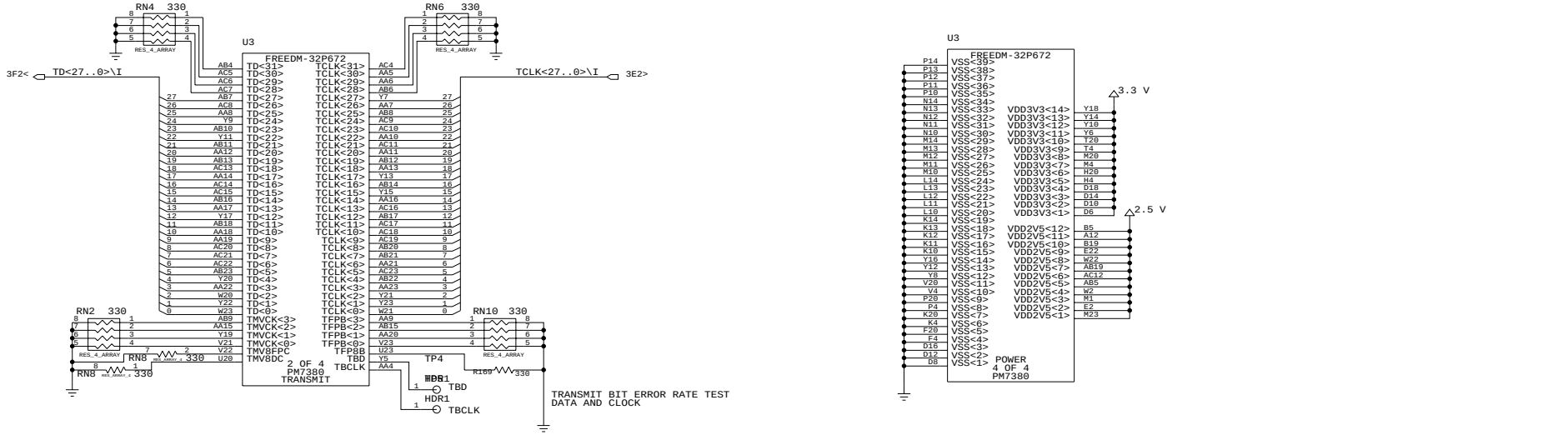

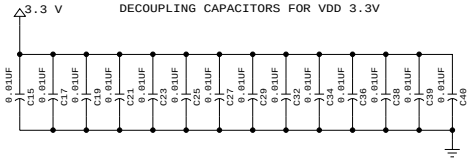

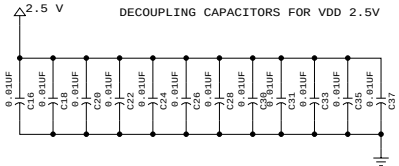

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LAST_MODIFIED=Wed Feb 9 18:14:58 2000

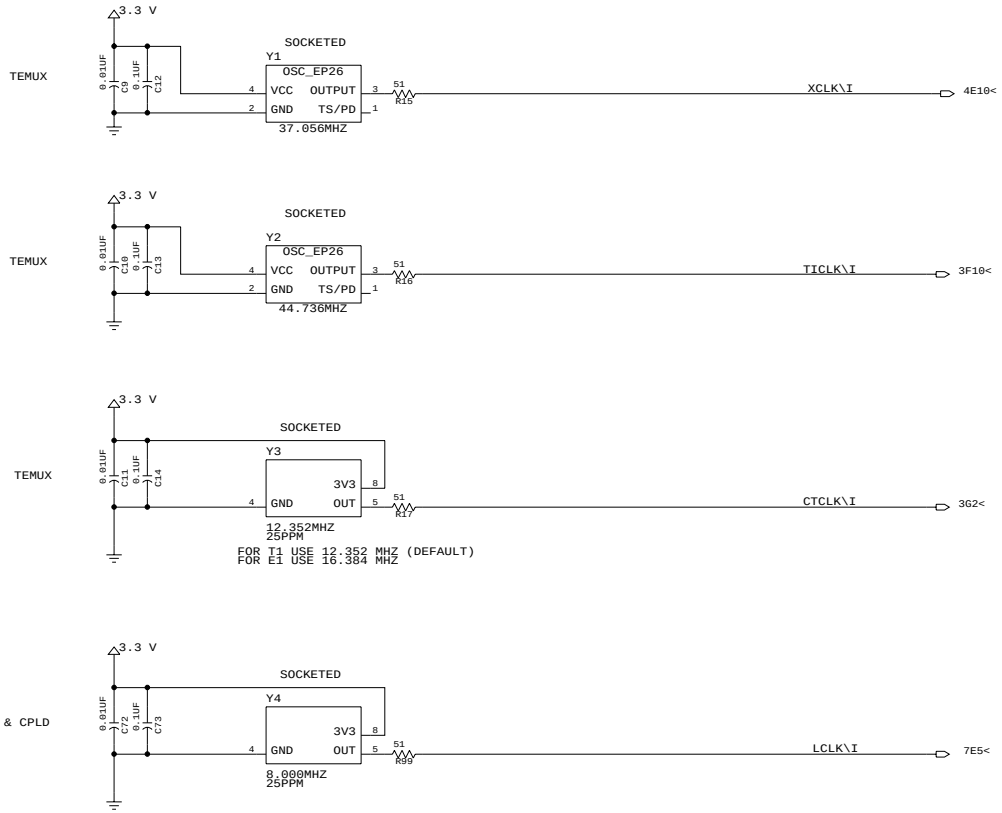
FREEDM32P672

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991724 DOCUMENT ISSUE NUMBER: 1 *PRELIMINARY*	ISSUE DATE: NOV. 15, 99
TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN FREEDM32P672	REVISION NUMBER: 0
ENGINEER: TN	PAGE:5 OF 9

OSCILLATOR BLOCK

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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OSCILLATOR BLOCK

PMC-Sierra, Inc.

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TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN OSCILLATORS	REVISION NUMBER: 0
ENGINEER: TN	PAGE:6 OF 9

LOCAL TO PCI BRIDGE & CPLD

REVISIONS				
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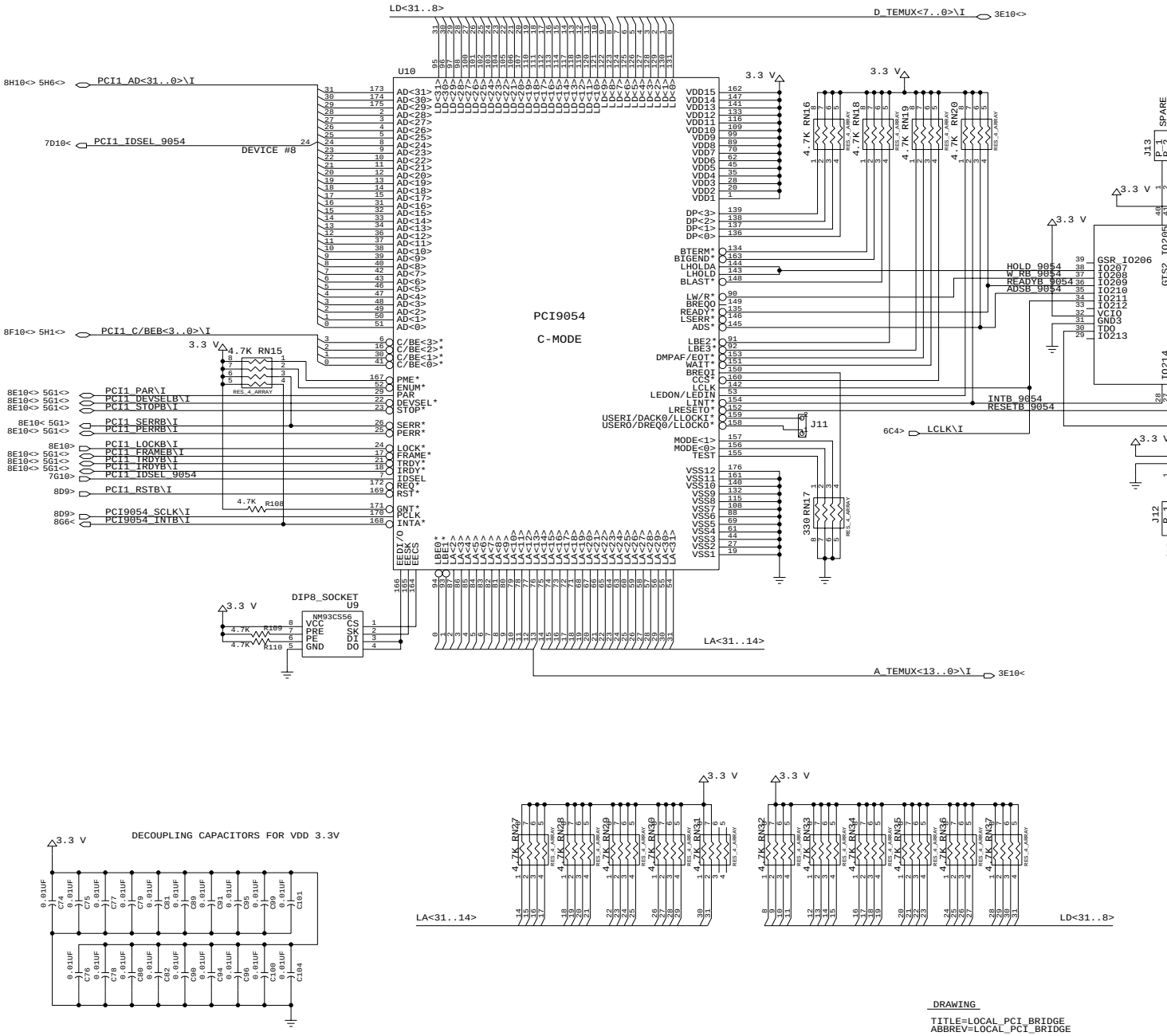

LOCAL TO PCI BRIDGE & CPLD

PMC-Sierra, Inc.

DRAWING

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LAST_MODIFIED=Wed Feb 9 18:15:11 2000

DOCUMENT NUMBER: PMC-991724 DOCUMENT ISSUE NUMBER: 1 *PRELIMINARY*	ISSUE DATE: DEC. 9, 99
TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN LOCAL_PCI_BRIDGE & CPLD	REVISION NUMBER: 0
ENGINEER: TN	PAGE:7 OF 9

PCI TO PCI BRIDGE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

S_VIO = P_VIO = 3.3V
PRIMARY AND SECONDARY
BUSES ARE BOTH 3.3V
SIGNALING ENVIRONMENT

U11

21152

CARD TO HOST

P1

PCI_UNIV_32BIT_CARD_CONNECTOR

U7 74HC08

NOTE:

USE 5V BACKPLANE
SIGNALING ENVIRONMENT
NOTE THE V_I/O PINS
ARE NOT USED

DECOUPLING CAPACITORS FOR VDD 3.3V

DRAWING

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ABBREV=PCI_PCI_BRIDGE
LAST_MODIFIED=Wed Feb 9 18:15:16 2000

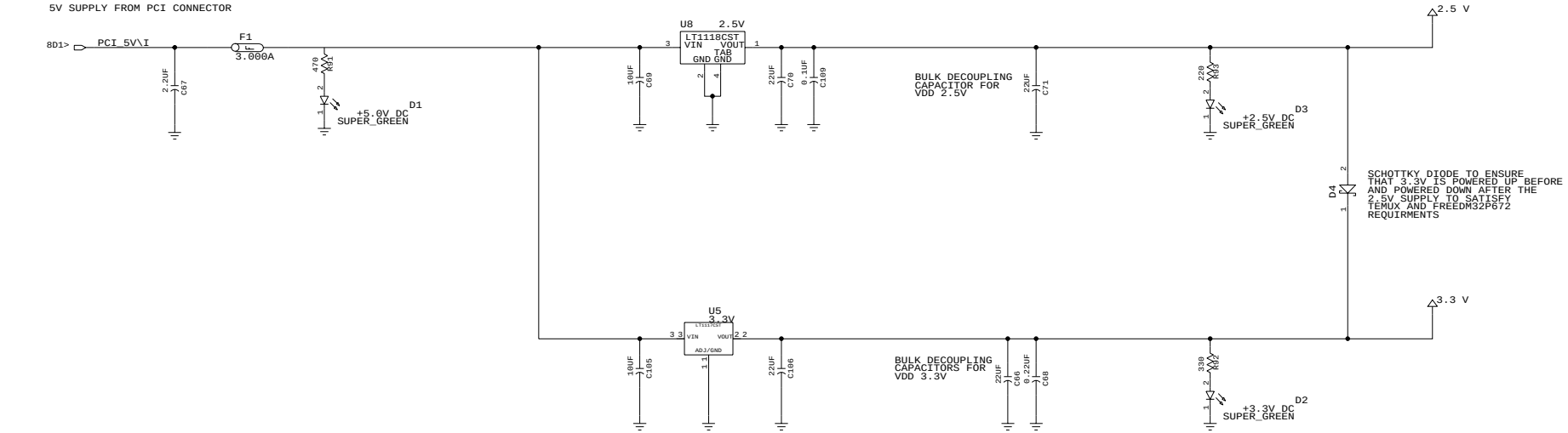
PCI TO PCI BRIDGE

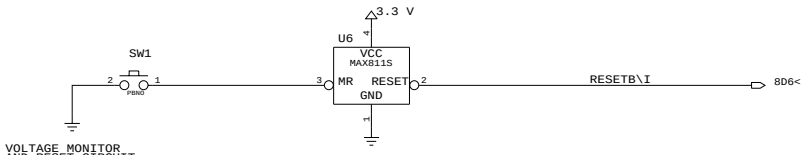
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991724 DOCUMENT ISSUE NUMBER: 1 *PRELIMINARY*	ISSUE DATE: NOV. 17, 99
TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN PCI_PCI_BRIDGE	REVISION NUMBER: 0
ENGINEER: TN	PAGE:8 OF 9

POWER BLOCK

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





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POWER BLOCK

PMC-Sierra, Inc.

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TITLE: FREEDM-32P672 DS3 LIU REF. DESIGN POWER BLOCK	REVISION NUMBER: 0
ENGINEER: TN	PAGE:9 OF 9

11 APPENDIX B: BILL OF MATERIALS

NO.	Part Number	Manufacturer	Ref Des	Description	Qty	Part Name - Value
1	21152	INTEL	U11	PCI-TO-PCI BRIDGE HARDWARE	1	21152_SOIC-BASE
2	PI74FCT3244S	PERICOM	U2	FAST CMOS 3.3V 8BIT BUFFER/LINE DRIVER	1	74FCT3244_SOIC-BASE
3	MM74HC08M	FAIRCHILD SEMI	U7	IC QUAD 2 IN AND GATE SOIC14	1	74XXX08_SOIC-HCMOS
4	78P2241	TDK SEMICONDUCTO R	U1	E3/DS3/STS-1 LINE INTERFACE TRANSCEIVER	1	78P2241_PLCC-BASE
5	ELECTRO SONIC -- PC-834-J-(BLACK)	?	"J2, J5"	?	2	BANTAM-BASE
6	DIGI-KEY -- PCC103BNCT-ND	?	"C4-C6, C9-C11, C15-C65, C72, C74-C104, C107, C108, C111, C112, C115, C116, C119, C120, C123, C124, C127"	X7R DIELECTRIC	100	"CAPACITOR-0.01UF, 50V, X7R_805"
7	AVX -- 08055C473JATN	?	C7	?	1	"CAPACITOR-0.047UF, 50V, X7R_805"
8	NEWARK -- 96F8740	?	"C8, C12-C14, C73, C109"	X7R	6	"CAPACITOR-0.1UF, 50V, X7R_805"
9	DIGI-KEY -- PCC1749CT-ND	?	C68	X7R DIELECTRIC	1	"CAPACITOR-0.22UF, 10V, X7R_603"
10	DIGI-KEY -- PCT2106CT-ND	?	"C69, C105"	PANASONIC TEH TANT. CAP.	2	"CAPACITOR-10UF, 10V, TANTTEH"

11	DIGI-KEY -- PCT2225CT-ND	?	C67	PANASONIC TEH TANT. CAP.	1	"CAPACITOR-2.2UF, 10V, TANT TEH"
12	DIGI-KEY -- PCT3226CT-ND	?	"C70, C106"	PANASONIC TEH TANT. CAP.	2	"CAPACITOR-22UF, 16V, TANT TEH"
13	DIGI-KEY -- PCT1226CT-ND	?	"C66, C71"	PANASONIC TEH TANT. CAP.	2	"CAPACITOR-22UF, 6.3V, TANT TEH"
14	DIGI-KEY -- PCT2475CT-ND	?	C1-C3	PANASONIC TEH TANT. CAP.	3	"CAPACITOR-4.7UF, 10V, TANT TEH"
15	DIGI-KEY -- 1N5820CT-ND	?	D4	?	1	"DIODE_SCHOTTKY_DO_20 1-3A, 20V"
16	PM7380	PMC-SIERRA	U3	FRAME ENGINE AND DATA LINK MANAGER 32P672	1	FREEDM32P672_PBGA-BA SE
17	DIGIKEY -- F1226CT-ND	?	F1	SOCKET PART NUMBER	1	"FUSE__SMD_SOCKET-3.0 00A, NANO"
18	PZC36SAAN	SULLINS ELECTRONICS	J12	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER10_100MIL-BASE
19	1-644695-4	AMP	J13	CONN MALE SINGLE ROW 14 PINS	1	HEADER14_MALE-BASE
20	PZC36SAAN	SULLINS ELECTRONICS	J11	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER2_100MIL-BASE
21	PZC36SAAN	SULLINS ELECTRONICS	J7	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER2_100MIL-BASE
22	PZC36SAAN	SULLINS ELECTRONICS	J8	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER2_100MIL-BASE
23	PZC36SAAN	SULLINS ELECTRONICS	J6	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER2_100MIL-BASE
24	PZC36SAAN	SULLINS ELECTRONICS	J10	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER2_100MIL-BASE
25	PZC36SAAN	SULLINS ELECTRONICS	J9	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER2_100MIL-BASE
26	PZC36SAAN	SULLINS ELECTRONICS	J1	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER4_100MIL-BASE
27	PZC36SAAN	SULLINS ELECTRONICS	J4	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER4_100MIL-BASE

28	PZC36SAAN	SULLINS ELECTRONICS	J3	"CONN HEADER STRAIGHT 36POS MALE .1"" SINGLE ROW"	1	HEADER4_100MIL-BASE
29	?	?	J14	HEADER 2X4 100MIL MALE	1	HEADER_4X2_100MIL-BA SE
30	NEWARK -- 95F9373	?	D1-D3	IDI7002X5	3	"LED-SUPER_GREEN, SURFACE MOUNT"
31	LT1117CST-3.3	LINEAR TECHNOLOGIES	U5	3.3V FIXED REGULATOR	1	LT1117_SOT-3.3V
32	LT1118CST-2.5	LINEAR TECHNOLOGIES	U8	"REGULATOR, 2.5V, 800MA, POSITIVE, LOW DROPOUT"	1	LT1118CST-2.5V
33	MAX811S	MAXIM	U6	4 PIN UP VOLTAGE MONITOR WITH MANUAL RESET INPUT 3.3V SOT143	1	MAX811S_SOT143-BASE
34	MB3025H-12.352MHZ	MMD COMPONENTS	Y3	OSC HCMOS/TTL HALF SIZE 8 PIN 12.352MHZ 25PPM	1	"MB3025H-12.352MHZ, 25PPM"
35	MB3025H-12.352MHZ	MMD COMPONENTS	Y4	OSC HCMOS/TTL HALF SIZE 8 PIN 8.000MHZ 25PPM	1	"MB3025H-8.000MHZ, 25PPM"
36	NM93CS56LEN	FAIRCHILD SEMI	U9	2048 BIT SERIAL EEPROM W/ DATA PROTECT AND SEQ READ DIP8	1	NM93CS56_DIP8_SOCKET -BASE
37	EP2632TTS-37.056M	ECLIPTEK	Y1	"OSCILLATOR, 37.056MHZ, 3.3V, 32PPM"	1	"OSC_EP26-37.056MHZ, 3.3V, 32PPM"
38	EP2645TTS-44.736M	ECLIPTEK	Y2	"OSCILLATOR, 44.736MHZ, 3.3V, 50PPM"	1	"OSC_EP26-44.736MHZ, 3.3V, 50PPM"
39	DIGIKEY -- P8009S-ND	?	SW1	VERT PCB MOUNT SPST PUSH BUTTOM	1	PBNO_VERT_6MM-BASE
40	PCI9054-AA50PI	PLX TECHNOLOGY	U10	PCI I/O ACCELERATOR	1	PCI9054_PQFP-BASE
41	PE65966	?	T1	?	1	PE65966-BASE
42	PE65969	?	T2	?	1	PE65969-BASE
43	?	?	R11	?	1	"RESISTOR-1, 5%, 603"
44	DIGI-KEY -- P<VALUE>CCT-ND	?	R7	?	1	"RESISTOR-100K, 1%, 805"

45	DIGI-KEY -- P<VALUE>ACT-ND	?	"R1-R6, R8, R12, R13"	?	9	"RESISTOR -10K, 5%, 805"
46	DIGI-KEY -- P<VALUE>ACT-ND	?	R100	?	1	"RESISTOR -1K0, 5%, 805"
47	DIGI-KEY -- P<VALUE>ACT-ND	?	R93	?	1	"RESISTOR -220, 5%, 805"
48	DIGI-KEY -- P301CCT-ND	?	R14	?	1	"RESISTOR -301, 1%, 805"
49	DIGI-KEY -- P<VALUE>ACT-ND	?	"R25, R26, R56, R62-R64, R92, R168, R169"	?	9	"RESISTOR -330, 5%, 805"
50	DIGI-KEY -- P<VALUE>ACT-ND	?	"R23, R24, R59, R104, R105, R108-R110"	?	8	"RESISTOR -4.7K, 5%, 805"
51	DIGI-KEY -- P<VALUE>ACT-ND	?	R91	?	1	"RESISTOR -470, 5%, 805"
52	DIGI-KEY -- P<VALUE>CCT-ND	?	R10	?	1	"RESISTOR -5.23K, 1%, 805"
53	DIGI-KEY -- P<VALUE>ACT-ND	?	"R15-R22, R27-R55, R57, R58, R60, R61, R65-R90, R94-R99, R102, R103, R106, R107, R164"	?	78	"RESISTOR -51, 5%, 805"
54	DIGI-KEY -- P75.0CCT-ND	?	R9	?	1	"RESISTOR -75, 1%, 805"
55	DIGI-KEY -- Y4<VALUE CODE>-ND	?	"RN1-RN10, RN12-RN14, RN17, RN21"	?	15	RES_ARRAY_4_SMD-330
56	DIGI-KEY -- Y4<VALUE	?	"RN11, RN15,	?	22	RES_ARRAY_4_SMD-

	CODE>-ND		RN16, RN18-RN20, RN22-RN37"			4.7K
57	PM8315-PI	PMC-SIERRA	U4	"T1/E1 FRAMER, VT/TU MAPPER, M13 MUX"	1	TEMUX_PBGA-BASE
58	XC9536XL-7PC44C	XILINX	U12	IC IN SYSTEM PROGRAMMABLE CPLD PLCC44 SOCKETED	1	XC9536XL_PC44_PLCC_SOCKET-BASE

12 APPENDIX C: VHDL CODE FOR GLUE LOGIC

CPLD code listing for interfacing the TEMUX and the PCI9054. Refer to the TEMUX micro interface timing diagrams in the TEMUX datasheet.

```
ENTITY TEMUX_9054 is
   PORT (
      RESETB_9054:      IN    STD_LOGIC;  -- reset from PCI9054
      LCLK_CPLD:        IN    STD_LOGIC;  -- external 8MHz clock
      HOLD_9054:        IN    STD_LOGIC;  -- HOLD request from PCI9054
      W_RB_9054:        IN    STD_LOGIC;  -- Write / Read from PCI9054
      ADSB_9054:        IN    STD_LOGIC;  -- address strobe from PCI9054
      READYB_9054:      OUT   STD_LOGIC;  -- Ready handshake to PCI9054
      INTB_9054:        OUT   STD_LOGIC;  -- Interrupt to PCI9054
      WRB_TEMUX:        OUT   STD_LOGIC;  -- write strobe to TEMUX
      RDB_TEMUX:        OUT   STD_LOGIC;  -- read strobe to TEMUX
      RSTB_TEMUX:       OUT   STD_LOGIC;  -- reset to TEMUX
      CSB_TEMUX:        OUT   STD_LOGIC;  -- TEMUX chip select
      INTB_TEMUX:       IN    STD_LOGIC;  -- Interrupt from TEMUX
);
END TEMUX_9054;

ARCHITECTUR TEMUX_9054 of TEMUX_9054 is
      COMPONENT BUFG                        -- global buffer component
            PORT (I: IN STD_LOGIC; O: OUT STD_LOGIC);
      END COMPONENT;

      SIGNAL falling: STD_LOGIC;
      SIGNAL rising: STD_LOGIC;
      SIGNAL CLK: STD_LOGIC;
      SIGNAL RESET: STD_LOGIC;
      SIGNAL INTB: STD_LOGIC;
      SIGNAL READ: STD_LOGIC;
      SIGNAL WRITE: STD_LOGIC;

BEGIN

BUFG_1:     BUFG  PORT MAP (I => LCLK_CPLD, O => CLK);
BUFG_2:     BUFG  PORT MAP (I => RESETB_9054, O => RESET);
BUFG_3:     BUFG  PORT MAP (I => INTB_9054, O => INTB);


RSTB_TEMUX <= RESET;
INTB_TEMUX <= INTB;
```

```
ADSB_FALLING:     PROCESS(CLK, RESET)
BEGIN
      IF (RESET = '0') THEN
            falling <= '1';
      ELSIF (CLK = '0' AND CLK'EVENT) THEN
            falling <= ((NOT ADSB_9054) NAND HOLD_9054);
      END IF;
END PROCESS ADSB_FALLING;

ADSB_RISING:      PROCESS(CLK, RESET)
BEGIN
      IF (RESET = '0') THEN
            rising <= '1';
      ELSIF (CLK = '1' AND CLK'EVENT) THEN
            rising <= falling;
      END IF;
END PROCESS ADSB_RISING;

READ_WRITE_CS:    PROCESS(W_RB_9054)
BEGIN
      IF (W_RB_9054 = '1') THEN
            CSB_TEMUX <= WRITE;
      ELSIF (W_RB_9054 = '0') THEN
            CSB_TEMUX <= READ;
      END IF;
END PROCESS READ_WRITE_CS;

READYB_9054 <= rising;
WRITE <= ((NOT falling) NAND W_RB_9054);
WRB_TEMUX <= WRITE;
READ <= ((NOT rising) NAND (NOT W_RB_9054));
RDB_TEMUX <= READ;

END TEMUX_9054;
```

NOTES

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