



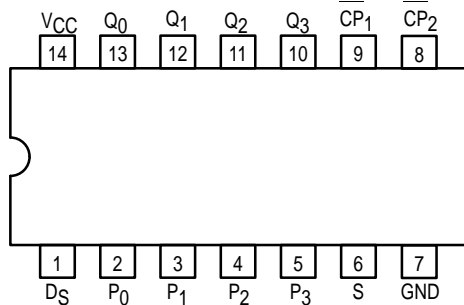
4-BIT SHIFT REGISTER

The SN54/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Synchronous, Expandable Shift Right
- Synchronous Shift Left Capability
- Synchronous Parallel Load
- Separate Shift and Load Clock Inputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

VCC = PIN 14
GND = PIN 7

PIN NAMES

S	Mode Control Input
DS	Serial Data Input
P ₀ -P ₃	Parallel Data Inputs
CP ₁	Serial Clock (Active LOW Going Edge) Input
CP ₂	Parallel Clock (Active LOW Going Edge) Input
Q ₀ -Q ₃	Parallel Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
S	0.5 U.L.	0.25 U.L.
DS	0.5 U.L.	0.25 U.L.
P ₀ -P ₃	0.5 U.L.	0.25 U.L.
CP ₁	0.5 U.L.	0.25 U.L.
CP ₂	0.5 U.L.	0.25 U.L.
Q ₀ -Q ₃	10 U.L.	5 (2.5) U.L.

NOTES:

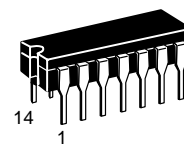
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

GUARANTEED OPERATING RANGES

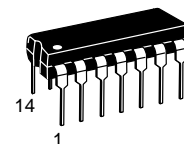
Symbol	Parameter		Min	Typ	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

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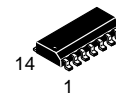
4-BIT SHIFT REGISTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



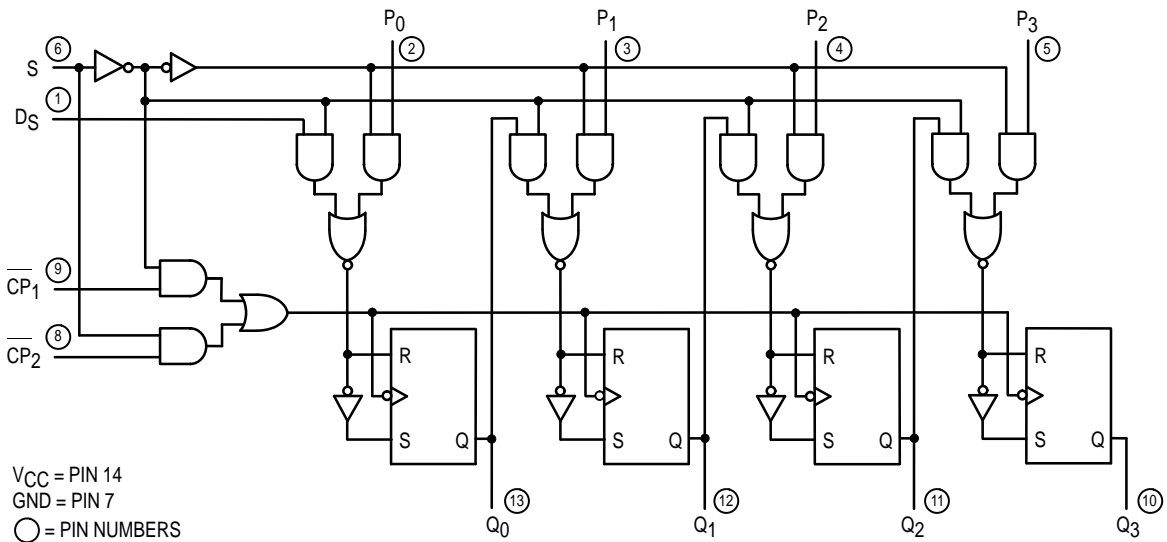
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

SN54/74LS95B

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0 – P_3) Data inputs and four Parallel Data outputs (Q_0 – Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs (CP_1) and (CP_2). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, CP_2 is enabled. A HIGH to LOW transition on enabled CP_2 transfers parallel data from the P_0 – P_3 inputs to the Q_0 – Q_3 outputs.

When the Mode Control input (S) is LOW, CP_1 is enabled. A

HIGH to LOW transition on enabled CP_1 transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2 , Q_2 to P_1 , and Q_1 to P_0 , and operating the LS95B in the parallel mode ($S = \text{HIGH}$).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while CP_2 is HIGH, or changing S from HIGH to LOW while CP_1 is HIGH and CP_2 is LOW will not cause any changes on the register outputs.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	CP_1	CP_2	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	\bar{L}	X	l	X	L	q_0	q_1	q_2
	L	\bar{L}	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	\bar{L}	X	P_n	P_0	P_1	P_2	P_3
Mode Change	\bar{L}	L	L	X	X	No Change			
	\bar{L}	L	L	X	X	No Change			
	\bar{L}	H	L	X	X	No Change			
	\bar{L}	H	L	X	X	Undetermined			
	\bar{L}	L	H	X	X	Undetermined			
	\bar{L}	L	H	X	X	No Change			
	\bar{L}	H	H	X	X	Undetermined			
	\bar{L}	H	H	X	X	No Change			

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Don't Care

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

P_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA, V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input HIGH Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				21	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency		25	36		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	CP to Output			18	27	ns	
				21	32	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _W	CP Pulse Width		20			ns	V _{CC} = 5.0 V
t _S	Data Setup Time		20			ns	
t _H	Data Hold Time		20			ns	
t _S	Mode Control Setup Time		20			ns	
t _H	Mode Control Hold Time		20			ns	

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DESCRIPTION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

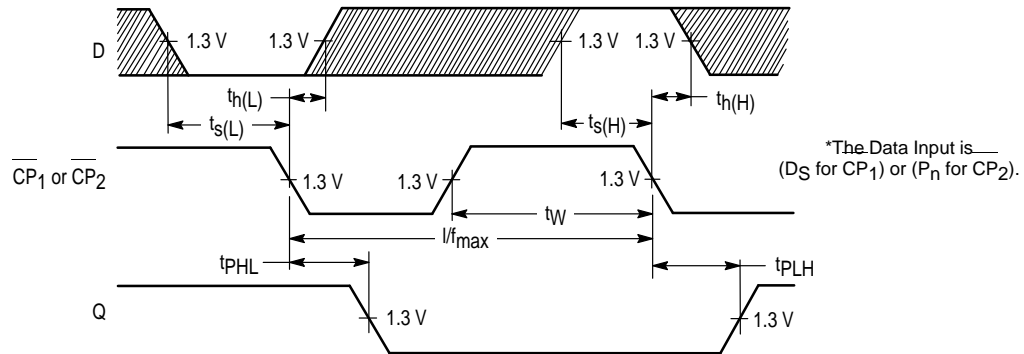


Figure 1

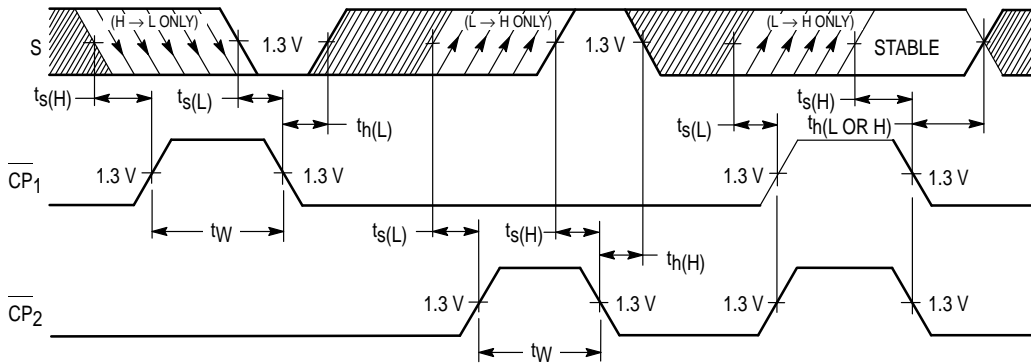


Figure 2