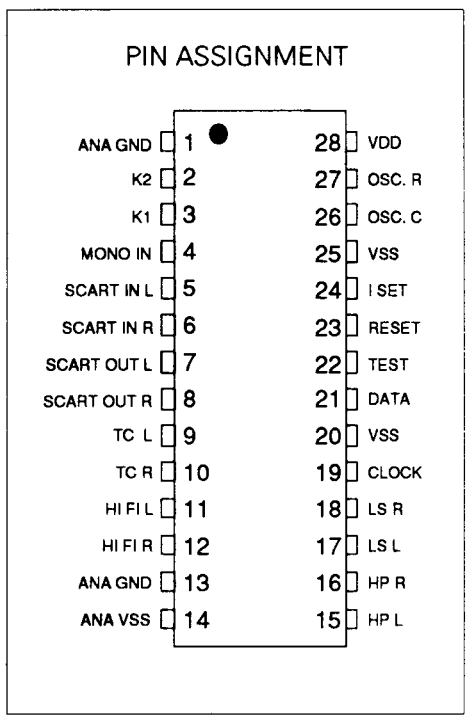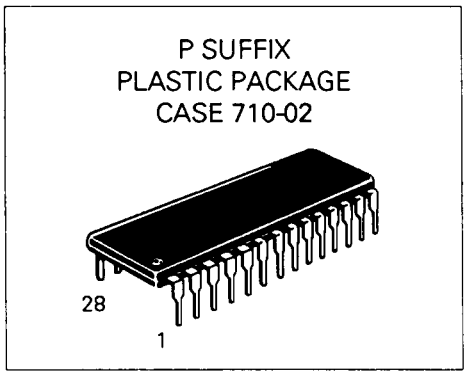**MOTOROLA**
SEMICONDUCTOR
TECHNICAL DATA

System 4 Stereotone
Single Chip TV Sound Control

MC44130

The Motorola MC44130 CMOS device provides, on a single chip, the sound system of the advanced TV SYSTEM 4. It has all the necessary functions for sound control required in a TV receiver for NICAM and SECAM as well as for the reception of stereo sound in German TV "standard transmission mode".

MAIN FEATURES:

- Part of Motorola System 4.

- Fully controlled through IIC Bus.

- Accepts base band dual carrier signals or NICAM decoded signals or SECAM decoded signals.

- "Pilot tone" demodulation and identification.

- Mono, Stereo and Dual Language processing.

- Maximum Stereo separation control.

- Volume, Treble and Bass control.

- Special effects: pseudo and extra wide stereo.

- Mute and separate power-on reset mute.

- Loudspeaker, Headphone, Hifi outputs.

- Independent left/right Volume Control on Loudspeaker and Headphone outputs.

- Peripheral (SCART) input/output.

- Mono Recorder Drive Capability.

P SUFFIX
PLASTIC PACKAGE
CASE 710-02

28

1

PIN ASSIGNMENT

ANA GND	1	28	VDD
K2	2	27	OSC. R
K1	3	26	OSC. C
MONO IN	4	25	VSS
SCART IN L	5	24	I SET
SCART IN R	6	23	RESET
SCART OUT L	7	22	TEST
SCART OUT R	8	21	DATA
TC L	9	20	VSS
TC R	10	19	CLOCK
HI FI L	11	18	LS R
HI FI R	12	17	LS L
ANA GND	13	16	HP R
ANA VSS	14	15	HP L

ORDERING INFORMATION

DEVICE	PACK
MC44130P	28 DIP

MOTOROLA

1

FUNCTIONAL DESCRIPTION

As shown in the internal block diagram below, the MC44130 combines all the following functions in a 28 pin DIP package with a minimum of external components:

- Pilot tone decoding.

- Baseband stereo signal decoding.

- Signal de-emphasis.

- Direct Balance adjustment via software (set-up).

- IIC Bus controlled routing of baseband/monaural/SCART inputs to Loudspeaker/Headphone/HIFI/SCART outputs.

- Loudspeaker output control (tone, extra effects, independent left/right volume control).

- Headphone output control (independent left/right volume control).

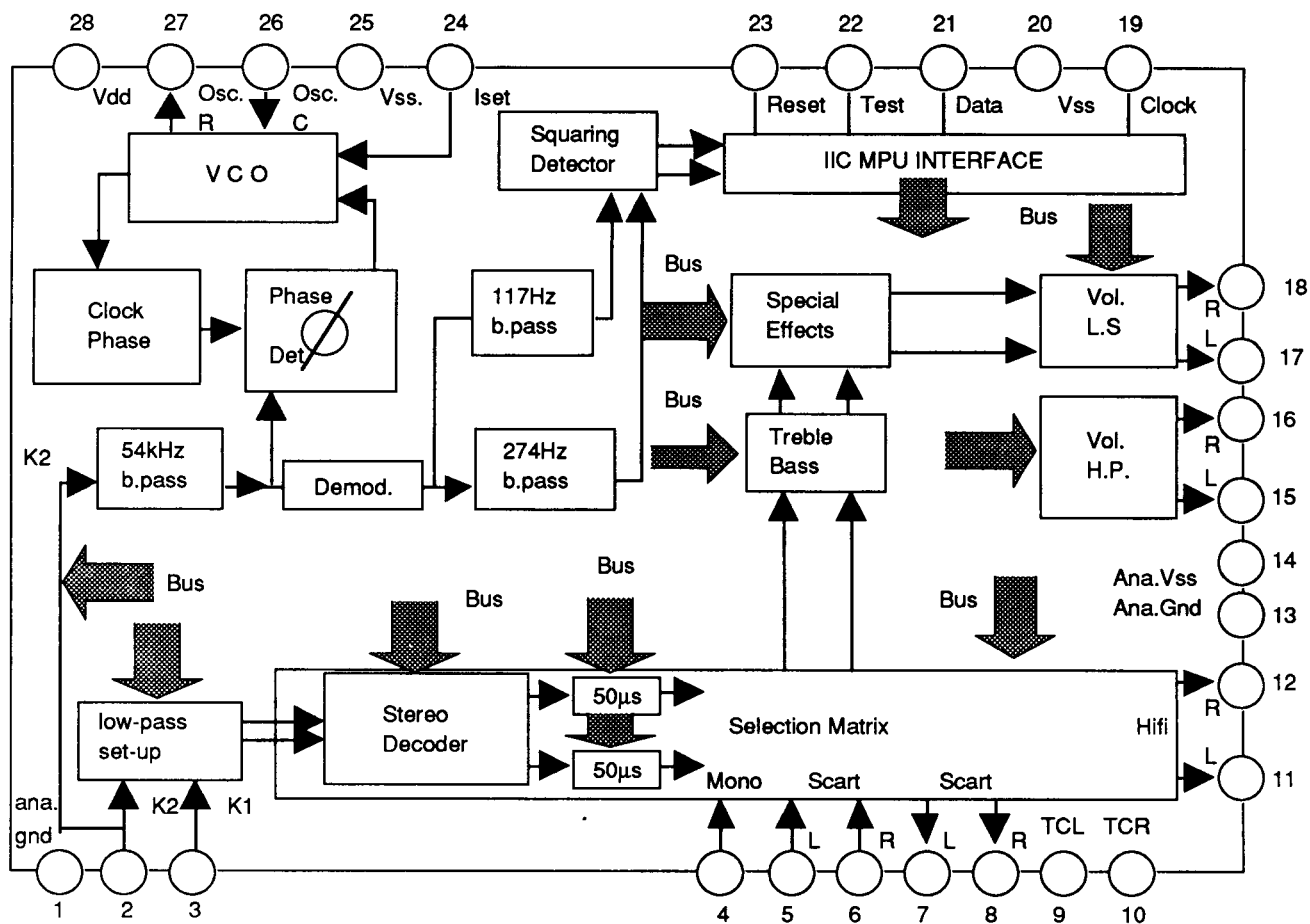- Re-creation of MONO output on SCART for Mono recorders.

Figure 1. Block diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC supply voltage	V_{DD}	-0.5 to 15	V
Operating Temperature range	T_A	0 to 70	°C
Storage Temperature	Tstg	-40 to +125	°C

ELECTRICAL CHARACTERISTICS

All tests used the circuit in Figure 2. The following conditions are assumed, unless stated otherwise.

- 1% accuracy resistors; resonator Murata CSB437F2 (fs=427 kHz, fp=464 kHz, Cstat at 1 kHz = 630 pF, Rs= 30 Ω); V_{DD} = 12 V, T_A = 25°C.

- Va amplitude is 500 mV rms, Va frequency is 1 kHz, Vr amplitude is 400 mV pp, Vr frequency is 1 kHz, Vp frequency is 54.6875 kHz with or without amplitude modulation.

- Values for subaddress, data and read bits are stated as hexadecimals.

- Treble/Bass: flat = subaddress 05 data 88.

- Volumes HP & LS : Maximum = subaddress 01, 02, 03, 04 data 00.

- K1, K2 Set-up: Mid range = subaddress 00, 07 data 20.

- Demute, matrix option 00, no special effects = subaddress 06 data 00.

- When switches are not mentioned, they are considered to be OFF.

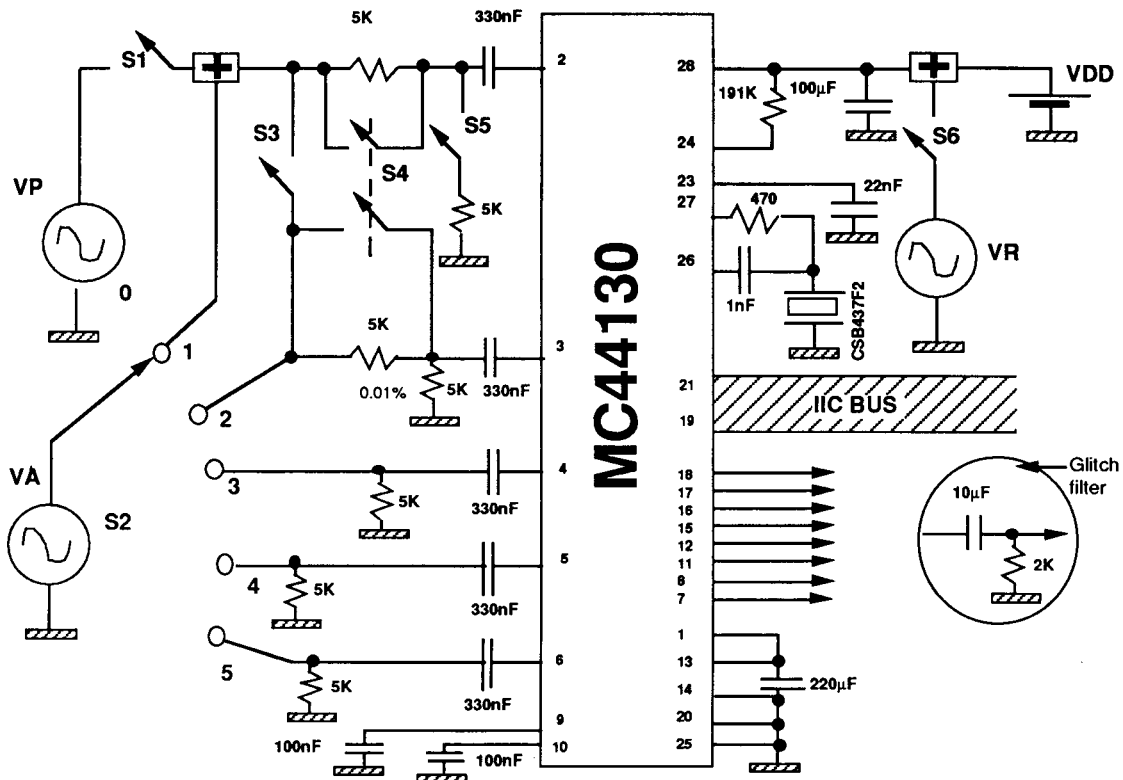- Pin 22 is not connected or is connected to Pin 20.

Figure 2. Device under test

POWER SUPPLY

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Power supply voltage	VDD	28		10.8	12	13.2	V
Power supply current	IDD	28			35	60	mA

OSCILLATOR

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Free running frequency	FOSC	27	Decoder and de-emphasis switched OFF (Table 2, Note 1).	430	437.5	450	kHz

CAPTURE RANGE

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Min pilot amplitude (without AM modulation)	LPA	2	Decoder and de-emphasis switched ON (Table 2, Note 1)		30	60	mV pp
Max pilot amplitude (without AM modulation) for lock in	HPA	2		500	600		mV pp
Capture range on pilot frequency	CRPF	2,27		2.2	2.7		kHz

IDENTIFICATION (See figures 3,4,5)

Read status byte   code 01 → AM modulation frequency = 117 Hz

code 10 → AM modulation frequency = 274 Hz

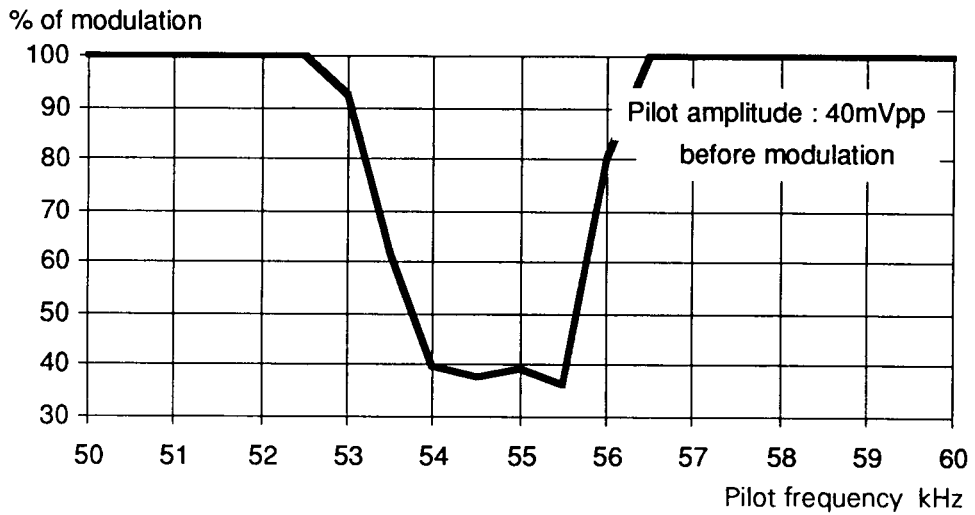| Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Min modulation	LMPA	2,27, 19,21	Pilot amplitude from 50 to 500 mV pp before AM modulation; decoder and de-emphasis ON (Table 2, Note 1)		30	40	%
Max Modulation				60			%

% of modulation

Figure 3: Identification

% of modulation

Figure 4: Identification

% of modulation
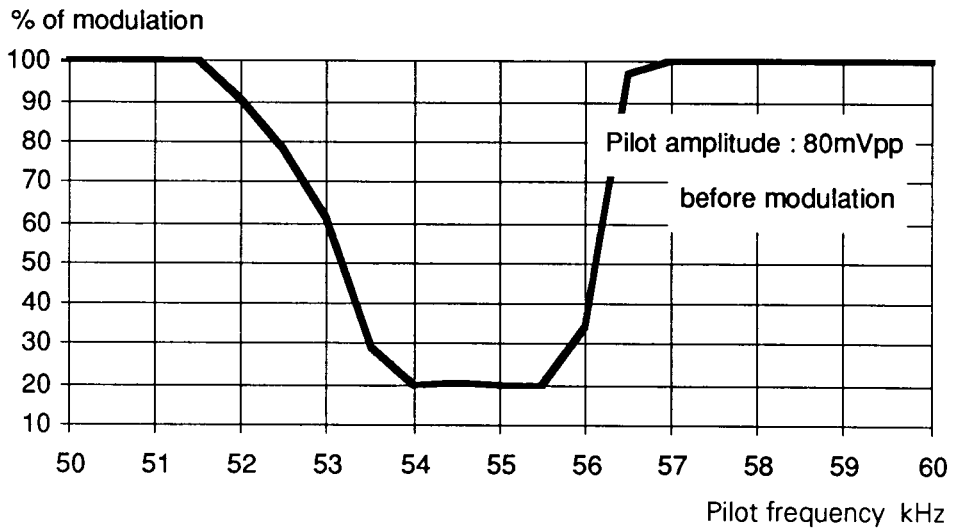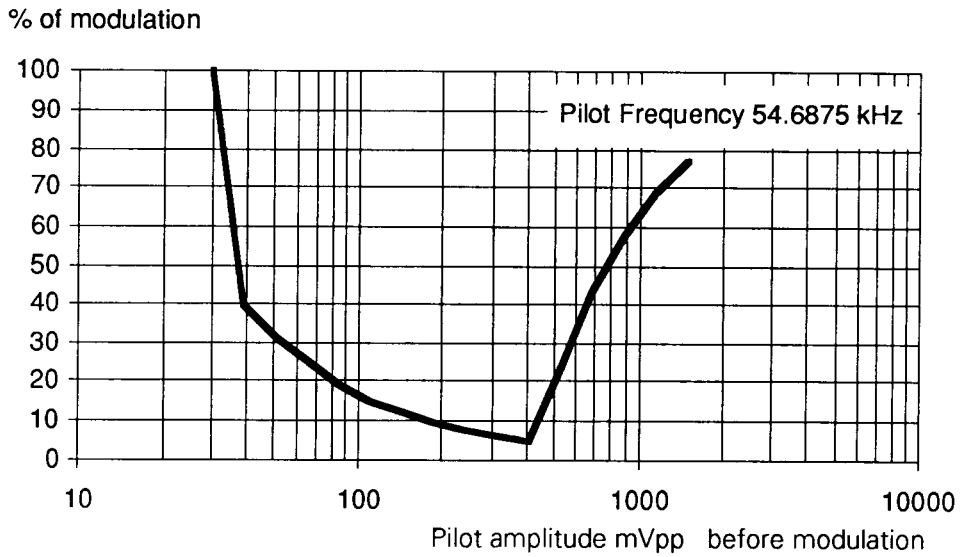

Figure 5: Identification

VOLUME CONTROLS

Left and right outputs may be balanced at any level to within half the step size by independent control of left/right attenuators.

HEADPHONE (See figures 6 and 7)

For these volume control tests, left and right channels are at the same setting. Subaddress 06 data 01, S2 = 4.

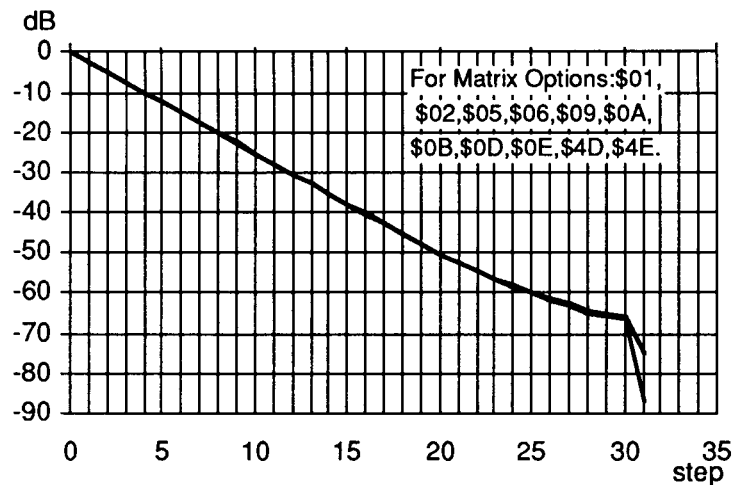| Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Step size from step 0 to step 25 (understood as decimal values)	HPSS	5, 15, 16	Subaddr. 03,04 Data n → Vout(n) Subaddr. 03,04 Data n+1 → Vout(n+1) HPSS=I20 log (Vout(n)/Vout(n+1))I	0	2.5	4.0	dB
Depth from step 0 to step 25	HPDP	5, 15, 16	Subaddr. 03,04 Data 00 → Vout(00) Subaddr. 03,04 Data 19 → Vout(19) HPDP=I20 log (Vout(0)/Vout(19))I	55	60	70	dB
Depth at step 30	HPDP	5, 15, 16	Subaddr. 03,04 Data 1E → Vout(1E) HPDP=I20 log (Vout(0)/Vout(1E))I	60			dB

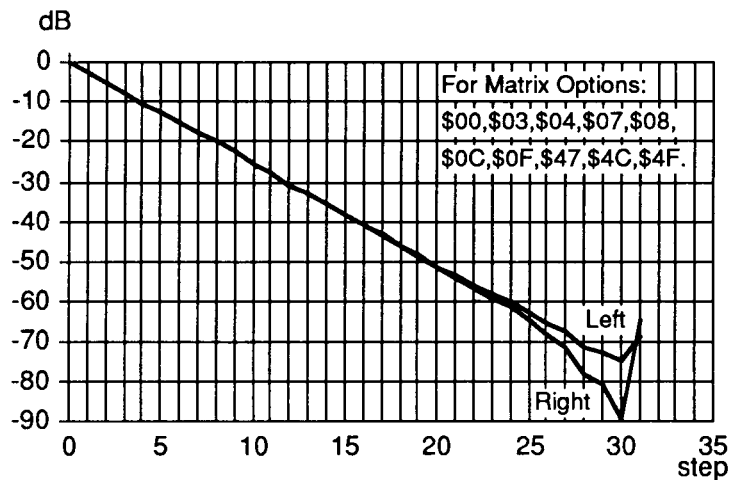**Figure 6: HP volume control**

Figure 7: HP volume control

LOUDSPEAKER (see figures 8 and 9)

For these volume control tests, left and right channels are at the same setting. Subaddress 06 data 01, S2 = 5.

| Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Step size from step 0 to step 50 (understood as decimal values)	LSSS	6, 17, 18	Subaddr. 01,02 Data n → Vout(n) Subaddr. 01,02 Data n+1 → Vout(n+1) LSSS=|20 log (Vout(n)/Vout(n+1))|	0	1.25	2.5	dB
Depth from step 0 to step 50	LSDL	6, 17, 18	Subaddr. 01,02 Data 32 → Vout(32) LSDL=|20 log (Vout(0)/Vout(32))|	55	60	70	dB
Depth at step 62	LSDL	6, 17, 18	Subaddr. 01,02 Data 3E → Vout(3E) LSDL=|20 log (Vout(0)/Vout(3E))|	65			dB
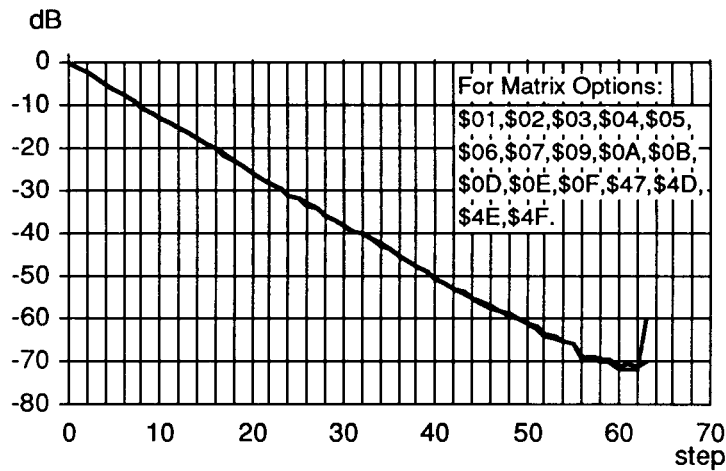
Figure 8: LS volume control
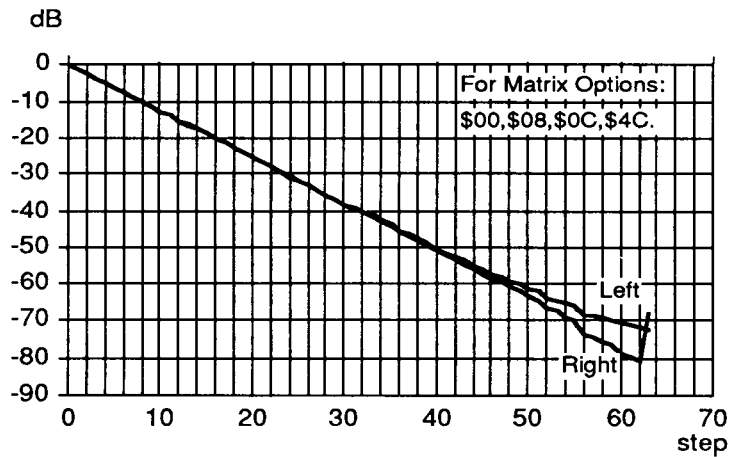
Figure 9: LS volume control

K1, K2 SET-UP CONTROL (see figures 10 and 11)

S2=2, S3=ON, S4=ON; Vout is measured on pins 7 and 8 for K1 and K2, respectively.

This set-up control may also be used to equalise gains in dual language mode.

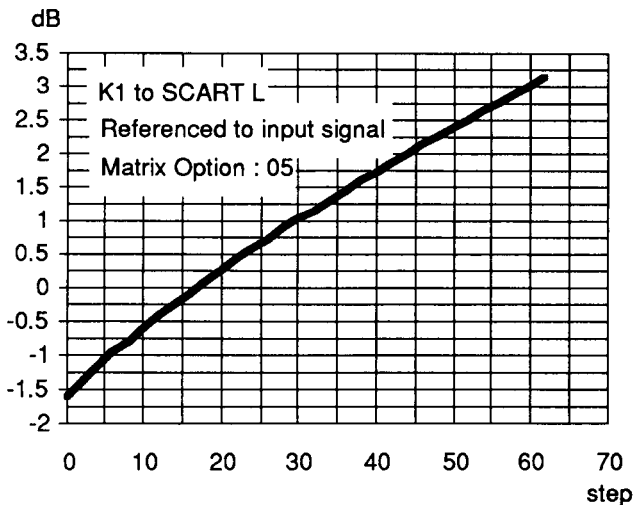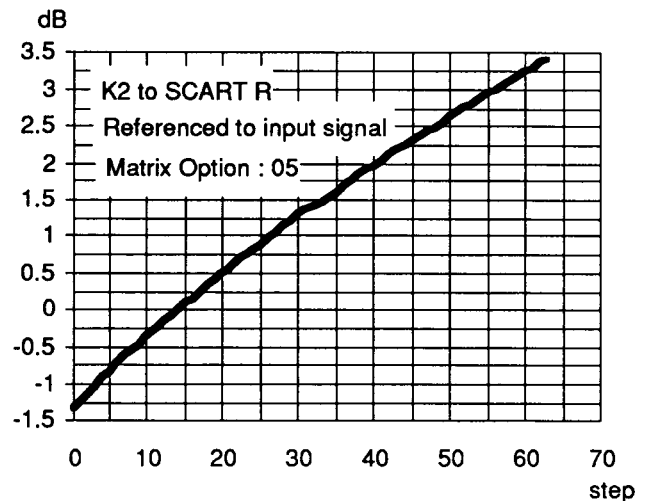| Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Control range	SUD	2,3,7 8	Subaddr. 06, data: 05 Subaddr. 00, 07, data: 3E, Vout(3E) Subaddr. 00, 07, data: 00, Vout(00) SUD = I20 log(Vout(3E)/Vout(00))I	3.5	4.5	5.5	dB
Step size K2	SSK2	2,3 8	Subaddr. 06, data: 05 Subaddr. 07, data: 00 ... 3F	0	0.1	0.2	dB
Step size K1	SSK1	2,3 7	Subaddr. 06, data: 05 Subaddr. 00, data: 00, 02 ... 3E	0	0.2	0.4	dB
Stereo separation set-up at K1/K2 mid.	SUSM	2,3,7, 8	Subaddr. 06, data: 00 Subaddr. 00, 07, data: 20 VoutL on pin 7, VoutR on pin 8 SUSM= I20 log(VoutL(20)/VoutR(20))I	20	40	–	dB
Stereo separation set-up optimized	SUSO	2,3,7, 8	Subaddr. 06, data: 00 Subaddr. 00, data: 20 Subaddr. 07, data: n SUSO= I20 log(VoutL(n)/VoutR(20))I	40	50	–	dB

Figure 10: K1 set-up control

Figure 11: K2 set-up control

DE-EMPHASIS

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
De-emphasis	DMP	2,3,7 8	Vp=50 mV rms, S1=ON, S2=1,2, S4=ON, S5=ON. Subaddr. 06, data: 05, Vout measured on pin 7,8. DMP= I20 log (Vout(200Hz)/ Vout(10kHz))I	9.8	10.3*	10.8	dB

* Corresponding to 50µs time constant (+/-7%; 46.5µs, 53.5µs)

TREBLE/BASS (See figures 12 and 13)

Subaddress 06, Data = 01, S2 = 5. Flat condition definition = Subaddress 05, data = 88 → Voutf

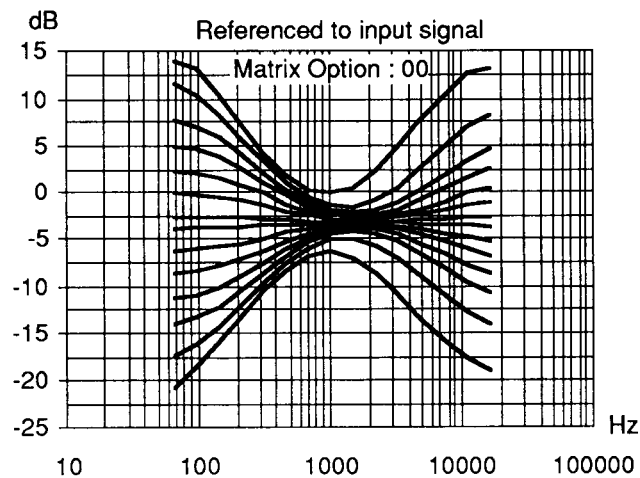| Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Flat condition variation	BSSL		From 100Hz to 10kHz			2	dB
Treble & bass range Range at 100 Hz	BRH	17,18	BRH= 20 log (Vout(8E)/Vout f) → max bass	+13	+16	+19	dB
	BRL	17,18	BRL= 20 log (Vout(81)/Vout f) → min bass	-19	-16	-13	dB
Range at 10 kHz	TRH	17,18	TRH= 20 log (Vout(E8)/Vout f) → max Treble	+13	+16	+19	dB
	TRL	17,18	TRL= 20 log (Vout(18)/Vout f) → min Treble	-19	-16	-13	dB
Maximum deviation at 1 kHz related to flat condition	DEV		Treble and bass min...max	-4		4	dB
Step size	STZ		Except for the 2 first and 2 last steps	0	-	4	dB

Figure 12: Treble/Bass Left
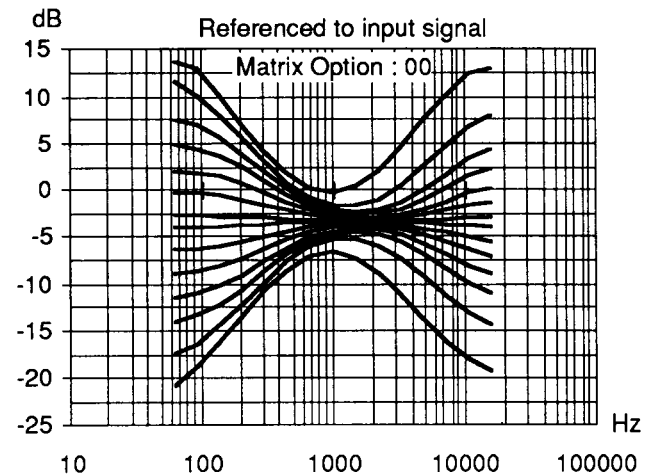
Figure 13: Treble/Bass Right

SPECIAL EFFECTS S2 = 4

PSEUDO-STEREO

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Frequency for 180° phase shift	FREO	5, 17, 18	Subaddr. 06 data 22 Input frequency Va for phase shift of 180° between Vout on pin 17,18 respectively.	1.2	1.25	1.4	kHz
Amplitude	PSA	5,18	Subaddr. 06 Data 02 : VoutN Subaddr. 06 Data 22 : VoutPS PSA=20 log (VoutPS/VoutN)I		0.1	0.6	dB
	VARI		For frequencies up to 15 kHz			3.0	dB

Extra-wide

Subaddr. 06 Data 00
  *Fva=300Hz
  -S2=4 output pin 17 : V300NL
  -S2=5 output pin 18 : V300NR
  *Fva=1kHz
  -S2=4 output pin 17 : VoutNL
  -S2=5 output pin 18 : VoutNR

Subaddr. 06 Data 10
  *Fva=300 Hz
  -S2=4 output pin 18 : VhpLR
  -S2=5 output pin 17 : VhpRL
  *Fva=1kHz
  -S2=4 output pin 17 : Vout LL
  -S2=4 output pin 18 : VoutLR
  -S2=5 output pin 17 : VoutRL
  -S2=5 output pin 18 : VoutRR

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Direct Gain left	LLA	5,6 17,18	LLA=(VoutLL/VoutNL)x100	110	120	130	%
Direct Gain Right	RRB	5,6	RRB=(VoutRR/VoutNR)x100	110	120	130	%
Left to Right CC	LRC	5,6 17,18	LRC=(VoutNRxVoutLR) x100/(VoutNLxVoutRR)	48	54	60	%
Right to Left CC	RLD	5,6 17,18	RLD=(VoutNLxVoutRL) x100/(VoutNRxVoutLL)	48	54	60	%
High Pass filter	HLPR	5,6 17,18	HLPR=20log((VoutLRxV300NL)/ (VoutNLxVhpLR))	2.8	3.2	3.6	dB
High Pass filter	HPRL	5,6 17,18	HPRL=20log((VoutRLxV300NR)/ (VoutNRxVhpRL))	2.8	3.2	3.6	dB

Extra-wide and pseudo-stereo

Fva = 1kHz; Subaddr. 06 Data 00, S2=4, output on pin 17:VspNL,
S2=5, output on pin 18:VspNR
Subaddr. 06 Data 30, S2=4, output on pin 17 : VspLL
and output on pin 18 : VspLR
S2=5, output on pin 17 : VspRL
and output on pin 18 : VspRR

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Left to Right CC	LRBT	5,6,17,18	LRBT=100(VspNRxVspLR)/(VspNLxVspRR)	32	37	42	%
Right to Left CC	RLBT	5,6,17,18	RLBT=100(VspNLxVspRL)/(VspNRxVspLL)	32	37	42	%

Insertion gain/loss

LIO is defined by LIO = 20 log (Vout/Vin). For matrix options 00 to 04, S2=2,4,5 and S3=ON, S4=ON.
For matrix options 05 to 0F, S2=1,2,4,5, S4=ON. For matrix options 47 to 4F, S2=3,4,5. See also Table 1.

Characteristics	Symbol	Pin	Input	Output	Min	Typ	Max	Units
Insertion Gain/Loss	LIO	2.3	K1/K2 (*)	Matrix options=03, 04,05,06,0B.				
		11,12		HIFI	-1		3	dB
		17,18		LS	-3		1	dB
		15,16		HP	-3		1	dB
				Matrix options = 07, 0F				
		11,12		HIFI	-2		2	dB
		17,18		LS	-5		-1	dB
		15,16		HP	-4		0	dB
				All matrix options (00 to 0F)				
		7,8		SCART	-1		3	dB
		4	AM MONO					
		11,12		HIFI (matrix option=47,4F)	-4		0	dB
		17,18		LS (matrix option=47,4F)	-7		-3	dB
		15,16		HP (matrix option=47,4F)	-6		-2	dB
		7,8		SCART (matrix option=47,4C,4D,4E,4F)	-3		+1	dB
		5,6	SCART					
		11,12		HIFI (matrix option = 00,01,02,08,09,0A,0C,0D,0E,4C,4D,4E).	-3		+1	dB
		17,18		LS (matrix option = 00,01,02,08,09,0A,0C,0D,0E,4C,4D,4E).	-6		-1	dB
		15,16		HP (matrix option = 00,01,02,08,09,0A,0C,0D,0E,4C,4D,4E)	-6		-1	dB

* For inputs on pins 2 & 3, values may be shifted by the set-up adjustment.

CROSS TALK

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Cross talk	XTLK	2,3,4 5,6,7,8 11,12 15,16 17,18	S2=1,2,3,4,5; S4=ON, S5=ON. For all switching matrix options : XTLK= I20 log (Vout/Va)I	60	-	-	dB

DISTORTION

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Distortion	DIST	2,3 4 5,6 7,8 11,12 15,16 17,18	For all selected matrix options, DIST is defined for each output by : DIST=100 X (Vharm/Vtot) where Vtot is measured on the output corresponding to the selected input (see S2 and the switching matrix table 1) with a low pass filter at 15 kHz and Vharm is measured on the same output with a high Q band pass filter from 2 kHz to 15 kHz.		0.2 0.4 *	0.5	% %

* Depending on matrix option

GLITCH

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Glitch on outputs when changing volume control	GLU	7,8,11, 12,15, 16,17, 18	S5=ON, use a first order RC high pass filter with a frequency cut-off of about 10 Hz as per Figure 5. For the first four steps : For the next four steps : For the remaining steps :	- - -	- - -	5 3 1	mV pp mV pp mV pp
DC level change when changing matrix option		7,8,11, 12,15, 16,17, 18		-	-	100	mV

OTHER PARAMETERS

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Analog Ground Polarisation *	VAGD	1,13	Vpin28=Vdd=12V Vpin14=Vpin20=Vpin25=Vss=0V Pin 1 and Pin 13 have to be connected together.	5	6	7	V
Input Output Polarisation *	VPOL	2,3,4 5,6 7,8 11,12 15,16 17,18	Force VAGD = Vdd/2 on pin 1 and pin 13 and measure VPOL(n) on each input and output pin.	5	6	7	V
Input and Output Impedance *			Force pins 1 and 13 to VAGD = Vdd/2 Force tested pin to VPOL(n) -0.1 V and measure the source current K(n) :				
	IKR	2,3	IKR(n) = 0.1/K(n)	25			kΩ
	IR	4,5,6	IR(n) = 0.1/K(n)	150			kΩ
	ORS	7,8	ORS(n)=0.1/K(n) except for matrix 03 and 0B.			1	kΩ
	ORA	11,12	ORA(n)=0.1/K(n)			200	Ω
		15,16	" "			200	Ω
		17,18	" "			200	Ω
Noise	NKST	7,8 11,12 15,16 17,18	S5=ON, Bandwidth 20Hz–15 kHz Matrix option Stereo Input K1 or K2	-	150	-	µV rms
	NKDM		Matrix option Dual or Mono or Nicam stereo Input K1 or K2	-	120	-	µV rms
	NLMS		Output LS Input Mono or SCART	-	90	-	µV rms
	NOMS		Output SCART & Input Mono or Output HiFi/HP & Inputs Mono/SCART	-	60	-	µV rms
	NVCT		Output LS volctrl step 24 Output HP volctrl step 12		5	-	µV rms
PSRR Power Supply Rejection	PSRR	15,16, 17,18, 28	S6=ON, Vout measured on each output PSRR = 20 log (Vout/Vr) - For LS outputs - For other outputs	-10 -30	-12 -40		dB dB

* This test measurement is done directly on the device without any external wiring and hardware, apart from a short circuit between pins 1 and 13

Note: output drive capability, when using the application circuit of Figure 16, is 1Vpp on 10 kΩ for all outputs.

FUNCTIONAL DESCRIPTION

Pilot Tone Decoding

The signal on the input K2, carrying AM modulated pilot signal for identification, passes through a high pass filter to remove the audio content. The signal is then demodulated using a PLL technique in which a VCO is synchronized to the 54kHz carrier. Using a synchronous demodulation, 117 Hz and 274 Hz signals are recovered indicating Stereo or Dual language transmission.

In the absence of the pilot tone carrier, the external ceramic resonator determines and sets the free running frequency of the PLL close to the value of 54.7kHz. In the NICAM transmission mode, the PLL is decoupled from the K2 input.
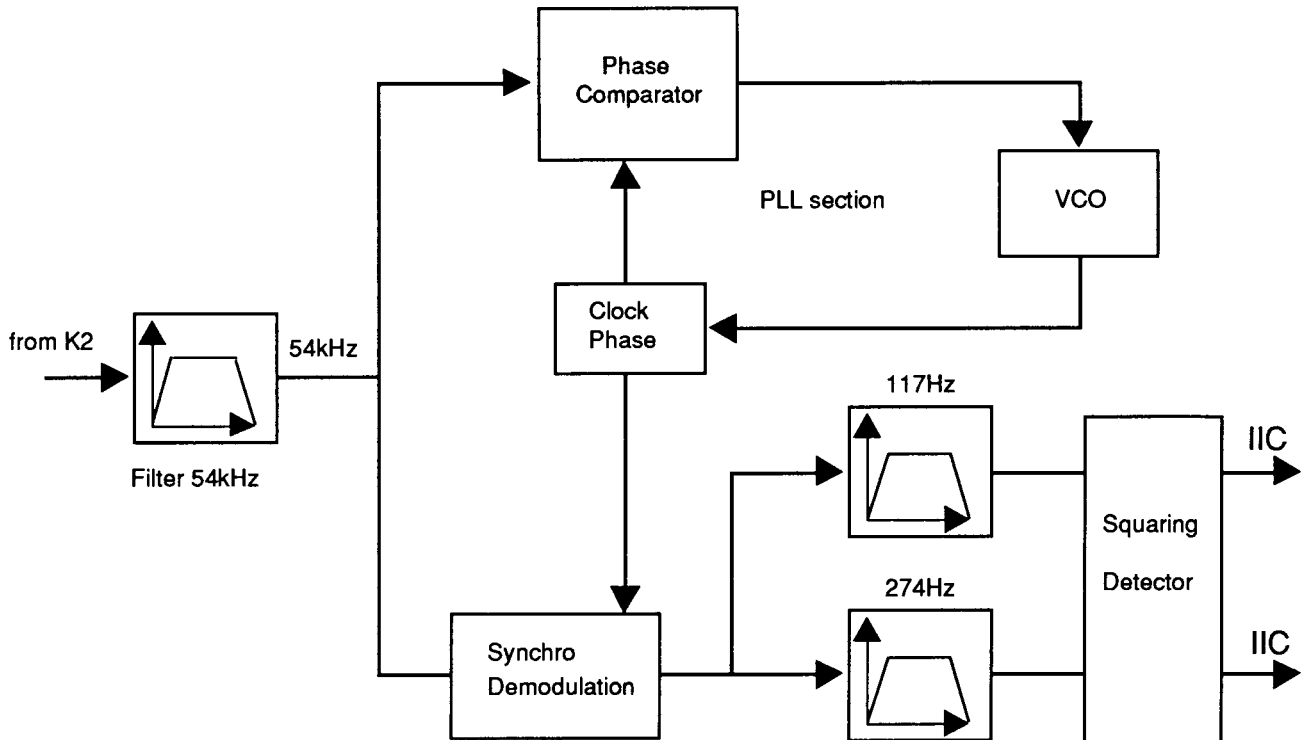
Figure 14. Pilot tone decoding

Audio Processing (German and SECAM mode)

Pins 2 and 3 are inputs for the two baseband signals K1 and K2 recovered by external demodulators. K1 contains the monocompatible 1/2 (L+R) information (or 1st language for dual sound) and K2 the R information (or 2nd language for dual sound) plus pilot tone. If mono transmission occurs, it is received on K1.

The mono pin 4, necessary for multistandard sets, inputs the baseband signal from an external demodulator (typically AM for L-transmission system) directly into the switching matrix without de-emphasis.

Stereo Decoding (German mode)

Before being processed, K1 and K2 signals have to be precisely balanced in order to optimize the stereo separation. Two independent and digitally adjustable networks allow input signal balancing. After being balanced these inputs are fed into the stereo decoder to produce the L information. Then the two channels are de-emphasised (50µs time constant) by independent networks, and fed to the switching matrix for routing.

NICAM Transmission

If NICAM transmission occurs, the decoder and de-emphasis are switched off, and the NICAM decoded signals are directly routed to the switching matrix.

Switching Matrix (see Table 1)

This selects the received and decoded mono, stereo, dual sound signals, or SCART inputs and switches them to one or more of the outputs. Selection is achieved by means of the IIC Bus interface.

For driving VCRs and HIFI sets, the signal is routed directly to the respective outputs. Input from a SCART can be routed to loudspeakers and/or headphones, while another SCART can record the broadcast in progress. (Caution: input from a SCART cannot be routed to the SCART outputs.)

A list of possible input/output combinations is shown in Table 1. Figure 15 shows the different routes from the inputs to the outputs.

Table 1. SWITCHING MATRIX

SELECTION CODE b efgh	HEXA CODE Note 4	Input					Ident Code	Output						Note
		MONO	K1	K2	SCART L	R		LS L	R	HP L	R	SCART L	R	
0 0000	00	–			L°	R°	01	L°	R°	L°	R°	L	R	
0 0001	01	–			1°	2°	01	2°	2°	1°	1°	L	R	
0 0010	02	–	(L+R)/2	R	1°	2°	01	1°	1°	2°	2°	L	R	
0 0011	03	–			–	–	01	L	R	L	R	M*	M*	2
0 0100	04	–			–	–	01	L	R	L	R	L	R	
0 0101	05	–	1	2	–	–	10	2	2	1	1	1	2	
0 0110	06	–	1	2	–	–	10	1	1	2	2	1	2	
0 0111	07	–	1	–	–	–	10	1	1	1	1	1	1	3
0 1000	08	–	1	2	L°	R°	10	L°	R°	L°	R°	1	2	
0 1001	09	–	1	2	1°	2°	10	2°	2°	1°	1°	1	2	
0 1010	0A	–	1	2	1°	2°	10	1°	1°	2°	2°	1	2	
0 1011	0B	–	1	2	–	–	10	2	2	1	1	2	2	
0 1100	0C	–	M	–	L°	R°	00	L°	R°	L°	R°	M	M	1
0 1101	0D	–	M	–	1°	2°	00	2°	2°	1°	1°	M	M	1
0 1110	0E	–	M	–	1°	2°	00	1°	1°	2°	2°	M	M	1
0 1111	0F	—	M	–	–	–	00	M	M	M	M	M	M	3
1 0111	47	Mn	–	–	–	–	–	Mn	Mn	Mn	Mn	Mn	Mn	3
1 1100	4C	Mn	–	–	L°	R°	–	L°	R°	L°	R°	Mn	Mn	
1 1101	4D	Mn	–	–	1°	2°	–	2°	2°	1°	1°	Mn	Mn	
1 1110	4E	Mn	–	–	1°	2°	–	1°	1°	2°	2°	Mn	Mn	
1 1111	4F	Mn	—	—	–	–	–	Mn	Mn	Mn	Mn	Mn	Mn	3

Remarks on Table 1

- To output HIFI the same input is fed as to output LS.

- L & R are the left/right channel information of a stereo transmission.

- 1 & 2 are the first/second language signals.

- 1° & 2° are first/second language signals applied to the SCART inputs.

- Mn signifies an amplitude modulated signal without preaccentuation.

Notes

1 If the ID. CODE is "11", this option can also be accepted.

2 M* is the de-emphasized signal of K1, generated in this way:

   (L+R)/2 & R → L & R → De-emphasis → (L+R)/2 = M*

3 Selection codes having efgh = 0111 and efgh = 1111 are equivalent. Codes 07 and 47 should not be used; in a future design, they may route K2 to all outputs.

4 With c = d = 0
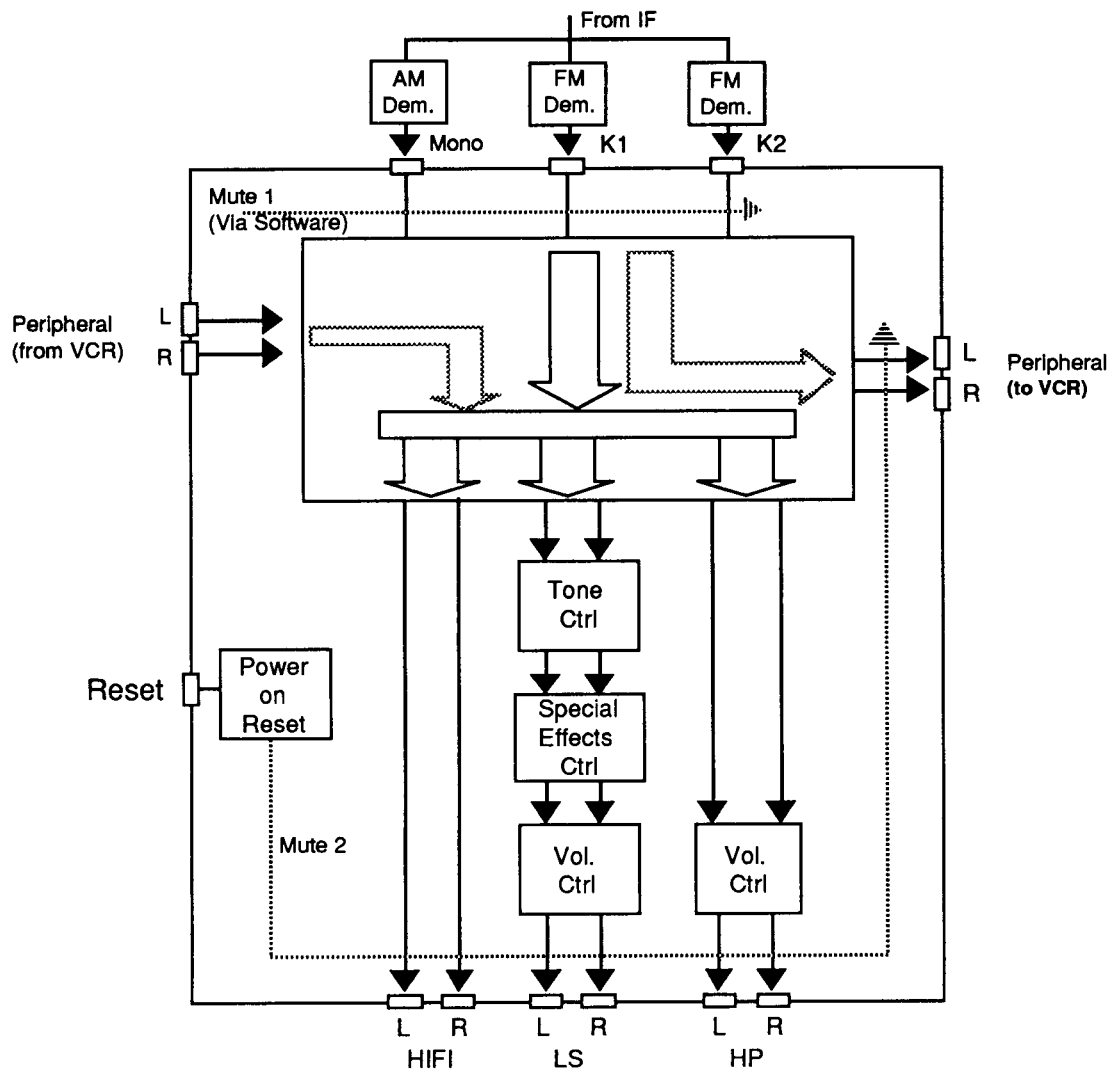
Figure 15. Input/Output Combinations

LOUDSPEAKER OUTPUT

Tone Control

Treble and bass are controlled in 14 steps from min. to max. using a 4-bit word for each. Signal alterations are identical on both channels and are realized by variable switched capacitor filters providing very low characteristic dispersion.

Volume Control

Volume control is realized by two independent attenuators controlled by two 6-bit words, one for the left channel and one for the right. This gives up to 50 equal control steps which is sufficiently fine to sound like a smooth continuous analog control. A balance control is easily implemented by altering, via software control, the left and right channel data.

Pseudo Stereo

Upon a one-bit control this function is either "on" or "off". The effect is to create, from a mono signal, an apparent stereo effect by altering the signals. The left channel is the original mono signal, while the right channel is a mono signal to which is added a frequency dependent time delay (2 poles delay with asymptotes to 627µs at DC; the phase shift is nearly 180° at 1kHz).

Extra-wide Stereo

Upon a one-bit control this function is also either "on" or "off". It causes an apparent increase of the stereo separation using the technique of cross coupling the left and right channels in antiphase. Since a zero separation (mono) input signal would be entirely cancelled in each channel, it is necessary to limit the percentage of cross coupling (60%) and increase the channel gain to prevent a change in volume. When sourced with pseudo-stereo operation, the cross coupling is reduced to 40%. Low frequency feedback is rolled off.

HEADPHONE OUTPUT

This route has independent volume controls realized in the same manner as for the loudspeaker output, but the dynamic range is performed with 31 steps (5-bit words).

SCART OUTPUT

As shown in table 1, SCART output may receive left or right channel information when stereo transmission occurs, or to support mono recorders, a re-constructed de-emphasized mono signal.

In dual mode transmission it can be switched to both languages. Note that the SCART input cannot be routed to the SCART output.

MUTE

All three input pins (K1 - K2 - mono) have muting gates which are controlled by the bus (Mute 1) (see Figure 15). All four output routes (loudspeakers, headphones, SCART, HIFI) also have muting gates (Mute 2) which are operated by the reset pin as follows:

- to enable mute 2: reset the power or, during normal operation, make reset pin (23) = low.

- to remove mute 2: let reset pin go high and address the chip through the bus. Demuting occurs with the first start or stop condition on the IIC Bus which follows a Chipaddress + Subaddress. Demuting should not occur until the reset pin is high, i.e. after about 100ms. We recommend addressing and loading all registers before demuting Mute 2.

Note that SCART input is not muted.

BUS CONTROL

The Stereotone I.C. is digitally controlled by using the MOTOROLA two wire serial bus (IIC compatible). A simple description is given in appendix A, with emphasis on the word structure. The MOTOROLA Bus electrical specification is given in Figure 19.

Details of the Stereotone Bus operation are as follows:

- The chip address is 1 000 000 Y, where Y is read/write bit (R/W).

- There are 8 subaddresses available to control volumes, treble-bass, set-up and decoder-de-emphasis switching, and to select switching matrix options

- Two flag bits representing the actual sound mode can be read by the master.

Table 2 shows function subaddresses and data definitions. Some communication protocols to be used follow.

Table 2: STEREOTONE M-Bus Protocol (Note: X = Don't care)

Function	Subaddress	Data
Level Set-up K1 Decoder & Deemphasis switch	XXXXX000	(Note 1)
Level Set-up K2	XXXXX111	XX000000<= gain => XX111111
Volume, left speaker	XXXXX001	XX000000<= volume =>XX111111 (Note 2)
Volume, right speaker	XXXXX010	XX000000<= volume =>XX111111 (Note 2)
Volume, left headphone	XXXXX011	XX000000<= volume =>XX111111 (Note 2)
Volume, right headphone	XXXXX100	XX000000<= volume =>XX111111 (Note 2)
Treble/Bass	XXXXX101	0001XXXX<= treble =>1110XXXX XXXX0001<= bass =>XXXX1110 Flat response 10001000
Selection matrix + Special Effects	XXXXX110	Mute 1 : 1XXXXXXX Not muted 1: 0XXXXXXX
Special Effects		XX00XXXX No special effect XX10XXXX Pseudo stereo XX01XXXX Extra-wide stereo XX11XXXX Both effects
Matrix Select		XbXXefgh (See Table 1)

Note 1: Level set-up K1 + decoder & de-emphasis data XX12345Y, a 6-bit word.
        The word XX00000Y corresponds to minimum gain (0.707x).
        The word XX10000Y corresponds to midrange gain (1.0x)
        The word XX11111Y corresponds to maximum gain (1.414x)
IMPORTANT: bit Y = 0 switches ON decoder & de-emphasis; bit Y = 1 switches it OFF.

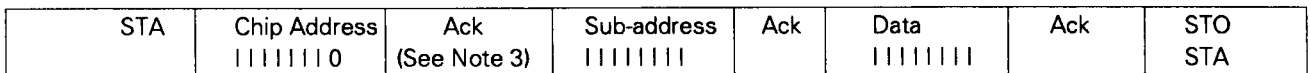Note 2: Performance is guaranteed only between:
        XX000000 and XX110010 for LS
        XX000000 and XXX11001 for HP
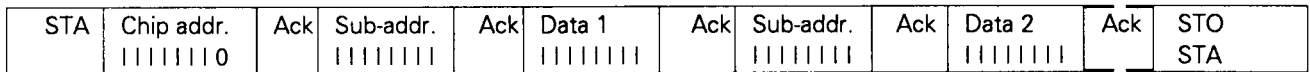   See also Figures 16 to 19.

Communication Protocols

-Write one Byte

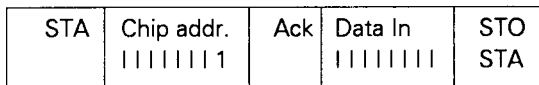| STA	Chip Address	Ack	Sub-address	Ack	Data	Ack	STO
	I I I I I I 0	(See Note 3)	I I I I I I I		I I I I I I I		STA

Note 3: The acknowledge flag is composed of one bit, and is generated by the MC44130, which pulls down the data line during one clock pulse (see Appendix A).

-Write N Bytes

STA	Chip addr.	Ack	Sub-addr.	Ack	Data 1	Ack	Sub-addr.	Ack	Data 2	Ack	STO
	I I I I I I 0		I I I I I I I		I I I I I I I		I I I I I I I		I I I I I I I		STA

Ack. for byte n

- Read Status Byte

STA	Chip addr.	Ack	Data In	STO
	I I I I I I 1		I I I I I I I	STA

X Y

With   X   Y
0   0   MONO
0   1   STEREO
1   0   DUAL LANGUAGE

APPLICATION

The MC 44130 has been designed to offer many high performance features and to realize maximum component and board savings for TV receivers. The typical application circuit is very simple as per Figure 16.

Software Considerations

The stereotone I.C. can be driven with great flexibility. Its internal registers are purely static and therefore updating can be realized at any rate.

Software Functions

The balance function is easily achieved by modifying the left and right volume control registers in opposite directions. Specific total volume compensation can be realized by special software using the TV set's non-volatile memory to store normalized balance if the user's ears are not equally sensitive.

Loudness control, boosting bass and treble when volume is low can be realized, upon fixed or variable patterns, by software relationships between volume and tone control words.

Pilot tone status display: as this data is permanently read by the MCU, software can easily make the latter drive the TV set's LED display; therefore there is no need for the Stereotone to drive any further LED to provide the viewer with this data.

A simple filtering program can be added to the currently used software program to improve identification when the signal delivered to inputs K1/K2 is very noisy.
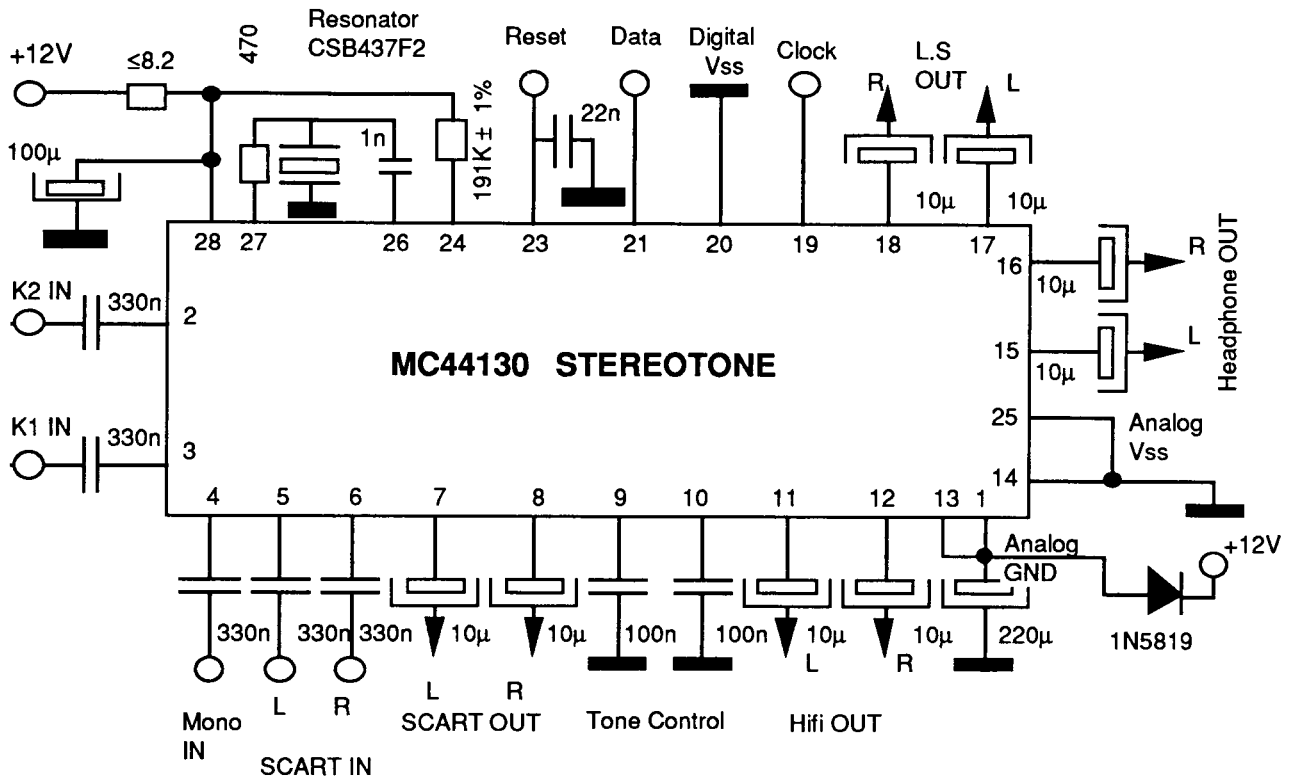
Figure 16. Typical Stereotone application

IIC Bus Control

The Bus System

This two wire serial bus system consists of the data line (DATA) and the clock line (CLOCK).

- One line is called SDA and carries the Data.
- One line is called SCL and carries the clock.

When the bus is free, both lines are "high". Both the SDA line and the SCL line are connected to a positive supply voltage via a pull-up resistor. The output stages of a device to be connected to the data line must have an open drain (or collector) in order to perform the wired-AND property.

1. Bit Transfer

There is one clock pulse per data bit. The data on the SDA line must be stable during the high period of the clock pulse. When data transmission occurs, the data line is only allowed to change state when the SCL line is low. In a transmission, the most significant bit is transmitted first.

2. Start and Stop conditions

The start and stop conditions respectively initiate and terminate the transfer of data on the bus. The SDA line is only allowed to change during the time when the SCL line is high to accomplish Start or Stop conditions (see Figure 17).

A high to low transition of the SDA line, while SCL is high, is a unique situation defined as the Start condition.

A low to high transition of the SDA line, while SCL is high, is a unique situation defined as the Stop condition.

Every receiver must reset its Bus logic on the reception of a Start condition. (See Figure 17).
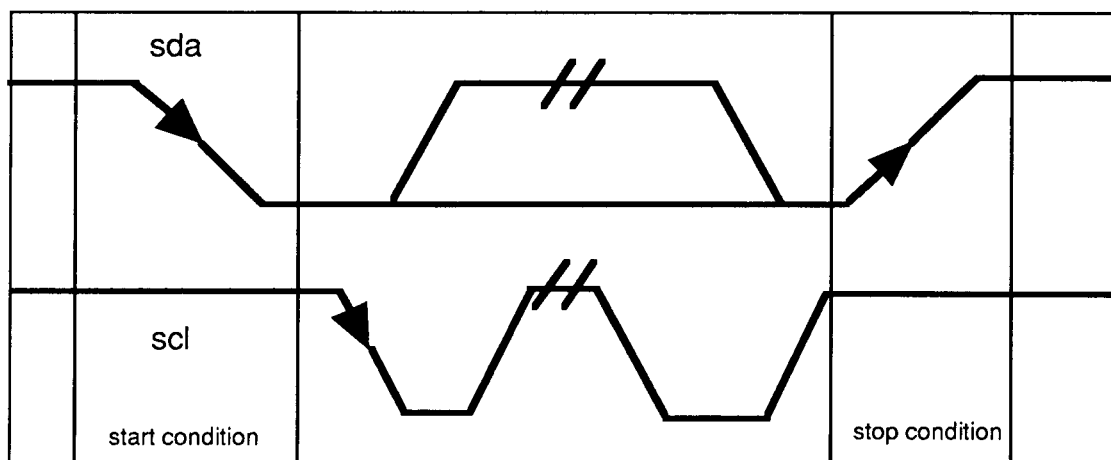
Figure 17. Start/Stop conditions

3. Acknowledge

IC's on the Bus are designated as "MASTERS" or "SLAVES" each of which can transmit and receive data. All clock timing, start and stop conditions must be generated by a master, normally an MPU.

The Stereotone is a slave transceiver, meaning that it cannot initiate a data transfer, but is capable of both receiving and transmitting data.

Each byte is followed by one acknowledge bit. During an acknowledge bit the master lets the data line go high.

A device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse.

Under normal conditions, a slave receiver which has been addressed is obliged to generate an acknowledge after the reception of each byte. When the slave transmits, the master receiver must signal an end of this mode by not generating an acknowledge after the last byte. Then the slave leaves the data line high to enable the master to generate a Stop condition.

The master may also signal an end of the read mode by generating a stop or a start condition during clock "high period" which does not correspond to a bit dedicated data transmission (7th & 8th bit).

4. Addressing/Data transfer

Data transfer is effected in 9-bit words (see Figure 18).

The Start condition can be seen first, it causes all receivers on the Bus to reset.

The addressing procedure is such that the first byte determines which slave has been selected by the master (chip address).

The chip address byte consists of a 7-bit slave address (MSD first), plus a R/W bit which is "0" if the master intends to transmit data and "1" if it intends to receive data.

The 7-bit address is a property of the slave.
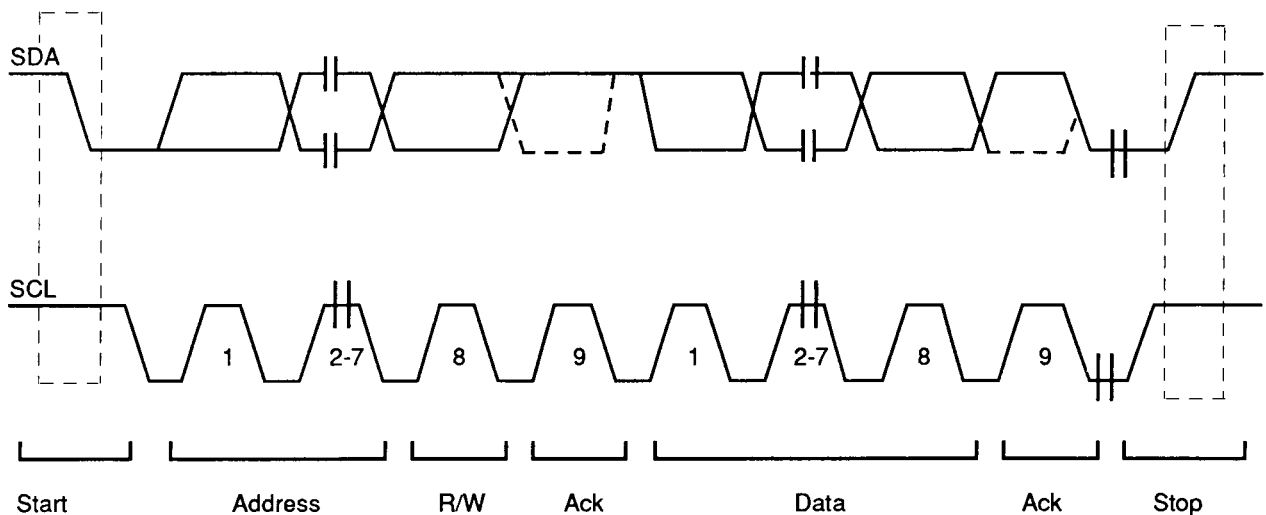
Figure 18. Data transfer on the Bus

Every slave on the Bus reads this byte, but only the one with the corresponding address acknowledges, by pulling down the data line. In other words, this indicates the master that the selected slave has recognized that it is being addressed and is ready to receive or transmit data as appropriate.

Now, the address byte is followed by one or more subadress data bytes (MSB first), from the transmitting I.C. Finally the stop condition is generated by the master at the end of each data transfer.

Note that a stop condition is not required to let data transmission restart.

For Motorola Bus electrical specification, see figure 19.
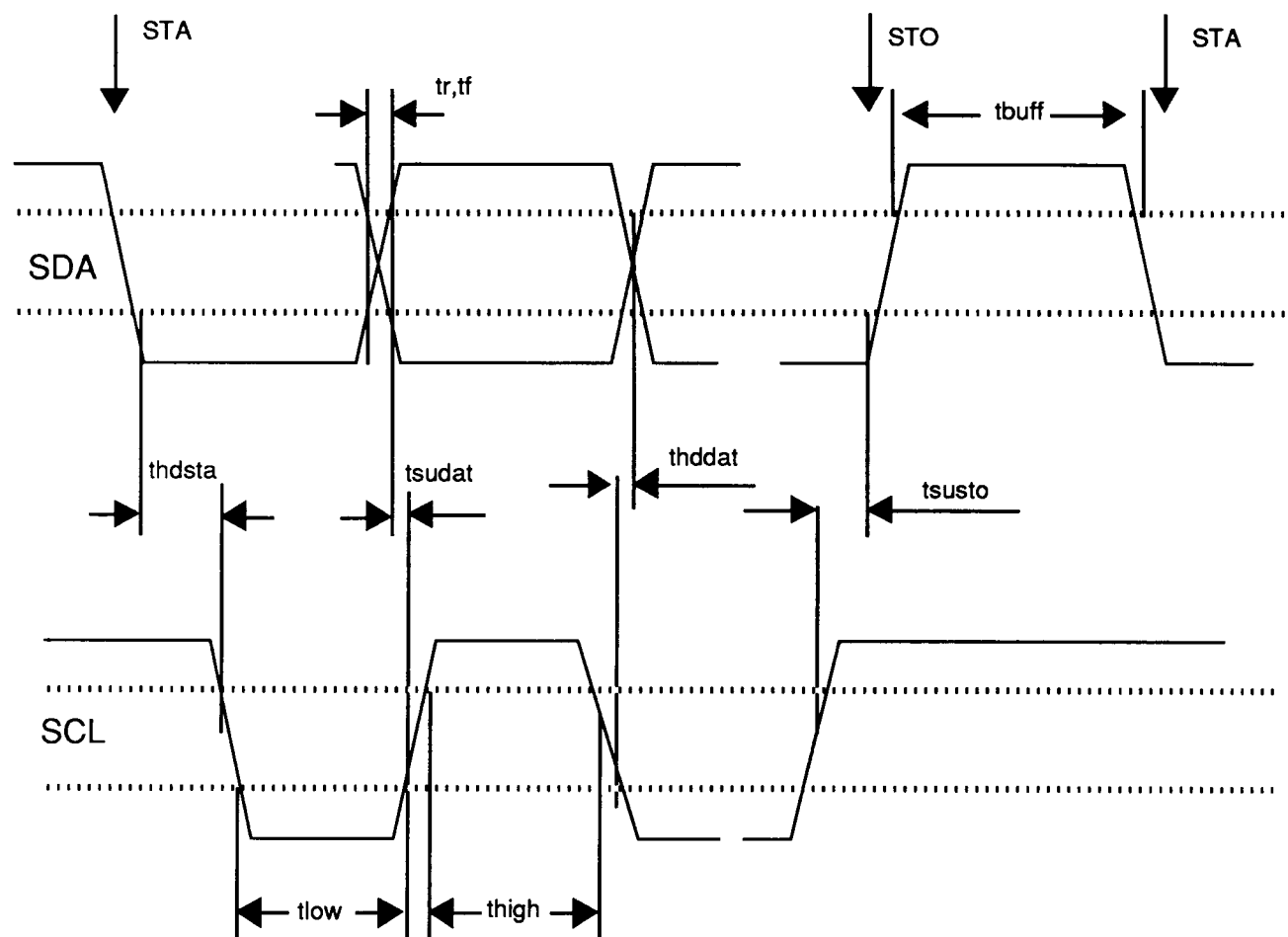
VOL	max. output low voltage	0.4V		tsusto	hold time stop control	>4µs
VIH	min. input high voltage	3.0V		thddat	hold time for data	> 0
VIL	max. input low voltage	1.5V		tsudat	set up time for data	>250µs
tbuf	bus free time	>4µs		tr	raise time for clock and data	<1µs
tlow	clock low period	>4µs		tf	full time for clock and data	<300ns
thigh	clock high period	>4µs		fmax	max.bus speed	100kHz
thdsta	hold time start control	>4µs				

Figure 19. BUS timing specification

CASE 710-02
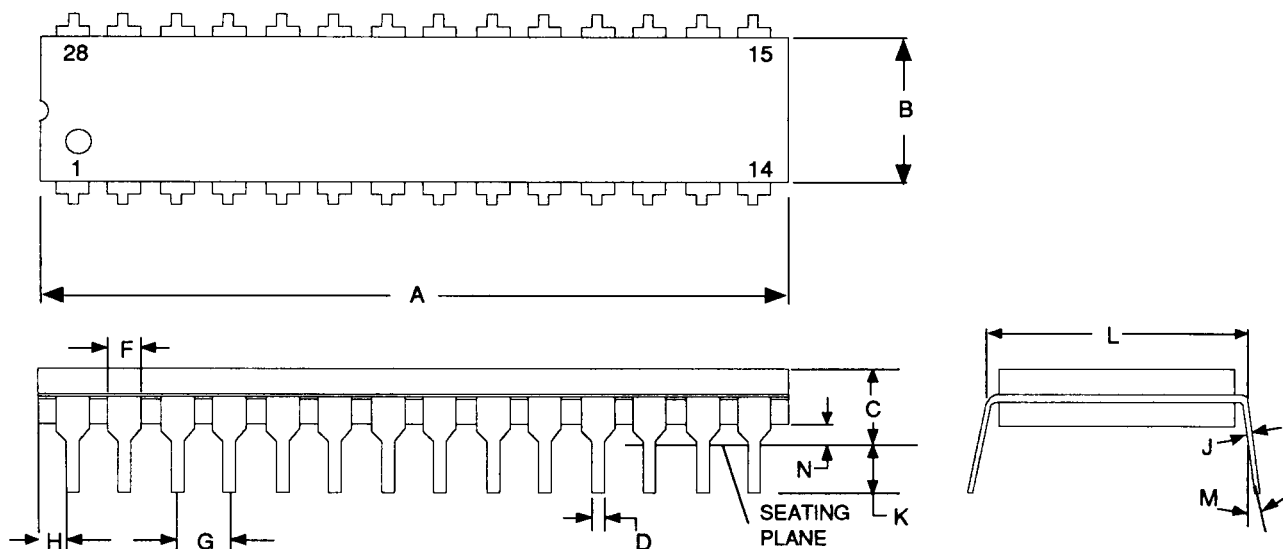
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.540	0.560
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		2.54 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D) SHALL BE WITHIN 0.25 MM (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STD 710-02.

(M) MOTOROLA

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