Integrated Device Technology, Inc.

VERY LOW POWER 3.3V CMOS FAST SRAM 256K (32K x 8-BIT)

PRELIMINARY INFORMATION IDT713256SL

FEATURES

- Ideal for 16/32-bit notebook/sub-notebook cache at 20, 25, and 33MHz, and for other battery-operated equipment
- Very low standby current (maximums):
  - — 3.0mA standby
  - — 500uA full standby
- Fast access times:
  - — 20/25/30ns
- Battery-backup operation: 2V data retention
  - — 300uA data retention current (max.)
- Small package for space-efficient layouts:
  - — 28-pin 300 mil SOJ
- Ideal configuration for large cache sizes, with minimum space and minimum power:
  - — 32K x 8
- Produced with advanced high-performance CMOS technology
- Input and output are TTL-compatible
- Single 3.3V(±0.3V) power supply

DESCRIPTION

The IDT713256SL is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

The IDT713256SL has outstanding low power characteristics, as well as fast speeds.

Address access times of 20, 25, and 30ns are ideal for 16 and 32-bit notebook and laptop cache designs running at 20, 25, and 33MHz, and operating from 3.3 volts. For instance, two of these SRAMs interface directly to many 386 notebook cache controllers to form a 64kB cache. Portable communications and test equipment benefit from these fast speeds and low power too.

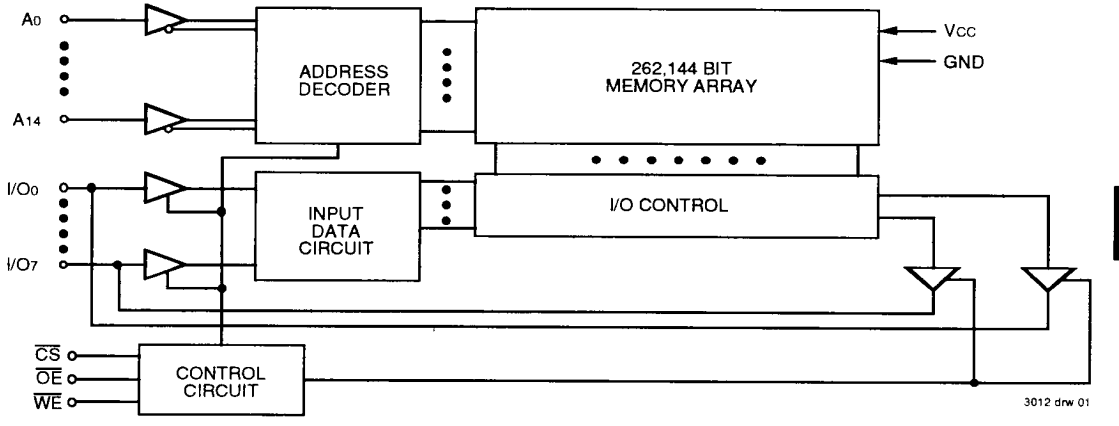
When the power management logic puts the IDT713256SL in standby mode, its very low power characteristics contribute to extended battery life.

When $\overline{CS}$ goes HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains HIGH. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less than 1.65mW and typically will be much smaller.

This SRAM also offers battery-backup data retention at as little as 2 volts. Under this condition, power consumption is guaranteed not to exceed 1.0mW and typically will be much smaller.

The package chosen for this device, 28-pin 300mil SOJ, helps the designer attain the stringent space goals typical of notebooks, sub-notebooks, and battery-operated portable equipment.

FUNCTIONAL BLOCK DIAGRAM



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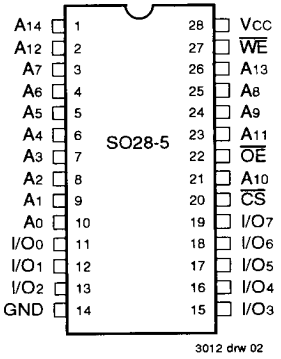
PIN CONFIGURATIONS



3012 drw 02

SOJ
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

3012 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	V_{HC}	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE: 3012 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to VCC+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3012 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals only
3. Input, Output, and I/O terminals; 4.6V maximum

CAPACITANCE (T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3012 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3012 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3012 tbl 06
1. V_{IL} (min.) = –1.0V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 3.3V ± 0.3V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	713256SL20 Com'l.	713256SL25 Com'l.	713256SL30 Com'l.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	SL	95	90	85	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ = V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	SL	3	3	3	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	SL	0.5	0.5	0.5	mA

3012 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only address inputs cycling at fmax; f = 0 means that no inputs are cycling.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3012 tbl 08

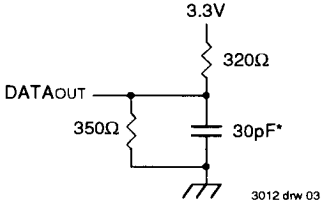


Figure 1. AC Test Load

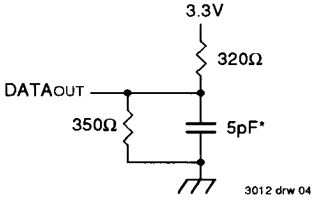


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V± 0.3V

Symbol	Parameter	Test Condition	IDT713256SL Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

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DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

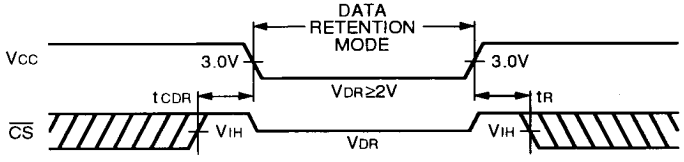
V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition	Min.	Typ. [1] Vcc @ 2.0v	Max. Vcc @ 2.0V	Unit
V_{DR}	VCC for Data Retention	—	2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	—	—	300	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
t_R[3]	Operation Recovery Time		t_{RC}[2]	—	—	ns

3012 tbl 10

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



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AC ELECTRICAL CHARACTERISTICS (Vcc = 3.3V ± 0.3V, ALL TEMPERATURE RANGES)

Symbol	Parameter	713256SL20		713256SL25		713256SL30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	20	—	25	—	30	—	ns
tAA	Address Access Time	—	20	—	25	—	30	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	ns
tCLZ	Chip Select to Output in Low-Z[1]	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	10	—	13	ns
tOLZ	Output Enable to Output in Low-Z[1]	3	—	3	—	3	—	ns
tCHZ	Chip Select to Output in High-Z[1]	0	10	0	11	0	13	ns
tOHZ	Output Disable to Output in High-Z[1]	2	8	2	10	2	13	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
Write Cycle								
tWC	Write Cycle Time	20	—	25	—	30	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	25	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	15	—	25	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z[1]	1	10	1	11	1	13	ns
tDW	Data to Write Time Overlap	8	—	10	—	13	—	ns
tDH1	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time ($\overline{CS}$)	0	—	0	—	0	—	ns
tOW	Output Active from End-of-Write[1]	5	—	5	—	5	—	ns

NOTE:
1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

3012 tbl 11

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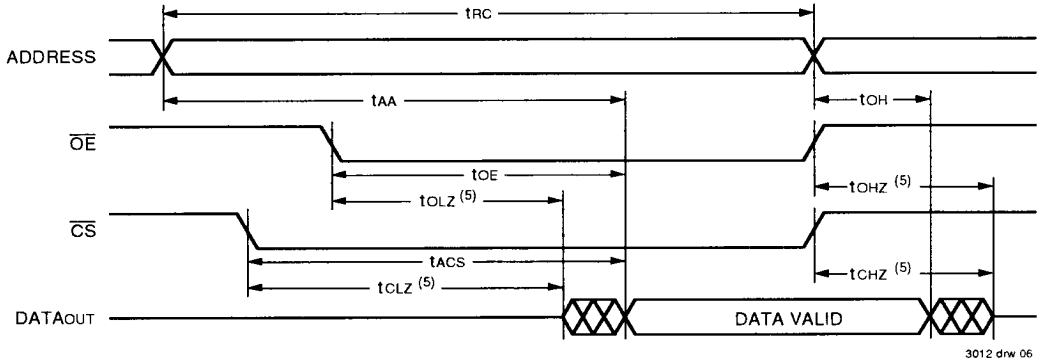
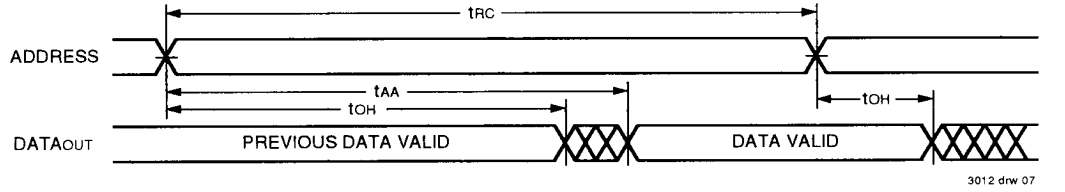
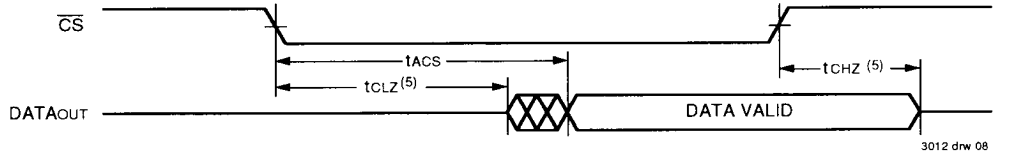
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

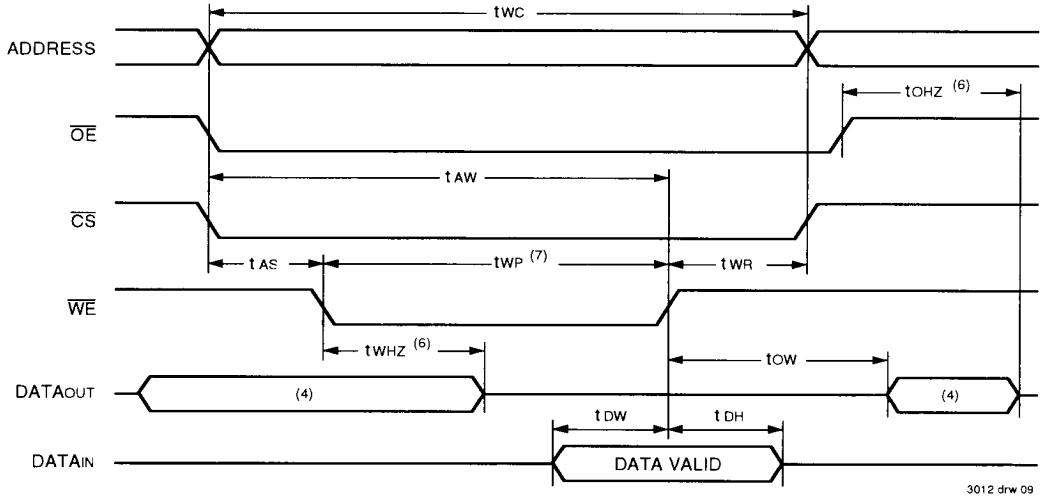


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

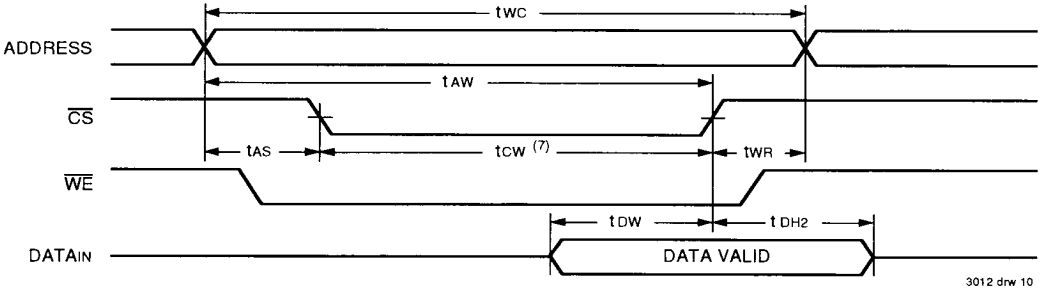


NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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ORDERING INFORMATION