ZARLINK SEMICONDUCTOR

ZL30462
Timing Module

Data Sheet

April 2003

Features

- Complete timing solution in a small outline package
- Selectable 8kHz, 1.544MHz, 2.048MHz or 19.44MHz input reference frequencies
- 8kHz (frame pulses), 2.048MHz, 8.192MHz, 16.384MHz, 19.44MHz and 155.52MHz (LVPECL) output clock frequencies
- Low intrinsic jitter and wander generation
- Fast lock and automatic holdover modes
- Holdover and lock indication
- Provides Time Interval Error (TIE) correction
- Accepts reference inputs from two independent sources
- 3.3V Supply Voltage

Applications

- SDH Add/Drop multiplexers
- Next Gen Digital Loop Carriers
- ATM edge switches
- Line cards

Ordering Information

ZL30462/MCG	40 SMT DIL (Tray + dry packed)

0°C to +70°C

Description

The ZL30462 is a Timing Module, which functions as a complete system clock solution for general timing applications.

The ZL30462 has been designed around Zarlink's Digital and Analog Phase Locked Loop (DPLL and APLL) technology and can lock to 1 of 2 inputs which can be derived from 2 independent sources. The module has two jitter attenuated output clocks at 19.44MHz (CMOS) and 155.52MHz (LVPECL). In addition to these outputs the module also supplies 2 8kHz frame pulses and 2.048MHz, 8.192MHz and 16.384MHz clocks.

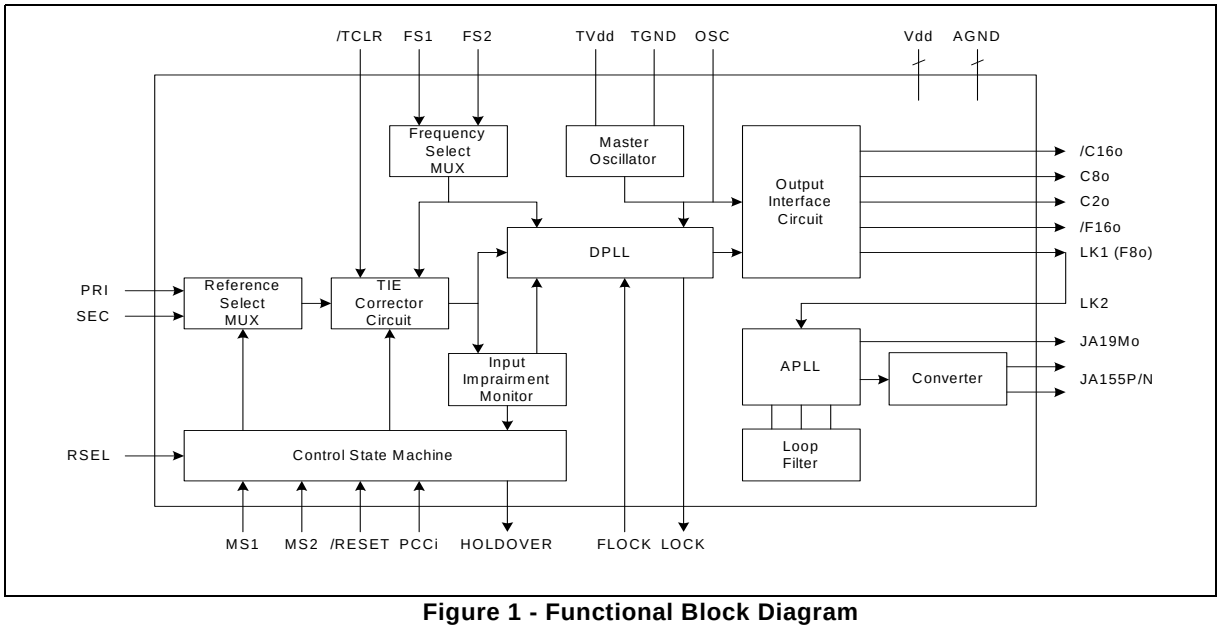


Figure 1 - Functional Block Diagram

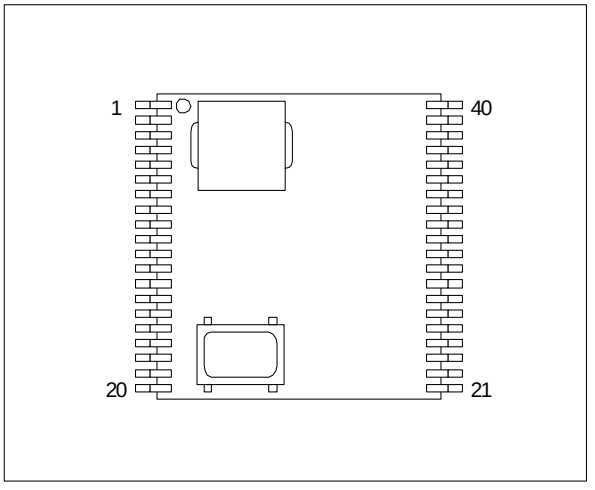


Figure 2 - 40 Pin SMT DIL Top View

Pin Description Table

Pin Number	Name	Description
1	$\overline{\text{C16o}}$	**Clock 16.384MHz (CMOS Output).** This output is used for ST-BUS operation with a 16.384MHz clock.
2	C8o	**Clock 8.192MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192Mb/s.
3	C2o	**Clock 2.048MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s.
4	$\overline{\text{F16o}}$	**Frame Pulse ST-BUS 16.384Mb/s (CMOS Output).** This is an 8kHz 61ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 16.384Mb/s.
5	LK1 (F8o)	**Link1.** Connect this pin to pin 6. This pin is also the F8o (8kHz 122ns) active high frame pulse, which marks the beginning of a frame and is also used by the DPLL's state machine. See Section 1.7 State Machine Control.
6	LK2	**Link2.** Connect this pin to pin 5.
7	AGND1	**Ground.**
8	IC	**Internal Connection.** Do not connect to this pin.
9	IC	**Internal Connection.** Do not connect to this pin.
10	AGND1	**Ground.**
11	IC	**Internal Connection.** Do not connect to this pin.
12	IC	**Internal Connection.** Do not connect to this pin.
13	V_{DD2}	**Positive Power Supply.** 3.3V
14	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is frequency locked to the input reference.
15	JA19Mo	**Clock 19.44MHz (CMOS Output).** This output provides a low jitter 19.44MHz clock.

Pin Description Table (continued)

Pin Number	Name	Description
16 17	JA155N JA155P	**JA 155.52MHz Clock (LVPECL Output)**. This differential output provides a low jitter 155.52MHz clock.
18	AGND2	**Ground.**
19	V_{DD3}	**Positive Power Supply.**3.3V
20	AGND1	**Ground.**
21	TV_{DD}	**Oscillator Positive Power Supply.** 3.3V
22	TGND	**Oscillator Ground.**
23	OSC	**Oscillator Master Clock (CMOS Output).** This pin can be used to monitor the output of the on-board master oscillator.
24	V_{DD1}	**Positive Power Supply.** 3.3V
25	PRI	**Primary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used. The selection of the input reference is based upon the MS1, MS2, FS1, FS2, and RSEL control inputs.This pin is internally pulled up to V_{DD}.
26	SEC	**Secondary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used. The selection of the input reference is based upon the MS1, MS2, FS1, FS2, and RSEL control inputs.This pin is internally pulled up to V_{DD}.
27	IC	**Internal Connection.** Do not connect to this pin.
28	$\overline{TCLR}$	**TIE Circuit Reset (Input).** A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a realignment of input phase with output phase. To ensure correct operation of this function, the $\overline{TCLR}$ pin should be held low for a minimum of 300ns. This pin is internally pulled down to GND.
29	$\overline{RESET}$	**Reset (Input).** A logic low at this input resets the DPLL. To ensure proper operation, the device must be reset after reference signal frequency changes and power-up. The $\overline{RESET}$ pin should be held low for a minimum of 300ns. While the $\overline{RESET}$ pin is low, all frame and clock outputs are at logic high. Following a reset, the input reference source and output clocks and frame pulses are phase aligned.
30	AGND1	**Ground.**
31	IC	**Internal Connection.** Do not connect to this pin.
32	FS1	**Frequency Select 1 (Input).** This input, in conjunction with FS2, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs. See Table 1.
33	FS2	**Frequency Select 2 (Input).** This input, in conjunction with FS1, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs. See Table 1.
34	RSEL	**Reference Source Select (Input).** A logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. This pin is internally pulled down to GND. See Table 2.
35	MS1	**Mode/Control Select 1 (Input).** This input, in conjunction with MS2, determines the state (Normal, Holdover or Freerun) of operation. See Table 3.
36	MS2	**Mode/Control Select 2 (Input).** This input, in conjunction with MS1, determines the state (Normal, Holdover or Freerun) of operation. See Table 3.

Pin Description Table (continued)

Pin Number	Name	Description
37	PCCi	**Phase Continuity Control Input (Input).** The signal at this pin affects the state changes between Holdover and Normal Modes. The logic level at this input is gated in by the rising edge of F8o (LK1). See Table 4.
38	HOLDOVER	**HOLDOVER (CMOS Output).** This output goes to a logic high whenever the PLL goes into holdover mode.
39	FLOCK	**Fast Lock Mode (Input).** Set high to allow the PLL to quickly lock to the input reference (less than 500 ms locking time).
40	V_{DD1}	**Positive Power Supply.** 3.3V

1.0 Functional Description

The ZL30462 offers a complete timing solution in a 1" x 1" module package. The module comprises 3 main components, a DPLL which performs the main operational functions, a APLL which provides 2 low jitter output clocks and an on-board master oscillator. Figure 1 shows a functional block diagram of the module, which is described in the following sections.

1.1 Reference Select MUX Circuit

The ZL30462 accepts two simultaneous reference input signals and operates on their falling edges. Either the primary reference (PRI) signal or the secondary reference (SEC) signal can be selected as input to the TIE Corrector Circuit. The selection is based on the Control, Mode and Reference Selection of the device. See Table 1 and Table 4.

1.2 Frequency Select MUX Circuit

The ZL30462 operates with one of four possible input reference frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz). The frequency select inputs (FS1 and FS2) determine which of the four frequencies may be used at the reference inputs (PRI and SEC). Both inputs must have the same frequency applied to them. A reset ($\overline{RESET}$) must be performed after every frequency select input change. See Table 1.

FS2	FS1	Input Frequency
0	0	19.44MHz
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

Table 1 - Input Frequency Selection

1.3 Time Interval Error (TIE) Corrector Circuit

The TIE corrector circuit, when enabled, prevents a step change in phase on the input reference signals (PRI or SEC) from causing a step change in phase at the input of the DPLL block of Figure 1.

During reference input rearrangement, such as during a switch from the primary reference (PRI) to the secondary reference (SEC), a step change in phase on the input signals will occur. A phase step at the input of the DPLL would lead to unacceptable phase changes in the output signal.

As shown in Figure 3, the TIE Corrector Circuit receives one of the two reference (PRI or SEC) signals, passes the signal through a programmable delay line, and uses this delayed signal as an internal virtual reference, which is input to the DPLL. Therefore, the virtual reference is a delayed version of the selected reference.

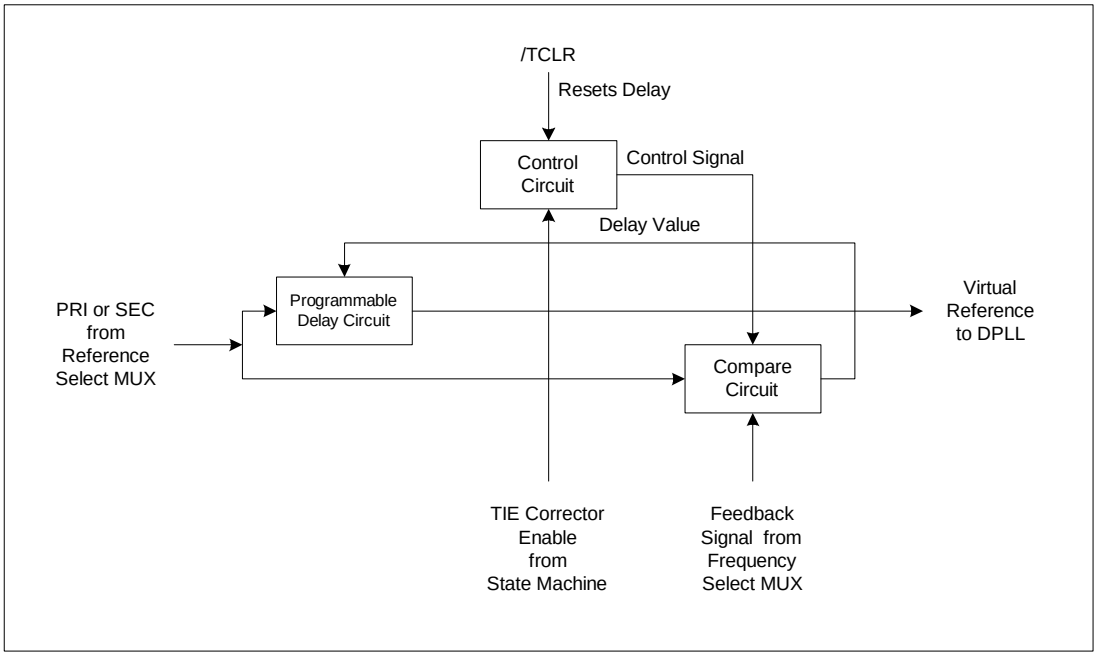


Figure 3 - TIE Corrector Circuit

During a switch from one reference to the other, the State Machine first changes the mode of the device from Normal to Holdover. In Holdover Mode, the DPLL no longer uses the virtual reference signal, but generates an accurate clock signal using storage techniques. The Compare Circuit then measures the phase delay between the current phase (feedback signal) and the phase of the new reference signal. This delay value is passed to the Programmable Delay Circuit (See Figure 3). The new virtual reference signal is now at the same phase position as the previous reference signal would have been if the reference switch not taken place. The State Machine then returns the device to Normal Mode.

The DPLL now uses the new virtual reference signal, and since no phase step took place at the input of the DPLL, no phase step occurs at the output of the DPLL. In other words, reference switching will not create a phase change at the input of the DPLL, or at the output of the DPLL.

Since internal delay circuitry maintains the alignment between the old virtual reference and the new virtual reference, a phase error may exist between the selected input reference signal and the output signal of the DPLL. This phase error is a function of the difference in phase between the two input reference signals during reference rearrangements. Each time a reference switch is made, the delay between input signal and output signal will change. The value of this delay is the accumulation of the error measured during each reference switch.

The programmable delay circuit can be zeroed by applying a logic low pulse to the TIE Circuit Reset ($\overline{\text{TCLR}}$) pin. The minimum reset pulse width is 300ns. The speed of the phase alignment correction is limited to 5ns per 125µs, and convergence is in the direction of least phase travel.

The state diagram of Figure 8 indicates which state changes the TIE Corrector Circuit is activated.

1.4 Digital Phase Lock Loop (DPLL)

As shown in Figure 8, Control State Diagram consists of a Phase Detector, Limiter, Loop Filter, Digitally Controlled Oscillator, and a Control Circuit.

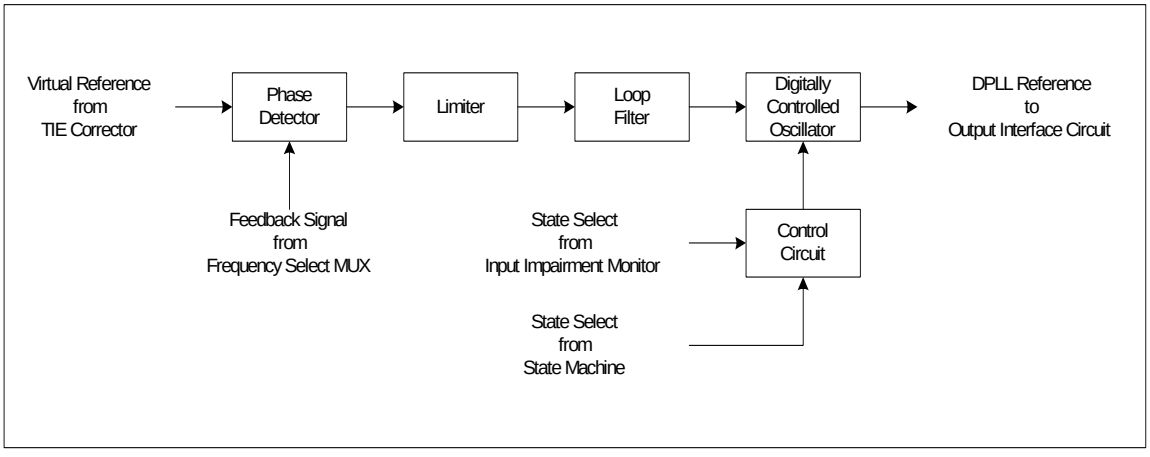


Figure 4 - DPLL Block Diagram

1.4.1 Phase Detector

The Phase Detector compares the virtual reference signal from the TIE Corrector circuit with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Limiter circuit. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8kHz, 1.544MHz, 2.048MHz or 19.44MHz).

1.4.2 Limiter

The Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 5ns per 125µs. This is well within the maximum phase slope of 7.6ns per 125µs or 81ns per 1.326ms specified by AT&T TR62411 and Telcordia GR-1244-CORE, respectively.

1.4.3 Loop Filter

The Loop Filter is similar to a first order low pass filter with a 1.9 Hz cutoff frequency for all four reference frequency selections (8kHz, 1.544MHz, 2.048MHz or 19.44MHz). This filter ensures that the jitter transfer requirements in ETS 300 011 and AT&T TR62411 are met.

1.4.4 Control Circuit

The Control Circuit uses status and control information from the State Machine and the Input Impairment Circuit to set the mode of the DPLL. The three possible modes are Normal, Holdover and Freerun.

1.4.5 Digitally Controlled Oscillator (DCO)

The DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30462.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the last (30ms to 60ms) frequency the DCO was generating while in Normal Mode.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSC 20MHz source.

1.4.6 Lock Indicator

If the PLL is in frequency lock (frequency lock means the center frequency of the PLL is identical to the line frequency), and the input phase offset is small enough such that no phase slope limiting is exhibited, then the lock signal will be set high.

1.5 Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 5. The Output Interface Circuit uses a Tapped Delay Line followed by a E1 Divider Circuit to generate the required output signals.

A tapped delay line is used to generate a 16.384MHz signal.

The E1 Divider Circuit uses the 16.384MHz signal to generate three output clocks and two frame pulses. The C8o and C2o clocks are generated by simply dividing the C16o clock, by two and eight respectively. These outputs have a 50% duty cycle. The F8o and F16o frame pulse outputs are also generated from this 16.384MHz signal. Both frame pulse outputs have limited drive capability and should be buffered when driving high capacitance (e.g., 30pF) loads.

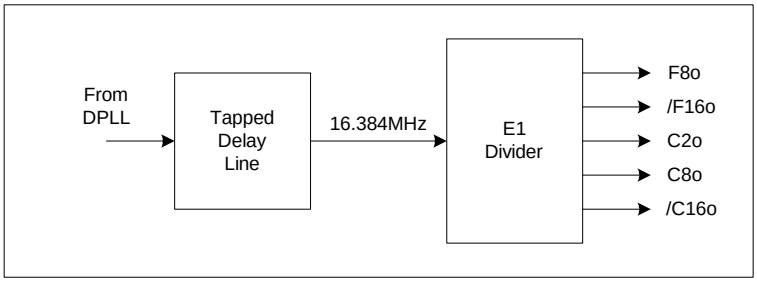


Figure 5 - Output Interface Circuit Block Diagram

1.6 Input Impairment Monitor

This circuit monitors the input signal to the DPLL and automatically enables the Holdover Mode (Auto-Holdover) when the frequency of the incoming signal is outside the Auto-Holdover capture range. (See AC Electrical Characteristics - Performance). This includes a complete loss of incoming signal, or a large frequency shift in the incoming signal. When the incoming signal returns to normal, the DPLL is returned to Normal Mode with the output signal locked to the input signal. The holdover output signal in the ZL30462 is based on the incoming signal 30ms minimum to 60ms prior to entering the Holdover Mode. The amount of phase drift while in holdover is negligible because the Holdover Mode is very accurate (e.g., ±0.05ppm, relative to the master oscillator frequency). Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved.

1.7 State Machine Control

As shown in Figure 1, this state machine controls the Reference Select MUX, the TIE Corrector Circuit and the DPLL. Control is based on the logic levels at the control inputs RSEL, MS1, MS2 and PCCi (See Figure 6). When switching from Primary Holdover to Primary Normal, the TIE Corrector Circuit is enabled when PCCi = 1, and disabled when PCCi = 0.

All state machine changes occur synchronously on the rising edge of F8o (internal 8kHz frame pulse), this signal is available form pin 3 (LK1). See the Control and Mode of Operation section for full details.

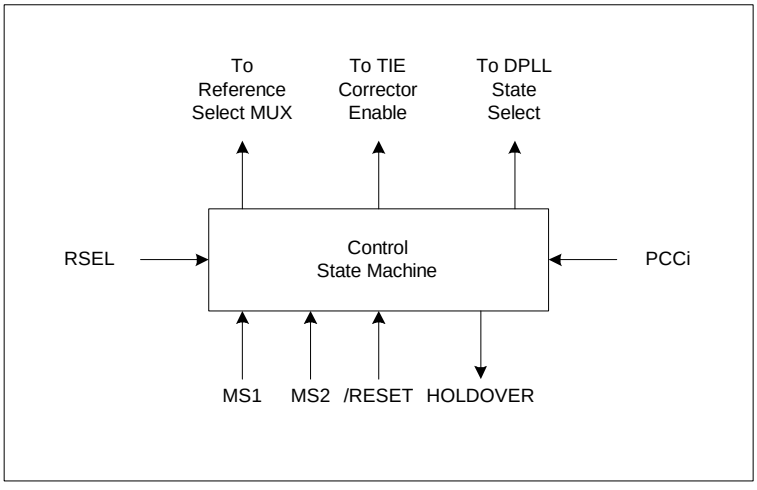


Figure 6 - Control State Machine Block Diagram

1.8 Master Oscillator

The ZL30462 uses a 20MHz 20ppm master oscillator, the output frequency of the oscillator can be monitored via the OSC pin. The on-board master oscillator is powered via the TV_{DD} and TGND pins, independently of the modules V_{DDx} and AGNDx pins,

2.0 Control and Mode of Operation

The active reference input (PRI or SEC) is selected by the RSEL pin as shown in Table 2. Refer to Table 4 and Figure 8 for details of the state change sequences.

RSEL	Input Reference
0	PRI
1	SEC

Table 2 - Input Reference Selection

The ZL30462 has three possible modes of operation, Normal, Holdover and Freerun.

As shown in Table 3, Mode/Control Select pins MS2 and MS1 select the mode and method of control.

MS2	MS1	Mode
0	0	NORMAL
0	1	HOLDOVER
1	0	FREERUN
1	1	Reserved

Table 3 - Operating Modes and States

2.1 Normal Mode

Normal Mode is typically used when a slave clock source, synchronized to the network is required.

In Normal Mode, the ZL30462 provides timing (C2o, C8o, $\overline{\text{C16o}}$, JA19Mo and JA155P/N) and frame synchronization (F8o & $\overline{\text{F16o}}$) signals, which are synchronized to one of two reference inputs (PRI or SEC). The input reference signal may have a nominal frequency of 8kHz, 1.544MHz, 2.048MHz or 19.44MHz.

From a reset condition, the ZL30462 will take up to 30 seconds (see AC Electrical Characteristics) for the output signals to be synchronized (phase locked) to a valid reference input.

The selection of input references is control dependent as shown in state Table 4. The reference frequencies are selected by the frequency control pins FS2 and FS1 as shown in Table 1.

During normal mode, whilst locked to a synchronization source input, the ZL30462 can tolerate a 10ppm frequency change (on that input) without generating alarms or charging state.

2.2 Fast Lock Mode

Fast Lock Mode is a sub-mode of Normal Mode, it is used to allow the ZL30462 to lock to a reference more quickly than Normal Mode will allow. Typically, the DPLL will lock to the incoming reference within 500ms if the FLOCK pin is set high.

2.3 Holdover Mode

Holdover Mode is typically used for short durations (e.g., 2 seconds) while network synchronization is temporarily disrupted.

In Holdover Mode, the ZL30462 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the ZL30462 output reference frequency is stored alternately in two memory locations every 30ms. When the device is switched into Holdover Mode, the value in memory from between 30ms and 60ms is used to set the output frequency of the device.

The frequency accuracy of Holdover Mode is ±0.05ppm, which translates to a worst case 35 frame (125µs) slips in 24 hours. This satisfies the AT&T TR62411 and Telcordia GR-1244-CORE Stratum 3 requirement of ±0.37ppm (255 frame slips per 24 hours).

Two factors affect the accuracy of Holdover Mode. One is drift on the master oscillator whilst in Holdover Mode, drift on the master oscillator directly affects the Holdover Mode accuracy. The other factor affecting accuracy is large jitter on the reference input prior (30ms to 60ms) to the mode switch. For instance, jitter of 7.5UI at 700Hz may reduce the Holdover Mode accuracy from ±0.05ppm to ±0.10ppm.

2.4 Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun Mode, the ZL30462 provides timing and synchronization signals which are based on the master oscillator frequency (OSC) only, and are not synchronized to the reference signals (PRI and SEC).

The accuracy of the output clock is equal to the accuracy of the master oscillator (OSC) which is ±20ppm.

2.5 Reset Circuit

A simple power up reset circuit with about a 50µs reset low time is shown in Figure 7. Resistor Rp is for protection only and limits current into the $\overline{\text{RESET}}$ pin during power down conditions. The reset low time is not critical but should be greater than 300ns.

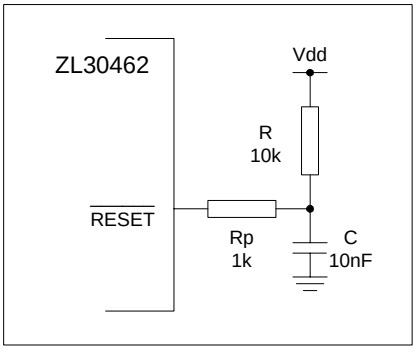


Figure 7 - Power-Up Reset Circuit

2.6 Warm-up Time

The ZL30462 should have a warm-up time of 10 hours to ensure that the module has reached a stable operating temperature (however reasonable operation can be expected with 30 minutes).

3.0 ZL30462 Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

3.1 Intrinsic Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band limiting filters depending on the applicable standards. To enhance the performance of the ZL30462 an additional APLL has been incorporated to provide two low jitter output. The JA155P/N (LVPECL) and JA19Mo (single ended) outputs both offer better than OC3 jitter performance.

3.2 Jitter Tolerance

Jitter tolerance is a measure of the ability of the ZL30462 to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

3.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, output jitter is measured with various filters, dependant on the required standard.

3.4 Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the ZL30462, the Freerun accuracy is equal to the Master Oscillator (OSC) accuracy.

3.5 Holdover Accuracy

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the ZL30462, the storage value is determined while the device is in Normal Mode and locked to an external (and stable) reference signal for at least 10 minute after the warm-up period.

The absolute Master Oscillator (OSC) accuracy of the ZL30462 does not affect Holdover accuracy, but the change in OSC accuracy while in Holdover Mode does.

3.6 Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The ZL30462 capture range is equal to ±230 ppm, which is offset by the accuracy of the Master Oscillator (OSC).

3.7 Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the ZL30462.

3.8 Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

3.9 Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

3.10 Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

$$MTIE(S) = \max_{j=1}^{N-n+1} \left(\max_{i=j}^{n+j-1}(x_i) - \min_{i=j}^{n+j-1}(x_i) \right)$$

3.11 Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the ZL30462, the output signal phase continuity is maintained to within ±5ns at the instance (over one frame) of all reference switches and all mode changes. The total phase shift, depending on the switch or type of mode change, may accumulate up to 200ns over many frames. The rate of change of the 200ns phase shift is limited to a maximum phase slope of approximately 5ns/125µs. This meets the AT&T TR62411 maximum phase slope requirement of 7.6ns/125µs and Telcordia GR-1244-CORE (81ns/1.326ms).

3.12 Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

- initial input to output phase difference
- initial input to output frequency difference
- synchronizer loop filter
- synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The ZL30462 loop filter and limiter were optimized to meet the AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standards requirement, may be longer than in other applications. See AC Electrical Characteristics - Performance for Maximum Phase Lock Time.

Description				State				
Input Controls				Freerun	Normal PRI	Normal SEC	Holdover PRI	Holdover SEC
MS2	MS1	RSEL	PCCi	S0	S1	S2	S1H	S2H
0	0	0	0	S1	-	S1 MTIE	S1	S1 MTIE
0	0	0	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	0	1	X	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
0	1	0	X	/	S1H	/	-	/
0	1	1	X	/	/	S2H	/	-
1	0	X	X	-	S0	S0	S0	S0

Legend:
- No Change
/ Not Valid
MTIE State change occurs with TIE Corrector Circuit
Refer to Control State Diagram for state changes to and from Auto-Holdover State

Table 4 - Control State Table

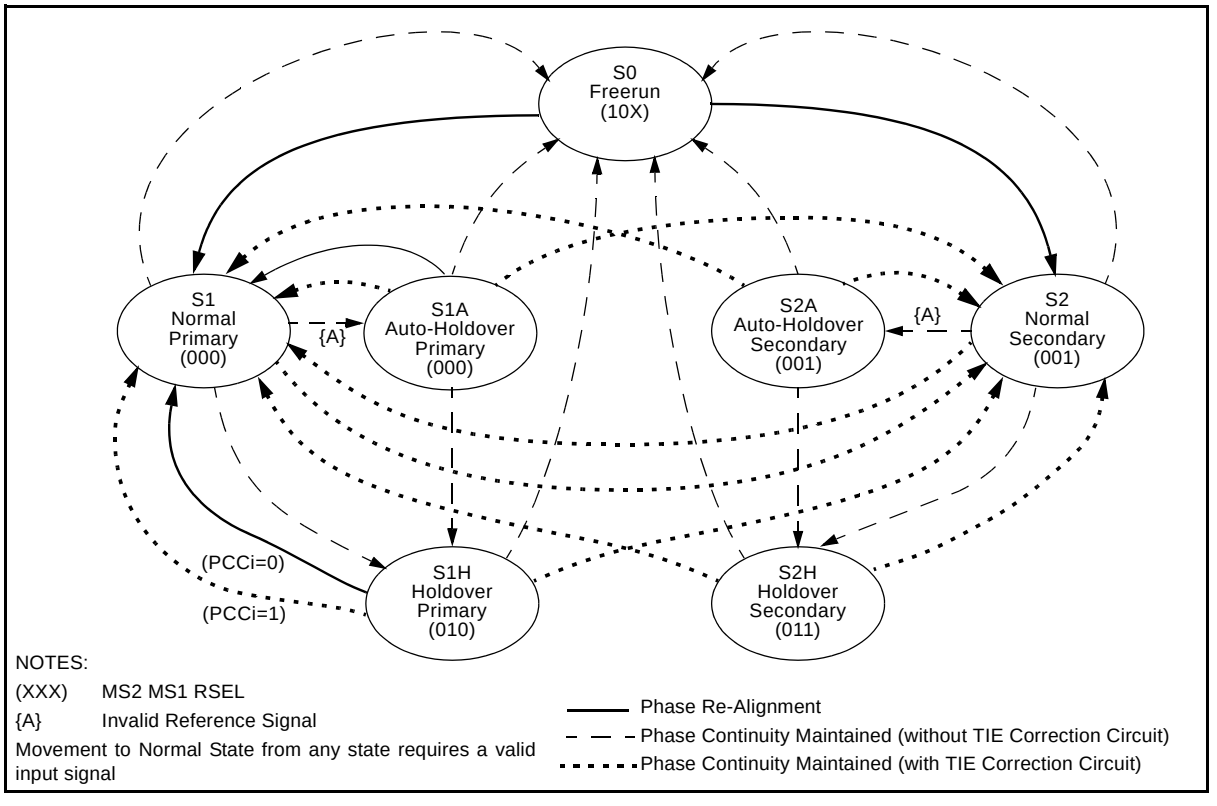


Figure 8 - Control State Diagram

4.0 Characteristics

4.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltages	V_{DD} TV_{DD}	-0.3 -0.3	5.0 5.0	V V
2	Input Voltage	V_{IN}	-0.05	V_{DD}+0.5	V

* Voltages are with respect to ground (GND) unless otherwise stated

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions*

	Parameter	Symbol	Min	Typ	Max	Units
1	Supply Voltages	V_{DD} TV_{DD}	3.0	3.3	3.6	V
2	Operating Temperature	T_A	0	25	70	^oC

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics*

	Characteristics	Symbol	Min	Typ	Max	Units	Test Conditions
1	Supply Current	I_{DD}		93	105	mA	Output unloaded
2	Supply Current	TI_{DD}		5	10	mA	Output unloaded
3	CMOS: High-level input voltage	V_{IH}	$0.7V_{DD}$			V	
4	CMOS: Low-level input voltage	V_{IL}	0		$0.3V_{DD}$	V	
5	CMOS: Input leakage current	I_{IL}			15	µA	$VI=V_{DD}$ or GND
6	CMOS: High-level output voltage	V_{OH}	2.4			V	I_{OH} = 8mA
7	CMOS: Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 8mA
8	LVPECL: Differential output voltage	$\|V_{OD}\|$	480	600	720	mVp	Z_T=100 Ohms
9	LVPECL: High-level output voltage	V_{OH}		V_{DD}-0.9		V	Z_T=100 Ohms
10	LVPECL: Low-level output voltage	V_{OL}		V_{DD}-1.5		V	
11	LVPECL: Output rise and fall times	T_{RF}	250	300	700	ps	Note 1

* Voltages are with respect to ground (GND) unless otherwise stated

Note 1: Rise and fall times are measured at 20% and 80% levels.

* Voltages are with respect to ground (GND) unless otherwise stated

AC Electrical Characteristics*

	Parameter	Symbol	Min	Max	Units	Test Conditions
1	Freerun Mode accuracy	F_A	-20	20	ppm	Note 2
2	Holdover Mode accuracy		F_A-0.05	F_A+0.05	ppm	Note 3
3	Capture range		F_A-230	F_A+230	ppm	Note 4
4	Intrinsic Jitter 500Hz - 1.3MHz 65kHz - 1.3MHz	J_{IN}		 500 400	 ps ps	Note 5
5	Wander Generation	W_{GEN}				ITU-T G.813 Option1
6	Wander Transfer	W_{TR}				ITU-T G.813 Option1
7	Phase response to input signal interruptions	P_{TT}				ITU-T G.813 Option1
8	Phase Transients	P_T				ITU-T G.813 Option1
9	Holdover Entry Phase Transients	H_{EPT}				ITU-T G.813 Option1
10	Lock Time	L_T		30	s	

Note 2: The Freerun accuracy is directly related to the accuracy of the master oscillator

Note 3: The DPLL Holdover accuracy is also affected by the holdover stability of the master oscillator

Note 4: This figure is offset by the accuracy of the master oscillator

Note 5: Applies to JA outputs only

AC Electrical Characteristics* - Timing Parameter Measurements - CMOS Voltage Levels*

	Characteristics	Symbol	Typical	Units
1	Threshold voltage	V_T	$0.5V_{DD}$	V
2	Rise and fall threshold voltage High	V_{HM}	$0.7V_{DD}$	V
3	Rise and fall threshold voltage Low	V_{LM}	$0.3V_{DD}$	V

* Voltages are with respect to ground (GND) unless otherwise stated

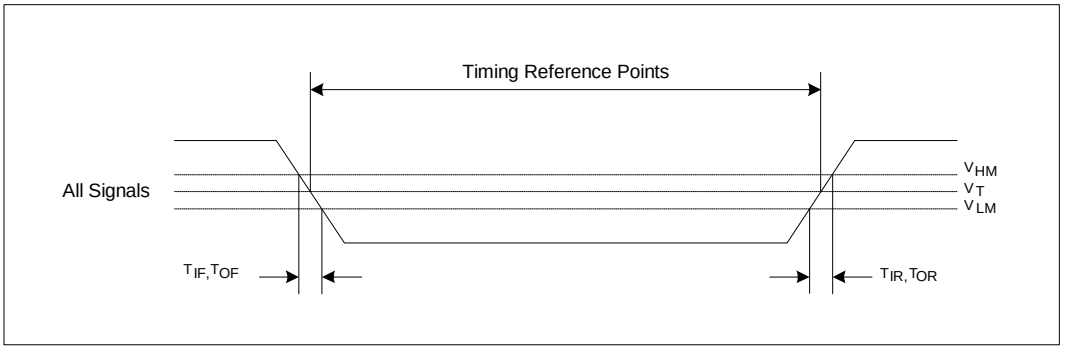


Figure 9 - Timing Parameters Measurement Voltage Levels

AC Electrical Characteristics - Input Phase Alignment

	Characteristics	Symbol	Min	Max	Units	Test Conditions
1	8kHz ref. pulse width low	t_{R8H}	100		ns	
2	8kHz ref. input to F8o delay	t_{R8D}	-21	6	ns	
3	1.544MHz ref. pulse width low	$t_{R1.5L}$	100		ns	
4	1.544MHz ref. input to F8o delay	$t_{R1.5D}$	337	363	ns	
5	2.048MHz ref. pulse width low	t_{R2L}	100		ns	
6	2.048MHz ref. input to F8o delay	t_{R2D}	222	238	ns	
7	19.44MHz ref. pulse width low	t_{R19L}	23		ns	
8	19.44MHz ref. input to F8o delay	t_{R19D}	46	57	ns	
9	Reference input rise and fall time	t_{IR}, t_{IF}		10	ns	

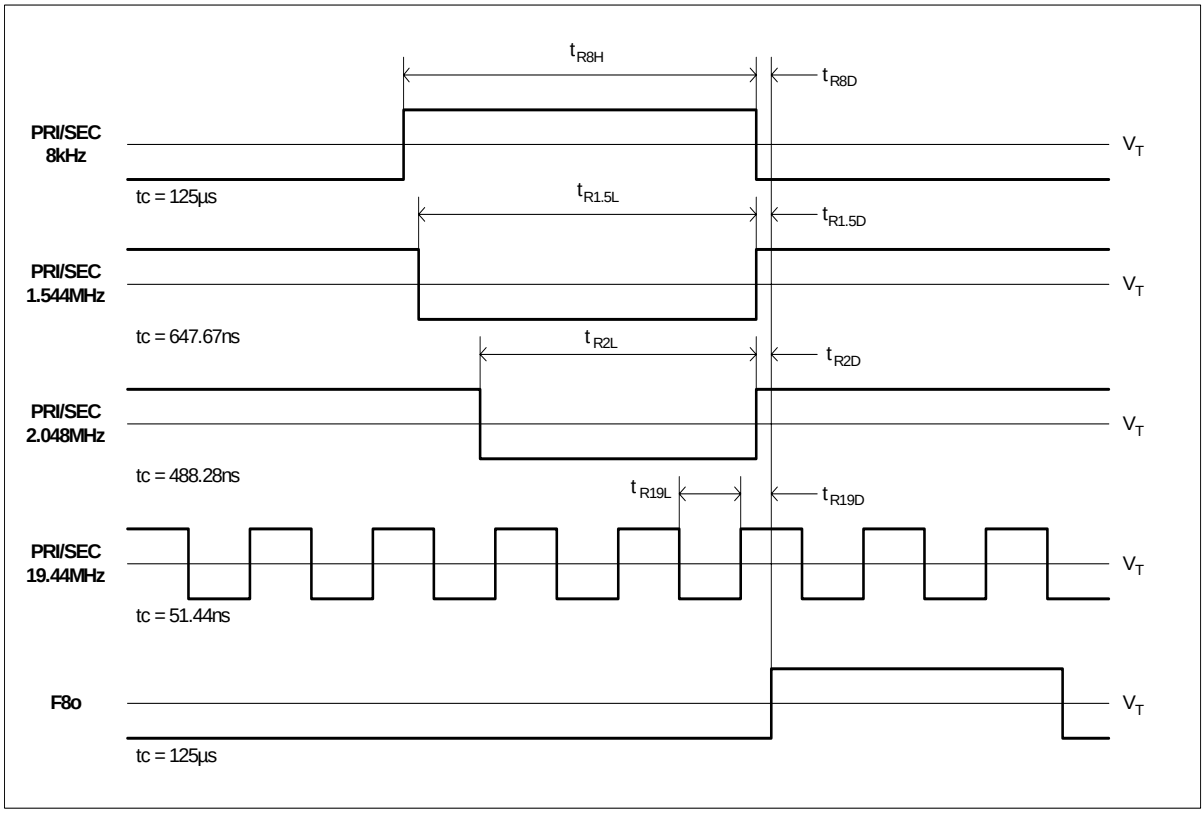


Figure 10 - Input to Output Timing (Normal Mode)

AC Electrical Characteristics - Input Control Signals

	Characteristics	Symbol	Min	Max	Units	Test Conditions
1	Input Controls Setup Time	t_S	100		ns	
2	Input Controls Hold Time	t_H	100		ns	

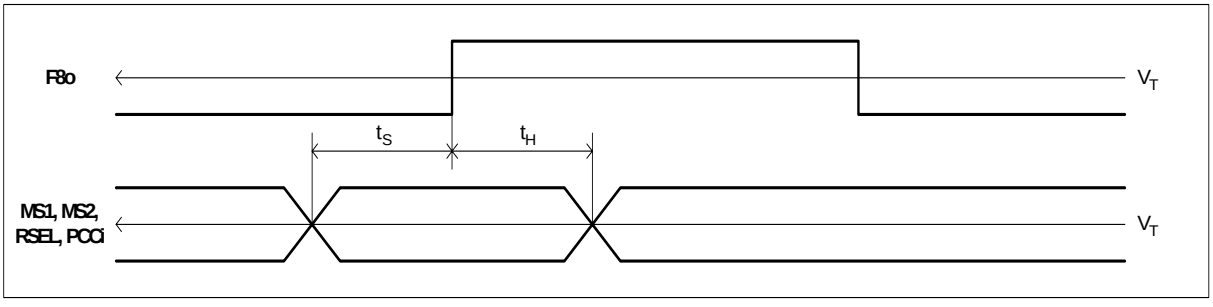


Figure 11 - Input Control Signal Setup and Hold Time

AC Electrical Characteristics - Outputs Timing

	Characteristics	Symbol	Min	Max	Units	Test Conditions
1	F8o to $\overline{\text{F16o}}$ delay	t_{F16D}	22	37	ns	
2	F8o to JA155P/N delay	t_{J155PD} t_{J155ND}	-5 -5	10 10	ns ns	
3	F8o to JA19Mo delay	t_{J19D}	-5	10	ns	
4	F8o to $\overline{\text{C16o}}$ delay	t_{C16D}	-11	5	ns	
5	F8o to C8o delay	t_{C8D}	-11	5	ns	
6	F8o to C2o delay	t_{C2D}	-11	5	ns	

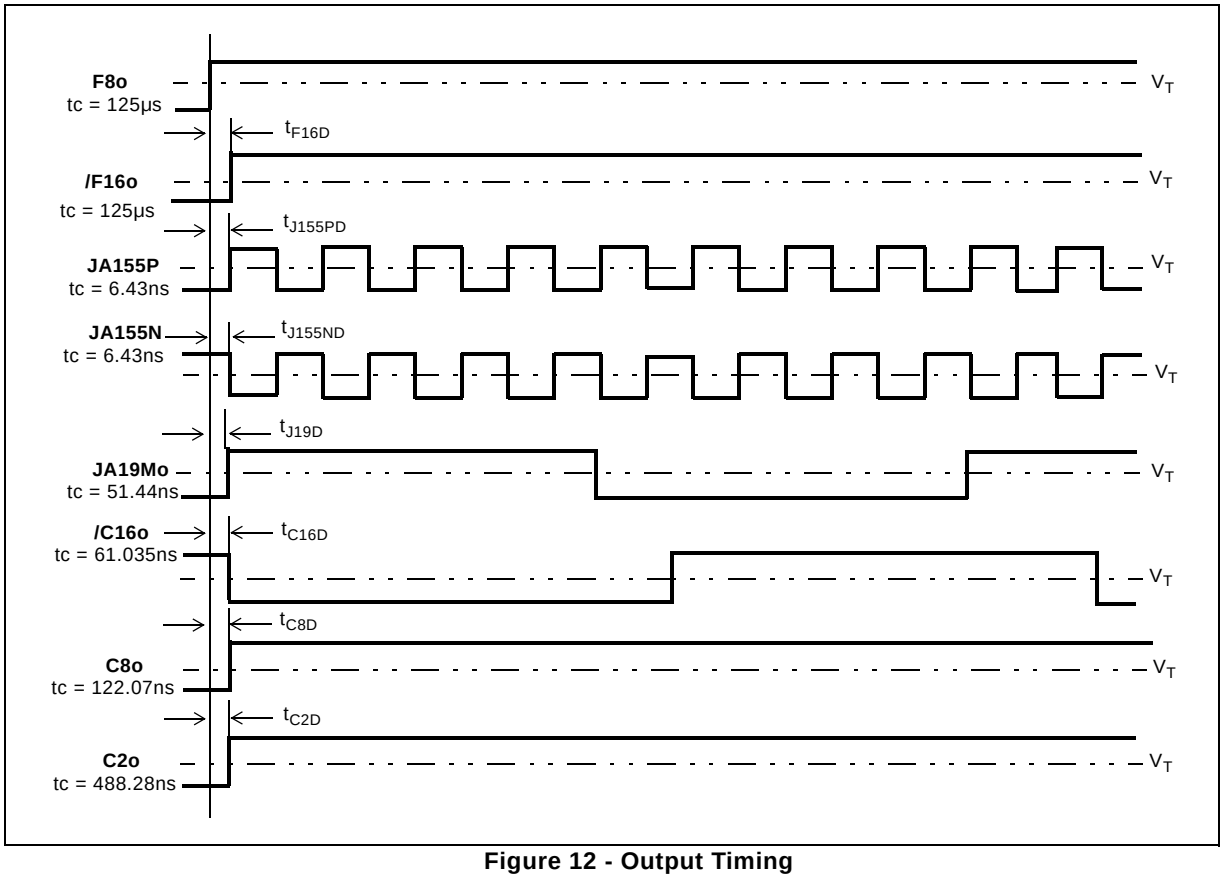
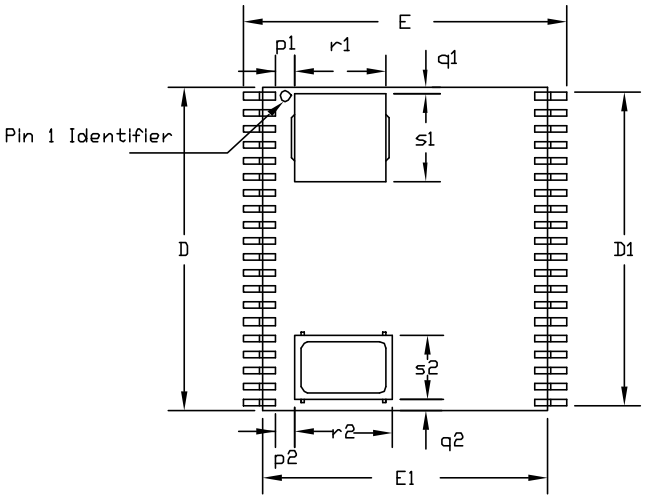
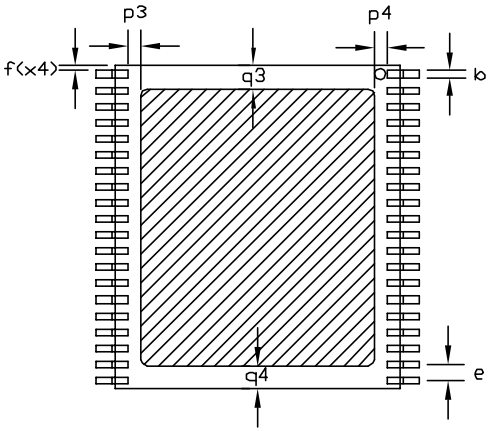


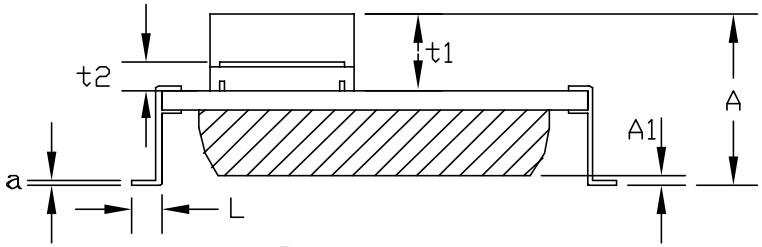
Figure 12 - Output Timing



Top View



Bottom View



Side View

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	9.00	---	---	0.354
A1	0.510	---	---	0.02	---	---
D	24.38	25.40	26.42	0.96	1.00	1.04
D1	23.62	24.64	25.39	0.93	0.97	1.01
E	24.64	25.40	26.16	0.97	1.00	1.03
E1	---	22.35	---	---	0.88	---
a	---	0.254	---	---	0.01	---
b	---	0.518	---	---	0.02	---
L	1.14	1.50	1.91	0.045	0.060	0.075
e	1.02	1.27	1.52	0.04	0.05	0.06
f	---	0.381	---	---	0.015	---
n		40			40	
p1	1.00	1.27	---	0.04	0.05	---
p2	1.27	1.52	---	0.05	0.06	---
p3/4	1.00	---	---	0.04	---	---
q1	---	0.50	---	---	0.02	---
q2	---	0.90	---	---	0.035	---
q3/4	1.80	---	---	0.07	---	---
r1/2	---	7.60	---	---	0.30	---
s1	---	6.90	---	---	0.27	---
s2	---	0.50	---	---	0.20	---
t1	---	---	4.00	---	---	0.16
t2	---	---	1.52	---	---	0.06
Drawing not to JEDEC Standard defined outline.						

Note:

Hatched Area represnts grouping of discrete componets.

ISSUE	1			
ACN	214170			
DATE	26Mar03			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code MC

Package Outline for ZL30462
40LD DIL Hybrid
(25.40x25.40)mm 1.27mm Pitch

GPD00836

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