HARRIS Semiconductor

HSP43481

NOT RECOMMENDED FOR NEW DESIGNS
See HSP43881

September 1997

Digital Filter

Features

- **Four Filter Cells**
- **0MHz to 30MHz Sample Rate**
- **8-Bit Coefficients and Signal Data**
- **26-Bit Accumulator per Stage**
- **Filter Lengths Up to 1032 Tap**
- **Expandable Coefficient Size, Data Size and Filter Length**
- **Decimation by 2, 3 or 4**

Applications

- **1-D and 2-D FIR Filters**
- **Radar/Sonar**
- **Adaptive Filters**
- **Echo Cancellation**
- **Complex Multiply-Add**
- **Sample Rate Converters**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43481JC-20	0^oC to $+70^oC$	68 Lead PLCC
HSP43481JC-25	0^oC to $+70^oC$	68 Lead PLCC
HSP43481JC-30	0^oC to $+70^oC$	68 Lead PLCC
HSP43481GC-20	0^oC to $+70^oC$	68 Lead PGA
HSP43481GC-25	0^oC to $+70^oC$	68 Lead PGA
HSP43481GC-30	0^oC to $+70^oC$	68 Lead PGA

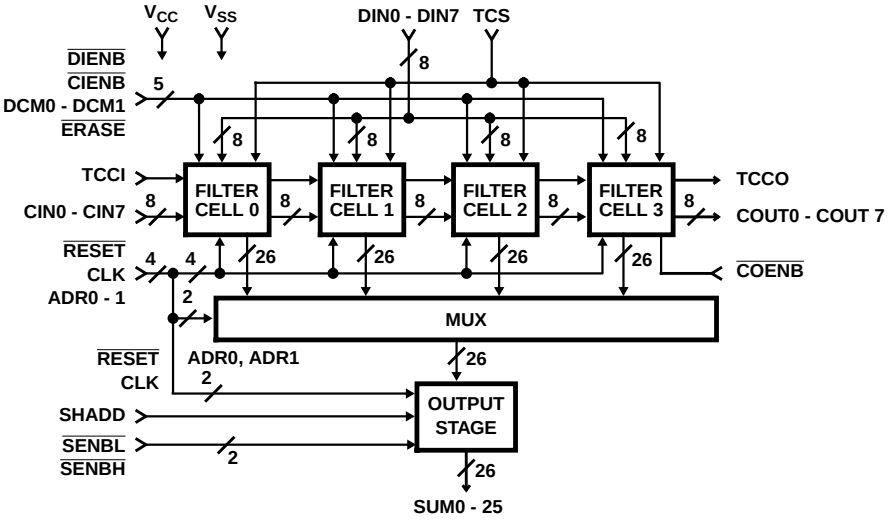
Description

The HSP43481 is a video-speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of four filter cells cascaded internally and a shift-and-add output stage, all in a single integrated circuit. Each filter cell contains an 8 x 8 multiplier, three decimation registers and a 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by eight-bits. The HSP43481 has a maximum sample rate of 30MHz. The effective multiply-accumulate (MAC) rate is 120MHz.

The HSP43481 can be configured to process expanded coefficient and word sizes. Multiple devices can be cascaded for larger filter lengths without degrading the sample rate or a single device can process larger filter lengths at less than 30MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The HSP43481 provides for unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of $^1/_2$, $^1/_3$ or $^1/_4$ the input sample rate. These registers also provide the capability to perform 2-D operations such as N x N spatial correlations/convolutions for image processing applications.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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