

1.1 Scope.

This specification covers the detail requirements for complete 8-bit and 10-bit resolution A/D converters with the three state logic outputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD570SD/883B
-2	AD571SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000; package outline: D-18.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Digital Common	+7V
V_{EE} to Digital Common	-16.5V
Analog Common to Digital Common	$\pm 1\text{V}$
Analog Input to Analog Common	$\pm 15\text{V}$
Control Inputs	0 to V_{CC}
Digital Outputs (Blank Mode)	0 to V_{CC}
Power Dissipation	800mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 88^\circ\text{C/W}$

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Table 1.

Test	Symbol	Device ²	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	-1	0.195	0.195	0.195		Unipolar and Bipolar Major Transitions ± 3 Codes	\pm % of FS max
		-2	0.098	0.195	0.098	0.098		
Differential Nonlinearity ³	DNL	-1	8	8	8		All Codes Test Unipolar and Bipolar	Bits min
		-2	10	8	10	10		
Full-Scale Error ⁴	A_E	-1, 2	40	40			Unipolar	\pm mV max
		-1, 2	20	20			Bipolar	
Full-Scale Temperature Drift	TCA_E	-1			0.781			\pm % of FS max
		-2			0.488			
Offset Error	V_{OS}	-1	20	20			First Transition	\pm mV max
		-2	10	20		10		
Offset Temperature Drift	TCV_{OS}	-1			0.391			\pm % of FS max
		-2			0.195			
Bipolar Zero Error	B_{PZE}	-1	20	20			Low Side MSB, Transition Bipolar	\pm mV max
		-2	10	20		10	Bipolar	
Bipolar Zero Temperature Drift	TCB_{PZE}	-1			0.391		Bipolar	\pm % of FS max
		-2			0.195			
Input Resistance	R_{IN}	-1, 2	3	3	3			k Ω min
			7	7	7			k Ω max
Conversion Time ⁵	TC	-1, 2	15	15	15			μ s min
			40	40	40			μ s max
Three-State Leakage Current	I_{OLT}	-1	40	40	40		$V_{OL} = 0.0V$, Bit 1–Bit 8	\pm μ A max
		-2	40	40	40		$V_{OL} = 0.0V$, Bit 1–Bit 10	
Power Supply Rejection Ratio	PSRR	-1	78.1	78.1	78.1		$-16.0V \leq V_{EE} \leq -13.5V$, $V_{CC} = +15V$	\pm mV max
		-2	19.5	78.1	78.1	19.5	$+4.5V \leq V_{CC} \leq 5.5V$, $V_{EE} = -15V$	
Power Supply Current	I_{CC}	-1, 2	10	10			Convert	+ mA max
			10	10			Blank	
		-1, 2	15	15				
Digital Input High Voltage	V_{IH}	-1, 2	2.0	2.0	2.0		Blank and Convert	+ V min
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8		Blank and Convert	+ V max
Digital Input High Current	I_{IH}	-1, 2	100	100	100		Blank and Convert, $V_{IH} = 5.0V$	\pm μ A max
Digital Input Low Current	I_{IL}	-1, 2	100	100	100		Blank and Convert, $V_{IL} = 0.0V$	\pm μ A max
Digital Output Low Voltage	V_{OL}	-1	0.4	0.4	0.4		\overline{DR} , Bit 1–Bit 8, $I_{OL} = +3.2mA$	+ V max
		-2	0.4	0.4	0.4		$I_{OL} = +3.2mA$, \overline{DR} , Bit 1–Bit 10	
Digital Output High Voltage	V_{OH}	-1	2.4	2.4	2.4		Bit 1–Bit 8, $I_{OH} = -0.5mA$	+ V min
		-2	2.4	2.4	2.4		$I_{OH} = -0.5mA$, Bit 1–Bit 10	

NOTES

¹ $V_{CC} = +5V$, $V_{EE} = -15V$, $V_{IH} = +2.0V$, $V_{IL} = +0.8V$, analog input through 15 Ω to Pin 13, Unipolar configuration.

$T_A = 25^\circ C$ unless otherwise indicated.

Unipolar configuration Pin 15 (Bipolar Offset Control) is grounded.

Bipolar configuration Pin 15 is not connected.

²For -1 (8-bit resolution device), 0.391% of full scale = 1LSB (Least Significant Bit).

For -2 (10-bit resolution device), 0.098% of full scale = 1LSB.

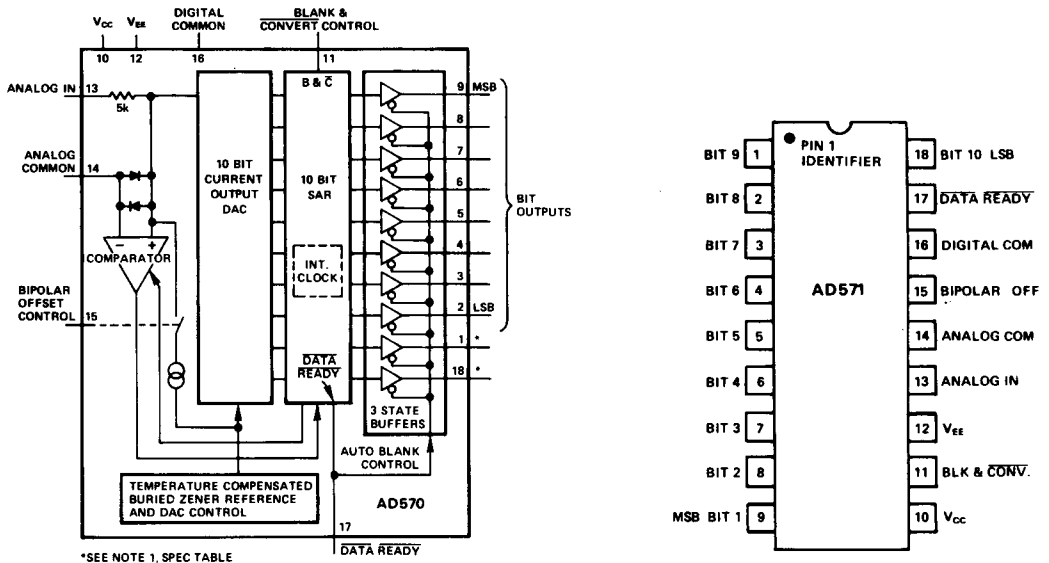
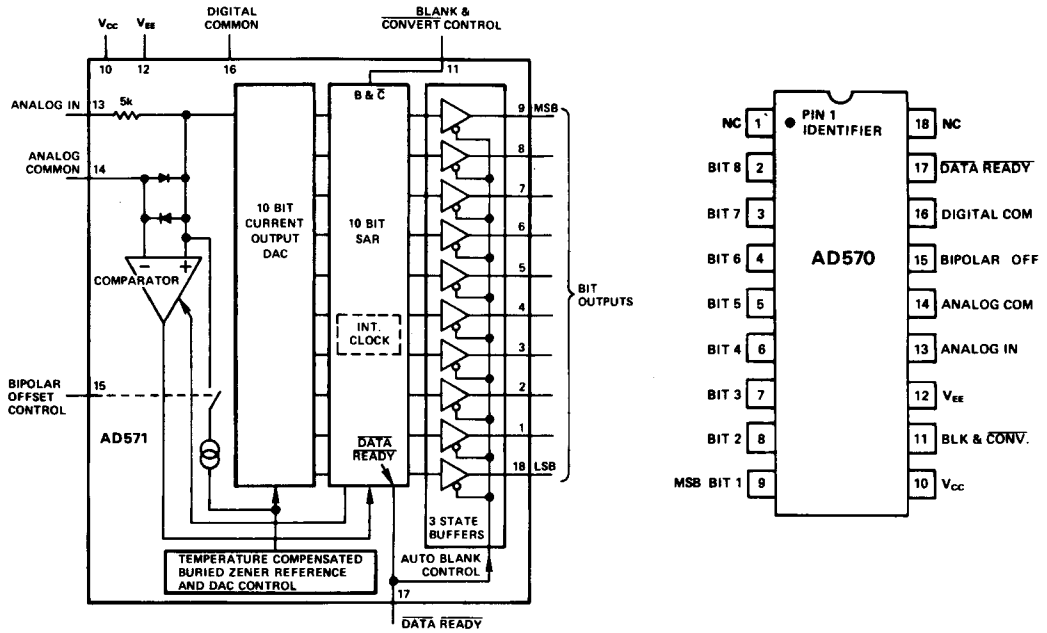
³Minimum resolution for which no missing codes are guaranteed.

⁴For -1 device Full Scale Error guaranteed trimmable with 200 Ω potentiometer.

For -2 device Full Scale Error guaranteed trimmable with 50 Ω potentiometer.

⁵See Figure 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

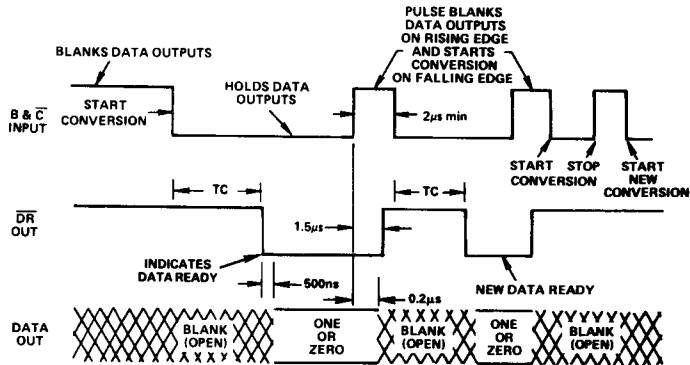
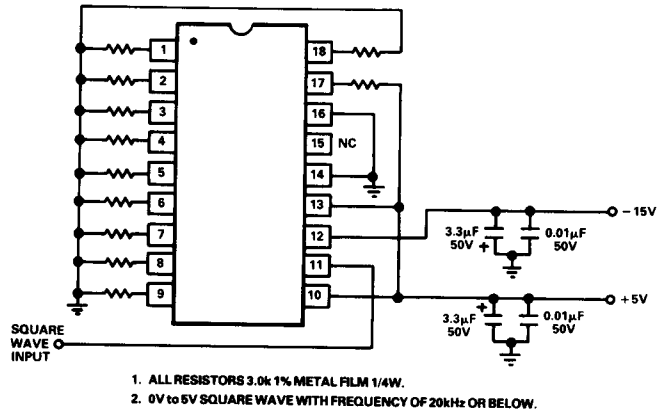


Figure 1. AD570 and AD571 Timing Control Sequences