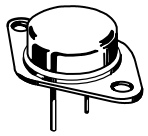
**NPN**
# 2N3715
# 2N3716

**10 AMPERE POWER TRANSISTORS SILICON NPN 60–80 VOLTS 150 WATTS**

# Silicon NPN Power Transistors

. . . designed for medium–speed switching and amplifier applications. These devices feature:

- Total Switching Time at 3 A typically 1.15 μs
- Gain Ranges Specified at 1 A and 3 A
- Low $V_{CE(sat)}$: typically 0.5 V at $I_C$ = 5 A and $I_B$ = 0.5 A
- Excellent Safe Operating Areas
- Complement to 2N3791–92



**CASE 1–07**
**TO–204AA**
**(TO–3)**

**MAXIMUM RATINGS**

| Rating | Symbol | 2N3715 | 2N3716 | Unit |
|---|---|---|---|---|
| Collector–Emitter Voltage | $V_{CEO}$ | 60 | 80 | Volts |
| Collector–Base Voltage | $V_{CB}$ | 80 | 100 | Volts |
| Emitter–Base Voltage | $V_{EB}$ | 7.0 | 7.0 | Volts |
| Collector Current | $I_C$ | 10 | 10 | Amps |
| Base Current | $I_B$ | 4.0 | 4.0 | Amps |
| Power Dissipation | $P_D$ | 150 | 150 | Watts |
| Thermal Resistance | $\theta_{JC}$ | 1.17 | 1.17 | °C/W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to +200 | | °C |

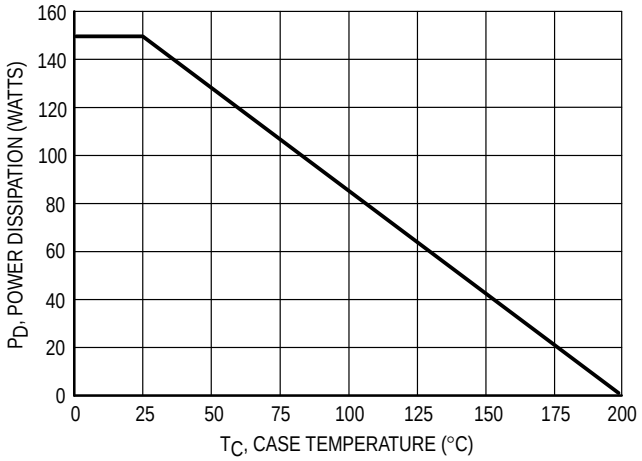



**Figure 1. Power–Temperature Derating Curve**

Safe Area Limits are indicated by Figures 12, 13. Both limits are applicable and must be observed.

**REV 7**

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Emitter–Base Cutoff Current<br>($V_{EB}$ = 7.0 Vdc) | All Types | $I_{EBO}$ | — | 5.0 | mAdc |
| Collector–Emitter Cutoff Current | | $I_{CEX}$ | | | mAdc |
| ($V_{CE}$ = 80 Vdc, $V_{BE}$ = –1.5 Vdc) | 2N3715 | | — | 1.0 | |
| ($V_{CE}$ = 100 Vdc, $V_{BE}$ = –1.5 Vdc) | 2N3716 | | — | 1.0 | |
| ($V_{CE}$ = 60 Vdc, $V_{BE}$ = –1.5 Vdc, $T_C$ = 150°C) | 2N3715 | | — | 10 | |
| ($V_{CE}$ = 80 Vdc, $V_{BE}$ = –1.5 Vdc, $T_C$ = 150°C) | 2N3716 | | — | 10 | |
| Collector–Emitter Sustaining Voltage (1) | | $V_{CEO(sus)}$* | | | Vdc |
| ($I_C$ = 200 mAdc, $I_B$ = 0) | 2N3715 | | 60 | — | |
| | 2N3716 | | 80 | — | |
| DC Current Gain (1) | | $h_{FE}$* | | | — |
| ($I_C$ = 1.0 Adc, $V_{CE}$ = 2.0 Vdc) | 2N3715, 2N3716 | | 50 | 150 | |
| ($I_C$ = 3.0 Adc, $V_{CE}$ = 2.0 Vdc) | 2N3715, 2N3716 | | 30 | — | |
| Collector–Emitter Saturation Voltage (1)<br>($I_C$ = 5.0 Adc, $I_B$ = 0.5 Adc) | 2N3715, 2N3716 | $V_{CE(sat)}$* | — | 0.8 | Vdc |
| Base–Emitter Saturation Voltage (1)<br>($I_C$ = 5.0 Adc, $I_B$ = 0.5 Adc) | 2N3715, 2N3716 | $V_{BE(sat)}$* | — | 1.5 | Vdc |
| Base–Emitter Voltage (1)<br>($I_C$ = 3.0 Adc, $V_{CE}$ = 2.0 Vdc) | All Types | $V_{BE}$* | — | 1.5 | Vdc |
| Small Signal Current Gain<br>($V_{CE}$ = 10 Vdc, $I_C$ = 0.5 Adc, f = 1.0 MHz) | All Types | $h_{fe}$ | 4.0 | — | — |
| Switching Times (Figure 2) | | | **Typ** | | µs |
| ($I_C$ = 5.0 A, $I_{B1}$ = $I_{B2}$ = 0.5 Adc) | | | | | |
| Rise Time | | $t_r$ | 0.45 | | |
| Storage Time | | $t_s$ | 0.3 | | |
| Fall Time | | $t_f$ | 0.4 | | |

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

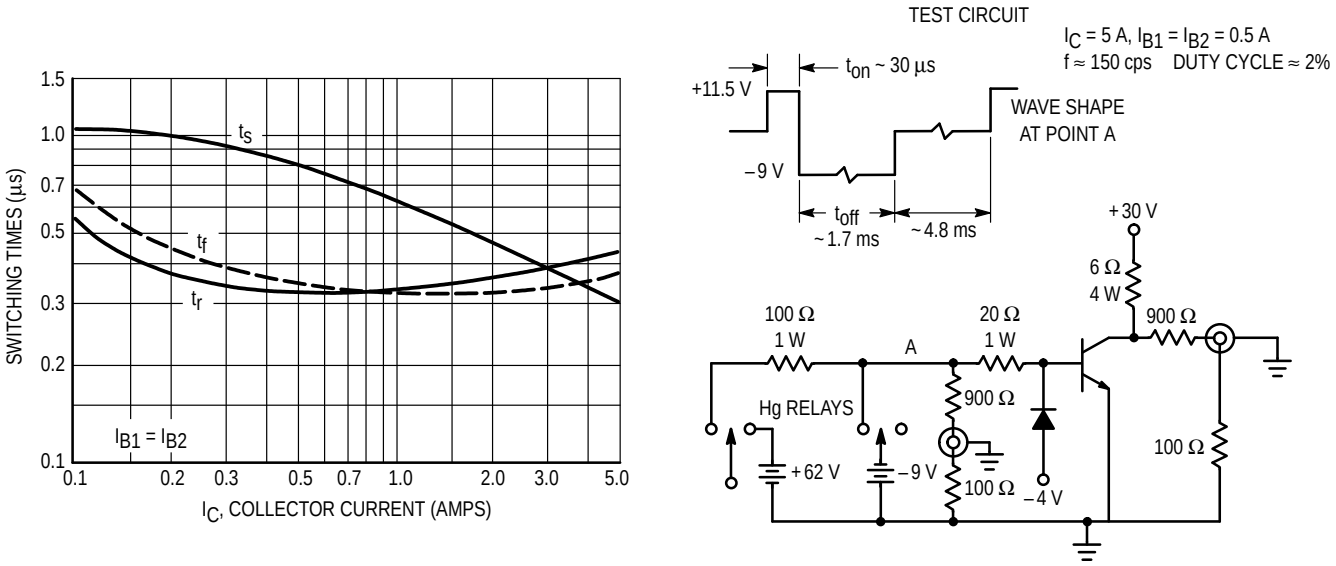



**Figure 2. Typical Switching Times**

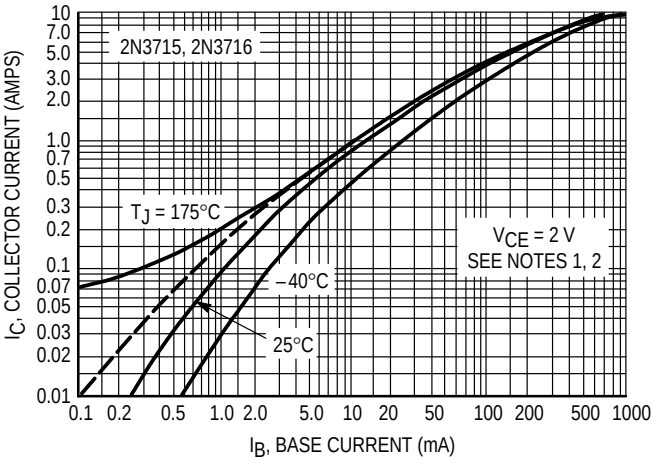



**Figure 3. Collector Current versus Base Current**

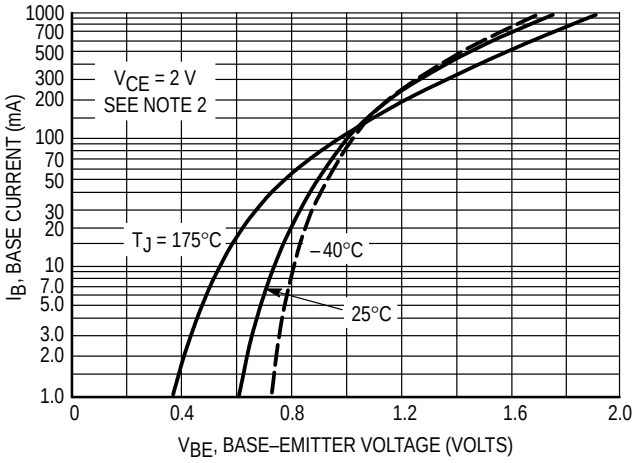



**Figure 4. Base Current–Voltage Variations**

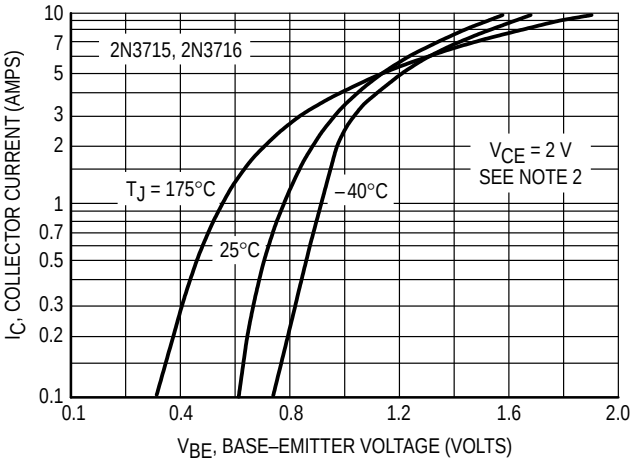



**Figure 5. Collector Current–Voltage Variations**

NOTE 1. Dotted line indicates metered base current plus the $I_{CBO}$ of the transistor at 175°C.
NOTE 2. Pulse test: pulse width ≈ 200 μsec, duty cycle ≈ 1.5%.

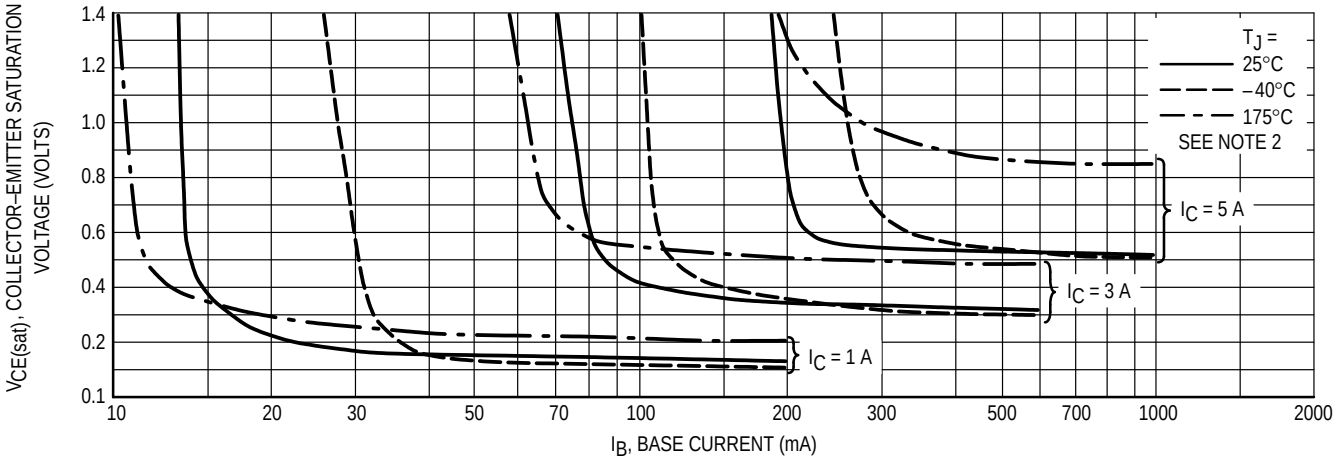



**Figure 6. Collector–Emitter Saturation Voltage Variations**

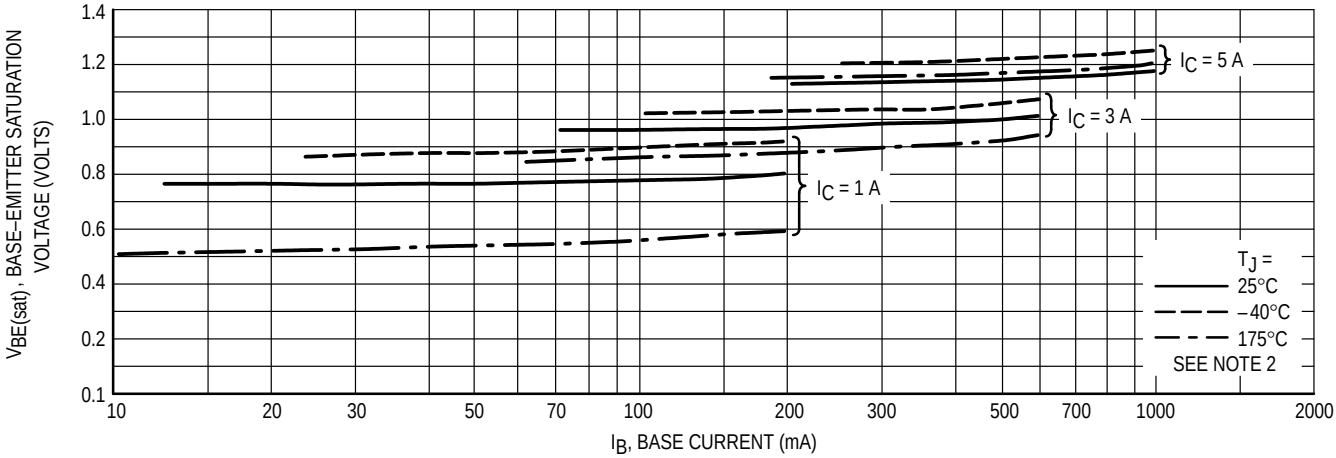



**Figure 7. Base–Emitter Saturation Voltage Variations**

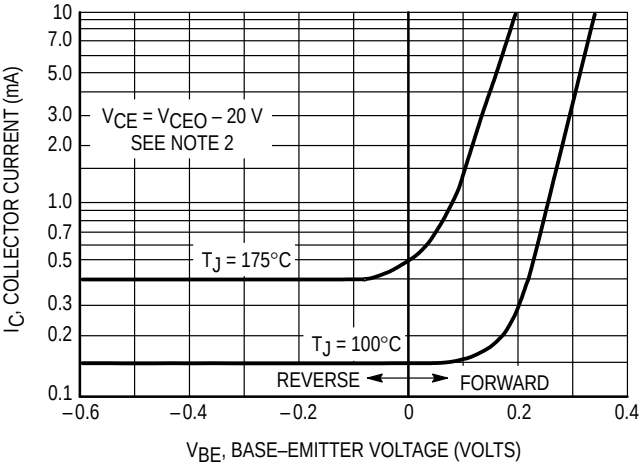



**Figure 8. Collector Current versus Base–Emitter Voltage**

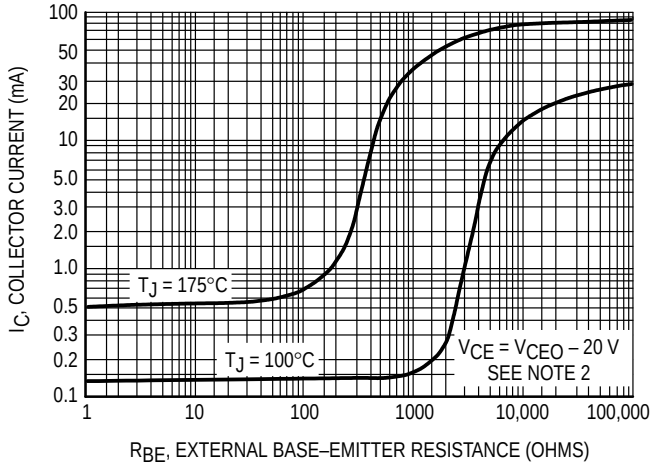



**Figure 9. Collector Current versus Base–Emitter Resistance**

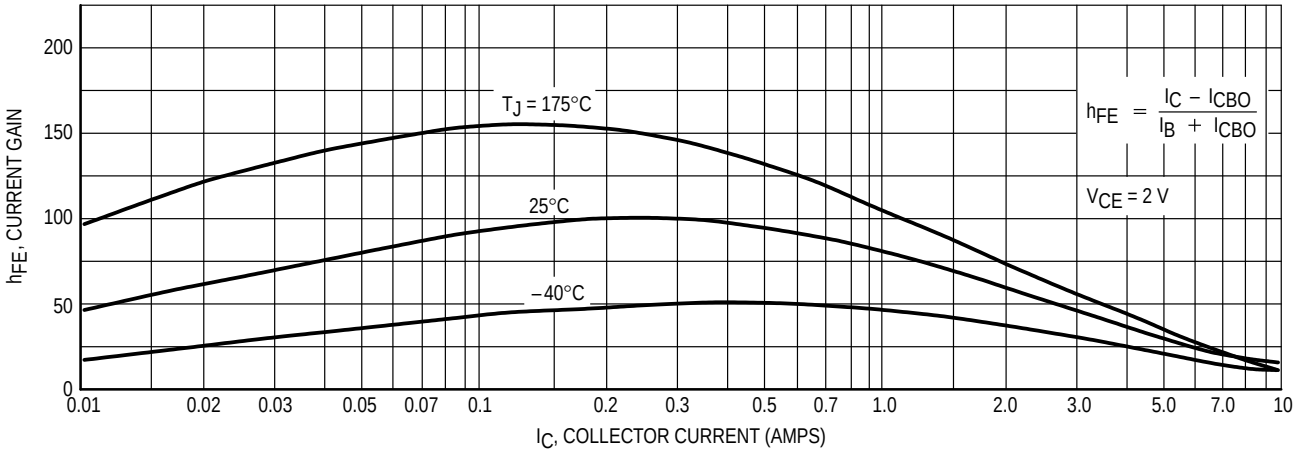



**Figure 10. Current Gain Variations**

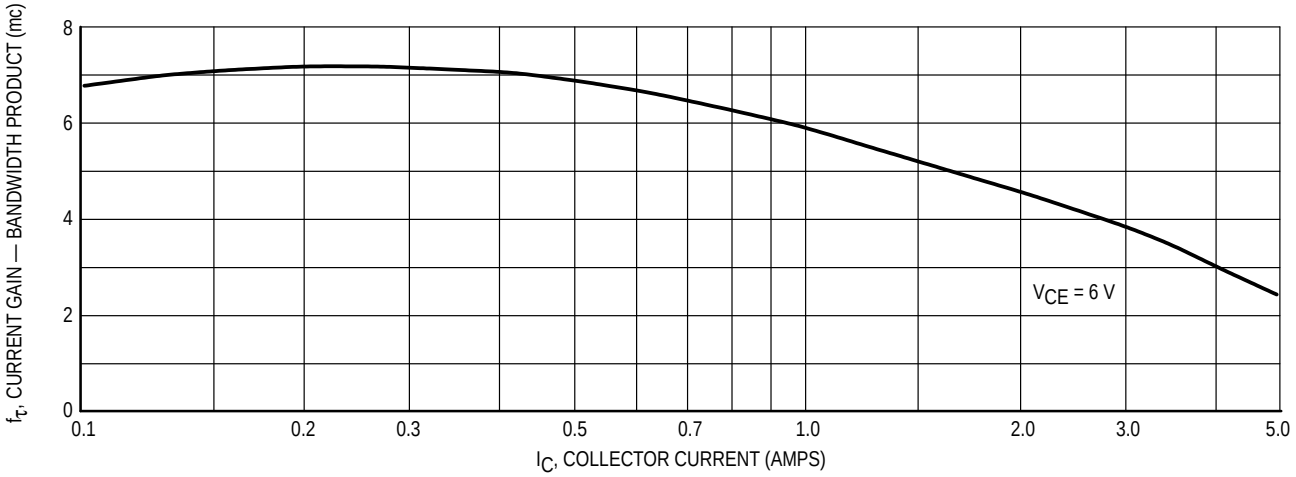



**Figure 11. Current Gain — Bandwidth Product versus Collector Current**

## SAFE OPERATING AREAS

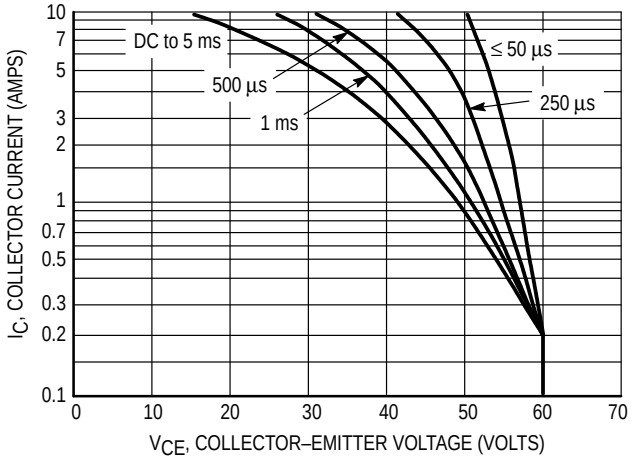



**Figure 12. 2N3715**

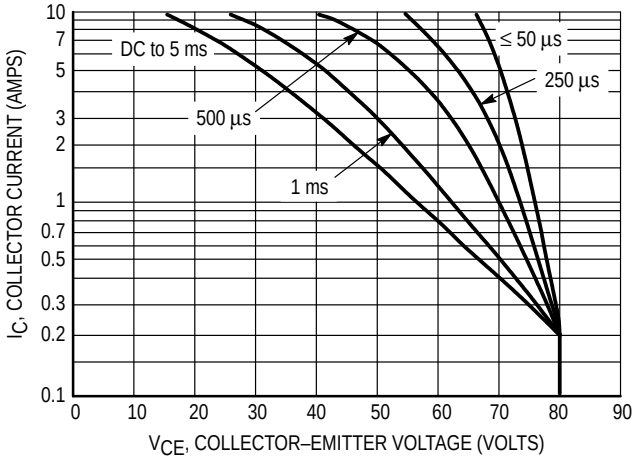
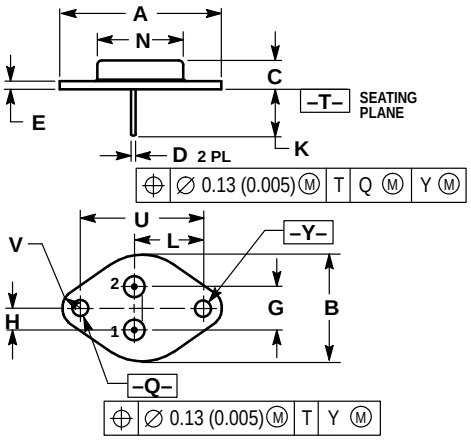



**Figure 13. 2N3716**

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector–emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum $T_J$, the power–temperature derating curve must be observed for both steady state and pulse power conditions.

## PACKAGE DIMENSIONS




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.550 REF | | 39.37 REF | |
| B | — | 1.050 | — | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC | | 10.92 BSC | |
| H | 0.215 BSC | | 5.46 BSC | |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | 0.665 BSC | | 16.89 BSC | |
| N | — | 0.830 | — | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC | | 30.15 BSC | |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

**CASE 1–07**
**TO–204AA (TO–3)**
**ISSUE Z**



**How to reach us:**
**USA / EUROPE**: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

**MFAX**: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
**INTERNET**: http://Design–NET.com

**JAPAN**: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

**HONG KONG**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298