KS82C54

PROGRAMMABLE INTERVAL TIMER

FEATURES/BENEFITS

- **A high performance device featuring pin and functional compatibility with the industry standard 8254**
- **High Speed — 8MHz and 10MHz versions**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **Compatible with 8080/85, 8086/88, 80286/386 and 680X0μP families**
- **Fully static operation**
- **Three independent 16 bit counters**
- **Six programmable counter modes**
- **Status read-back command**
- **Binary or BCD counting**

DESCRIPTION

The KS82C54 is a counter/timer device that includes complete pin and functional compatibility with the industry standard 8254. Designed for fast 10MHz operation, it has three independently programmable 16 bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats.

The KS82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, it can be used to implement event counters, elapsed time indicators, waveform generators plus a host of other functions.

The low power consumption of the KS82C54 makes it ideally suited to portable systems or those with low power standby modes. It is manufactured using proven CMOS process technology to produce a solid, reliable product.

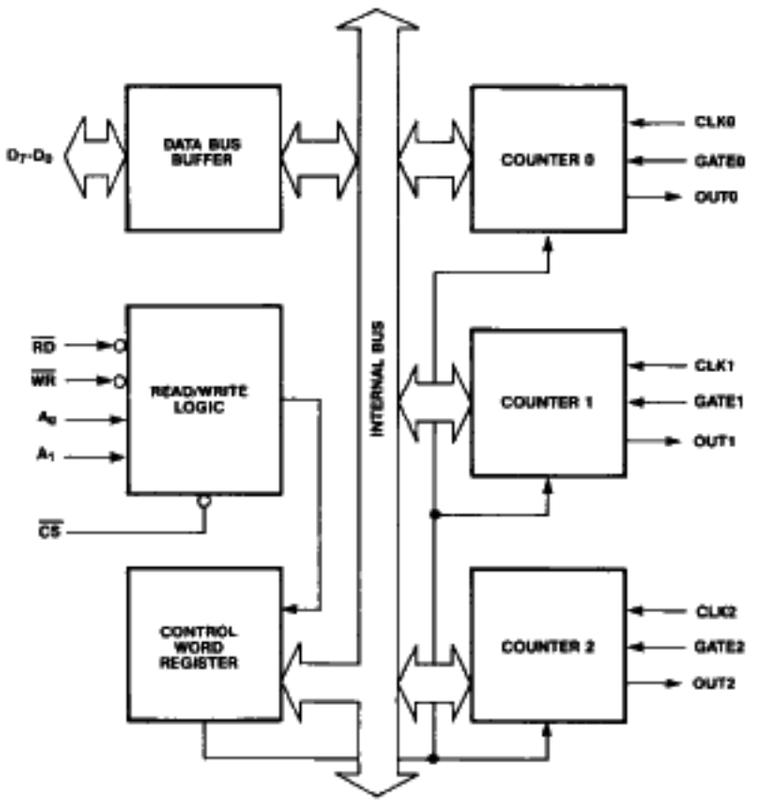

Figure 2: KS82C54 Block Diagram

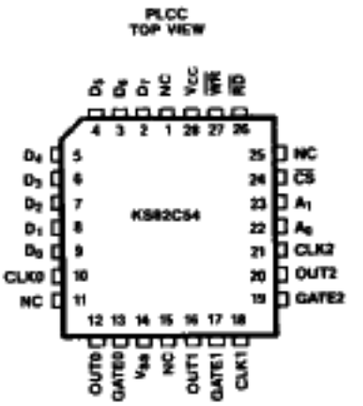

Figure 1a: Plastic Leaded Chip Carrier

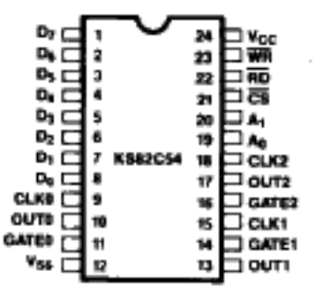

Figure 1b: 24-Pin Configuration

Table 1a: 28-Pin PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	—	NC	15	—	NC
2	I/O	D_7	16	O	OUT1
3	I/O	D_6	17	I	GATE1
4	I/O	D_5	18	I	CLK1
5	I/O	D_4	19	I	GATE2
6	I/O	D_3	20	O	OUT2
7	I/O	D_2	21	I	CLK2
8	I/O	D_1	22	I	A_0
9	I/O	D_0	23	I	A_1
10	I	CLK0	24	I	$\overline{CS}$
11	—	NC	25	—	NC
12	O	OUT0	26	I	$\overline{RD}$
13	I	GATE0	27	I	$\overline{WR}$
14	—	V_{SS}	28	—	V_{CC}

Table 1b: 24-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I/O	D_7	13	O	OUT1
2	I/O	D_6	14	I	GATE1
3	I/O	D_5	15	I	CLK1
4	I/O	D_4	16	I	GATE2
5	I/O	D_3	17	O	OUT2
6	I/O	D_2	18	I	CLK2
7	I/O	D_1	19	I	A_0
8	I/O	D_0	20	I	A_1
9	I	CLK0	21	I	$\overline{CS}$
10	O	OUT0	22	I	$\overline{RD}$
11	I	GATE0	23	I	$\overline{WR}$
12	—	V_{SS}	24	—	V_{CC}

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Table 2: Pin Descriptions

Symbol	Type	Name and Function
A_0, A_1	I	**Address:** These two address pins are used to select the Control Word Register (for read or write operations), or one of the three counters. They are normally connected to the system address bus.
$\overline{CS}$	I	**Chip Select:** Active LOW control signal to enable the KS82C54 to respond to RD and WR signals. If CS is not LOW, RD and WR are ignored.
D_7 - D_0	I/O	**Data:** Bi-directional 3-state data bus lines, connected to system data bus.
CLK0	I	**Clock 0:** Clock input of Counter 0.
CLK1	I	**Clock 1:** Clock input of Counter 1.
CLK2	I	**Clock 2:** Clock input of Counter 2.
GATE0	I	**Gate 0:** Gate input of Counter 0.
GATE1	I	**Gate 1:** Gate input of Counter 1.

A_1	A_0	Selects
0	0	Counter 0
0	0	Counter 1
0	1	Counter 2
1	1	Control Word Register

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
GATE2	I	**Gate 2:** Gate input of Counter 2.
OUT0	O	**Output 0:** Output of Counter 0.
OUT1	O	**Output 1:** Output of Counter 1.
OUT2	O	**Output 2:** Output of Counter 2.
$\overline{RD}$	I	**Read Control:** Active LOW control signal used to enable the KS82C54 for read operations by the CPU.
$\overline{WR}$	I	**Write Control:** Active LOW control signal used to enable the KS82C54 to be written to by the CPU.
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

The KS82C54 is a versatile programmable interval timer/counter designed for use in high speed 8, 16 and 32-bit microprocessor systems. It provides a means of generating accurate time delays in hardware that is fully software configurable. It can be treated as an array of I/O ports, with minimal software overhead.

The internal structure of the KS82C54 is illustrated in the block diagram of Figure 2. Major functional blocks include a data bus buffer, read/write logic, control word register, and three programmable counters.

Data bus Buffer Block

The 8-bit, 3-state data bus buffer provides controllable, bidirectional interface between the KS82C54 and the microprocessor system bus.

Read/Write Logic Block

The read/write logic block generates internal control signals for the different functional blocks using address and control information obtained from the system. The active LOW signals: $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are used to select the KS82C54 for operation, read a counter, and write to a counter (or the control word register) respectively. $\overline{CS}$ must be LOW for $\overline{RD}$ or $\overline{WR}$ to be recognized. Note that $\overline{RD}$ and $\overline{WR}$ must not be active at the same time.

The inputs A_0 and A_1 are used to select the Control Word Register, or one of the three counters that is to be written to or read from (see Table 4). A_0 and A_1 connect directly to the corresponding signals of the microprocessor address bus, while $\overline{CS}$ is derived from the address bus using either a linear select method, or an address decoder device.

Control Word Register

The Control Word Register is a write only register that is selected by the read/write logic block when A_0 and A_1 = 1. When $\overline{CS}$ and $\overline{WR}$ are LOW, data is written into the KS82C54 Control Word Register from the CPU via the data bus buffer. Control word data is interpreted as a number of different commands which are used to program the various device functions. For example, status information is available with the Read-Back Command. These are discussed further in the section on programming.

Counter Blocks

The KS82C54 contains three identical, independent counter blocks. Each counter provides the same functions, but can be programmed to operate in different modes relative to each other. A typical KS82C54 counter is illustrated in Figure 3, and contains the following functional elements: control logic, counter, output latches, count registers and status register.

The Control Logic provides the interface between the Counter Element, the program instructions contained in the Control Word Register and the external signals CLKn, GATEn and OUTn. It also keeps the Status Register information current, controls the access of OL and CR to the internal data bus, and the loading of CE from the CR registers.

The Counter Element (shown in the Figure 3 as CE, for Counting Element) is a 16-bit presettable synchronous down counter.

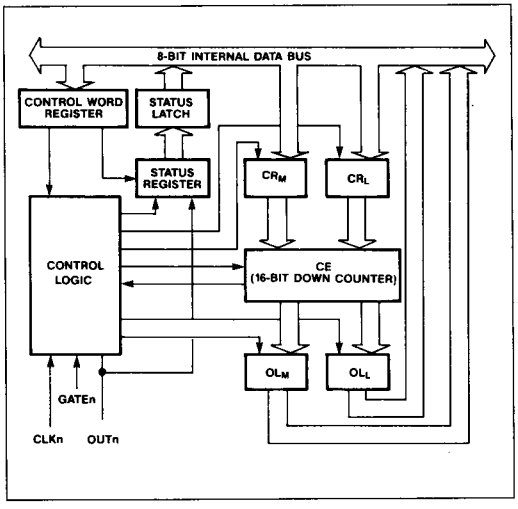
The Output Latches (shown as OL_M and OL_L) provide a mechanism whereby the CPU can read the current contents of the CE. These two 8-bit latches (M for most significant byte and L for least significant byte) together form a 16-bit latch capable of holding the complete content of the CE. Note that this arrangement is also used for communicating 16-bit values over the 8-bit internal data bus.

During normal operation, the contents of OL track with the contents of CE. When a Counter Latch Command is issued by the CPU to a particular counter, its OL latches the current value of CE so that it can be read by the CPU (the CE cannot be read directly). OL then returns to tracking with CE. Note that only one latch (OL_M followed by OL_L) at a time is enabled by the counter's control logic.

The Count Registers (shown as CR_M and CR_L) behave as input latches to the CE, and provide a mechanism whereby the initial count value can be downloaded from the CPU to the CE. Similar in operation to OL, CR is controlled by the counter control logic. When a two byte initial count is to be downloaded, it is transferred one byte at a time across the internal KS82C54 data bus to the appropriate register (CR_M if the most significant byte, CR_L otherwise). CE is loaded by transferring both bytes simultaneously from CR. Note that CR is the interface between CE and the data bus, since CE cannot be accessed directly.

Both CR_M and CR_L are cleared automatically when the counter is programmed and a new initial count is to be written. Thus, regardless of the counter's previous programming, both CR bytes will be initialized to a known zero state. This is important in the case where one byte counts are programmed (either most significant or least significant byte), so that the unused byte is always zero, and won't co. up: the initial count value loaded into CE.

Figure 3: Block Diagram of a Counter



The Status Register and Status Latch is used to hold the current contents of the Control Word Register and the status of the output and null count flag (see section on Programming). The contents of the Status Register must be latched to become available to the data bus, where they can be read by the CPU.

Note that the Control Word Register is also shown in the Counter block diagram. While not a part of the Counter Element, its contents determine the functional operation of the counter, including mode selection programmed.

OPERATIONAL DESCRIPTION

The following operations are common to all modes.

Control Word: When a Control Word is written to a Counter, all Control Logic is Reset, and OUT is initialized to a known state. No CLK pulses are needed.

Gate: The GATE input is always sampled on the rising edge of CLK. In modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is sampled on the next rising edge of CLK, then is immediately reset. In this way, a trigger will be detected no matter when it occurs and a high logic level does not have to be maintained until the next CLK pulse. A summary is given in Table 5.

Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive. If a CLK source other than the system clock is used in modes 2 and 3, GATE should be pulsed immediately after the $\overline{WR}$ for a new count value.

Counter: New Counts are loaded, with the largest possible initial COUNT being 0; (equivalent to 2^{16} for binary counting and 10^4 for BCD counting, as in Table 3)

Counters decremented on the falling edge of CLK do not stop when they reach zero. In Modes 0, 1, 4, and 5 the Counters wrap around to the highest count (either FFFF hex for binary counting or 9999 for BCD counting), then continue counting. Modes 2 and 3 are periodic; the Counters reload themselves with the initial count, then continue counting from there.

Table 3: MIN and MAX Initial Counts

Mode	Minimum Count	Maximum Count*
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

* 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Table 4: Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

If both the Count and Status Registers of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads (the counter can be programmed for one or two type counts) will return the latched count. Subsequent reads will return an unlatched count. Read and write operations are summarized in Table 4.

PROGRAMMING THE KS82C54

The KS82C54 is programmed by writing a Control Word into the Control Word Register (selected by A_0, A'1, 1') and an initial count to the Counter to be written into. A_0 and A_1 are used to select the appropriate Counter. The format of the count depends on the Control Word used.

Write Operation

As mentioned previously, programming of the KS82C54 is performed in two steps:

- Each counter requires a Control Word before the initial count can be written into the selected Counter.
- The initial count must follow the convention in the Control Word for the particular Counter; i.e., LSB or MSB only or LSB and then MSB.

The instruction sequence has to be followed as shown above, however, the sequence of programming the Counter can be random, since every Counter has its associated Control Word Register. A new initial count may be written to the Counter without rewriting the Control Word for that Counter. Of course, the new count must follow the programmed count format.

Table 5: Gate Pin Operations Summary

Signal Status Modes	Low, or Going Low	Rising	High
0	—	• Disables counting	• Enables counting
1	—	• Initiates counting • Resets output after next clock	—
2	• Disables counting • Sets output immediately high	• Initiates counting	• Enables counting
3	• Disables counting • Sets output immediately high	• Initiates counting	• Enables counting
4	• Disables counting	—	• Enables counting
5	—	• Initiates counting	—

Figure 4: Control Word Format

A_1, A_0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC-SELECT COUNTER

0	0	SELECT COUNTER 0
0	1	SELECT COUNTER 1
1	0	SELECT COUNTER 2
1	1	READ-BACK COMMAND (SEE OPERATIONS)

M-MODE

0	0	0	MODE 0
0	0	1	MODE 1
X	1	0	MODE 2
X	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

RW-READ/WRITE

RW1	RW0	
0	0	COUNTER LATCH COMMAND (SEE READ OPERATIONS)
0	1	READ/WRITE LEAST SIGNIFICANT BYTE ONLY
1	0	READ/WRITE MOST SIGNIFICANT BYTE ONLY
1	1	READ/WRITE LEAST SIGNIFICANT BYTE FIRST THEN MOST SIGNIFICANT BYTE

BCD

0	BINARY COUNTER 16-BITS
1	BINARY CODED DECIMAL (BCD) COUNTER (4-DECADES)

Note: Don't care bits (X) should be 0 to ensure compatibility with future Samsung products.

If a Counter is programmed as a 16 bit counter, the Control Register should not be accessed between writing the first and second byte count. Otherwise, the Counter will be loaded incorrectly.

Read Operation

There are three methods of reading the Counters:

- by a simple read operation
- by a Counter Latch Command
- by a Read-Back Command

The first method is performed just by performing a read of the desired Counter Register. The value read is the current status and may be changing if the CLK input is not inhibited.

Counter Latch Command

This method of reading the Counter requires a write command to the Control Word Register of the Counter selected by SC0 and SC1 in the Control Word and RW0 and RW1 = '0'. See Figure 5. The selected counter output will be latched in the OL latch of the Counter at the time the Control Word is received and is held until it is read by the CPU or the Counter is reprogrammed. The OL latch is then loaded according to the Counter Element. This allows reading the Counter at any time without affecting counting. More than one Latch Command may be issued since all counter blocks are built identical. Latching the count by the Latch Command does not influence the programmed Mode of the Counter. Multiple successive Latch Commands do not overwrite the value latched at the first Latch Command. Only a read of the OL or reprogramming of the Counter will alter the latched Counter value. It is also important that two read commands have to be issued if the Counter is programmed as a 16 bit counter. A program may not transfer commands between the two read cycles. Otherwise, an incorrect count value will be read.

Read-Back Command

A third method of reading the count value requires issuing a Read-Back Command prior to the read operation. See Figure 6. If the $\overline{COUNT}$ bit is set, the appropriate count values of the Counter selected by CNT0, 1, 2 are latched. The status of the Counter are latched if the STATUS bit is '1'. Multiple counters may be selected.

The Counter Status format is shown in Figure 7. D0 to D5 contain the Mode of the counter as programmed by the last Control Word.

D6 (Null Count) indicate when the last Count Register (CR) has been loaded into the Counting Element (CE). See also Mode Definition.

Figure 5: Counter Latching Command Format

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC00	0	0	X	X	X	X

SC1, SC0—SPECIFY COUNTER TO BE LATCHED

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	1
1	1	READ-BACK COMMAND

D5, D4-00 DESIGNATED COUNTER LATCH COMMAND
X — DON'T CARE

Note: Don't care bits (X) should be 0 to ensure compatibility with future Samsung products.

'1' After a write to the Word Control Register (Note 1)
'1' After a write to the Counter Register (CR) (Note 2)
'0' After a new count is loaded into the Count Element (CR → CE).

Note 1: Only the Counter specified by the Control Word is affected.
Note 2: If the Counter is programmed for two byte counts, the $\overline{COUNT}$ bit goes to '1' after the second byte is written.

The output OUT of the selected counter can be read by D7 (OUTPUT) of the Status byte. If both $\overline{COUNT}$ and $\overline{STATUS}$ has been selected, the first read operation of that Counter will return the latched status and the next one or two read will return the latched count. Subsequent reads return unlatched counts.

Figure 6: Read-Back Command Format

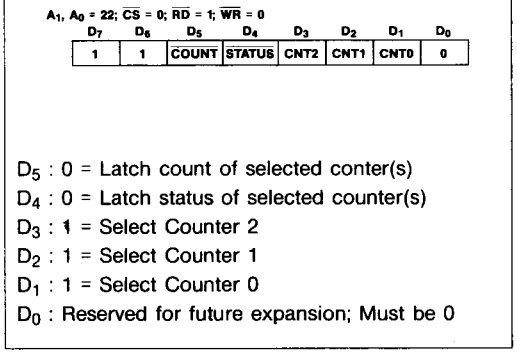
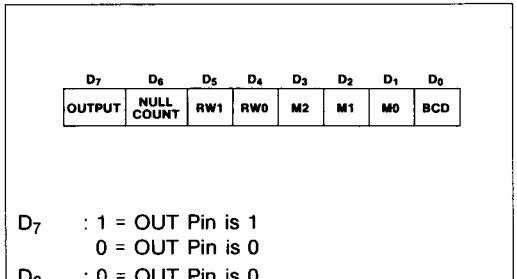


Figure 7: Status Byte



MODE DEFINITIONS

The following terms are useful in describing the operation of the KS82C84.

- CLK pulse: A rising edge, followed by a falling edge, of a Counter's CLK input.
- Trigger: A rising edge of a Counter's GATE input.
- Counter loading: Transfer of a count from the CR to the CE (see Functional Description)

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is set low, and remains low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting while GATE = 0 disables counting. GATE has no effect on OUT.

After a Control Word and initial count are written to a Counter, the initial count is loaded on the next CLK pulse. Since this CLK pulse does not decrement the count, OUT does not go high until N + 1 CLK pulses after the initial count is written (where N is the initial count value).

If a new count is written to the Counter, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

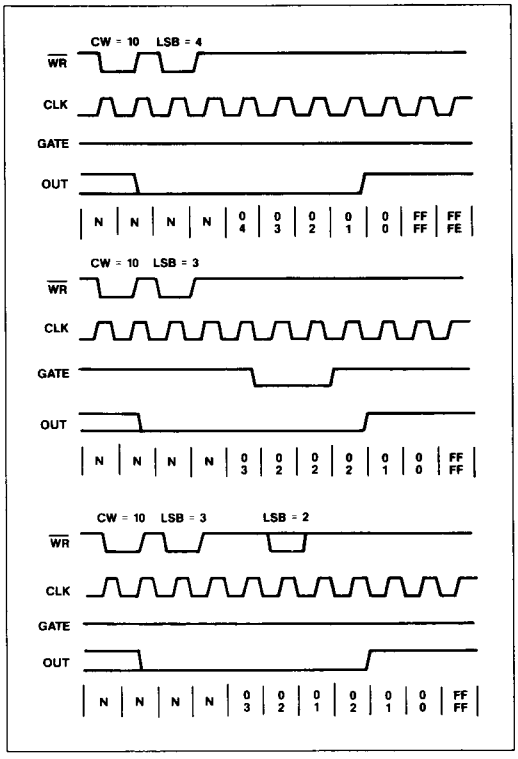
If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later. A CLK pulse is not required to load the Counter as this has already been done.

Mode 1: Hardware Retriggerable One-Shot

OUT is initially high. To begin the one-shot pulse, OUT goes low on the CLK pulse following a trigger and remains low until the Counter reaches zero. OUT then goes high and remains high until the CLK pulse following the next trigger.

After a Control Word and intial count have been written, the Counter is armed. A trigger causes the Counter to be loaded and OUT to be set low on the next CLK pulse, starting the one-shot pulse. An initial count of N results in a one-shot pulse N CLK cycles long. Since the one-shot is retriggerable, OUT remains low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

Figure 8: Mode 0 Timing



Notes: These conventions apply to all mode timing diagrams:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for Control Word; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB is the Least Significant Byte of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write only, the most significant byte cannot be read.
6. N stands for an undefined count. Vertical lines show transitions between count values.

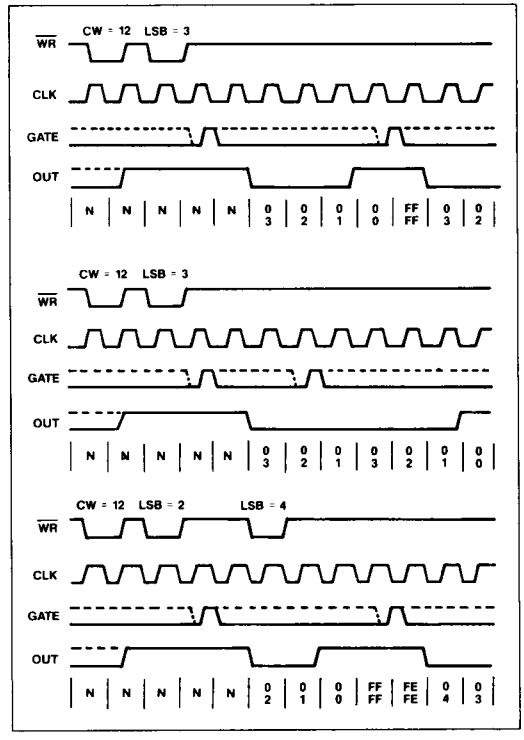
If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In this case, the new count is loaded into the Counter and the one-shot pulse continues for the duration of the count.

Mode 2: Rate Generator

This mode functions like a divide-by-N counter and is typically used for generating Real Time Clock Interrupts. OUT is initially high. When the initial count has decremented to 1, OUT goes low for one CLK pulse, then high again. The Counter reloads the initial count and the process is repeated. Mode 2 is periodic, with the same sequence repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the initial count into the Counter on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

Figure 9: Mode 1 Timing



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After a Control Word and intial count have been written, the Counter is loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written, which allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after a new count is written but before the end of the current period, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Otherwise, the new count is loaded at the end of the current counting cycle. In Mode 2, a COUNT of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation, and is similar to Mode 2 except for the duty cycle of OUT. OUT is initially high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is also periodic, with the sequence above repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

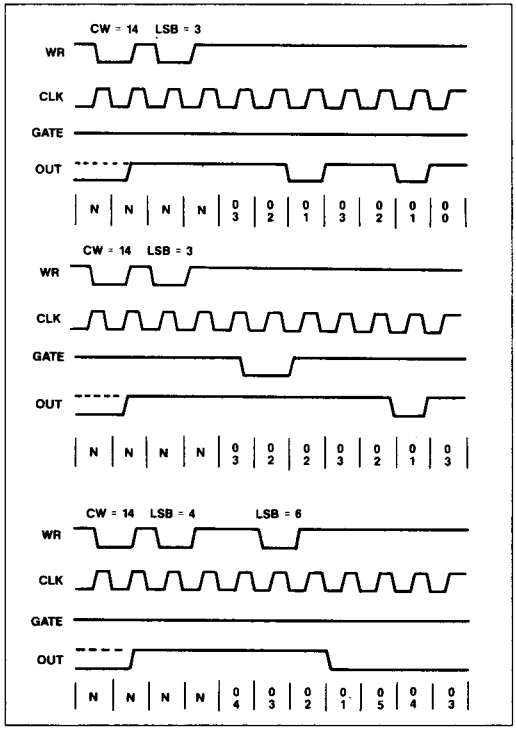
GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately (no CLK pulse is needed). A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Otherwise, the new count is loaded at the end of the current half-cycle.

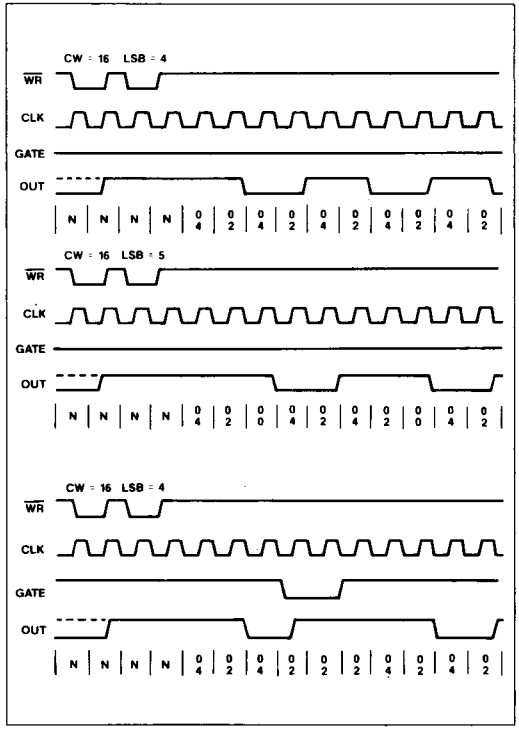
Mode 3 is implemented as follows according to whether the initial count value is even or odd:

Figure 10: Mode 2 Timing



Note: A gate transition should not occur one clock cycle prior to reaching the terminal count (TC).

Figure 11: Mode 3 Timing

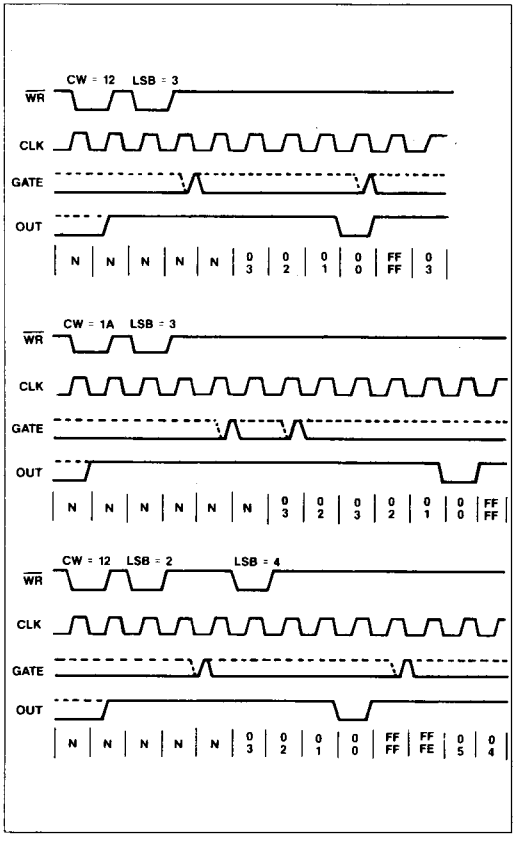


Note: A gate transition should not occur one clock cycle prior to reaching the terminal count (TC).

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (to given an even number) is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT is high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Figure 12: Mode 4 Timing



Mode 4: Software Triggered Strobe

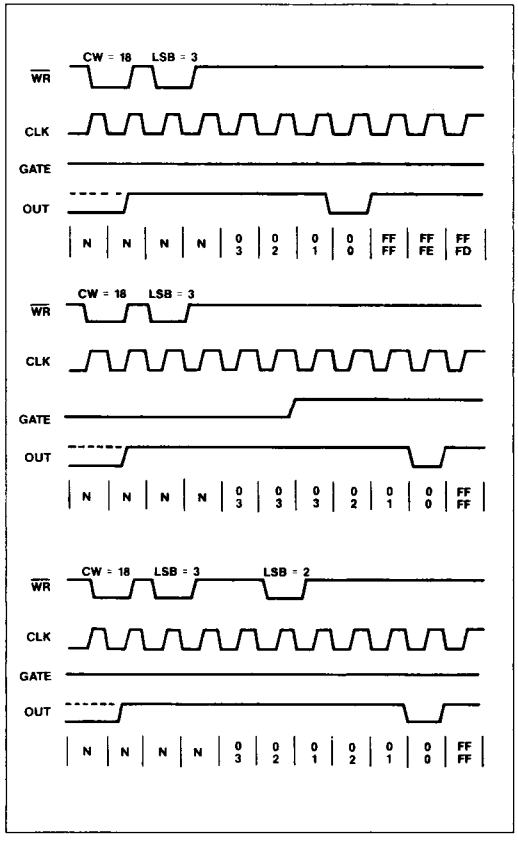
OUT is initially high. When the initial count expires, OUT goes low for one CLK pulse and then goes high again. The counting sequence is triggered by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following events occur:

Figure 13: Mode 5 Timing



2

1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be retriggered by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5:
HARDWARE TRIGGERED strobe (Retriggerable).

OUT is initially high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT goes low for one CLK pulse, then goes high again.

After a Control Word and initial count has been written, the counter is loaded on the first CLK pulse following a trigger. This CLK pulse does not decrement the count, so, given an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger causes the Counter to be loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable, so OUT will not go low until N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written, but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Table 6: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 7: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1MHz Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output Capacitance		20	pF

Table 9: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{CC}	V_{CC} Supply Current		—	20	mA
I_{CCSB}	Standby Supply Current		—	10	μA
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0V	—	±20	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0.45V	—	±10	μA
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5V	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -400μA I_{OH} = -2.5mA	3.0 2.4	— —	V V
V_{OL}	Output Low Voltage	I_{OL} = 2.5mA	—	0.4	V

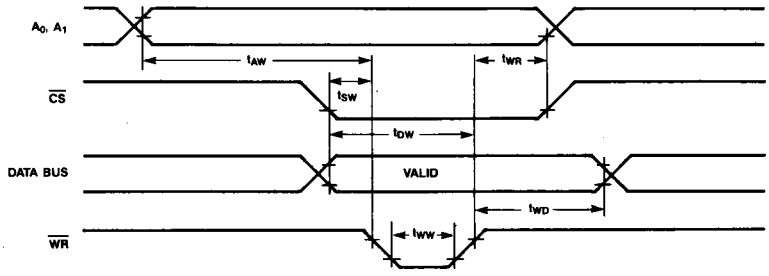
Table 10: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) Bus Parameters[1]

Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AD}	Data delay from address		—	220	—	185	ns
t_{AR}	Address stable before $\overline{RD}$↓		45	—	30	—	ns
t_{AW}	Address stable before $\overline{WR}$		0	—	0	—	ns
t_{CL}	CLK setup for count latch		-40	45	-40	40	ns
t_{CLK}	Clock period		125	DC	100	DC	ns
t_{DF}	$\overline{RD}$↑ to data floating		5	90	5	65	ns
t_{DW}	Data setup time before $\overline{WR}$↑		120	—	95	—	ns
t_F	Clock fall time		—	25	—	25	ns
t_{GH}	Gate hold time after CLK↑	Note 2	50	—	50	—	ns
t_{GL}	Gate width low		50	—	50	—	ns
t_{GS}	Gate setup time to CLK↑		50	—	40	—	ns
t_{GW}	Gate width high		50	—	50	—	ns
t_{OD}	Output delay from CLK↓		—	150	—	100	ns
t_{ODG}	Output delay from GATE↓		—	120	—	100	ns
t_{PWH}	High pulse width	Note 3	60	—	30	—	ns
t_{PWL}	Low pulse width	Note 3	60	—	50	—	ns
t_R	Clock rise time		—	25	—	25	ns
t_{RA}	Address hold time after $\overline{RD}$↑		0	—	0	—	ns
t_{RD}	Data delay from $\overline{RD}$↓		—	120	—	85	ns
t_{RR}	$\overline{RD}$ pulse width		150	—	95	—	ns
t_{RV}	Command recovery time		200	—	165	—	ns
t_{SR}	$\overline{CS}$ stable before $\overline{RD}$↓		0	—	0	—	ns
t_{SW}	$\overline{CS}$ stable before $\overline{WR}$↓		0	—	0	—	ns
t_{WA}	Address hold time $\overline{WR}$↑		0	—	0	—	ns
t_{WC}	CLK delay for loading		0	55	0	55	ns
t_{WD}	Data hold time after $\overline{WR}$↑		0	—	0	—	ns
t_{WG}	Gate delay for sampling		-5	50	-5	40	ns
t_{WO}	OUT delay from Mode Write		—	260	—	240	ns
t_{WW}	$\overline{WR}$ pulse width		150	—	95	—	ns

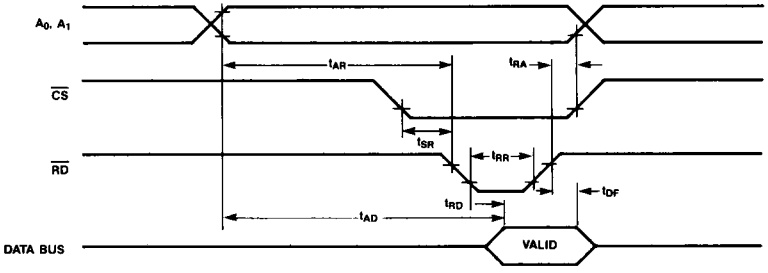
Notes:
1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V.
2. In modes 1 and 5, triggers are sampled on each rising clock edge. A second trigger within 120ns of the rising clock edge may not be detected (70ns for KS82C54-10).
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

Figure 14: Timing Diagrams

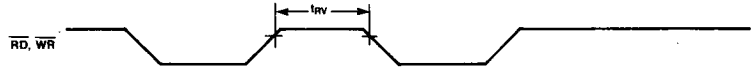
a) Write Timing



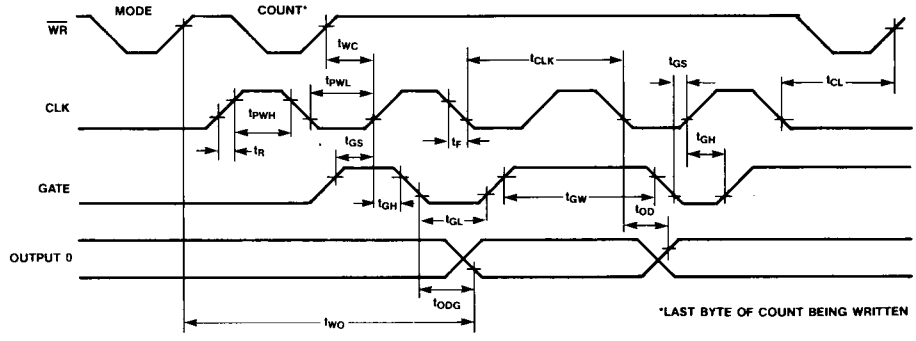
b) Read Timing



c) Recover Timing



d) Clock and Gate Timing



PACKAGE DIMENSIONS

Units: Inches

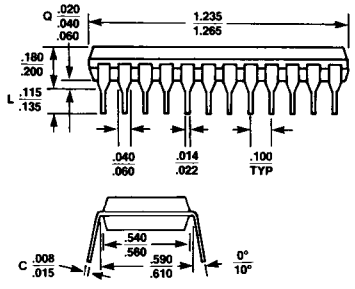


Figure 15: Plastic Package

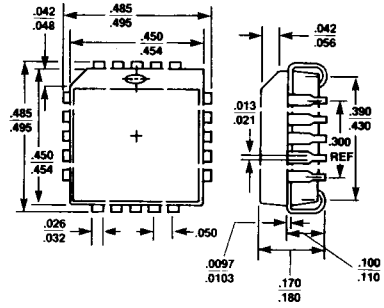


Figure 16: PLCC Package

ORDERING INFORMATION & PRODUCT CODE

KS 82C54 X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (–40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.